ARIZONA MICROTEK, INC.

# AZ100LVEL33

## ECL/PECL ÷4 Divider

## FEATURES

- Green / RoHS Compliant / Lead (Pb) Free package available
- Operating Range of 3.0V to 5.5V
- 470ps Propagation Delay
- 5.0+ GHz Toggle Frequency
- Internal Input Pulldown Resistors
- Direct Replacement for ON Semiconductor MC100EL33 & MC100LVEL33
- Transistor Count = 91 Devices
- IBIS Model Files Available on Arizona Microtek Web Site
- >2 kV HBM ESD Protection
- Additional ESD Data Available on Arizona Microtek Website

**PACKAGE AVAILABILITY**

| PACKAGE | PART NUMBER | MARKING | NOTES |
|---|---|---|---|
| MLP 8 (2x2) Green / RoHS Compliant / Lead (Pb) Free | AZ100LVEL33NG | C3G <Date Code> | 1,2 |
| SOIC 8 Green / RoHS Compliant / Lead (Pb) Free | AZ100LVEL33DG | AZM100G LVEL33 | 1,2,3 |
| MSOP 8 Green / RoHS Compliant / Lead (Pb) Free | AZ100LVEL33TG | AZHG LV33 | 1,2,3 |

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
2 Date code format: "Y" or "YY" for year followed by "WW" for week.
3 Date code "YWW" or "YYWW" on underside of part.

## DESCRIPTION

The AZ100LVEL33 is an integrated ÷4 divider. The RESET pin is asynchronous and clears the output (Q Low, $\overline{Q}$ High) on the rising edge. Upon power-up, the internal flip-flop will be in a random logic state. RESET allows for the synchronization of multiple LVEL33's in a system.

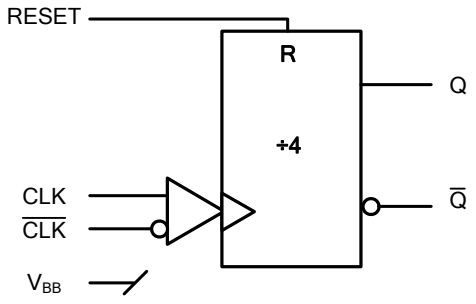
The LVEL33 provides a $V_{BB}$ output for single-end use or a DC bias reference for AC coupling to the device. For single-ended input applications, the $V_{BB}$ reference should be connected to one side of the CLK/$\overline{CLK}$ differential input pair. The input signal is then fed to the other CLK/$\overline{CLK}$ input. The $V_{BB}$ pin can support 1.0mA sink/source current. When used, the $V_{BB}$ pin should be bypassed to ground via a 0.01μF capacitor.

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

**PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| CLK, $\overline{CLK}$ | Clock Inputs |
| RESET | Asynchronous Reset |
| $V_{BB}$ | Reference Voltage Output |
| Q, $\overline{Q}$ | Data Outputs |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |

**LOGIC DIAGRAM**



**Absolute Maximum Ratings are those values beyond which device life may be impaired.**

| Symbol | Characteristic | Rating | Unit |
|---|---|---|---|
| $V_{CC}$ | PECL Power Supply ($V_{EE}$ = 0V) | 0 to +8.0 | Vdc |
| $V_I$ | PECL Input Voltage ($V_{EE}$ = 0V) | 0 to +6.0 | Vdc |
| $V_{EE}$ | ECL Power Supply ($V_{CC}$ = 0V) | -8.0 to 0 | Vdc |
| $V_I$ | ECL Input Voltage ($V_{CC}$ = 0V) | -6.0 to 0 | Vdc |
| $I_{OUT}$ | Output Current --- Continuous<br>--- Surge | 50<br>100 | mA |
| $T_A$ | Operating Temperature Range | -40 to +85 | °C |
| $T_{STG}$ | Storage Temperature Range | -65 to +150 | °C |

**ECL DC Characteristics** ($V_{EE}$ = -3.0V to -5.5V, $V_{CC}$ = GND)

| Symbol | Characteristic | -40°C | | | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH Voltage[1] | -1085 | -1005 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | mV |
| $V_{OL}$ | Output LOW Voltage[1] | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV |
| $V_{IH}$ | Input HIGH Voltage | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| $V_{IL}$ | Input LOW Voltage | -1810 | | -1475 | -1810 | | -1475 | -1810 | | -1475 | -1810 | | -1475 | mV |
| $V_{BB}$ | Reference Voltage | -1380 | | -1260 | -1380 | | -1260 | -1380 | | -1260 | -1380 | | -1260 | mV |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | | | 150 | µA |
| $I_{IL}$ | Input LOW Current<br>CLK, $\overline{CLK}$<br>RESET | -150<br>0.5 | | | -150<br>0.5 | | | -150<br>0.5 | | | -150<br>0.5 | | | µA |
| $I_{EE}$ | Power Supply Current | | 27 | 33 | | 27 | 33 | | 27 | 33 | | 31 | 37 | mA |

1. Each output is terminated through a 50Ω resistor to $V_{CC}$ – 2V.

**LVPECL DC Characteristics** ($V_{EE}$ = GND, $V_{CC}$ = +3.3V)

| Symbol | Characteristic | -40°C | | | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH Voltage[1,2] | 2215 | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV |
| $V_{OL}$ | Output LOW Voltage[1,2] | 1470 | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV |
| $V_{IH}$ | Input HIGH Voltage[1] | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage[1] | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| $V_{BB}$ | Reference Voltage[1] | 1920 | | 2040 | 1920 | | 2040 | 1920 | | 2040 | 1920 | | 2040 | mV |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | | | 150 | µA |
| $I_{IL}$ | Input LOW Current<br>CLK, $\overline{CLK}$<br>RESET | -150<br>0.5 | | | -150<br>0.5 | | | -150<br>0.5 | | | -150<br>0.5 | | | µA |
| $I_{EE}$ | Power Supply Current | | 27 | 33 | | 27 | 33 | | 27 | 33 | | 31 | 37 | mA |

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to $V_{CC}$ – 2V.

**PECL DC Characteristics** ($V_{EE}$ = GND, $V_{CC}$ = +5.0V)

| Symbol | Characteristic | -40°C | | | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH Voltage[1,2] | 3915 | 3995 | 4120 | 3975 | 4045 | 4120 | 3975 | 4045 | 4120 | 3975 | 4045 | 4120 | mV |
| $V_{OL}$ | Output LOW Voltage[1,2] | 3170 | 3305 | 3445 | 3190 | 3295 | 3380 | 3190 | 3295 | 3380 | 3190 | 3295 | 3380 | mV |
| $V_{IH}$ | Input HIGH Voltage[1] | 3835 | | 4120 | 3835 | | 4120 | 3835 | | 4120 | 3835 | | 4120 | mV |
| $V_{IL}$ | Input LOW Voltage[1] | 3190 | | 3525 | 3190 | | 3525 | 3190 | | 3525 | 3190 | | 3525 | mV |
| $V_{BB}$ | Reference Voltage[1] | 3620 | | 3740 | 3620 | | 3740 | 3620 | | 3740 | 3620 | | 3740 | mV |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | | | 150 | µA |
| $I_{IL}$ | Input LOW Current<br>CLK, $\overline{CLK}$<br>RESET | -150<br>0.5 | | | -150<br>0.5 | | | -150<br>0.5 | | | -150<br>0.5 | | | µA |
| $I_{EE}$ | Power Supply Current | | 27 | 33 | | 27 | 33 | | 27 | 33 | | 31 | 37 | mA |

1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to $V_{CC}$ – 2V.

**AC Characteristics** ($V_{EE}$ = -3.0V to -5.5V; $V_{CC}$ = GND or $V_{EE}$ = GND; $V_{CC}$ = +3.0V to +5.5V)

| Symbol | Characteristic | -40°C | | | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Toggle Frequency | 4.2 | | | 4.2 | | | 4.2 | | | 4.2 | | | GHz |
| $t_{PLH}$ / $t_{PHL}$ | Propagation Delay<br>CLK, $\overline{CLK}$ to Q/$\overline{Q}$<br>RESET to Q/$\overline{Q}$ | <br>360<br>310 | <br>450<br>460 | <br>540<br>610 | <br>320<br>340 | <br>460<br>460 | <br>550<br>580 | <br>380<br>360 | <br>470<br>460 | <br>560<br>560 | <br>400<br>380 | <br>490<br>480 | <br>580<br>580 | ps |
| $t_{RR}$ | Reset Recovery | 300 | | | 300 | | | 300 | | | 300 | | | ps |
| $t_{skew}$ | Within-Device Skew | | | 20 | | | 20 | | | 20 | | | 20 | ps |
| $V_{PP}$ (AC) | Input Swing[1] | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| $V_{CMR}$ | Common Mode Range[2]<br>Vpp < 500mV<br>Vpp ≥ 500mV | $V_{EE}$ +<br>1.2<br>1.4 | | $V_{CC}$ -<br>0.4<br>0.4 | $V_{EE}$ +<br>1.1<br>1.3 | | $V_{CC}$ -<br>0.4<br>0.4 | $V_{EE}$ +<br>1.1<br>1.3 | | $V_{CC}$ -<br>0.4<br>0.4 | $V_{EE}$ +<br>1.1<br>1.3 | | $V_{CC}$ -<br>0.4<br>0.4 | V |
| $t_r$ / $t_f$ | Output Rise/Fall Times Q/$\overline{Q}$ (20% - 80%) | 100 | | 260 | 100 | | 260 | 100 | | 260 | 100 | | 260 | ps |

1. $V_{PP}$ is the peak-to-peak differential input swing for which AC parameters are guaranteed.
2. $V_{CMR}$ is defined as the range within which the $V_{IH}$ level may vary, with the device still meeting the propagation delay specification. The $V_{IL}$ level must be such that $V_{PP}$ is within the differential input swing range specified.

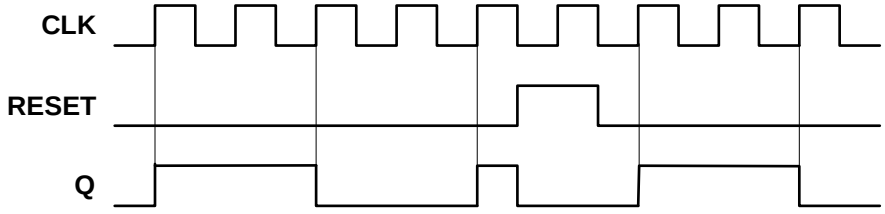
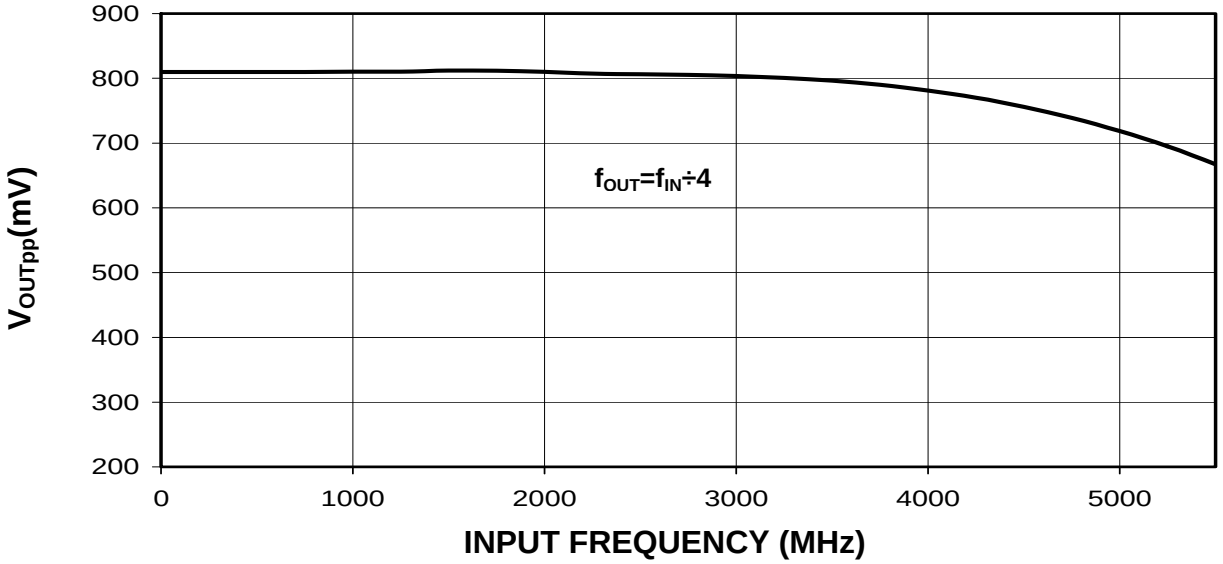



**Figure 1. Timing Diagram**

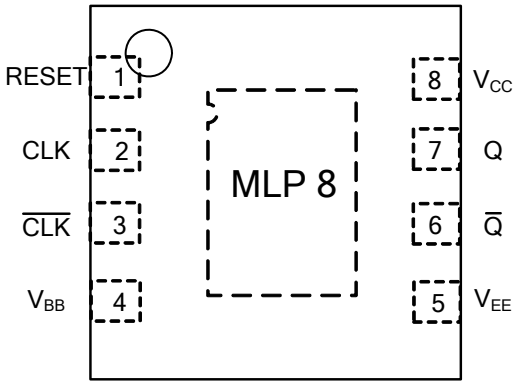
## Typical Large Signal Output Swing, Q/$\overline{Q}$




Measured with 750mv D input, Q/$\overline{Q}$ each terminated to $V_{CC}$-2V via 50 Ω resistors.

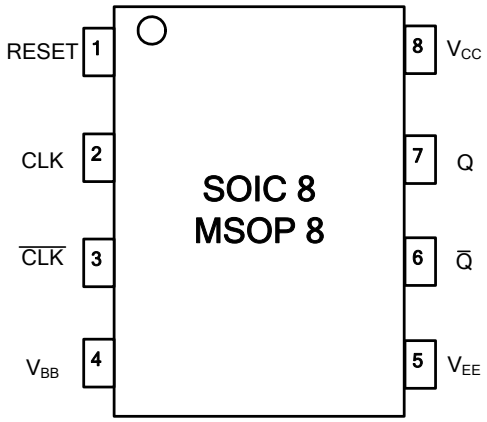
## PACKAGE PINOUTS
## TOP VIEW

**AZ100LVEL33N**

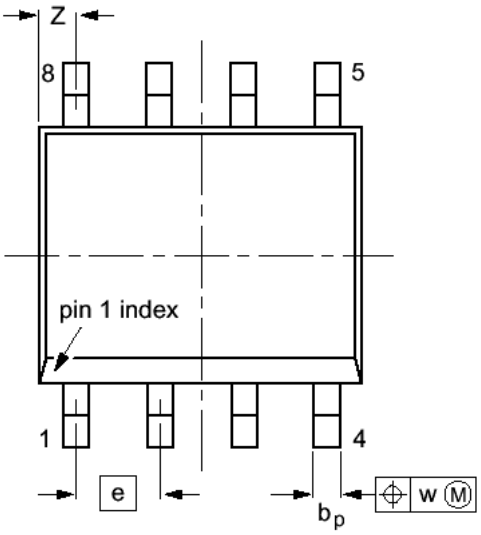


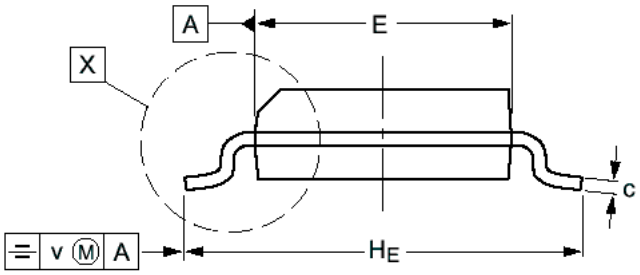

**Bottom Center Pad may be left open or tied to $V_{EE}$.**

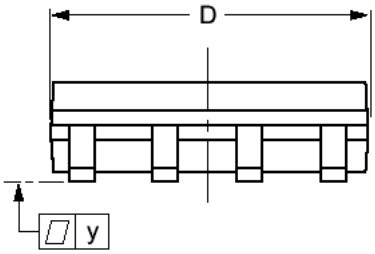
**AZ100LVEL33D**
**AZ100LVEL33T**

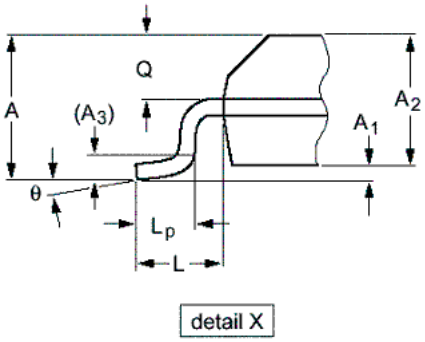


## PACKAGE DIAGRAM
## SOIC 8



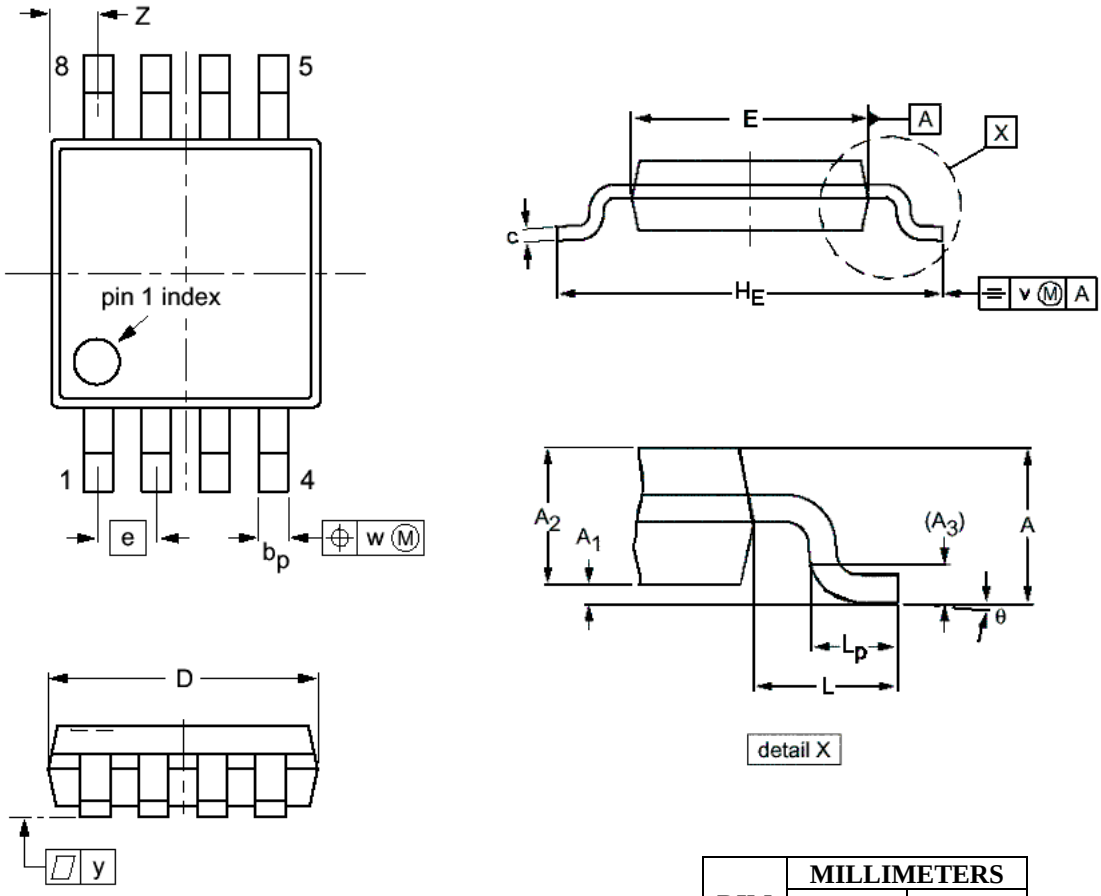




NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| **DIM** | **MIN** | **MAX** | **MIN** | **MAX** |
| **A** | | 1.75 | | 0.069 |
| **$A_1$** | 0.10 | 0.25 | 0.004 | 0.010 |
| **$A_2$** | 1.25 | 1.45 | 0.049 | 0.057 |
| **$A_3$** | 0.25 | | 0.01 | |
| **$b_p$** | 0.36 | 0.49 | 0.014 | 0.019 |
| **c** | 0.19 | 0.25 | 0.0075 | 0.0100 |
| **D** | 4.8 | 5.0 | 0.19 | 0.20 |
| **E** | 3.8 | 4.0 | 0.15 | 0.16 |
| **e** | 1.27 | | 0.050 | |
| **$H_E$** | 5.80 | 6.20 | 0.228 | 0.244 |
| **L** | 1.05 | | 0.041 | |
| **$L_p$** | 0.40 | 1.00 | 0.016 | 0.039 |
| **Q** | 0.60 | 0.70 | 0.024 | 0.028 |
| **v** | 0.25 | | 0.01 | |
| **w** | 0.25 | | 0.01 | |
| **y** | 0.10 | | 0.004 | |
| **Z** | 0.30 | 0.70 | 0.012 | 0.028 |
| **θ** | $0^O$ | $8^O$ | $0^O$ | $8^O$ |

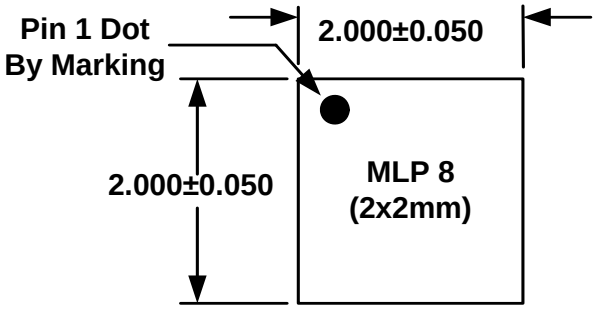
## PACKAGE DIAGRAM
## MSOP 8



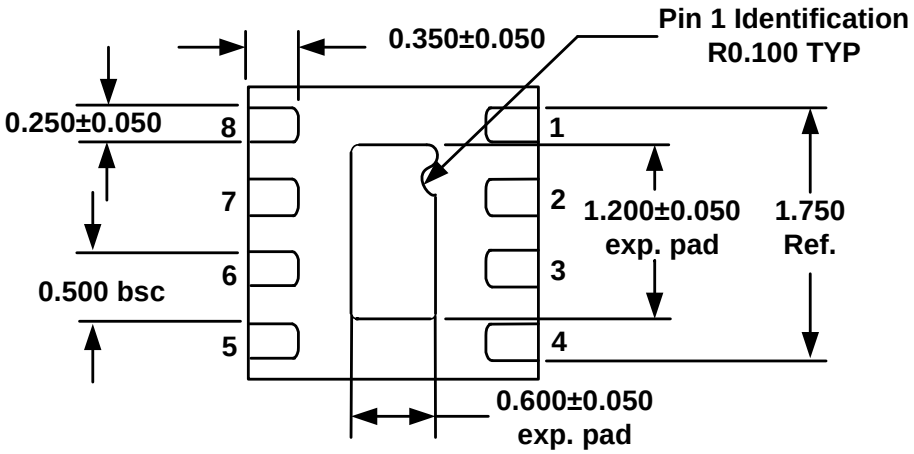

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

| DIM | MILLIMETERS | |
|---|---|---|
| | MIN | MAX |
| **A** | | 1.10 |
| **$A_1$** | 0.05 | 0.15 |
| **$A_2$** | 0.80 | 0.95 |
| **$A_3$** | 0.25 | |
| **$b_p$** | 0.25 | 0.45 |
| **c** | 0.15 | 0.28 |
| **D** | 2.90 | 3.10 |
| **E** | 2.90 | 3.10 |
| **e** | 0.65 | |
| **$H_E$** | 4.70 | 5.10 |
| **L** | 0.94 | |
| **$L_p$** | 0.40 | 0.70 |
| **v** | 0.10 | |
| **w** | 0.10 | |
| **y** | 0.10 | |
| **Z** | 0.35 | 0.70 |
| **θ** | $0^O$ | $6^O$ |

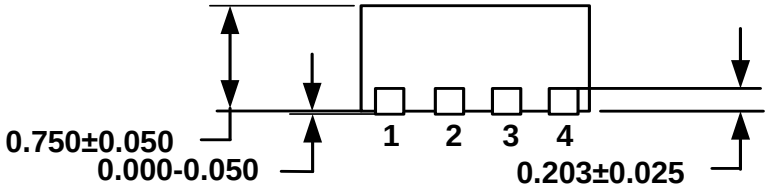
## PACKAGE DIAGRAM
## MLP 8 2x2mm




TOP VIEW




BOTTOM VIEW




SIDE VIEW

**Note: All dimensions are in mm**

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