DATA SHEET

ABT22V10A5, A7

5V high-speed universal PLD device with live insertion capability

Product specification

1996 Dec 16

IC13 Data Handbook

PHILIPS

5V high-speed universal PLD device with live insertion capability

ABT22V10A5, A7

DESCRIPTION

The ABT22V10A is a versatile PAL® device fabricated on Philips BiCMOS process known as QUBiC.

The QUBiC process produces very high speed, 5 volt devices (5.0ns) which have excellent noise immunity. The ground bounce of an output held low while the 9 remaining outputs are switching is less than 1.0V (typical).

The ABT22V10A outputs are designed to support Live Insertion/Extraction into powered-up systems. The output is specially designed so that during V_{CC} ramp, the output remains 3-Stated until $V_{CC} \approx 2.1V$. At that time, the outputs become fully functional, depending upon device inputs. (See DC Electrical Characteristics, Symbol $I_{PU/PD}$, Page 4).

The ABT family of devices have virtually no ground bounce— less than 1.0 volts V_{OLP}, measured on an unswitched output (9 remaining outputs switching, each with a 50pF load tied to ground).

The ABT family of devices has been designed with high drive outputs (48mA sink and 16mA source currents), which allow for direct connection to a backplane bus. This feature eliminates the need for additional, standalone bus drivers, which are traditionally required to boost the drive of a standard 16/–4mA PLDs.

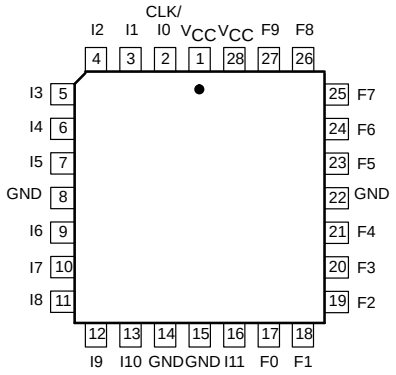
Philips has developed a new means of testing the integrity of fuses, both blown and intact fuses, which insures that all the fuses have been correctly programmed and that each and every fuse—whether “blown” or “intact”—is at the appropriate and optimal fuse resistance. This dual verify scheme represents a significant improvement over single reference voltage comparison schemes that have been used for bipolar devices since the late 1980’s.

The ABT22V10A uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-products equations.

This device has a programmable AND array, which drives a fixed OR array. The OR sum-of-products feeds an “Output Macro Cell” (OMC) that can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback.

PIN CONFIGURATIONS

A Package



A = Plastic Leaded Chip Carrier

SP00367

PIN LABEL DESCRIPTIONS

SYMBOL	FUNCTION
I1 – I11	Dedicated Input
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V_{CC}	Supply Voltage
GND	Ground

FEATURES

- Fastest 5V 22V10
- Low ground bounce (<1.0V typical)
- Live insertion/extraction permitted
- High output drive capability: 48mA/–16mA
- Varied product term distribution with up to 16 product terms per output for complex functions
- Metastable hardened flip-flops
- Programmable output polarity
- Design support provided for third party CAD development and programming hardware
- Improved fuse verification circuitry increases reliability

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		DRAWING NUMBER
28-Pin Plastic Leaded Chip Carrier	ABT22V10A5A ABT22V10A7A	(5ns device) (7.5ns device)	SOT261-3

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage[2]	–0.5	+7.0	V_{DC}
V_{IN}	Input voltage[2]	–1.2	V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	–0.5	V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. Except in programming mode.

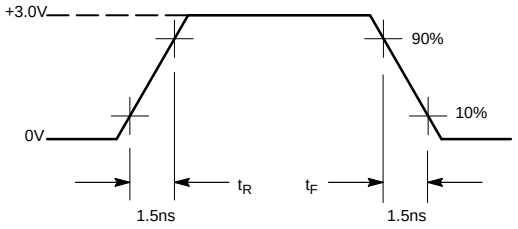
OPERATING RANGES

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

VOLTAGE WAVEFORM

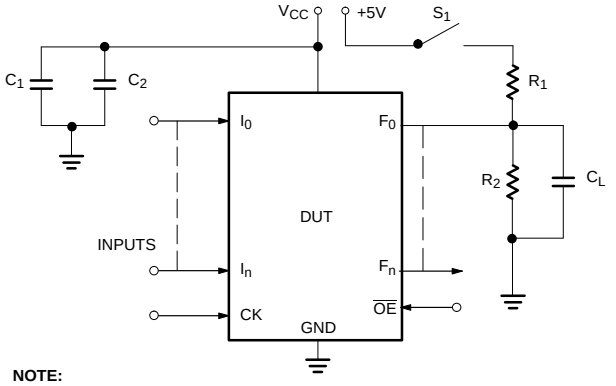


MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

SP00368

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

SP00369

DC ELECTRICAL CHARACTERISTICS

Over operating ranges.

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS		UNIT
				MIN	MAX	
Input voltage						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX		2.0		V
V_I	Clamp	V_{CC} = MIN, I_{IN} = –18mA			–1.2	V
Output voltage						
V_{OH}	High-level output voltage	V_{CC} = MIN V_I = V_{IH} or V_{IL}	I_{OH} = –32mA	2.0		V
			I_{OH} = –16mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN V_I = V_{IH} or V_{IL}	I_{OL} = 48mA		0.5	V
Input current						
I_{IL}	Low	V_{CC} = MAX, V_{IN} = 0.4V			–10	µA
I_{IH}	High	V_{CC} = MAX, V_{IN} = 2.7V			10	µA
I_I	Max input current	V_{CC} = MAX, V_{IN} = 5.5V			20	µA
Output current						
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} <2.1V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; OE/$\overline{OE}$ = X			50	µA
		V_{CC} = MAX				
I_{OZH}	Output leakage[2]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} = 2.7V			20	µA
I_{OZL}	Output leakage[2]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} =0.4V			–20	µA
I_{SC}	Short circuit[3]	V_{OUT} = 0.5V		–30	–220	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX, Outputs enabled, V_I = V_{CC} or GND; I_O = 0			200	mA
Ground Bounce				**TYP**	**MAX**	**UNIT**
V_{OLP}	Minimum dynamic V_{OH} [5]	V_{CC} = MAX, 25°C C_L = 50pF (including jig capacitance)		1.0	1.2	V

NOTES:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
3. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. This parameter is valid for any V_{CC} between 0V and 1.2 V with a transition time up to 10 mS. From V_{CC} = 1.2 to V_{CC} = 5.0V ±0.25V a transition time of 100 µS is permitted. X = Don't care.
5. Guaranteed by design, but not tested. Measured holding one output (the output under test) Low and simultaneously switching all remianing output from a High to a Low state. Switch S1 is closed; 50pF load.

AC ELECTRICAL CHARACTERISTICS[1]

$4.75V \le V_{CC} \le 5.25V$; $0°C \le T_{amb} \le +75°C$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS						UNIT
				ABT22V10A5			ABT22V10A7			
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to non-registered output[2]	Active-LOW		2.0	4.5	5.0	2.0	6.0	7.5	ns
		Active-HIGH		2.0	4.5	5.0	2.0	6.0	7.5	ns
t_S	Setup time from input or SP to Clock			2.0	1.3		3.5	3.0		ns
t_{SIO}	Setup time from feedback to Clock			2.25	1.5		3.5	3.0		ns
t_H	Hold time			0			0			ns
t_{SKEWR}	Skew between registered outputs [4, 7]					1.0			1.0	ns
t_{CO}	Clock to output			2.0	3.5	4.0	2.0	4.5	5.5	ns
t_{CF}	Clock to feedback[3]				2.0	4.0		3.0	5.0	ns
t_{AR}	Asynchronous Reset to registered output					10.0			10.0	ns
t_{ARW}	Asynchronous Reset width			6.0			7.5			ns
t_{ARR}	Asynchronous Reset recovery time			4.0			5.5			ns
t_{SPR}	Synchronous Preset recovery time			4.5			5.0			ns
t_{WL}	Width of Clock LOW			2.0			3.0			ns
t_{WH}	Width of Clock HIGH			2.0			3.0			ns
f_{MAX}	Maximum frequency; External feedback $1/(t_S + t_{CO})$[4]			167	208		111	133		MHz
	Maximum frequency; Internal feedback $1/(t_S + t_{CF})$[4]			167	303		125	166		MHz
t_{EA}	Input to Output Enable[5]					8.0			8.0	ns
t_{ER}	Input to Output Disable[5]					7.5			7.5	ns
Capacitance[6]										
C_{IN}	Input Capacitance (Pin 2)	V_{IN} = 2.0V	V_{CC} = 5.0V, T_{amb} = 25°C, f = 1MHz		8			8		pF
	Input Capacitance (Others)	V_{IN} = 2.0V			4			4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V			8			8		pF

NOTES:

1. Test Conditions: $R_1 = 300\Omega$, $R_2 = 390\Omega$
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$ (including jig capacitance). $V_{IH} = 3V$, $V_{IL} = 0V$, $V_T = 1.5V$.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_{L\,=}$ 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} – 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
7. Skew is measured with all outputs switching in the same direction.

PRODUCT FEATURES

Low Ground Bounce

The Philips Semiconductors BiCMOS QUBiC process produces exceptional noise immunity. The typical ground bounce, with 9 outputs simultaneously switching and the 10th output held low, is less than 1.0V. V_{OLP} is tested by holding one output (the output uncer test) in the Low state and then simultaneously switching all remaining outputs from a High to a Low state (each output is loaded with 50pF). The maximum peak voltage on the output under test is guaranteed to be less than 1.2 Volts.

Live Insertion/Extraction Capability

There are some inherent problems associated with inserting or extracting an unpowered module from a powered-up, active system. The ABT22V10A outputs have been designed such that any chance of bus contention, glitching or clamping is eliminated.

Detailed information on this feature is provided in an application note AN051: *Philips PLDs Support Live Insertion Applications*.

Improved Fuse Verification Circuitry Increases Reliability

Philips has developed a new means of testing the integrity of fuses, both blown and intact fuses, which insures that all the fuses have been correctly programmed and that each and every fuse – whether “blown” or “intact” – is at the appropriate and optimal fuse resistance. This dual verify scheme represents a significant improvement over single reference voltage comparisons schemes that have been used for bipolar devices since the late 1980s. Detailed information on this feature is provided in an application note entitled *Dual Verify Technique Increases Reliability of PLDs*.

Programmable 3-stage Outputs

Each output has a 3-Stage output buffer with 3-State control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macro cell output can be Active-HIGH or Active-LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save “DeMorganizing” efforts.

Selection is controlled by programmable bit S_0 in the Output Macro Cell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be Active-HIGH (S_0 = 1).

Preset/Reset

For initialization, the ABT22V10A has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW, independent of the clock.

Note that Preset and Reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the ABT22V10A will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1–10µs maximum.

Security Fuse

After programming and verification, ABT22V10A designs can be secured by programming the security fuse link. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The ABT22V10A offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies programmability and functionality of the device to provide the highest programming and post-programming functional yields.

Technology

The BiCMOS ABT22V10A is fabricated with the Philips Semiconductors process known as QUBiC. QUBiC combines an advanced, state-of-the-art 1.0µm (drawn feature size) CMOS process with an ultra fast bipolar process to achieve superior speed and drive capabilities. QUBiC incorporates three layers of Al/Cu interconnects for reduced chip size, and our proven Ti-W fuse technology ensures highest programming yields.

Programming

The ABT22V10A is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ CUPL™ and PALASM® 90 design software packages also support the ABT22V10A architecture.

All packages allow Boolean and state equation entry formats, SNAP, ABEL and CUPL also accept, as input, schematic capture format.

Output Register Preload

The register on the ABT22V10A can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. The procedure for preloading follows:

1. Raise V_{CC} to 5.0V ± 0.25V.
2. Set pin 2 or 3 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock Pin 1 from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower pin 2 or 3 to V_{ILP}.
7. Enable the output registers according to the programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.

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CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

Metastable Characteristics

Philips provides complete data on the ABT22V10A5's metastable characteristics. While the ABT22V10A5 **does not** employ Philips patented metastable immune flip-flop, its metastabel characteristics are still quite favorable relative to competitive devices. For information on metastable immune PLDs, refer to the datasheets for the ABT22V10-7 for 5V applications or the LVT22V10-7 for 3.3V designs.

Design Example

Suppose a designer wants to use the ABT22V10A5 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), in a 5V system that has a clock frequency of 50MHz, at an ambient temperature of 25°C. The next device in the sytem samples the output fo the ABT22V10A5 5.5ns after the clock edge to ensure that any metastable conditions that occur have time to resolve to the correct state. The MTBF for this situatio can be calcuclated by using the equation below:

$$MTBF = e(t'/\tau)/T_0F_CF_1$$

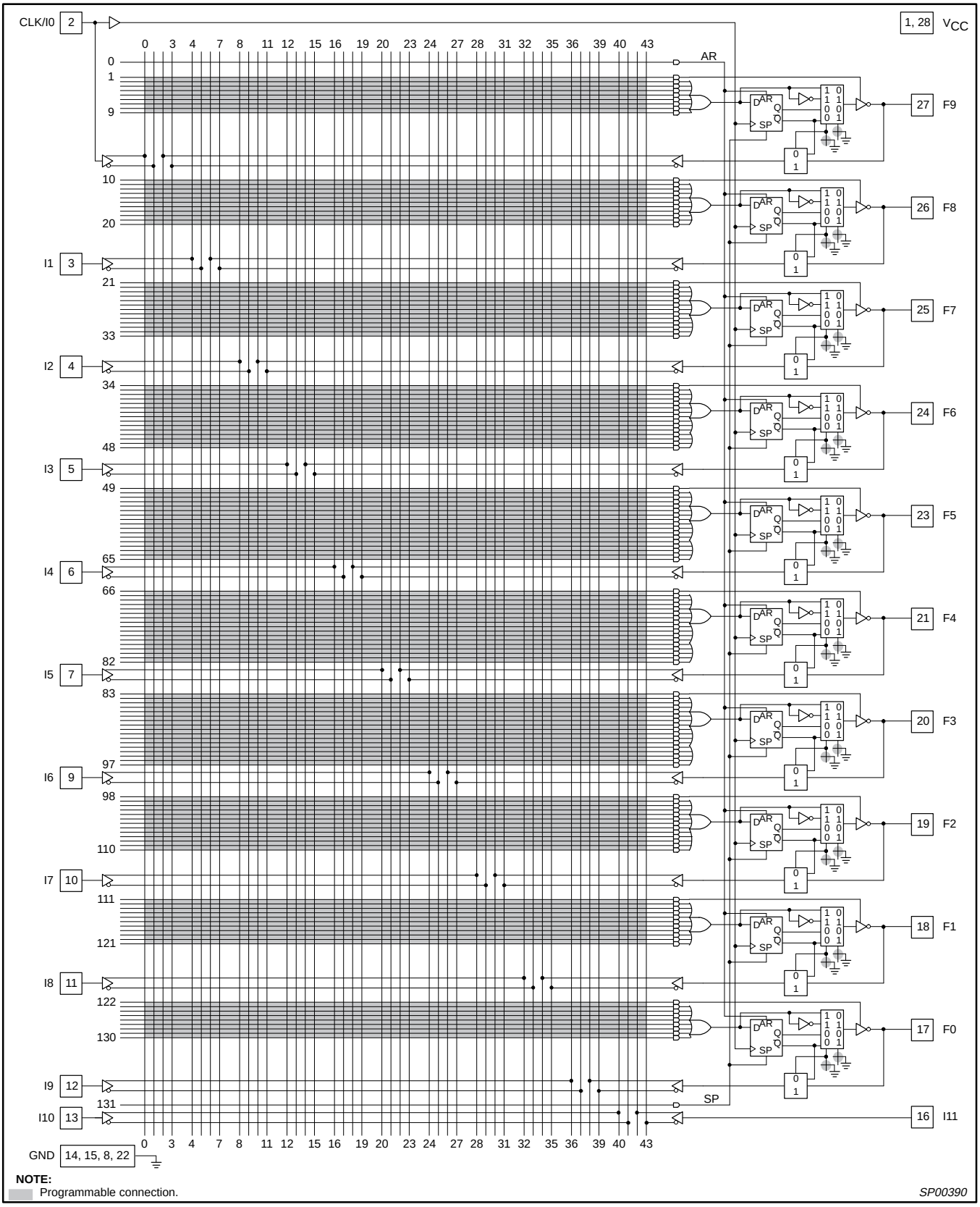
In this formula, F_C is the frequency of the clock, F_1 is the average input event frequency, and t' is the time after the clock pulse that the output is sampled ($t' > T_{CO}$). T_0 and τ are device parameters provided by the semiconductor manufacturer (refer to Table 1 for the ABT22V10A5 metastability specifications). T_0 and τ are derived from tests and can be most nearly be defined as follows: τ is a function of the rate at which a latch in a metastable state resolves that condition. T_0 is a function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a normalization constant which is a very strong function of the normal propagation dely of the device.

In this situation, the F_1 will be twice that data frequency, or 20MHz, because input events consist of both low and high transitions. Thus in this case F_C is 50MHz, F_1 is 20MHz, τ is 85.6ps, t' is 5.5ns, and T_0 is 4.55 seconds. Using the above formula, the actual MTBF for this situation is 1.76×10^{12} seconds, or 55,889 years for the ABT22V10A5.

Table 1. Typical Values for τ and T_0 at various V_{CC}'s and Temperatures

	0°C		+25°C		+75°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.25V	72.00ps	7.20E+01	96.70ps	4.59E–01	105.00ps	1.43E–01
5.00V	72.80ps	2.06E+02	85.60ps	4.55E+00	100.00ps	8.37E–01
4.75V	68.70ps	9.97E+03	81.70ps	4.85E+01	99.80ps	1.29E+00

LOGIC DIAGRAM



NOTE:
Programmable connection.

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FUNCTIONAL DIAGRAM

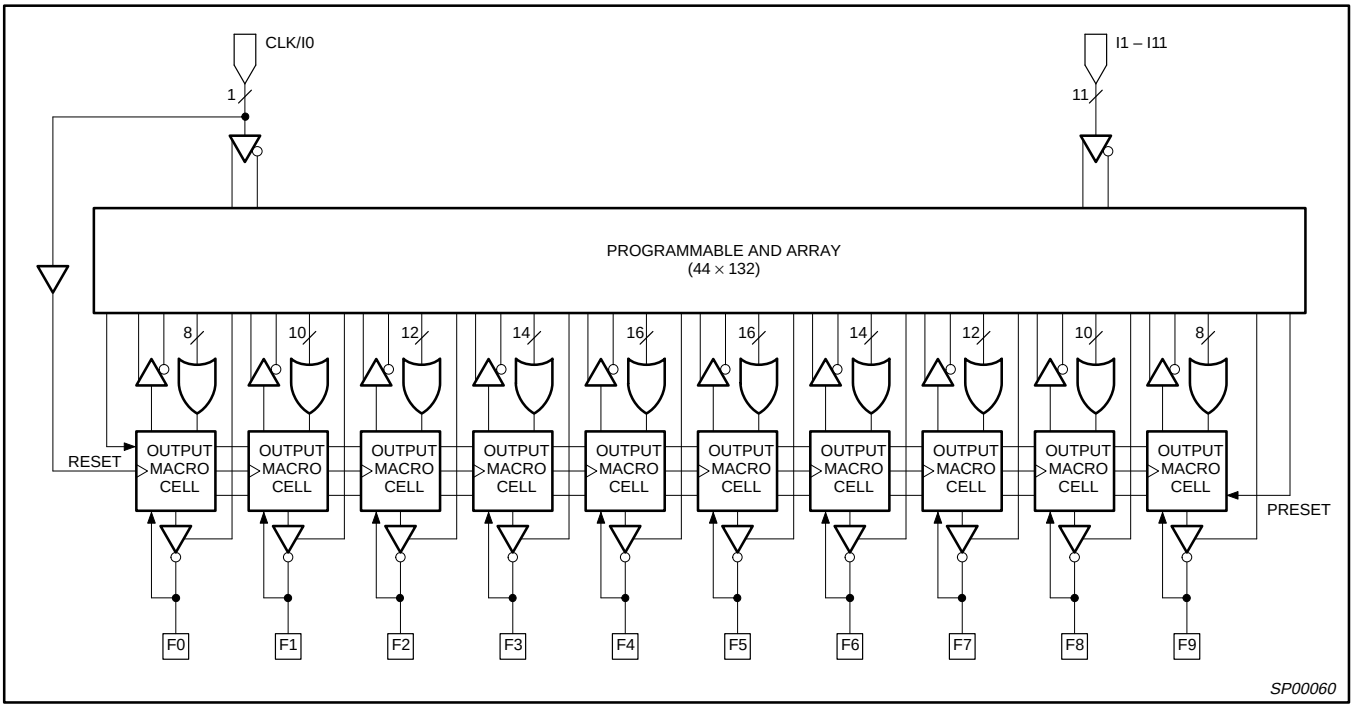


Figure 1. Functional Diagram

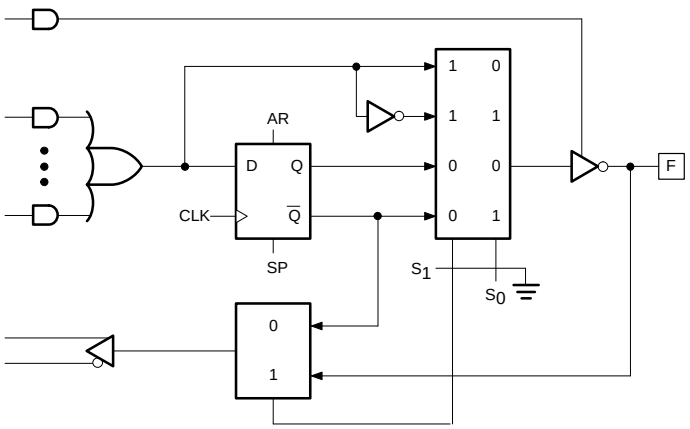
FUNCTIONAL DESCRIPTION

The ABT22V10A allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both True and Complement of any single input assume the logical LOW state.

The ABT22V10A has 12 inputs and 10 I/O Macro Cells (Figure 1). The Macro Cell allows one of four potential output configurations, registered output or combinatorial I/O, Active-HIGH or Active-LOW (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 –S_1. Multiplexer controls are connected to ground (0) through a programmable fuse link, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

OUTPUT MACRO CELL

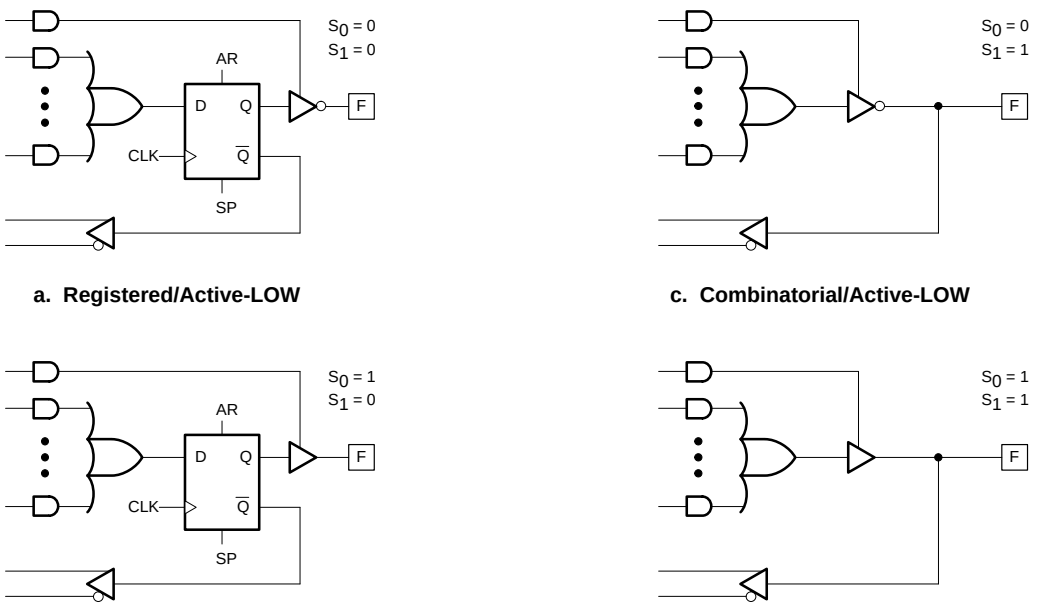


S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW
0	1	Registered/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed fuse
1 = Programmed fuse

SP00375

Figure 2. Output Macro Cell Logic Diagram



SP00376

Figure 3. Output Macro Cell Configurations

Registered Output Configuration

Each Macro Cell of the ABT22V10A includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration (S_1 = 0), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

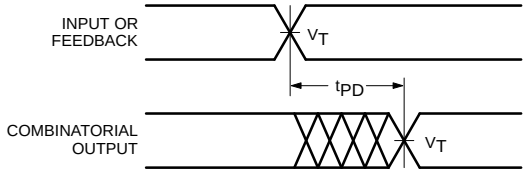
Any Macro Cell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop (S_1 = 1). In the combinatorial configuration, the feedback is from the pin.

Variable Input/Output Pin Ratio

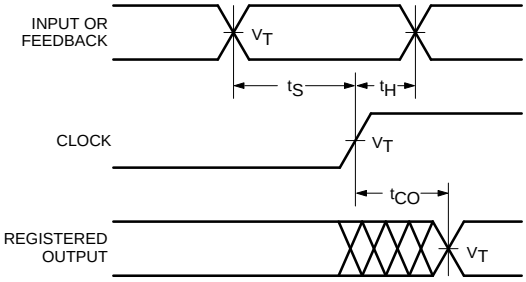
The ABT22V10A has twelve dedicated input lines, and each Macro Cell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity.

SWITCHING WAVEFORMS

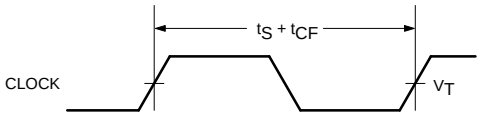
V_T = 1.5V.
Input pulse amplitude 0V to 3.0V.
Input rise and fall times 1.5ns max.



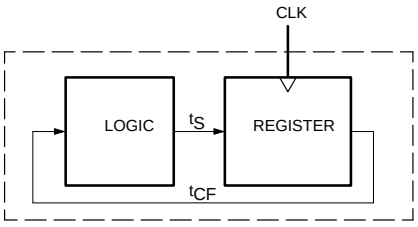
Combinatorial Output



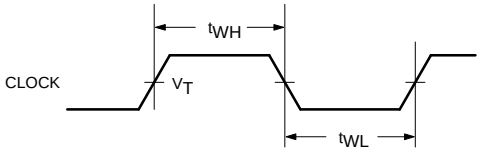
Registered Output



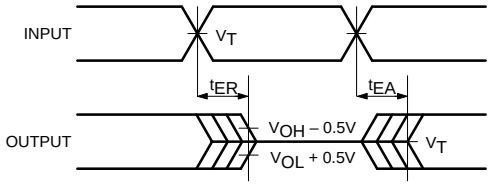
Clock to Feedback (f_{MAX} Internal) (See Path at Right)



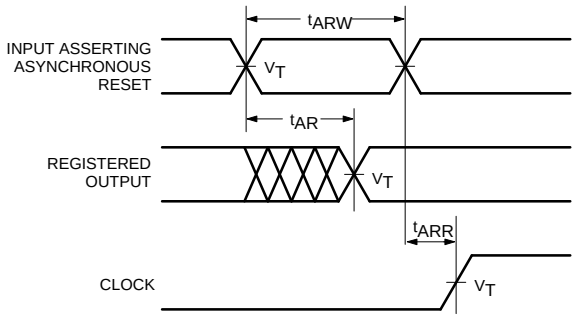
Clock to Feedback



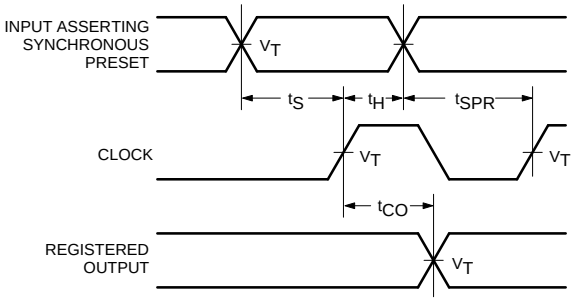
Clock Width



Input to Output Disable/Enable



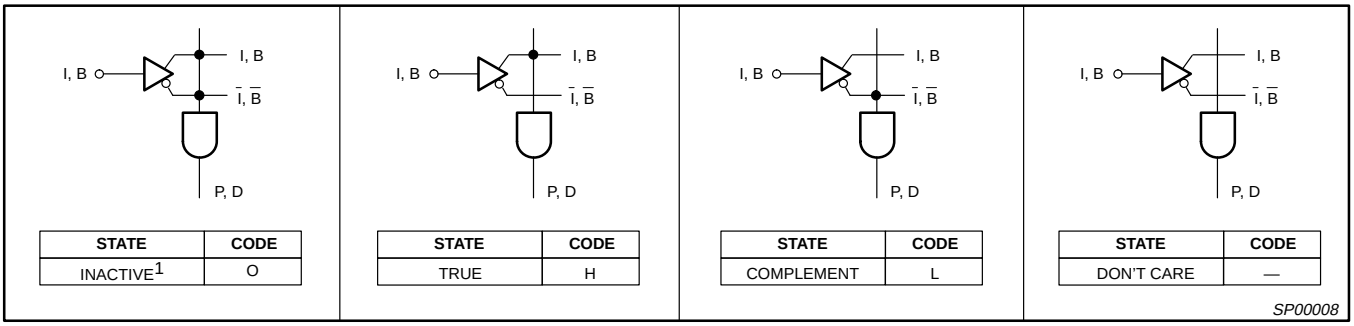
Asynchronous Reset



Synchronous Preset

SP00377

"AND" ARRAY – (I, B)



STATE	CODE
INACTIVE[1]	O

STATE	CODE
TRUE	H

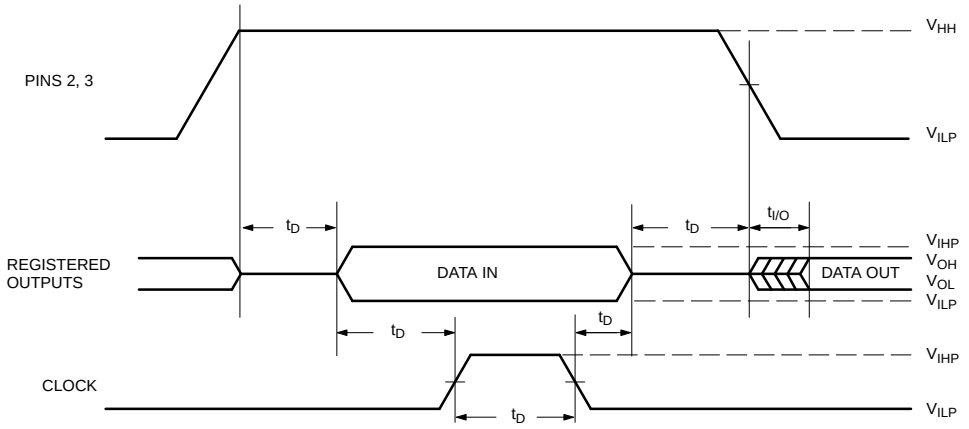
STATE	CODE
COMPLEMENT	L

STATE	CODE
DON'T CARE	—

NOTE:
1. This is the initial state.

PRELOAD SET-UP

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	REC	MAX	
V_{HH}	Super-level input voltage	9.5	9.5	10	V
V_{ILH}	Low-level input voltage	0	0	0.8	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	100	200	1000	ns
$t_{I/O}$	I/O valid after Pin 2 or 3 drops from V_{HH} to V_{ILP}	100			ns



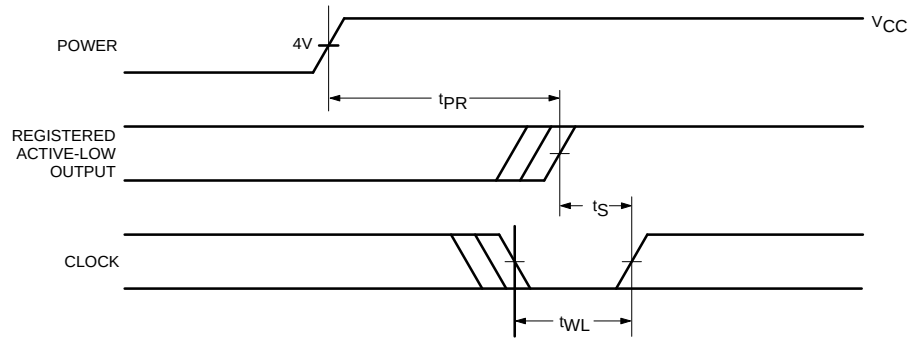
Output Register Preload Waveform

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t_{PR}	Power-up Reset Time		1	µs
t_S	Input or Feedback Setup Time	See AC Electrical Characteristics		
t_{WL}	Clock Width LOW			



Power-Up Reset Waveform

SP00066

OTHER PHILIPS 22V10 DEVICES

Philips offers a complete family of 22V10 devices, addressing a wide variety of design applications. This Features Matrix summarizes the basic features of each specific device.

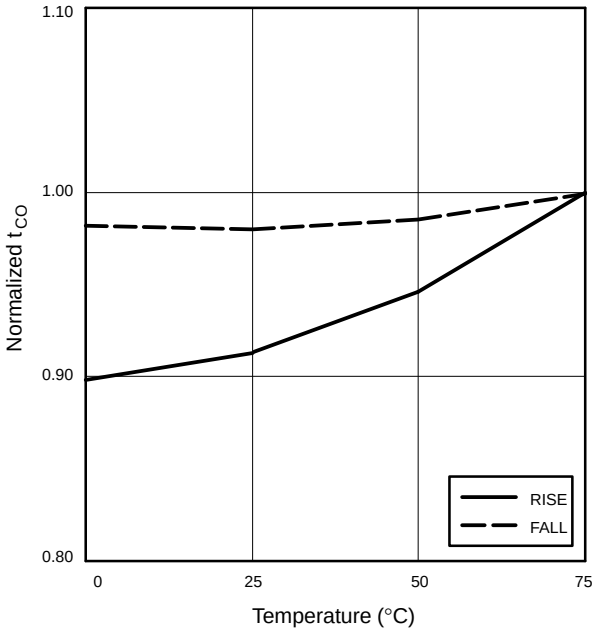
PHILIPS 22V10 FEATURES MATRIX

	PL22V10-10/-15	LVT22V10-7	ABT22V10-7	ABT22V10A5	ABT22V10A7
Operating supply voltage	+4.75 to +5.25V	+3.0 to +3.6V [1]	+4.75 to +5.25V	+4.75 to +5.25V	+4.75 to +5.25V
Live Insertion	No	Yes	No	Yes	Yes
Dual Verify	No	Yes	No	Yes	Yes
Metastability	No	Hardened	Immune	No	No
Source Drive Capability	4mA (V_{OH} = 2.4V)	16mA (V_{OH} = 2.0V)	16mA (V_{OH} = 2.4V)	16mA (V_{OH} = 2.4V)	16mA (V_{OH} = 2.4V)
Sink Drive Capability	16mA (V_{OL} = 0.5V)	32mA (V_{OL} = 0.5V)	48mA (V_{OL} = 0.5V)	48mA (V_{OL} = 0.5V)	48mA (V_{OL} = 0.5V)
Low Ground Bounce	No	Yes	Yes	Yes	Yes
Package Availability:					
Plastic Dual In-Line (N)	24-Pin	24-Pin	24-Pin	not available	not available
Plastic Leaded Chip Carrier (A)	24-Pin	28-Pin	28-Pin	28-Pin	28-Pin
Plastic Small Outline Large (D)	24-Pin	24-Pin	not available	not available	not available

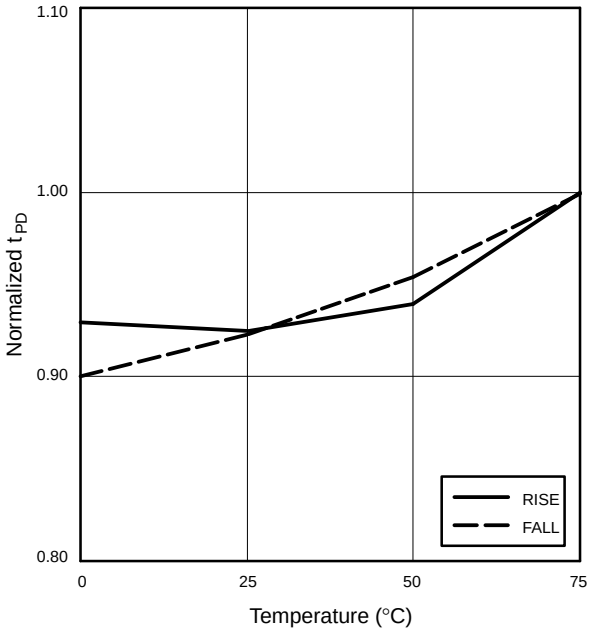
NOTE:
1. 5 volt compatible I/O. Inputs are capable of handling 7V and the outputs can also be pulled up to 7 volts.

ABT22V10A5 TIMING CHARACTERIZATION

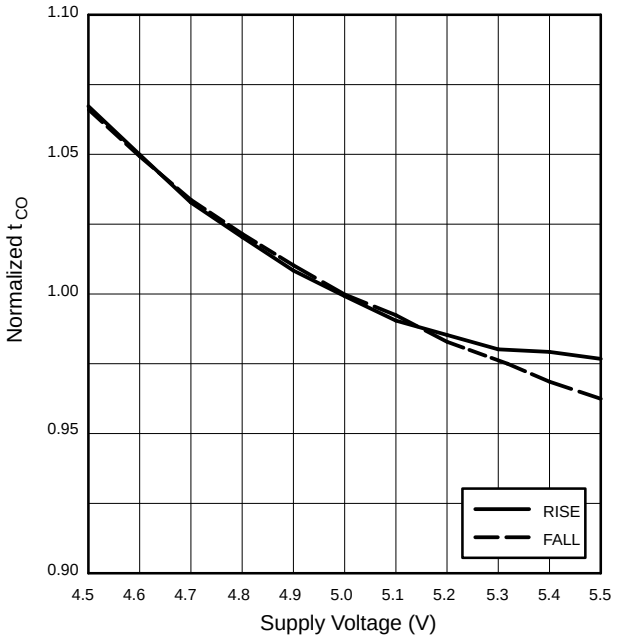
Normalized t_{CO} vs Temperature
(V_{CC} = 5.0V, output capacitance = 50pF, 5 outputs switching)



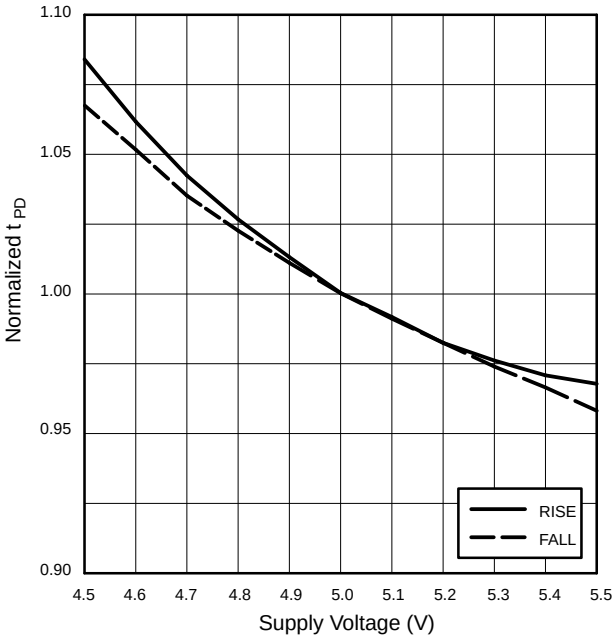
Normalized t_{PD} vs Temperature
(V_{CC} = 5.0V, output capacitance = 50pF, 5 outputs switching)



Normalized tCO vs VCC
(temp = 25°C, output capacitance = 50pF, 5 outputs switching)



Normalized tPD vs VCC
(temp = 25°C, output capacitance = 50pF, 5 outputs switching)

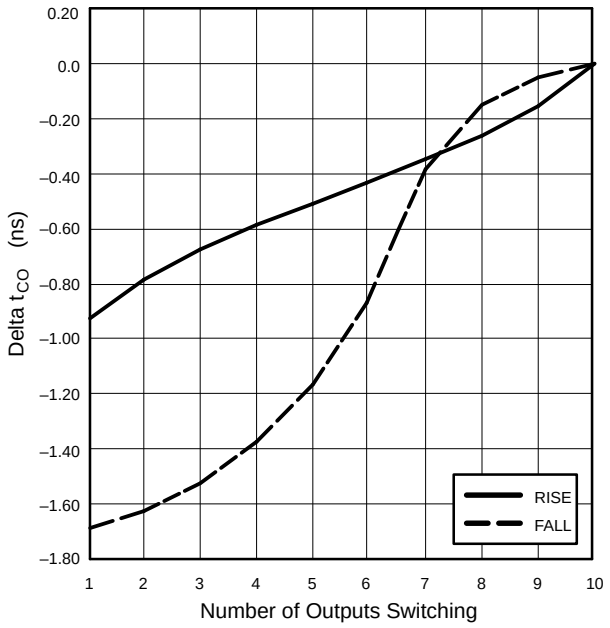


The timing characterization represents the average values of a representative sample for each parameter.
The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design.
Philips guarantees the MAX AC CHARACTERIZATION specifications.

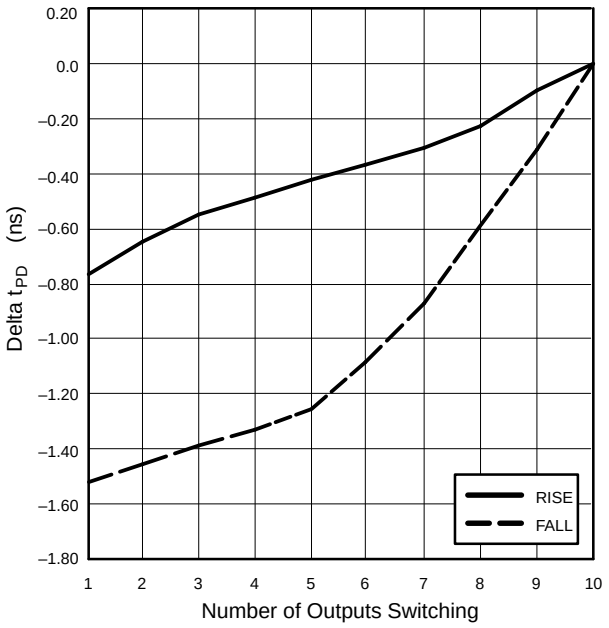
SP00370

ABT22V10A5 TIMING CHARACTERIZATION

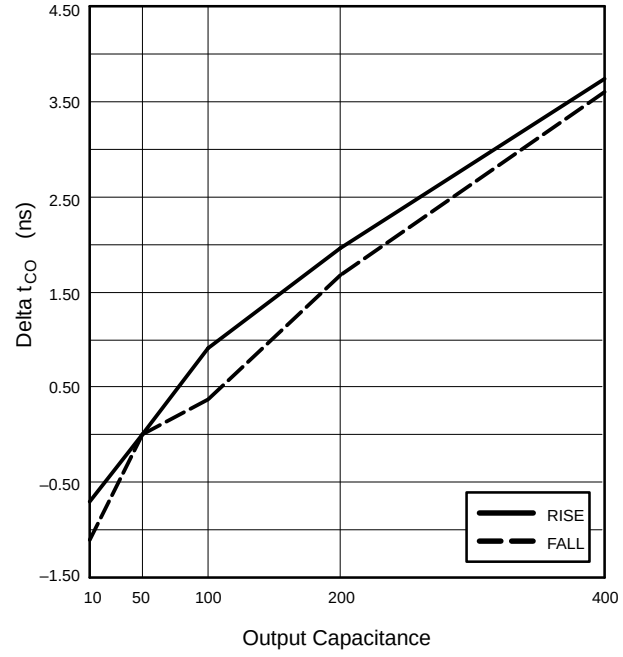
Delta t_{CO} vs Number of Outputs Switching (V_{CC} = 5.0V, temp = 25°C, output capacitance = 50pF)



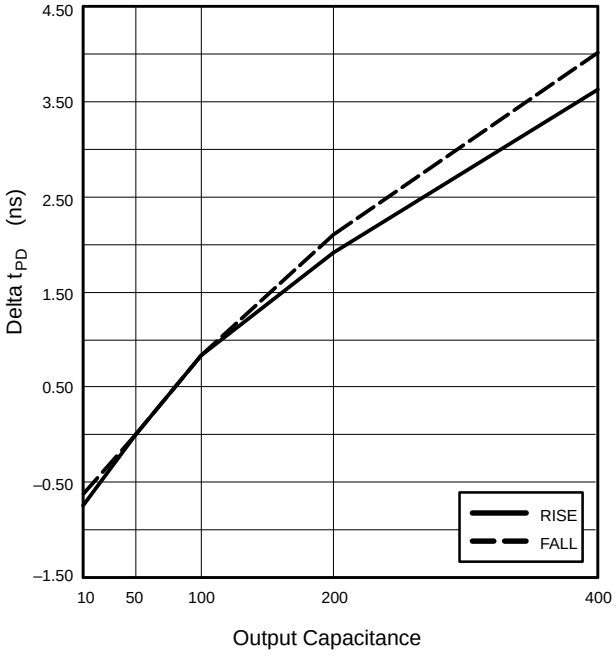
Delta t_{PD} vs Number of Outputs Switching (V_{CC} = 5.0V, temp = 25°C, output capacitance = 50pF)



Delta t_{CO} vs Output Capacitance (V_{CC} = 5.0V, temp = 25°C, 5 Outputs Switching)



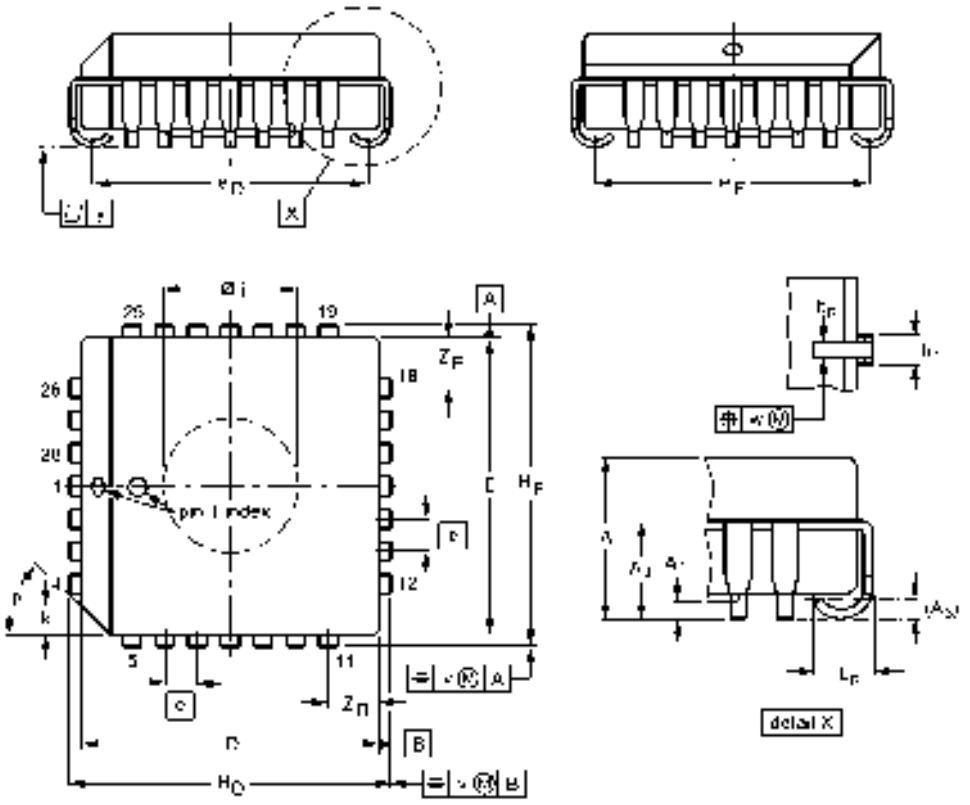
Delta t_{PD} vs Output Capacitance (V_{CC} = 5.0V, temp = 25°C, 5 Outputs Switching)

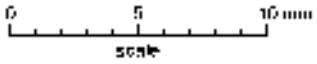


The timing characterization represents the average values of a representative sample for each parameter.
The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design.
Philips guarantees the MAX AC CHARACTERIZATION specifications.

SP00371

PLCC28: plastic leaded chip carrer; 28 leads; pedestal **SOT261-3**





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 (min.)	A_3	A_4 (max.)	b_p	b_1	D[1]	E[1]	e	e_D	e_E	H_D	H_E	k	k_1	L_p	v	w	y	Z_D[1] (max.)	Z_E[1] (max.)	β
mm	4.57 4.19	0.51	0.25	0.25	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	0.99 0.53	1.44 1.02	0.18	0.18	0.10	2.05	2.05	45°
inches	0.180 0.165	0.020	0.01	0.01	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.039 0.021	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT261-3		MO-047AB			92-11-17 95-02-25

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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