# 36 Vin to 60 Vin Cool-Power ZVS Buck Regulator & LED Driver

## Product Description

The PI354x-00 is a family of high input voltage, wide input range DC-DC ZVS-Buck regulators integrating controller, power switches, and support components all within a high density System-in-Package (SiP). The integration of a high-performance Zero-Voltage Switching (ZVS) topology, within the PI354x-00 series, increases point of load performance providing best in class power efficiency. The PI354x-00 requires only an external inductor, two voltage selection resistors and minimal capacitors to form a complete DC-DC switching mode buck regulator.

| Device | Output Voltage | | $I_{OUT}$ Max |
|---|---|---|---|
| | Set | Range | |
| PI3542-00-LGIZ | 2.5 V | 2.2 V to 3.0 V | 10 A |
| PI3543-00-LGIZ | 3.3 V | 2.6 V to 3.6 V | 10 A |
| PI3545-00-LGIZ | 5.0 V | 4.0 V to 5.5 V | 10 A |
| PI3546-00-LGIZ | 12 V | 6.5 V to 14 V | 9 A |

PI354x-00 Family can operate in constant voltage output for typical buck regulation applications in addition to constant current output for LED lighting and battery charging applications.

## Features

- High Efficiency HV ZVS-Buck Topology
- Wide input voltage range of 36 V to 60 V
- Very fast transient response
- Constant voltage or constant current operation
- Constant current error amplifier and reference
- Power-up into pre-biased load
- Parallel capable with single wire current sharing
- Two phase interleaving
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- Differential amplifier for output remote sensing
- User adjustable soft-start & tracking
- -40°C to 125°C operating range ($T_J$)

## Applications

- HV to PoL Buck Regulator Applications
- Computing, Communications, Industrial, Automotive Equipment
- Constant current output operation:
  - LED Lighting
  - Battery Charging

## Package Information

- 10 mm x 10 mm x 2.6 mm LGA SiP

## Contents

## Order Information

| Cool-Power | Output Range | | $I_{OUT}$ Max | Package | Transport Media |
|---|---|---|---|---|---|
| | Set | Range | | | |
| PI3542-00-LGIZ | 2.5 V | 2.2 V to 3.0 V | 10 A | 10 mm x 10 mm LGA | TRAY |
| PI3543-00-LGIZ | 3.3 V | 2.6 V to 3.6 V | 10 A | 10 mm x 10 mm LGA | TRAY |
| PI3545-00-LGIZ | 5.0 V | 4.0 V to 5.5 V | 10 A | 10 mm x 10 mm LGA | TRAY |
| PI3546-00-LGIZ | 12 V | 6.5 V to 14 V | 9 A | 10 mm x 10 mm LGA | TRAY |

## Thermal, Storage, and Handling Information

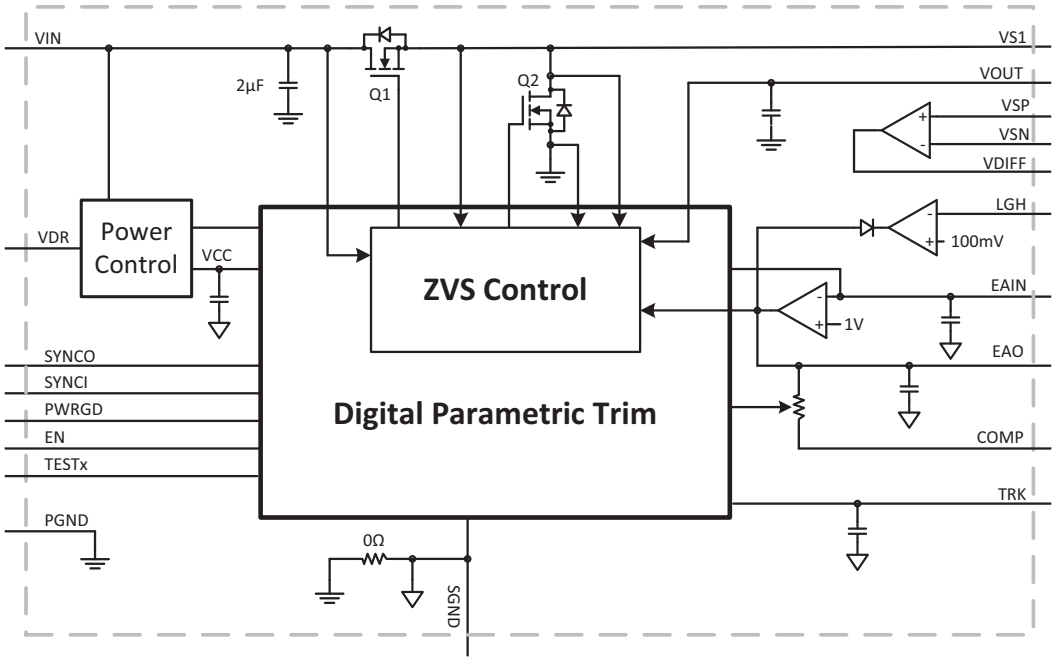
| Name | Rating |
|---|---|
| Storage Temperature | -65°C to 150°C |
| Operating Junction Temperature | -40°C to 125°C |
| Soldering Temperature for 20 seconds | 245°C |
| MSL Rating | 3 |

## Absolute Maximum Ratings

| Name | Rating |
|---|---|
| $V_{IN}$ | -0.7 V to 75 V |
| VS1 | -0.7 to 75 V, -4 V for 5 ns |
| $V_{OUT}$ | -0.5 V to 25 V |
| SGND | 100 mA |
| TRK | -0.3 V to 5.5 V / 30 mA |
| VDR, SYNCI, SYNCO, PWRGD, EN, LGH, COMP, EAO, EAIN, VDIFF, VSN, VSP, TESTx | -0.3 V to 5.5 V / 5 mA |

**Notes:** At 25°C ambient temperature. Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted.

## Functional Block Diagram

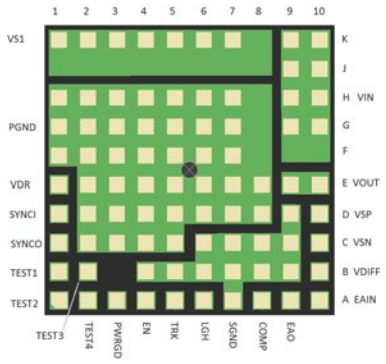



*Simplified Block Diagram*

## Pin Description

| Name | Location | I/O | Description |
|---|---|---|---|
| **VS1** | Block 2 (See Pkg Pin-Out dwg) | I/O | **Switching node:** and ZVS sense for power switches. |
| **VIN** | Block 1 | I | **Input voltage:** and sense for UVLO, OVLO and feed forward ramp. |
| **VDR** | 1E | I/O | **Gate Driver $V_{CC}$ :** Internally generated 5.1 V. May be used as reference or low power bias supply for up to 2 mA. Must be impedance limited by the user. |
| **SYNCI** | 1D | I | **Synchronization input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high impedance digital input node and should always be connected to SGND when not in use. |
| **SYNCO** | 1C | O | **Synchronization output:** Outputs a high signal for ½ of the minimum period for synchronization of other regulators. |
| **TESTx** | 1B, 1A, 2B, 2A | I/O | **Test Connections:** Use only with factory guidance. Connect to SGND for proper operation. |
| **PWRGD** | 3A | O | **Power Good:** High impedance when regulator is operating and $V_{OUT}$ is in regulation. May also be used as "Parallel Good" – see applications section. |
| **EN** | 4A | I | **Enable Input:** Regulator enable control. Asserted high or left floating – regulator enabled; asserted low, regulator output disabled. |
| **TRK** | 5A | I | **Soft-start and track input:** An external capacitor may be connected between TRK pin and SGND to decrease the rate of rise during soft-start. |
| **LGH** | 6A | I | **Lighting (LGH)/Constant Current (CC) Sense Input:** Input with a 100 mV threshold. Used for lighting and constant current type applications.When not using the constant current mode (CC mode), the LGH pin should be connected to SGND. |
| **COMP** | 8A | O | **Compensation Capacitor:** Connect capacitor for control loop dominant pole. |
| **EAO** | 9A | O | **Error amp output**: External connection for additional compensation and current sharing. |
| **EAIN** | 10A | I | **Error Amp Inverting Input:** Connection for the feedback divider tap. |
| **VDIFF** | 10B | O | **Independent Amplifier Output:** If unused connect in unity gain with VSP connected to SGND. |
| **VSN** | 10C | I | **Independent Amplifier Inverting Input** |
| **VSP** | 10D | I | **Independent Amplifier Non-Inverting Input** |
| **VOUT** | 9E, 10E | I/O | **Output voltage:** and sense for power switches and feed-forward ramp. |
| **SGND** | Block 4 | - | **Signal ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO communication returns. SGND and PGND are star connected within the regulator package. |
| **PGND** | Block 3 | - | **Power ground:** $V_{IN}$ and $V_{OUT}$ power returns. |

## Package Pin-Out




**85 Pad LGA Sip (10 mm x 10mm)**
**(Top through view)**

**Block 1:** $V_{IN}$; K9-10, J9-10, H9-10, G9-10

**Block 2:** VS1; K1-7

**Block 3:** PGND; H1-7, G1-7,F1-7, E2-8, D2-8, C2-5

**Block 4:** SGND; D9, C6-9, B4-9, A7

## PI354x-00 Common Electrical Characteristics

Specifications apply for -40°C <$T_J$ < 125°C, $V_{IN}$ = 48 V, EN = High, $V_{VDR}$ = 5.1 V +/- 2%, L1 = 340 nH [1] unless other conditions are noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Differential Amp** | | | | | | |
| Open Loop Gain | | | 96 | 120 | 140 | dB |
| Small Signal Gain-bandwidth | | | 5 | 7 | 12 | MHz |
| Offset | | | -1 | 0.5 | 1 | mV |
| Common Mode Input Range | | | -0.1 | | 2.5 | V |
| Differential Mode Input Range | | | | | 2 | V |
| Input Bias Current | | | -1 | | 1 | µA |
| Maximum $V_{OUT}$ | | $I_{DIFF}$ = -1 mA | $V_{VDR}$ -0.2 | | | V |
| Minimum $V_{OUT}$ | | | | | 20 | mV |
| Capacitive Load Range for Stability | | | 0 | | 50 | pF |
| Slew Rate Rising | | | | 11 | | V/µsec |
| Slew Rate Falling | | | | 11 | | V/µsec |
| Sink/Source Current | | | -1 | | 1 | mA |
| **Current Source Function (LGH)** | | | | | | |
| Reference | | | 95 | 100 | 105 | mV |
| Input Offset | | | | 0.5 | | mV |
| Gain-Bandwidth Product | | | 3 | | | MHz |
| Internal Feedback Capacitance | | | | 20 | | pF |
| **Gain Amp** | | | | | | |
| Gain | | | | 10 | | V/V |
| Intermediate Reference | | | | 1 | | V |
| Gain-Bandwidth Product | | | 3 | | | MHz |
| Transconductance | | | | 1 | | mS |
| Output Current Capability | | Sink current only | 1 | | | mA |
| **PGD** | | | | | | |
| PGD Rising Threshold | $V_{PG\_HI\%}$ | [2] | 79 | 85 | 91 | % $V_{OUT\_DC}$ |
| PGD Falling Threshold | $V_{PG\_LO\%}$ | [2] | 77 | 83 | 89 | % $V_{OUT\_DC}$ |
| PGD Output Low | $V_{PG\_SAT}$ | Sink = 4 mA [2] | | | 0.4 | V |
| PGD Sink Current | $I_{PG\_SAT}$ | [2] | | 4 | | mA |

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

## PI3542-00 (2.5 $V_{OUT}$) Electrical Characteristics

Specifications apply for -40°C <$T_J$ < 125°C, $V_{IN}$ = 48 V, $V_{VDR}$ = 5.1 V +/- 2%, L1 = 340 nH [1] unless other conditions are noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Input Specifications** | | | | | | |
| Input Voltage | $V_{IN\_DC}$ | | 36 | 48 | 60 | V |
| Input Current | $I_{IN\_DC}$ | $V_{IN}$ = 48 V, $T_C$ = 25°C, $I_{OUT}$ = 10 A | | 0.597 | | A |
| Input Current At Output Short (fault condition duty cycle) | $I_{IN\_Short}$ | Short at terminals | | 3.1 | - | mA |
| Input Quiescent Current | $I_{Q\_VIN}$ | Disabled | | 1.27 | | mA |
| | | Enabled (no load) | | 2.42 | | |
| Input Voltage Slew Rate | $V_{IN\_SR}$ | | | | 1 | V/µs |
| **Output Specifications** | | | | | | |
| EAIN Voltage Total Regulation | $V_{OUT\_DC}$ | [2] | 0.985 | 1.00 | 1.015 | V |
| Output Voltage Trim Range | $V_{OUT\_DC}$ | [2][3] | 2.2 | 2.5 | 3.0 | V |
| Line Regulation | $\Delta V_{OUT}(\Delta V_{IN})$ | @ 25°C, 36 V <$V_{IN}$ <60 V | | 0.10 | | % |
| Load Regulation | $\Delta V_{OUT}(\Delta I_{OUT})$ | @ 25°C, 0.5 A <$I_{OUT}$ <10 A | | 0.10 | | % |
| Output Voltage Ripple | $V_{OUT\_AC}$ | $I_{OUT}$ = 10 A, $C_{OUT}$ = 6 x 100 µF, 20 MHz BW [4] | | 47 | | mVp-p |
| Output Current | $I_{OUT\_DC}$ | [5] | 0 | | 10 | A |
| Current Limit | $I_{OUT\_CL}$ | L1 = 340 nH ±1% | - | 12 | - | A |
| **Protection** | | | | | | |
| Input UVLO Start Threshold | $V_{UVLO\_START}$ | | 33.8 | 34.8 | 35.8 | V |
| Input UVLO Stop Hysteresis | $V_{UVLO\_HYS}$ | | | 0.9 | | V |
| Input UVLO Response Time | | | | 1.25 | | usec |
| Input OVLO Stop Threshold | $V_{OVLO}$ | | 62 | 64.3 | 66.2 | V |
| Input OVLO Start Hysteresis | $V_{OVLO\_HYS}$ | | | 1.3 | | V |
| Input OVLO Response Time | $t_f$ | | | 1.25 | | usec |
| Output Overvoltage Protection | $V_{OVP}$ | Above set $V_{OUT}$ | | 20 | | % |
| Overtemperature Fault Threshold | $T_{OTP}$ | | | 130 | | °C |
| Ovetemperature Restart Hysteresis | $T_{OTP\_HYS}$ | | | 30 | | °C |
| **Timing** | | | | | | |
| Switching Frequency | $f_S$ | [6] 48 $V_{IN}$ to 2.5 $V_{OUT}$, 3 A out, L1 = 30 nH ±1% | - | 400 | - | kHz |
| Fault Restart Delay | $t_{FR\_DLY}$ | | | 30 | | ms |
| **Sync In (SYNCI)** | | | | | | |
| Synchronization Frequency Range | $\Delta f_{SYNCI}$ | Relative to set switching frequency [3] | 50 | | 110 | % |
| SYNCI Threshold | $V_{SYNCI}$ | | | $V_{VDR}$/2 | | V |

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

## PI3542-00 (2.5 $V_{OUT}$) Electrical Characteristics

Specifications apply for -40°C <$T_J$ < 125°C, $V_{IN}$ = 48 V, $V_{VDR}$ = 5.1 V +/- 2%, L1 = 340 nH [1] unless other conditions are noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Sync Out (SYNCO)** | | | | | | |
| SYNCO High | $V_{SYNCO\_HI}$ | Source 1 mA | $V_{VDR}$ –0.5 | | | V |
| SYNCO Low | $V_{SYNCO\_LO}$ | Sink 1 mA | | | 0.5 | V |
| SYNCO Rise Time | $t_{SYNCO\_RT}$ | 20 pF load | | 10 | | ns |
| SYNCO Fall Time | $t_{SYNCO\_FT}$ | 20 pF load | | 10 | | ns |
| **Soft Start, Tracking and Error Amplifier** | | | | | | |
| TRK Active Range (Nominal) | $V_{TRK}$ | | 0 | | 1.08 | V |
| TRK Enable Threshold | $V_{TRK\_OV}$ | | 20 | 40 | 60 | mV |
| TRK to EAIN Offset | $V_{EIAN\_OV}$ | | 50 | 80 | 110 | mV |
| Charge Current (Soft – Start) | $I_{TRK}$ | | -70 | -50 | -30 | µA |
| Discharge Current (Fault) | $I_{TRK\_DIS}$ | $V_{TRK}$ = 0.5 V | | 10 | | mA |
| Soft-Start Time | $t_{SS}$ | $C_{TRK}$ = 0 | 0.6 | .94 | 1.6 | mS |
| Error Amplifier Trans-Conductance | GMeao | [2] | | 5.1 | | ms |
| PSM Skip Threshold | $PSM_{SKIP}$ | [2] | | 0.8 | | V |
| Error Amplifier Output Impedance | $R_{OUT}$ | [2] | 1 | | | MOhm |
| Internal Compensation Capacitor | Chf | [2] | | 56 | | pf |
| Internal Compensation Resistor | Rzi | [2] | | 5k | | Ohm |
| **Enable** | | | | | | |
| High Threshold | $V_{EN\_HI}$ | | 0.9 | 1 | 1.1 | V |
| Low Threshold | $V_{EN\_LO}$ | | 0.7 | 0.8 | 0.9 | V |
| Threshold Hysteresis | $V_{EN\_HYS}$ | | 100 | 200 | 300 | mV |
| Enable Pull-Up Voltage (floating, no faulted) | $V_{EN\_PU}$ | | | 2 | | V |
| Enable Pull-Down Voltage (floating, fault) | $V_{EN\_PD}$ | | | 0 | | V |
| Source Current | $I_{EN\_SO}$ | | | -50 | | µA |
| Sink Current | $I_{EN\_SK}$ | | | 50 | | µA |

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

## PI3542-00 (2.5 $V_{OUT}$) Electrical Characteristics

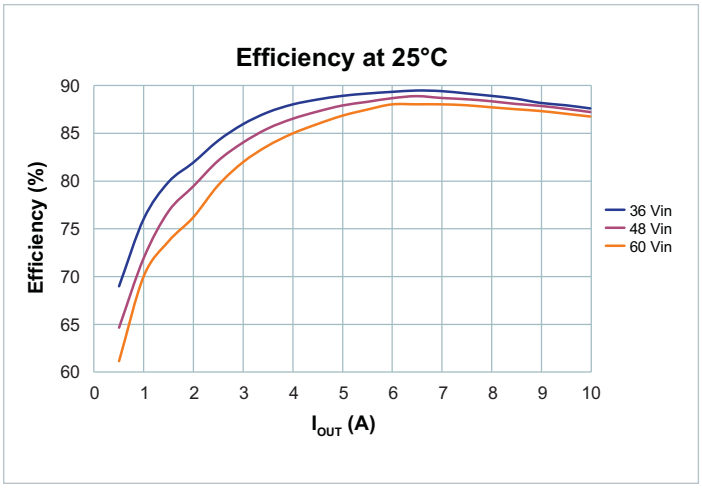



***Figure 1*** — *Regulator Efficiency*

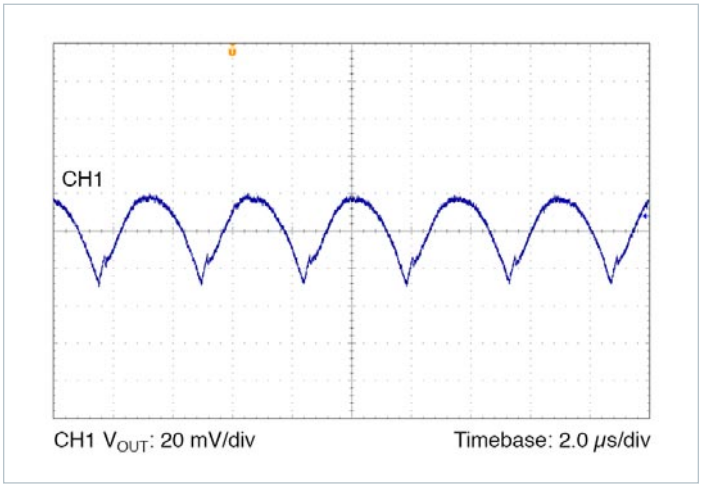



***Figure 4*** — *Output Ripple: 48 $V_{IN}$, 2.5 $V_{OUT}$ at 10 A. $V_{OUT}$ = 20 mV/Div, 2.0 µs/Div; $C_{OUT}$ = 6 x 100 µF Ceramic*

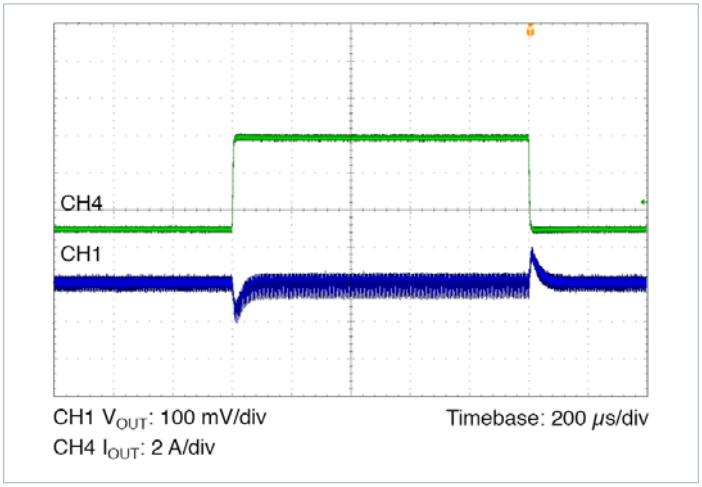



***Figure 2*** — *Transient Response: 5 A to 10 A, at 1 A/µs. 48 $V_{IN}$ to 2.5 $V_{OUT}$, $C_{OUT}$ = 6 x 100 µF Ceramic*

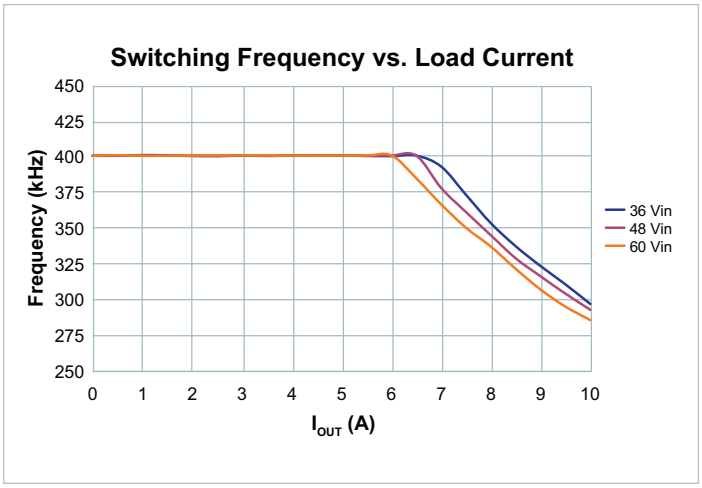



***Figure 5*** — *Switching Frequency vs. Load Current*

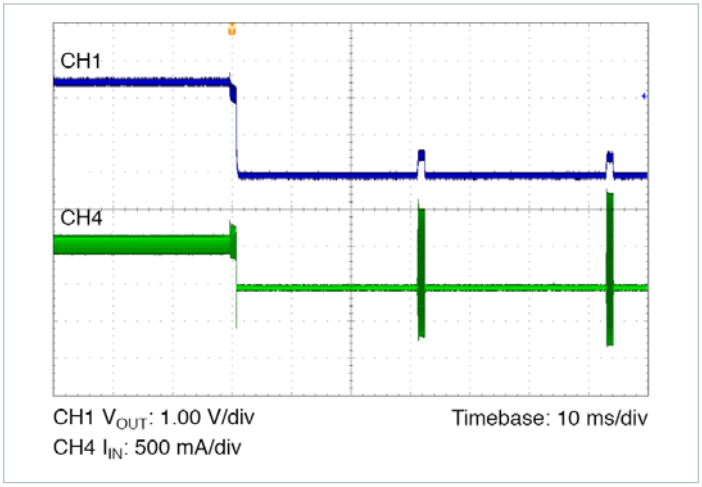



***Figure 3*** — *Output Short Circuit @ $V_{IN}$ = 48 V*

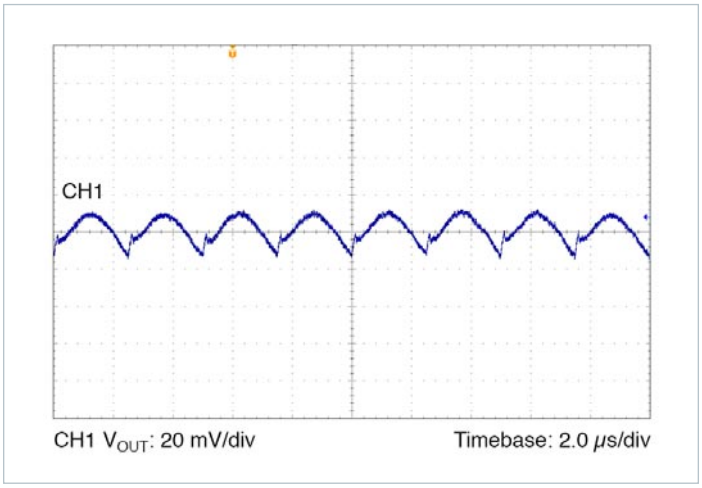



***Figure 6*** — *Output Ripple: 48 $V_{IN}$, 2.5 $V_{OUT}$ at 5 A. $V_{OUT}$ = 20 mV/Div, 2.0 µs/Div; $C_{OUT}$ = 6 x 100 µF Ceramic*

## PI3542-00 (2.5 $V_{OUT}$) Electrical Characteristics

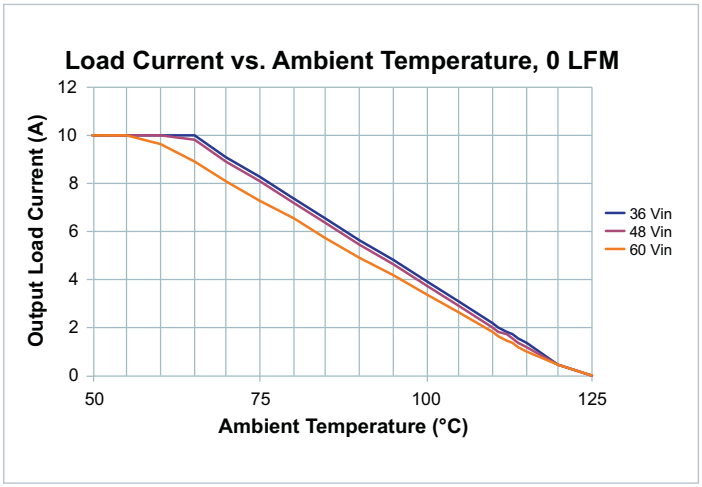



***Figure 7*** *— Load Current vs. Ambient Temperature, 0 LFM*

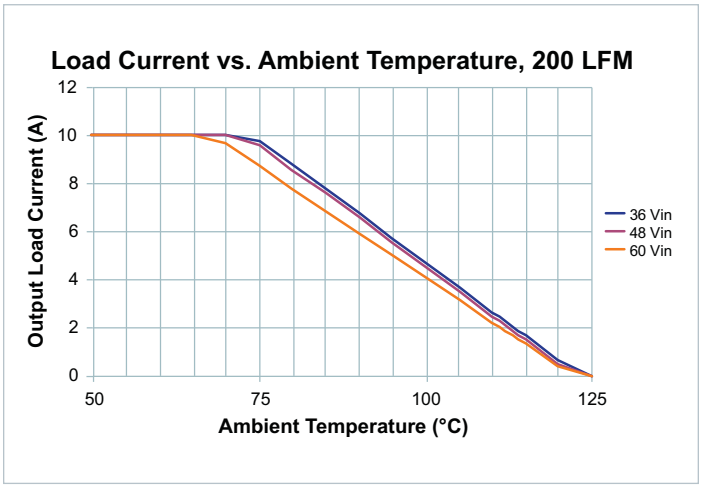



***Figure 8*** *— Load Current vs. Ambient Temperature, 200 LFM*

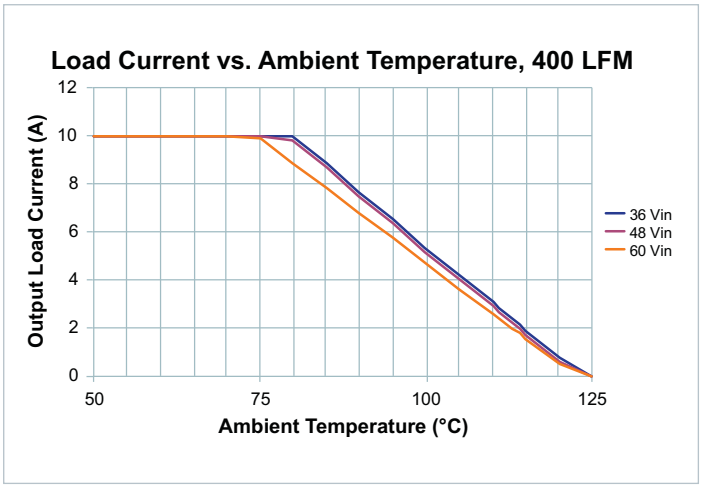



***Figure 9*** *— Load Current vs. Ambient Temperature, 400 LFM*

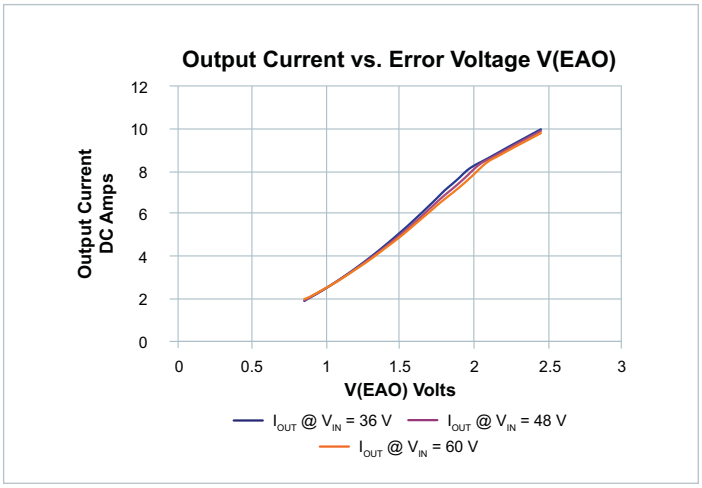



***Figure 10*** *— Output Current vs. Error Voltage V(EAO)*

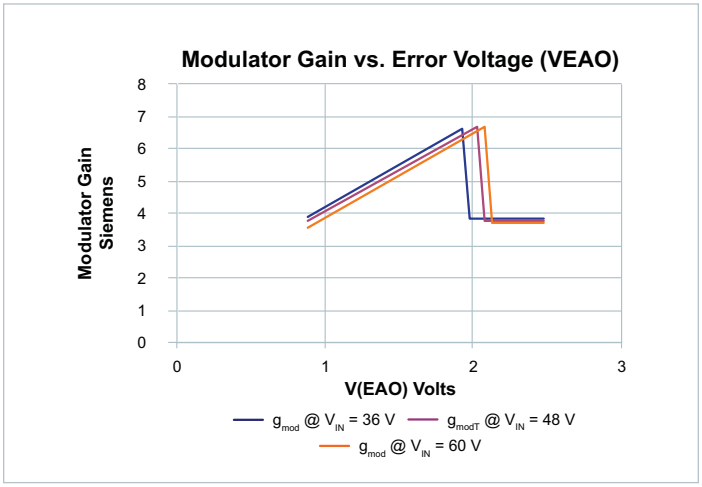



***Figure 11*** *— Modulator Gain vs. Error Voltage (VEAO)*

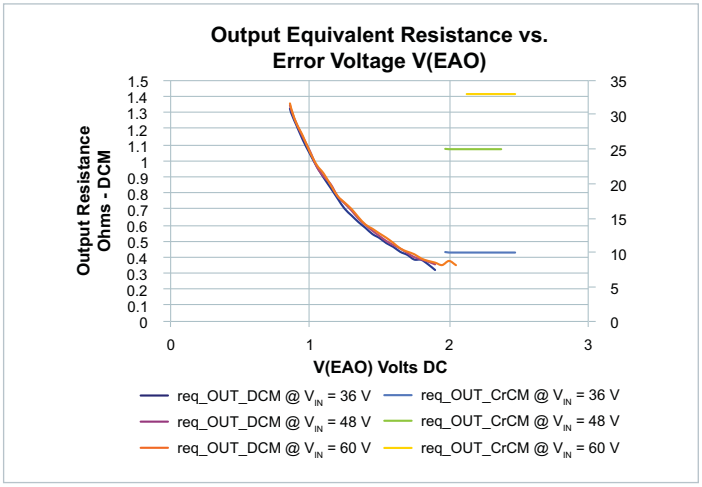



***Figure 12*** *— Output Equivalent Resistance vs.Error Voltage V(EAO)*

## PI3543-00 (3.3 $V_{OUT}$) Electrical Characteristics

Specifications apply for -40°C <$T_J$ < 125°C, $V_{IN}$ = 48 V, $V_{VDR}$ = 5.1 V +/- 2%, L1 = 420 nH [1] unless other conditions are noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Input Specifications** | | | | | | |
| Input Voltage | $V_{IN\_DC}$ | | 36 | 48 | 60 | V |
| Input Current | $I_{IN\_DC}$ | $V_{IN}$ = 48 V, $T_C$ = 25°C, $I_{OUT}$ = 10 A | | 0.762 | | A |
| Input Current At Output Short (fault condition duty cycle) | $I_{IN\_Short}$ | Short at terminals | | 3 | - | mA |
| Input Quiescent Current | $I_{Q\_VIN}$ | Disabled | | 1.265 | | mA |
| | | Enabled (no load) | | 2.4 | | |
| Input Voltage Slew Rate | $V_{IN\_SR}$ | | | | 1 | V/µs |
| **Output Specifications** | | | | | | |
| EAIN Voltage Total Regulation | $V_{OUT\_DC}$ | [2] | 0.985 | 1.00 | 1.015 | V |
| Output Voltage Trim Range | $V_{OUT\_DC}$ | [2][3] | 2.6 | 3.3 | 3.6 | V |
| Line Regulation | $\Delta V_{OUT}(\Delta V_{IN})$ | @ 25°C, 36 V <$V_{IN}$ <60 V | | 0.10 | | % |
| Load Regulation | $\Delta V_{OUT}(\Delta I_{OUT})$ | @ 25°C, 0.5 A <$I_{OUT}$ <10 A | | 0.10 | | % |
| Output Voltage Ripple | $V_{OUT\_AC}$ | $I_{OUT}$ = 10 A, $C_{OUT}$ = 6 x 100 µF, 20 MHz BW [4] | | 62 | | mVp-p |
| Output Current | $I_{OUT\_DC}$ | [5] | 0 | | 10 | A |
| Current Limit | $I_{OUT\_CL}$ | L1 = 420 nH ±1% | - | 11.5 | - | A |
| **Protection** | | | | | | |
| Input UVLO Start Threshold | $V_{UVLO\_START}$ | | 33.8 | 34.8 | 35.8 | V |
| Input UVLO Stop Hysteresis | $V_{UVLO\_HYS}$ | | | 0.9 | | V |
| Input UVLO Response Time | | | | 1.25 | | usec |
| Input OVLO Stop Threshold | $V_{OVLO}$ | | 62 | 64.3 | 66.2 | V |
| Input OVLO Start Hysteresis | $V_{OVLO\_HYS}$ | | | 1.3 | | V |
| Input OVLO Response Time | $t_f$ | | | 1.25 | | usec |
| Output Overvoltage Protection | $V_{OVP}$ | Above set $V_{OUT}$ | | 20 | | % |
| Overtemperature Fault Threshold | $T_{OTP}$ | | | 130 | | °C |
| Ovetemperature Restart Hysteresis | $T_{OTP\_HYS}$ | | | 30 | | °C |
| **Timing** | | | | | | |
| Switching Frequency | $f_S$ | [6] 48 $V_{IN}$ to 3.3 $V_{OUT}$, 6 A out, L1 = 420 nH ±1% | - | 400 | - | kHz |
| Fault Restart Delay | $t_{FR\_DLY}$ | | | 30 | | ms |
| **Sync In (SYNCI)** | | | | | | |
| Synchronization Frequency Range | $\Delta f_{SYNCI}$ | Relative to set switching frequency [3] | 50 | | 110 | % |
| SYNCI Threshold | $V_{SYNCI}$ | | | $V_{VDR}$/2 | | V |

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

## PI3543-00 (3.3 $V_{OUT}$) Electrical Characteristics

Specifications apply for -40°C <$T_J$ < 125°C, $V_{IN}$ = 48 V, $V_{VDR}$ = 5.1 V +/- 2%, L1 = 420 nH [1] unless other conditions are noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Sync Out (SYNCO)** | | | | | | |
| SYNCO High | $V_{SYNCO\_HI}$ | Source 1 mA | $V_{VDR}$ –0.5 | | | V |
| SYNCO Low | $V_{SYNCO\_LO}$ | Sink 1 mA | | | 0.5 | V |
| SYNCO Rise Time | $t_{SYNCO\_RT}$ | 20 pF load | | 10 | | ns |
| SYNCO Fall Time | $t_{SYNCO\_FT}$ | 20 pF load | | 10 | | ns |
| **Soft Start, Tracking and Error Amplifier** | | | | | | |
| TRK Active Range (Nominal) | $V_{TRK}$ | | 0 | | 1.08 | V |
| TRK Enable Threshold | $V_{TRK\_OV}$ | | 20 | 40 | 60 | mV |
| TRK to EAIN Offset | $V_{EIAN\_OV}$ | | 50 | 80 | 110 | mV |
| Charge Current (Soft – Start) | $I_{TRK}$ | | -70 | -50 | -30 | µA |
| Discharge Current (Fault) | $I_{TRK\_DIS}$ | $V_{TRK}$ = 0.5 V | | 10 | | mA |
| Soft-Start Time | $t_{SS}$ | $C_{TRK}$ = 0 | 0.6 | .94 | 1.6 | mS |
| Error Amplifier Trans-Conductance | GMeao | [2] | | 5.1 | | ms |
| PSM Skip Threshold | $PSM_{SKIP}$ | [2] | | 0.8 | | V |
| Error Amplifier Output Impedance | $R_{OUT}$ | [2] | 1 | | | MOhm |
| Internal Compensation Capacitor | Chf | [2] | | 56 | | pf |
| Internal Compensation Resistor | Rzi | [2] | | 6k | | Ohm |
| **Enable** | | | | | | |
| High Threshold | $V_{EN\_HI}$ | | 0.9 | 1 | 1.1 | V |
| Low Threshold | $V_{EN\_LO}$ | | 0.7 | 0.8 | 0.9 | V |
| Threshold Hysteresis | $V_{EN\_HYS}$ | | 100 | 200 | 300 | mV |
| Enable Pull-Up Voltage (floating, no fault) | $V_{EN\_PU}$ | | | 2 | | V |
| Enable Pull-Down Voltage (floating, faulted) | $V_{EN\_PD}$ | | | 0 | | V |
| Source Current | $I_{EN\_SO}$ | | | -50 | | µA |
| Sink Current | $I_{EN\_SK}$ | | | 50 | | µA |

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

## PI3543-00 (3.3 $V_{OUT}$) Electrical Characteristics

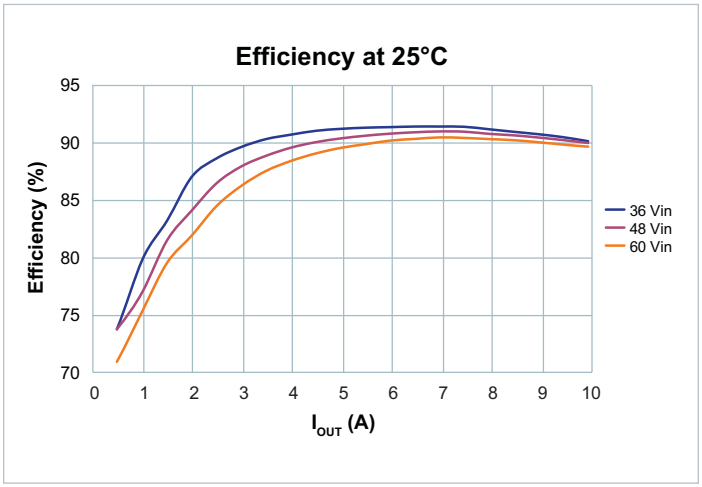



***Figure 13*** *— Regulator Efficiency*

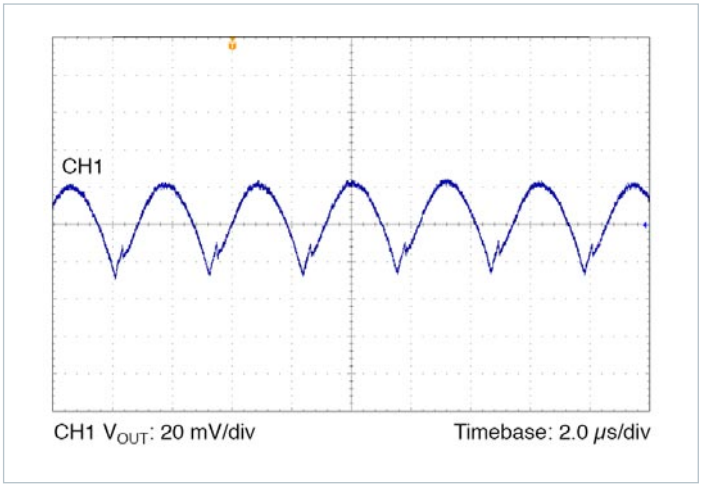



***Figure 16*** *— Output Ripple: 48 $V_{IN}$, 3.3 $V_{OUT}$ at 10 A. $V_{OUT}$ = 20 mV/Div, 2.0 µs/Div; $C_{OUT}$ = 6 x 100 µF Ceramic*

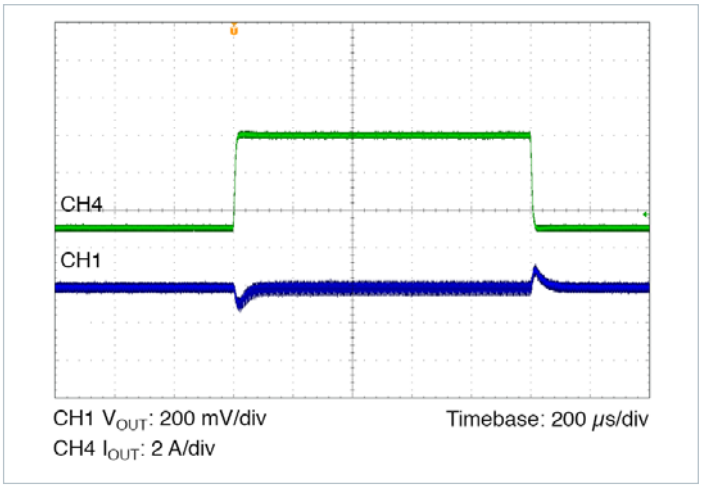



***Figure 14*** *— Transient Response: 5 A to 10 A, at 1 A/µs. 48 $V_{IN}$ to 3.3 $V_{OUT}$,*

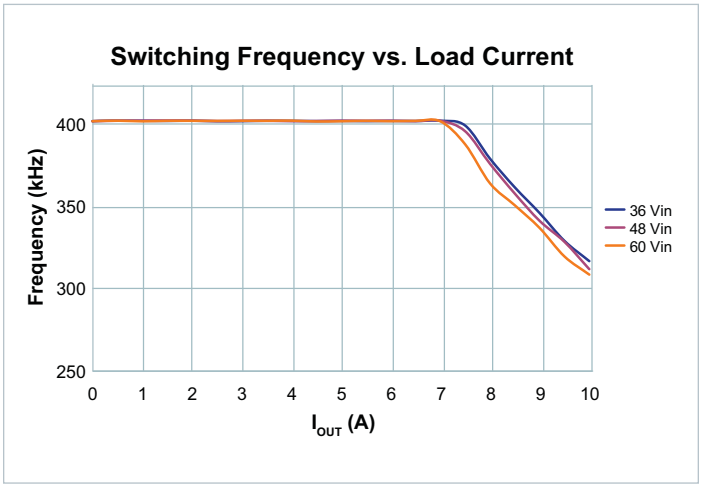



***Figure 17*** *— Switching Frequency vs. Load Current*

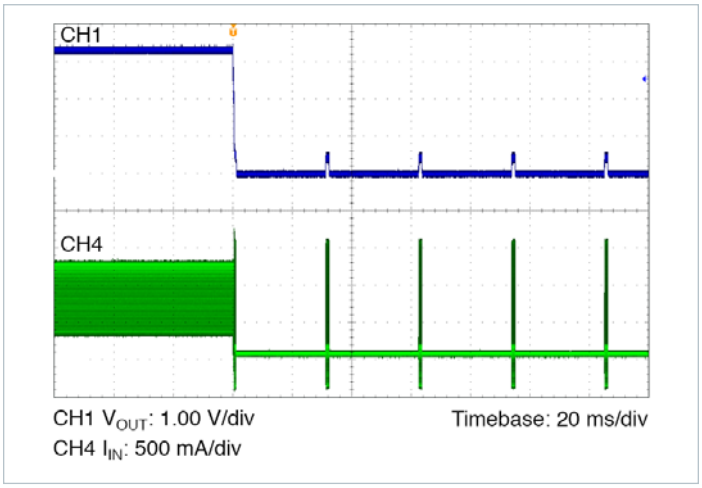



***Figure 15*** *— Output Short Circuit @ $V_{IN}$ = 48 V*

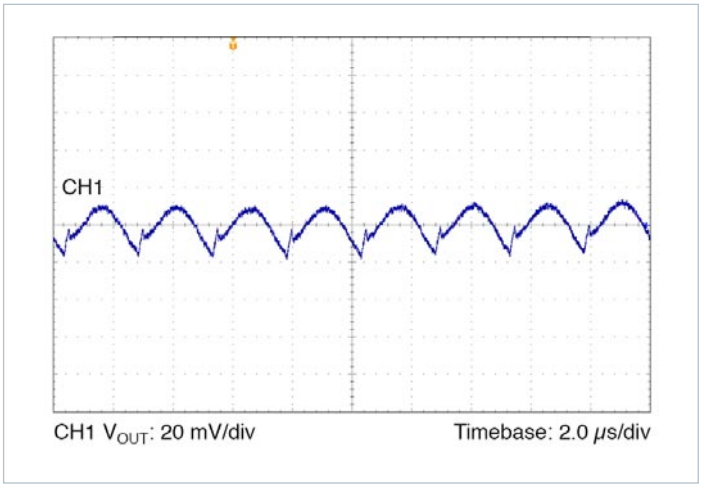



***Figure 18*** *— Output Ripple: 48 $V_{IN}$, 3.3 $V_{OUT}$ at 5 A. $V_{OUT}$ = 20 mV/Div, 2.0 µs/Div; $C_{OUT}$ = 6 x 100 µF Ceramic*

## PI3543-00 (3.3 $V_{OUT}$) Electrical Characteristics

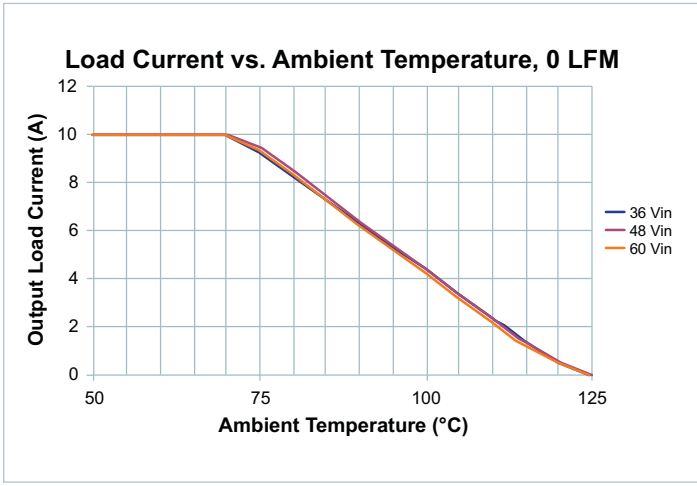



***Figure 19*** *— Load Current vs. Ambient Temperature, 0 LFM*

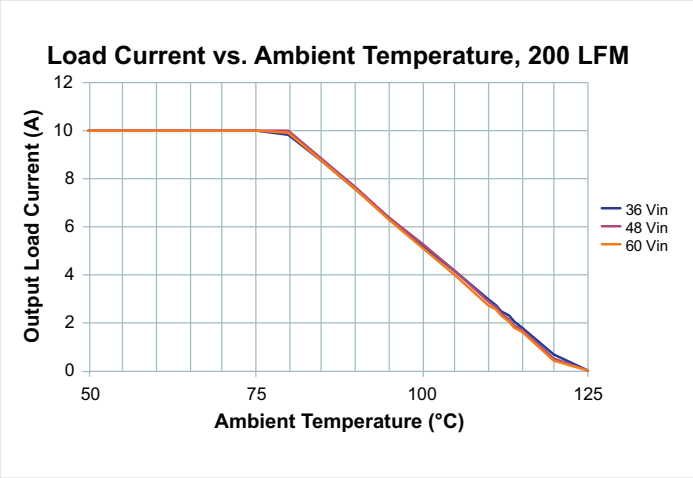



***Figure 20*** *— Load Current vs. Ambient Temperature, 200 LFM*

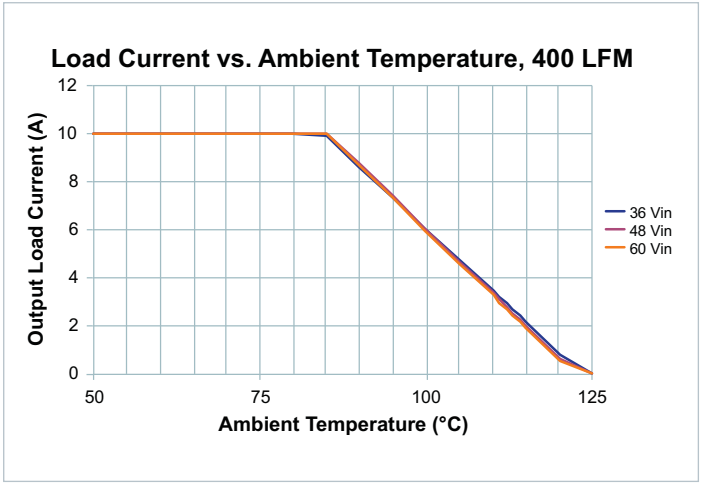



***Figure 21*** *— Load Current vs. Ambient Temperature, 400 LFM*

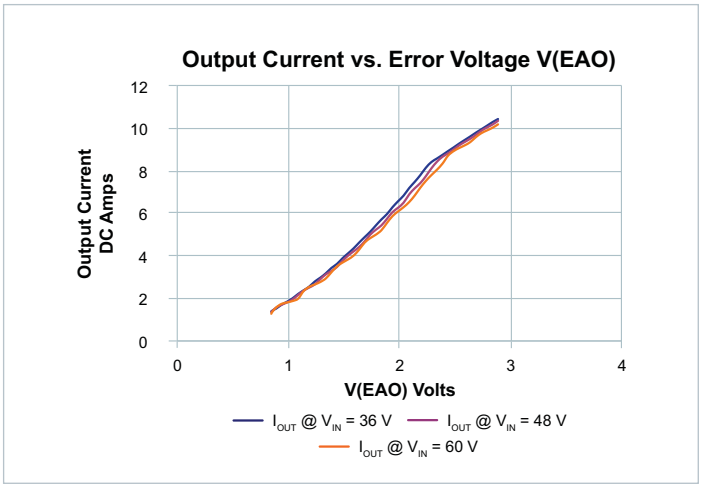



***Figure 22*** *— Output Current vs. Error Voltage V(EAO)*

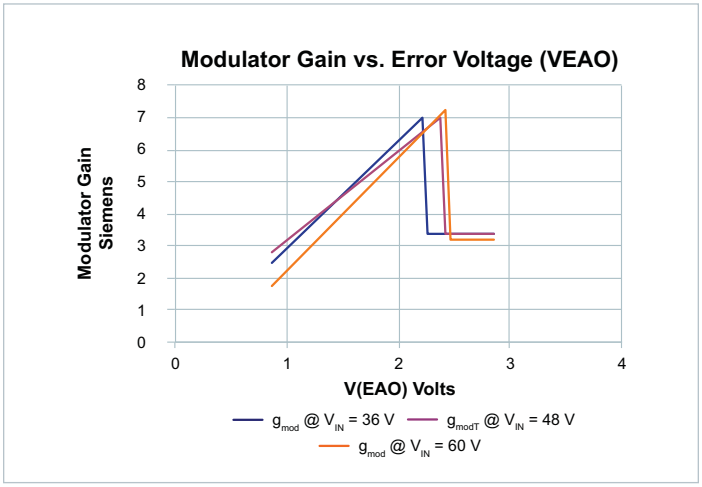



***Figure 23*** *— Modulator Gain vs. Error Voltage (VEAO)*

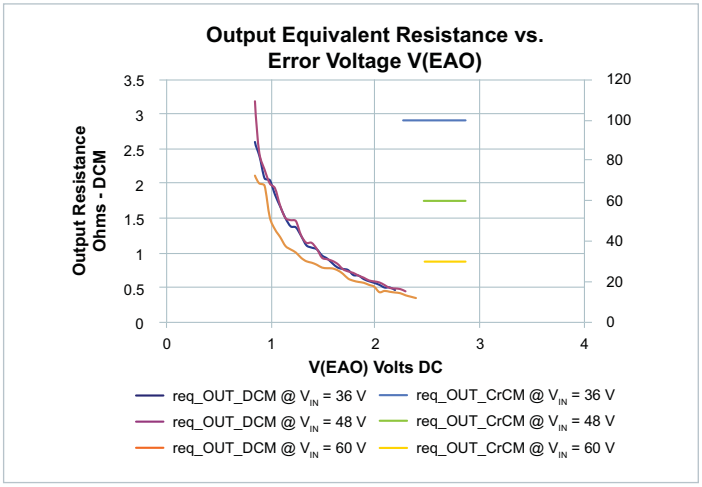



***Figure 24*** *— Output Equivalent Resistance vs. Error Voltage V(EAO)*

## PI3545-00 (5.0 $V_{OUT}$) Electrical Characteristics

Specifications apply for -40°C <$T_J$ < 125°C, $V_{IN}$ = 48 V, $V_{VDR}$ = 5.1 V +/- 2%, L1 = 420 nH [1] unless other conditions are noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Input Specifications** | | | | | | |
| Input Voltage | $V_{IN\_DC}$ | | 36 | 48 | 60 | V |
| Input Current | $I_{IN\_DC}$ | $V_{IN}$ = 48 V, $T_C$ = 25°C, $I_{OUT}$ = 10 A | | 1.126 | | A |
| Input Current At Output Short (fault condition duty cycle) | $I_{IN\_Short}$ | Short at terminals | | 3.2 | - | mA |
| Input Quiescent Current | $I_{Q\_VIN}$ | Disabled | | 1.26 | | mA |
| | | Enabled (no load) | | 2.42 | | |
| Input Voltage Slew Rate | $V_{IN\_SR}$ | | | | 1 | V/µs |
| **Output Specifications** | | | | | | |
| EAIN Voltage Total Regulation | $V_{OUT\_DC}$ | [2] | 0.985 | 1.00 | 1.015 | V |
| Output Voltage Trim Range | $V_{OUT\_DC}$ | [2][3] | 4.0 | 5.0 | 5.5 | V |
| Line Regulation | $\Delta V_{OUT}(\Delta V_{IN})$ | @ 25°C, 36 V <$V_{IN}$ <60 V | | 0.10 | | % |
| Load Regulation | $\Delta V_{OUT}(\Delta I_{OUT})$ | @ 25°C, 0.5 A <$I_{OUT}$ <10 A | | 0.10 | | % |
| Output Voltage Ripple | $V_{OUT\_AC}$ | $I_{OUT}$ = 10 A, $C_{OUT}$ = 6 x 47 µF, 20 MHz BW [4] | | 62.4 | | mVp-p |
| Output Current | $I_{OUT\_DC}$ | [5] | 0 | | 10 | A |
| Current Limit | $I_{OUT\_CL}$ | L1 = 420 nH ±1% | - | 12 | - | A |
| **Protection** | | | | | | |
| Input UVLO Start Threshold | $V_{UVLO\_START}$ | | 33.8 | 34.8 | 35.8 | V |
| Input UVLO Stop Hysteresis | $V_{UVLO\_HYS}$ | | | 2.6 | | V |
| Input UVLO Response Time | | | | 1.25 | | usec |
| Input OVLO Stop Threshold | $V_{OVLO}$ | | 62 | 64.3 | 66.2 | V |
| Input OVLO Start Hysteresis | $V_{OVLO\_HYS}$ | | | 1.3 | | V |
| Input OVLO Response Time | $t_f$ | | | 1.25 | | usec |
| Output Overvoltage Protection | $V_{OVP}$ | Above set $V_{OUT}$ | | 20 | | % |
| Overtemperature Fault Threshold | $T_{OTP}$ | | | 130 | | °C |
| Ovetemperature Restart Hysteresis | $T_{OTP\_HYS}$ | | | 30 | | °C |
| **Timing** | | | | | | |
| Switching Frequency | $f_S$ | [6] 48 $V_{IN}$ to 55 $V_{OUT}$, 3 A out, L1 = 420 nH ±1% | - | 600 | - | kHz |
| Fault Restart Delay | $t_{FR\_DLY}$ | | | 30 | | ms |
| **Sync In (SYNCI)** | | | | | | |
| Synchronization Frequency Range | $\Delta f_{SYNCI}$ | Relative to set switching frequency [3] | 50 | | 110 | % |
| SYNCI Threshold | $V_{SYNCI}$ | | | $V_{VDR}$/2 | | V |

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

## PI3545-00 (5.0 $V_{OUT}$) Electrical Characteristics

Specifications apply for -40°C <$T_J$ < 125°C, $V_{IN}$ = 48 V, $V_{VDR}$ = 5.1 V +/- 2%, L1 = 420 nH [1] unless other conditions are noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Sync Out (SYNCO)** | | | | | | |
| SYNCO High | $V_{SYNCO\_HI}$ | Source 1 mA | $V_{VDR}$ –0.5 | | | V |
| SYNCO Low | $V_{SYNCO\_LO}$ | Sink 1 mA | | | 0.5 | V |
| SYNCO Rise Time | $t_{SYNCO\_RT}$ | 20 pF load | | 10 | | ns |
| SYNCO Fall Time | $t_{SYNCO\_FT}$ | 20 pF load | | 10 | | ns |
| **Soft Start, Tracking and Error Amplifier** | | | | | | |
| TRK Active Range (Nominal) | $V_{TRK}$ | | 0 | | 1.08 | V |
| TRK Enable Threshold | $V_{TRK\_OV}$ | | 20 | 40 | 60 | mV |
| TRK to EAIN Offset | $V_{EIAN\_OV}$ | | 50 | 80 | 110 | mV |
| Charge Current (Soft – Start) | $I_{TRK}$ | | -70 | -50 | -30 | µA |
| Discharge Current (Fault) | $I_{TRK\_DIS}$ | $V_{TRK}$ = 0.5 V | | 10 | | mA |
| Soft-Start Time | $t_{SS}$ | $C_{TRK}$ = 0 | 0.6 | .94 | 1.6 | mS |
| Error Amplifier Trans-Conductance | GMeao | [2] | | 5.1 | | ms |
| PSM Skip Threshold | $PSM_{SKIP}$ | [2] | | 0.8 | | V |
| Error Amplifier Output Impedance | $R_{OUT}$ | [2] | 1 | | | MOhm |
| Internal Compensation Capacitor | Chf | [2] | | 56 | | pf |
| Internal Compensation Resistor | Rzi | [2] | | 6k | | Ohm |
| **Enable** | | | | | | |
| High Threshold | $V_{EN\_HI}$ | | 0.9 | 1 | 1.1 | V |
| Low Threshold | $V_{EN\_LO}$ | | 0.7 | 0.8 | 0.9 | V |
| Threshold Hysteresis | $V_{EN\_HYS}$ | | 100 | 200 | 300 | mV |
| Enable Pull-Up Voltage (floating, no fault) | $V_{EN\_PU}$ | | | 2 | | V |
| Enable Pull-Down Voltage (floating, faulted) | $V_{EN\_PD}$ | | | 0 | | V |
| Source Current | $I_{EN\_SO}$ | | | -50 | | µA |
| Sink Current | $I_{EN\_SK}$ | | | 50 | | µA |

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

## PI3545-00 (5.0 $V_{OUT}$) Electrical Characteristics

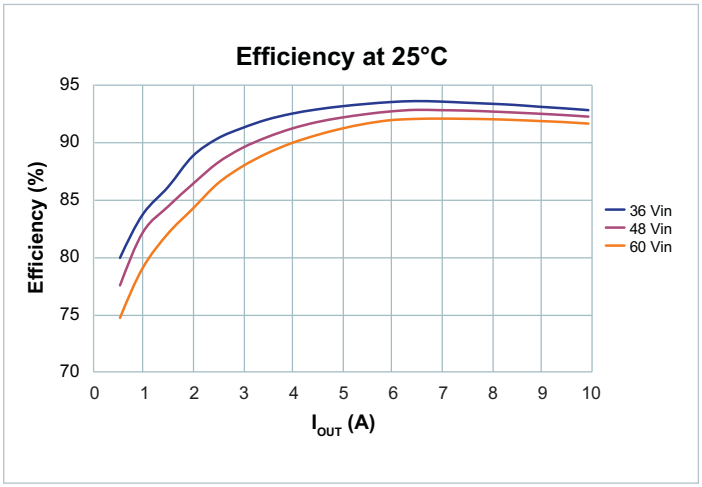



***Figure 25*** *— Regulator Efficiency*

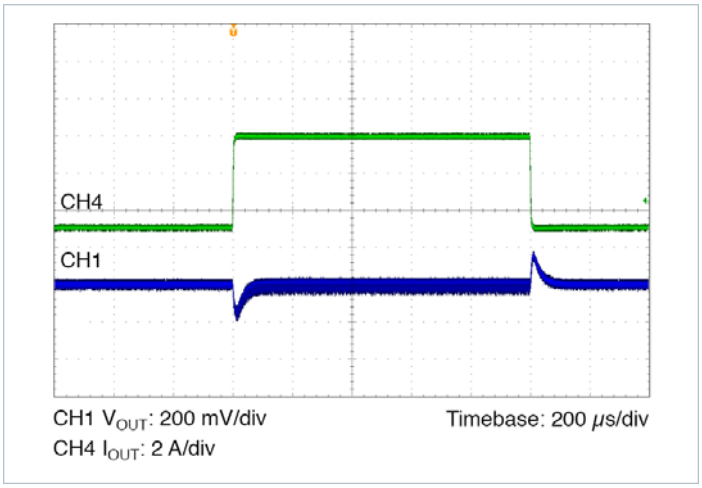



***Figure 26*** *— Transient Response: 5 A to 10 A, at 1 A/µs. 48 $V_{IN}$ to 5.0 $V_{OUT}$ $C_{OUT}$ = 6 x 47 µF Ceramic*

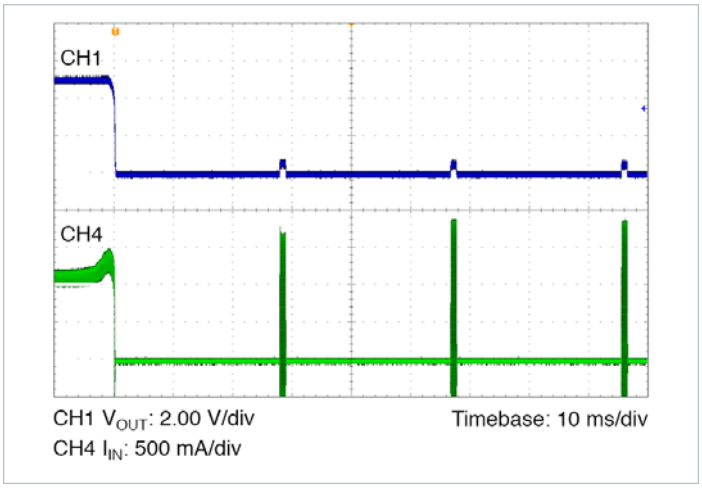



***Figure 27*** *— Output Short Circuit @ $V_{IN}$ = 48 V*

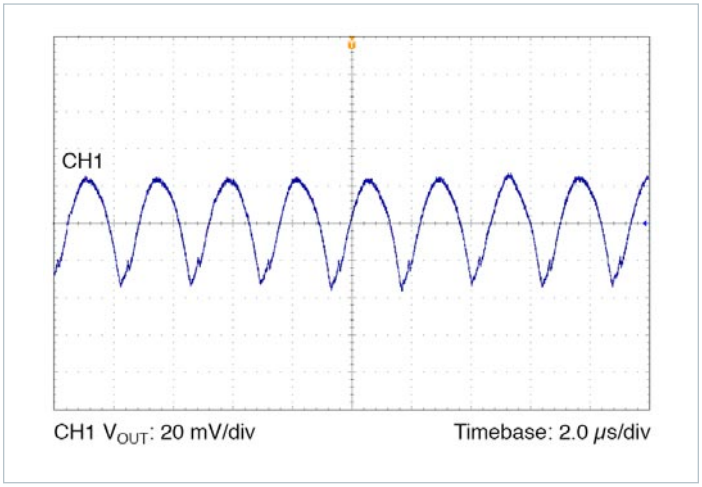



***Figure 28*** *— Output Ripple: 48 $V_{IN}$, 5.0 $V_{OUT}$ at 10 A. $V_{OUT}$ = 20 mV/Div, 2.0 µs/Div; $C_{OUT}$ = 6 x 47 µF Ceramic*

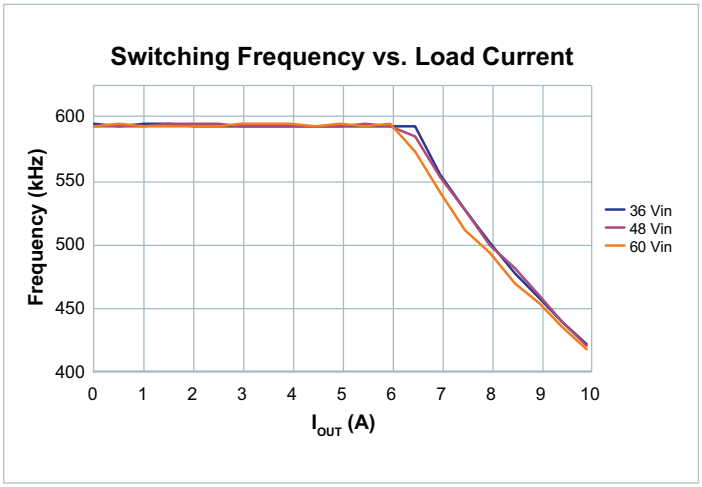



***Figure 29*** *— Switching Frequency vs. Load Current*

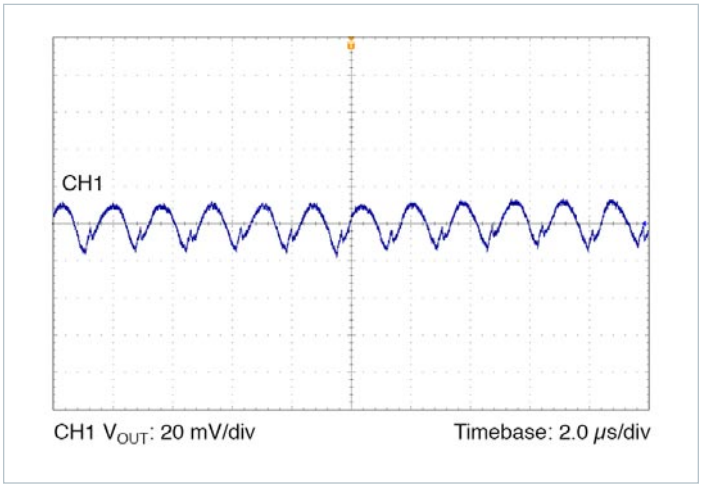



***Figure 30*** *— Output Ripple: 48 $V_{IN}$, 5.0 $V_{OUT}$ at 5 A. $V_{OUT}$ = 20 mV/Div, 2.0 µs/Div; $C_{OUT}$ = 6 x 47 µF Ceramic*

## PI3545-00 (5.0 $V_{OUT}$) Electrical Characteristics

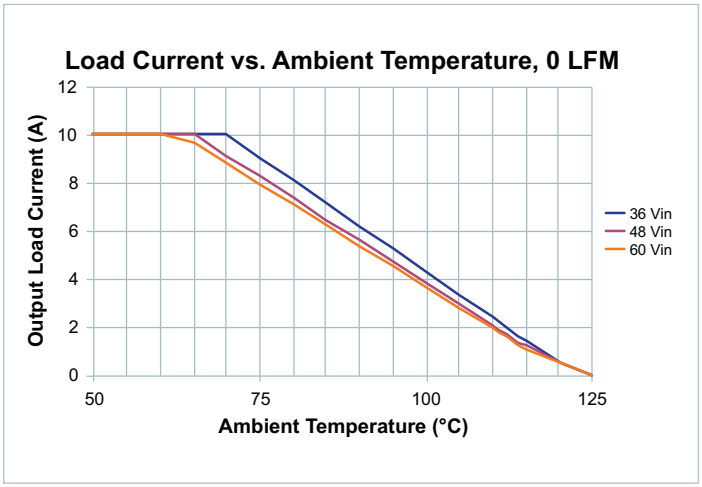



***Figure 31*** *— Load Current vs. Ambient Temperature, 0 LFM*

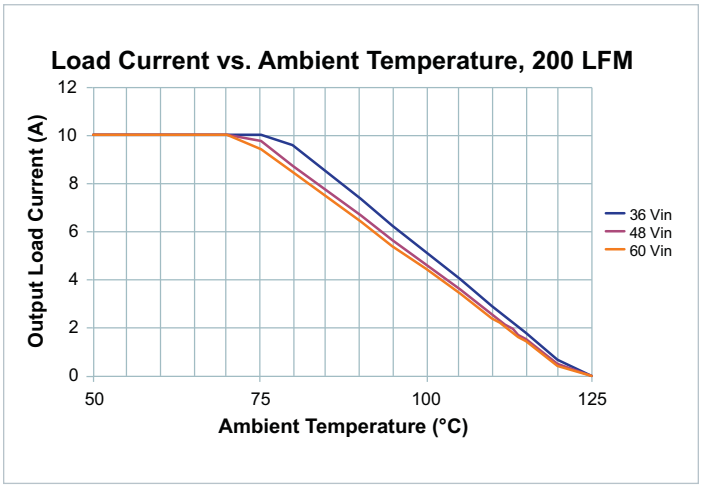



***Figure 32*** *— Load Current vs. Ambient Temperature, 200 LFM*

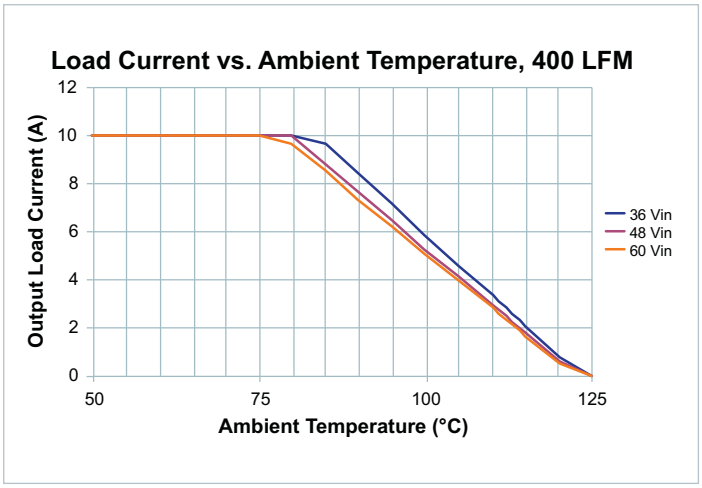



***Figure 33*** *— Load Current vs. Ambient Temperature, 400 LFM*

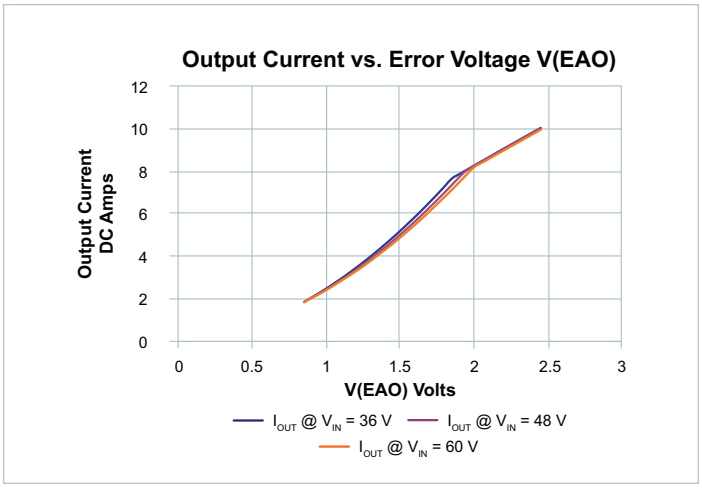



***Figure 34*** *— Output Current vs. Error Voltage V(EAO)*

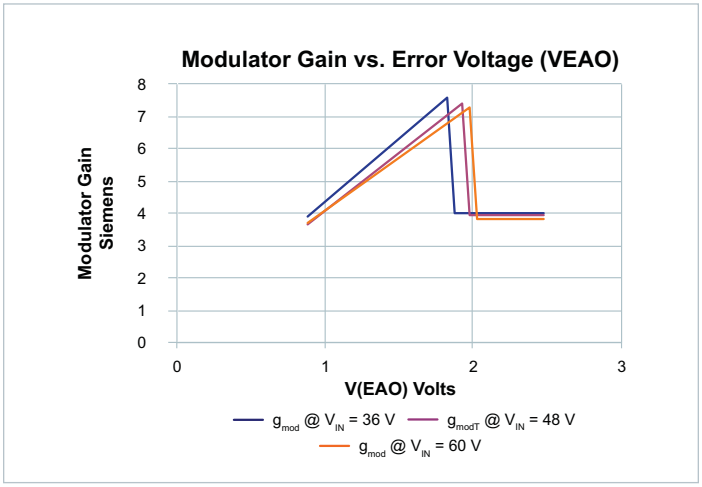



***Figure 35*** *— Modulator Gain vs. Error Voltage (VEAO)*

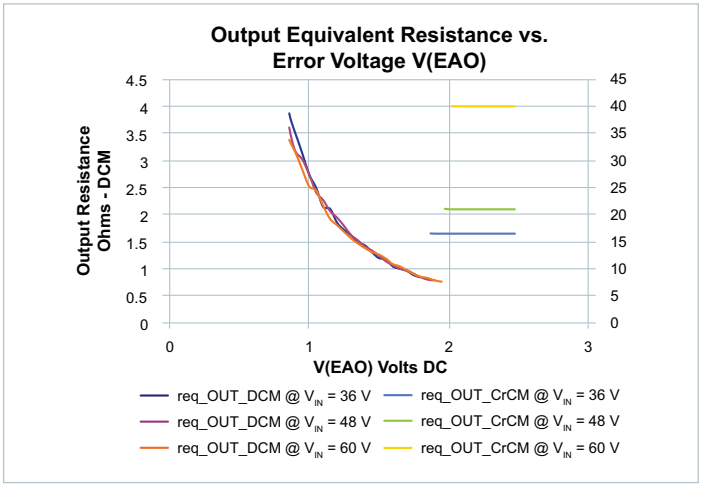



***Figure 36*** *— Output Equivalent Resistance vs. Error Voltage V(EAO)*

## PI3546-00 (12.0 $V_{OUT}$) Electrical Characteristics

Specifications apply for -40°C <$T_J$ < 125°C, $V_{IN}$ = 48 V, $V_{VDR}$ = 5.1 V +/- 2%, L1 = 900 nH [1] unless other conditions are noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Input Specifications** | | | | | | |
| Input Voltage | $V_{IN\_DC}$ | | 36 | 48 | 60 | V |
| Input Current | $I_{IN\_DC}$ | $V_{IN}$ = 48 V, $T_C$ = 25°C, $I_{OUT}$ = 9 A | | 2.33 | | A |
| Input Current At Output Short (fault condition duty cycle) | $I_{IN\_Short}$ | Short at terminals | | 3.3 | - | mA |
| Input Quiescent Current | $I_{Q\_VIN}$ | Disabled | | 1.26 | | mA |
| | | Enabled (no load) | | 2.9 | | |
| Input Voltage Slew Rate | $V_{IN\_SR}$ | | | | 1 | V/µs |
| **Output Specifications** | | | | | | |
| EAIN Voltage Total Regulation | $V_{OUT\_DC}$ | [2] | 0.985 | 1.00 | 1.015 | V |
| Output Voltage Trim Range | $V_{OUT\_DC}$ | [2][3] | 6.5 | 12 | 14 | V |
| Line Regulation | $\Delta V_{OUT}(\Delta V_{IN})$ | @ 25°C, 36 V <$V_{IN}$ <60 V | | 0.10 | | % |
| Load Regulation | $\Delta V_{OUT}(\Delta I_{OUT})$ | @ 25°C, 0.5 A <$I_{OUT}$ <9 A | | 0.10 | | % |
| Output Voltage Ripple | $V_{OUT\_AC}$ | $I_{OUT}$ = 9 A, $C_{OUT}$ = 6 x 10 µF, 20 MHz BW [4] | | 114 | | mVp-p |
| Output Current | $I_{OUT\_DC}$ | [5] | 0 | | 9 | A |
| Current Limit | $I_{OUT\_CL}$ | L1 = 900 nH ±1% | - | 10.5 | - | A |
| **Protection** | | | | | | |
| Input UVLO Start Threshold | $V_{UVLO\_START}$ | | 33.8 | 34.8 | 35.8 | V |
| Input UVLO Stop Hysteresis | $V_{UVLO\_HYS}$ | | | 2.6 | | V |
| Input UVLO Response Time | | | | 1.25 | | usec |
| Input OVLO Stop Threshold | $V_{OVLO}$ | | 62 | 64.3 | 66.2 | V |
| Input OVLO Start Hysteresis | $V_{OVLO\_HYS}$ | | | 1.3 | | V |
| Input OVLO Response Time | $t_f$ | | | 1.25 | | usec |
| Output Overvoltage Protection | $V_{OVP}$ | Above set $V_{OUT}$ | | 20 | | % |
| Overtemperature Fault Threshold | $T_{OTP}$ | | | 130 | | °C |
| Ovetemperature Restart Hysteresis | $T_{OTP\_HYS}$ | | | 30 | | °C |
| **Timing** | | | | | | |
| Switching Frequency | $f_S$ | [6] 48 $V_{IN}$ to 12 $V_{OUT}$, 2 A out, L1 = 900 nH ±1% | - | 800 | - | kHz |
| Fault Restart Delay | $t_{FR\_DLY}$ | | | 30 | | ms |
| **Sync In (SYNCI)** | | | | | | |
| Synchronization Frequency Range | $\Delta f_{SYNCI}$ | Relative to set switching frequency [3] | 50 | | 110 | % |
| SYNCI Threshold | $V_{SYNCI}$ | | | $V_{VDR}$/2 | | V |

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

## PI3546-00 (12.0 $V_{OUT}$) Electrical Characteristics

Specifications apply for -40°C <$T_J$ < 125°C, $V_{IN}$ = 48 V, $V_{VDR}$ = 5.1 V +/- 2%, L1 = 900 nH [1] unless other conditions are noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | | | | | |
| **Sync Out (SYNCO)** | | | | | | |
| SYNCO High | $V_{SYNCO\_HI}$ | Source 1 mA | $V_{VDR}$ –0.5 | | | V |
| SYNCO Low | $V_{SYNCO\_LO}$ | Sink 1 mA | | | 0.5 | V |
| SYNCO Rise Time | $t_{SYNCO\_RT}$ | 20 pF load | | 10 | | ns |
| SYNCO Fall Time | $t_{SYNCO\_FT}$ | 20 pF load | | 10 | | ns |
| **Soft Start, Tracking and Error Amplifier** | | | | | | |
| TRK Active Range (Nominal) | $V_{TRK}$ | | 0 | | 1.08 | V |
| TRK Enable Threshold | $V_{TRK\_OV}$ | | 20 | 40 | 60 | mV |
| TRK to EAIN Offset | $V_{EIAN\_OV}$ | | 50 | 80 | 110 | mV |
| Charge Current (Soft – Start) | $I_{TRK}$ | | -70 | -50 | -30 | µA |
| Discharge Current (Fault) | $I_{TRK\_DIS}$ | $V_{TRK}$ = 0.5 V | | 10 | | mA |
| Soft-Start Time | $t_{SS}$ | $C_{TRK}$ = 0 | 0.6 | .94 | 1.6 | mS |
| Error Amplifier Trans-Conductance | GMeao | [2] | | 7.6 | | ms |
| PSM Skip Threshold | $PSM_{SKIP}$ | [2] | | 0.8 | | V |
| Error Amplifier Output Impedance | $R_{OUT}$ | [2] | 1 | | | MOhm |
| Internal Compensation Capacitor | Chf | [2] | | 56 | | pf |
| Internal Compensation Resistor | Rzi | [2] | | 5k | | Ohm |
| **Enable** | | | | | | |
| High Threshold | $V_{EN\_HI}$ | | 0.9 | 1 | 1.1 | V |
| Low Threshold | $V_{EN\_LO}$ | | 0.7 | 0.8 | 0.9 | V |
| Threshold Hysteresis | $V_{EN\_HYS}$ | | 100 | 200 | 300 | mV |
| Enable Pull-Up Voltage (floating, no fault) | $V_{EN\_PU}$ | | | 2 | | V |
| Enable Pull-Down Voltage (floating, faulted) | $V_{EN\_PD}$ | | | 0 | | V |
| Source Current | $I_{EN\_SO}$ | | | -50 | | µA |
| Sink Current | $I_{EN\_SK}$ | | | 50 | | µA |

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

## PI3546-00 (12.0 $V_{OUT}$) Electrical Characteristics

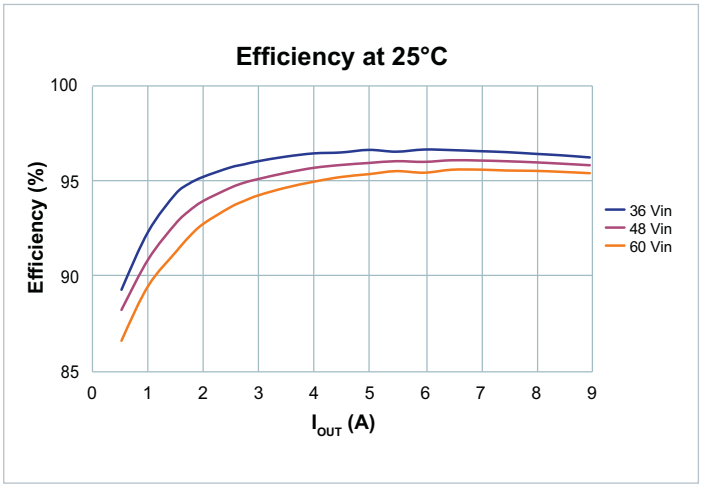



***Figure 37*** *— Regulator Efficiency*

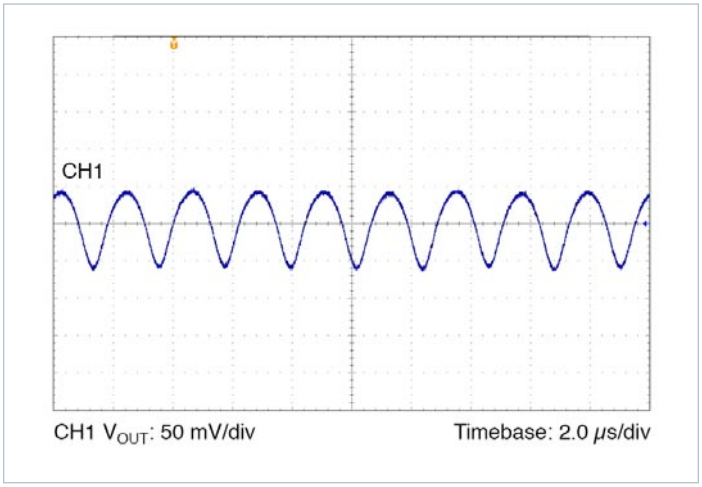



***Figure 40*** *— Output Ripple: 48 $V_{IN}$, 12.0 $V_{OUT}$ at 9 A. $V_{OUT}$ = 50 mV/Div, 2.0 µs/Div; $C_{OUT}$ = 6 x 10 µF Ceramic*

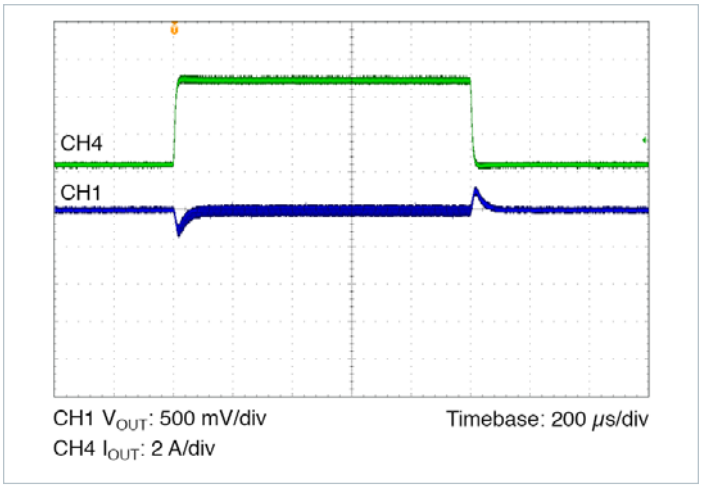



***Figure 38*** *— Transient Response: 5 A to 10 A, at 1 A/µs. 48 $V_{IN}$ to 12.0 $V_{OUT}$, $C_{OUT}$ = 6 x 10 µF Ceramic*

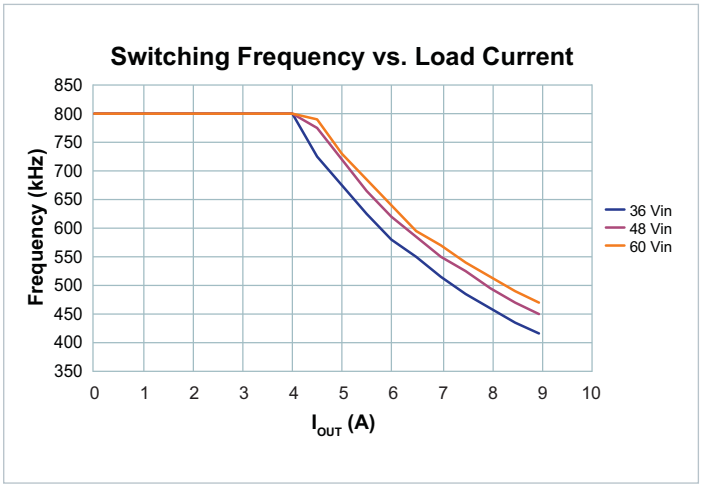



***Figure 41*** *— Switching Frequency vs. Load Current*

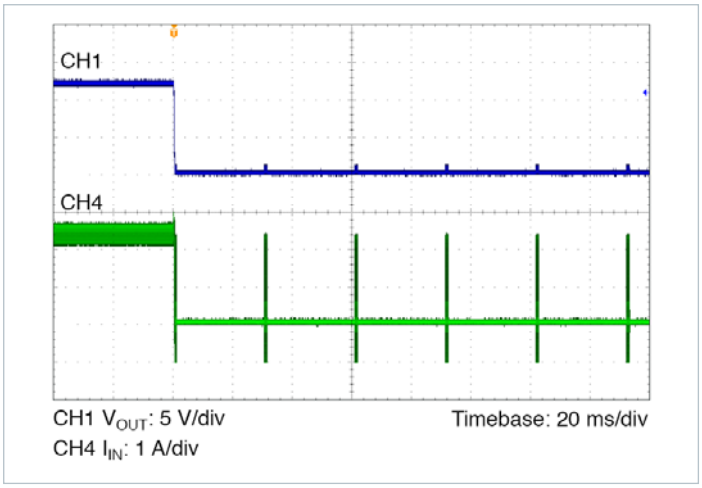



***Figure 39*** *— Output Short Circuit @ $V_{IN}$ = 48 V*

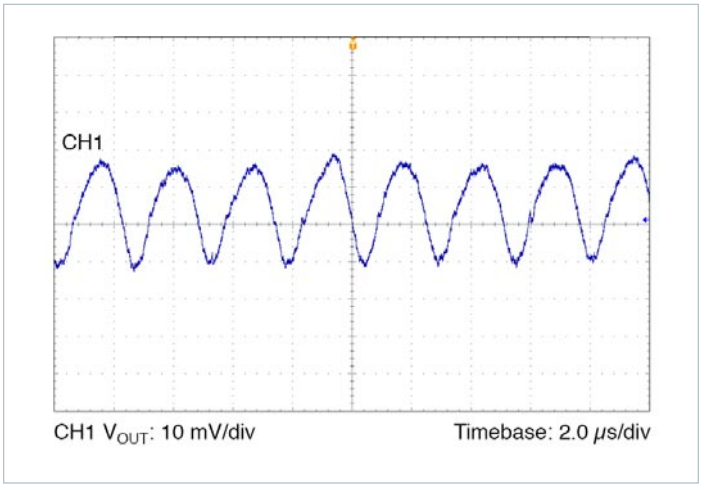



***Figure 42*** *— Output Ripple: 48 $V_{IN}$, 12.0 $V_{OUT}$ at 4.5 A. $V_{OUT}$ = 10 mV/Div, 2.0 µs/Div; $C_{OUT}$ = 6 x 10 µF Ceramic*

## PI3546-00 (12.0 $V_{OUT}$) Electrical Characteristics

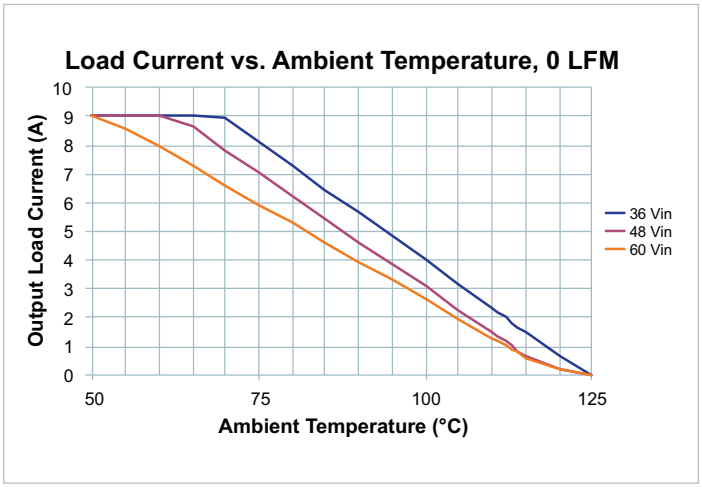



***Figure 43*** *— Load Current vs. Ambient Temperature, 0 LFM*

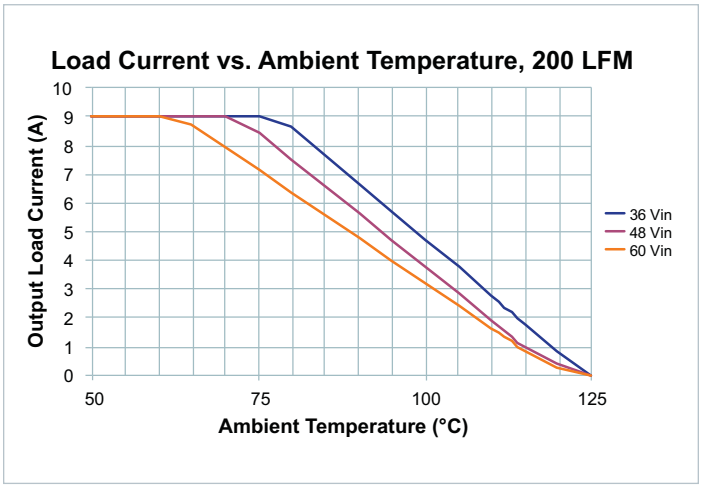



***Figure 44*** *— Load Current vs. Ambient Temperature, 200 LFM*

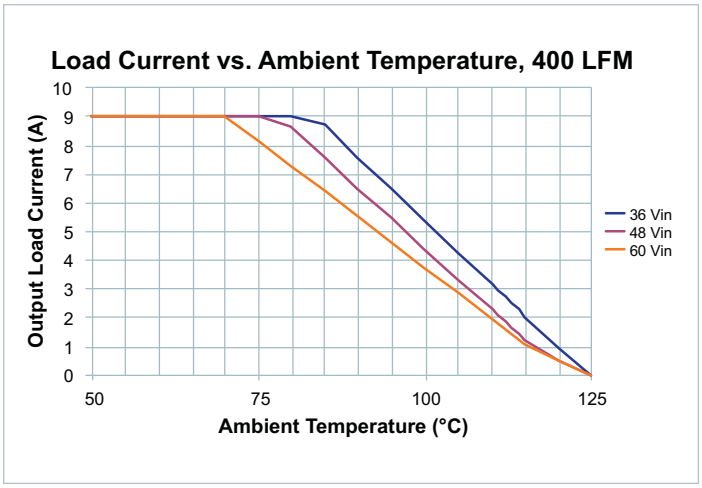



***Figure 45*** *— Load Current vs. Ambient Temperature, 400 LFM*

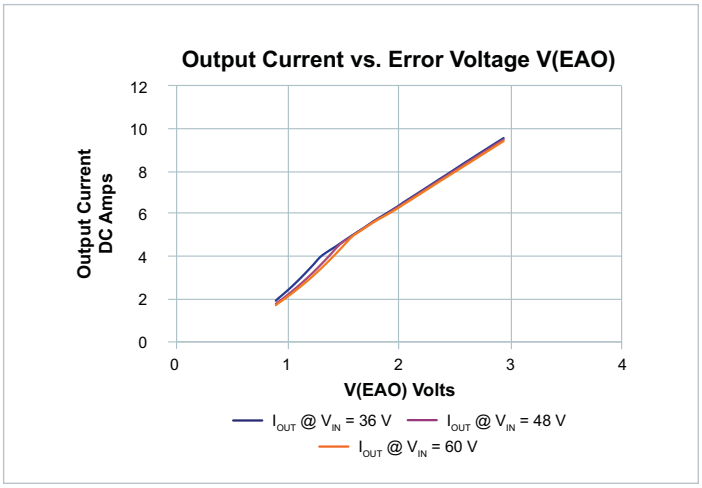



***Figure 46*** *— Output Current vs. Error Voltage V(EAO)*

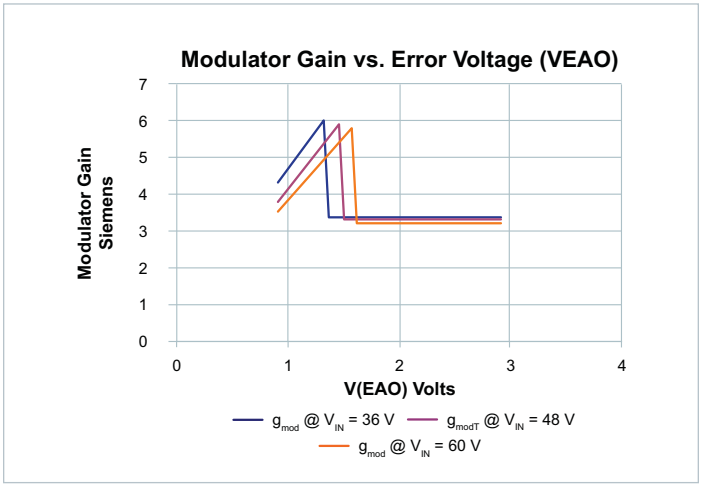



***Figure 47*** *— Modulator Gain vs. Error Voltage (VEAO)*

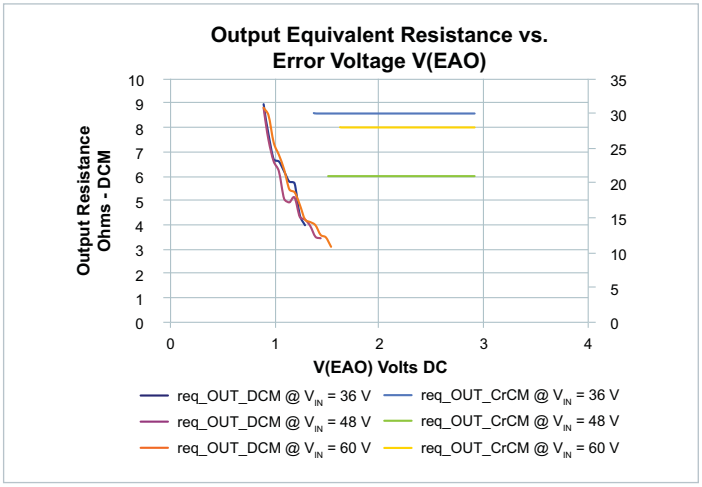



***Figure 48*** *— Output Equivalent Resistance vs. Error Voltage V(EAO*

## Functional Description

The PI354x-00 is a family of highly integrated ZVS-Buck regulators. The PI354x-00 has an output voltage that can be set within a prescribed range shown in Table 1. Performance and maximum output current are characterized with a specific external power inductor (see Table 2).

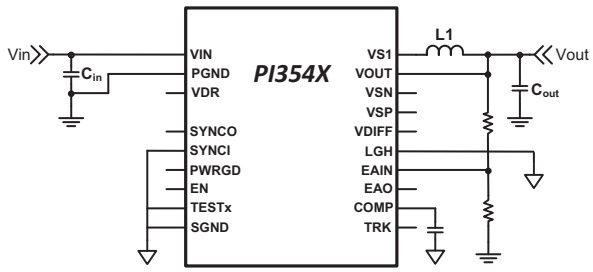



***Figure 49*** *— ZVS-Buck with required components*

For basic operation, Figure 49 shows the connections and components required. No additional design or settings are required.

### ENABLE (EN)

EN is the enable pin of the converter. The EN Pin is referenced to SGND and permits the user to turn the regulator on or off. The EN default polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the converter output is enabled. Pulling EN pin below 0.8 Vdc with respect to SGND will disable the regulator output.

### Remote Sensing

If remote sensing is required, the PI354x-00 product family is equipped with an undedicated differential amplifier. This amplifier can allow full differential remote sense by configuring it as a differential follower and connecting the VDIFF pin to the EAIN pin.

### Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency by an external clock referenced to SGND. The external clock can synchronize the unit between 50% and 110% of the preset switching frequency (fS). The PI354x-00 syncs to the falling edge of the applied clock, providing 180 degrees of phase shift with respect to SYNCO.

This allows for the interleaved paralleling of two PI354x-00 devices. The SYNCI pin should be connected to SGND through a zero Ohm resistor when not in use and should never be left floating.

When using the internal oscillator, the SYNCO pin provides a 5 V clock that can be used to sync other regulators. Therefore, one PI354x-00 can act as the lead regulator and have additional PI354x-00s running in parallel and synchronized.

### Soft-Start

The PI354x-00 includes an internal soft-start capacitor to control the rate of rise of the output voltage. See the Electrical Characteristics Section for the default value. Connecting an external capacitor from the TRK pin to SGND will increase the start-up ramp period. See, "Soft Start Adjustment and Track," in the Applications Description section for more details.

### Output Voltage Selection

The PI354x-00 output voltage can be selected by connecting a resistor from EAIN pin to SGND and a resistor from Vout to the EAIN pin as shown in Figure 49. Table 1 defines the allowable operational voltage ranges for the PI354x-00 family.

| Device | Output Voltage | |
|---|---|---|
| | Nom. | Range |
| PI3542-00-LGIZ | 2.5 V | 2.2 V to 3.0 V |
| PI3543-00-LGIZ | 3.3 V | 2.6 V to 3.6 V |
| PI3545-00-LGIZ | 5.0 V | 4.0 V to 5.5 V |
| PI3546-00-LGIZ | 12 V | 6.5 V to 14.0 V |

***Table 1*** *— PI354x-00 family output voltage ranges*

### Output Current Limit Protection

PI354x-00 has two methods implemented to protect from output short or over current condition.

***Slow Current Limit protection:*** prevents the output from sourcing current higher than the regulator's maximum rated current. If the output current exceeds the Current Limit ($I_{OUT\_CL}$) for 1024 µs, a slow current limit fault is initiated and the regulator is shutdown which eliminates output current flow. After Fault Restart Delay ($t_{FR\_DLY}$), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

***Fast Current Limit protection:*** PI354x-00 monitors the regulator inductor current pulse-by-pulse to prevent the output from supplying very high current due to sudden low impedance short. If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching until Fault Restart Delay ends and then initiate a soft-start cycle.

### Input Undervoltage Lockout

If $V_{IN}$ falls below the input Under Voltage Lockout (UVLO) threshold, but remains high enough to power the internal bias supply, the PI354x-00 will complete the current cycle and stop switching. The system will soft start once the input voltage is reestablished and after the Fault Restart Delay.

### Input Overvoltage Lockout

If $V_{IN}$ exceeds the input Over Voltage Lockout (OVLO) threshold ($V_{OVLO}$), while the controller is running, the PI354x-00 will complete the current cycle and stop switching. The system will soft start once the input voltage is reestablished and after the Fault Restart Delay.

### Output Overvoltage Protection

The PI354x-00 family is equipped with output Overvoltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds 20% of its set regulated value, the regulator will complete the current cycle and stop switching. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay.

### Overtemperature Protection

The internal package temperature is monitored to prevent internal components from reaching their thermal maximum. If the Overtemperature Protection Threshold (OTP) is exceeded ($T_{OTP}$), the regulator will complete the current switching cycle, enter a low power mode and will soft-start when the internal temperature falls below Over-Temperature Restart Hysteresis ($T_{OTP\_HYS}$).

### Pulse Skip Mode (PSM)

PI354x-00 features a PSM to achieve high efficiency at light loads. The regulators are setup to skip pulses if EAO falls below a PSM threshold. Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Skip Mode threshold.

### Variable Frequency Operation

Each PI354x-00 is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 2), to operate at peak efficiency across line and load variations. At low line and high load applications, the base frequency will decrease to accommodate these extreme operating ranges. By stretching the frequency, the ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

### Parallel Operation

Paralleling modules can be used to increase the output current capability of a single power rail and when interleaved, reduce output voltage ripple.

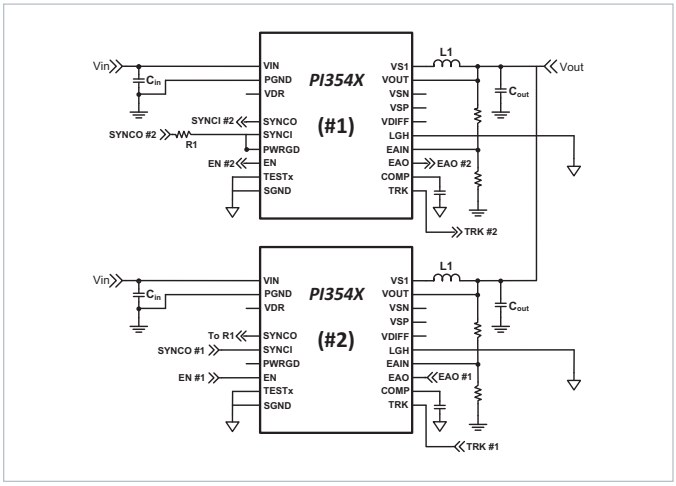



***Figure 50*** *— PI354x-00 parallel operations*

The PI354x-00 can support a maximum number of two interleaved modules. A higher number of modules (up to six maximum) may be connected in parallel without interleaving or synchronization. A user may connect three groups of two phase interleaved modules together, for example.

By connecting the EAO pins and SGND pins of each module together the units will share the current equally, independent of synchronization or interleaving. When the TRK pins of each unit are connected together, the units will track each other during soft-start. All units EN pins have to be released together to allow the units to start (See Figure 50). A fault event occurring in any regulator will disable the other regulators.

To provide synchronization between regulators over a limited operational frequency range, the Power Good (PGD) pin must be connected to the lead regulator's (#1) SYNCI pin and a 2.4 kΩ Resistor, R1, must be placed between SYNCO (#2) return and the lead regulator's SYNCI (#1) pin, as shown in Figure 50. In this configuration, at system soft-start, the PWRGD pin pulls SYNCI low forcing the lead regulator to initialize the open-loop startup synchronization. Once the regulators reach regulation, SYNCI is released and the system is now synchronized in a closed-loop configuration which allows the system to adjust, on the fly, when any of the individual regulators begin to enter variable frequency mode in the loop. The closed loop method is effective in maintaining synchronization if the switching frequency varies to 75% of each regulators programmed switching frequency. If the application requires synchronization over a wider range, please contact Applications Support.

## Application Description

### Output Voltage Set Point

The PI354x-00 family of Buck Regulators utilizes an internal 1 V reference. The output voltage setting is accomplished using external resistors as shown in Figure 51. Select R2 to be at or around 1 k for best noise immunity. Use equations (1) and (2) to determine the proper value based on the desired output voltage.

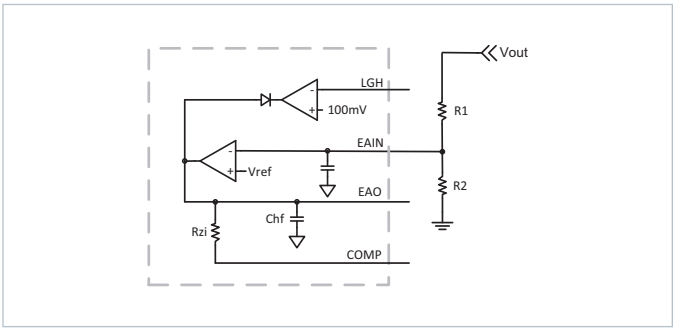



***Figure 51*** *— External resistor divider network*

$$V_{OUT} = V_{ref} \bullet \frac{(R1 + R2)}{R2} \quad (1)$$

$$R1 = -R2 \bullet \frac{(Vref - V_{OUT})}{Vref} \quad (2)$$

*where, Vref = 1 V*

### Soft-Start Adjust and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal capacitor and a fixed charge current to provide a Soft-Start Time tSS for all PI354x-00 regulators. By adding an additional external capacitor to the TRK pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

$C_{TRK} = (t_{TRK} \bullet I_{TRK}) - 47 \bullet 10^{-9}$,

Where, $t_{TRK}$ is the soft-start time and $I_{TRK}$ is a 50 µA internal charge current (see Electrical Characteristics for limits).

There is typically either proportional or direct tracking implemented within a design. For proportional tracking between several regulators at startup, simply connect all PI354x-00 device TRK pins together. This type of tracking will force all connected regulators to startup and reach regulation at the same time (see Figure 52a).

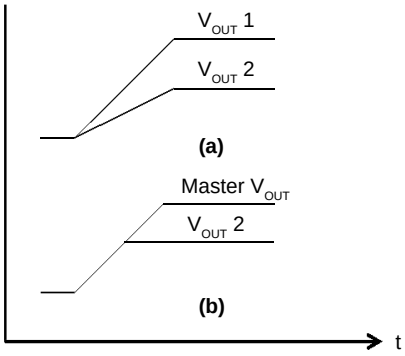



***Figure 52*** *— PI354x-00 tracking methods*

For Direct Tracking, choose the PI354x-00 with the highest output voltage as the master and connect the master to the TRK pin of the other PI354x-00 regulators through a divider (Figure 53) with the same ratio as the slave's feedback divider.

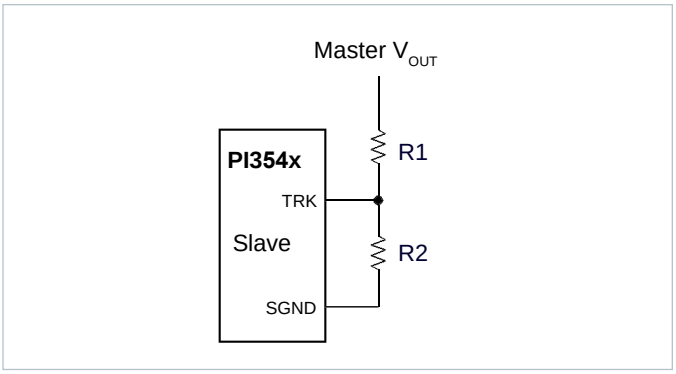



***Figure 53*** *— Voltage divider connections for direct tracking*

All connected PI354x-00 regulator soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 52b. All tracking regulators should have their Enable (EN) pins connected together to work properly.

### Inductor Pairing

The PI354x-00 utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. Table 2 details the specific inductor value and part number utilized for each PI354x-00.

| Device | Inductor (nH) | Inductor Part Number | Manufacturer |
|---|---|---|---|
| PI3542-00 | 340 | FPT1006-340-R | Eaton |
| PI3543-00 | 420 | HCV1206-R42-R | Eaton |
| PI3545-00 | 420 | HCV1206-R42-R | Eaton |
| PI3546-00 | 900 | HCV1206-R90-R | Eaton |

***Table 2*** *— PI354x-00 Inductor pairing*

### Thermal De-rating

Thermal de-rating curves are provided that are based on component temperature changes versus load current, input voltage and air flow. It is recommended to use these curves as a guideline for proper thermal de-rating. These curves represent the entire system and are inclusive to both the Picor regulator and the external inductor. Maximum thermal operation is limited by either the MOSFETs or inductor depending upon line and load conditions.

Thermal measurements were made using a standard PI354x-00 Evaluation board which is 2.5 x 4 inches in area and uses 4-layer, 2oz copper. Thermal measurements were made on the three main power devices, the two internal MOSFETs and the external inductor, with air flows of 0, 200, and 400 LFM.

### Small Signal Model - Constant Voltage Mode

The PI354X product family is a variable frequency CCM/DCM ZVS Buck Regulator. The small signal model for this powertrain is that of a voltage controlled current source which has a trans-conductance that varies depending on the operating mode. When the converter is operating at its normal frequency, it is in discontinuous mode. As the load increases to the point at which the boundary between

discontinuous and continuous modes is reached, the powertrain changes frequency to remain in critical conduction mode. This mode of operation allows the PI354x-00 product family to have a very simple compensation scheme, as the control to output transfer function always has a slope of -1. In addition, when critical conduction is reached, the voltage controlled current source becomes nearly ideal with a high output equivalent resistance.

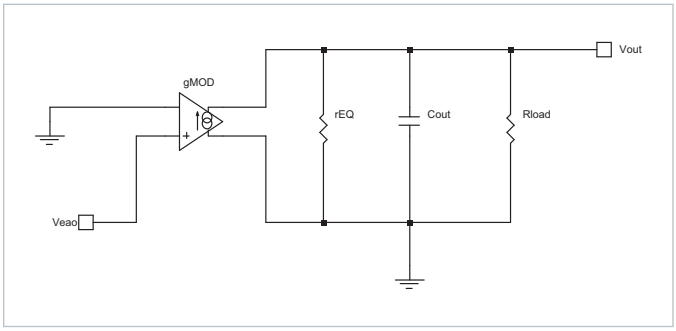



***Figure 54*** *— PI354X Small Signal Model Control-Output*

The control to output transfer function of the PI354x-00 product family is defined as the gain from the output of the error amplifier , through the modulator and to the output voltage. The transfer function equation is shown in Equation (3), where gMOD is assumed to be 7S, rEQ = 0.4 Ohms, $C_{OUT}$ = 600 µF and Rload = 1 Ohm:

$$Gco(s) = \frac{gMOD}{\frac{1}{Rload} + \frac{1}{rEQ} + s\,(C_{OUT})} \qquad (3)$$

The Control-Output transfer function (also known as the small signal modulator gain) has a single pole response determined by the parallel combination of Rload and rEQ and the output capacitor Cout. Equation (4) determines the frequency of the modulator pole:

$$Fpmod = \frac{1}{2 \bullet \pi \bullet \frac{Rload \bullet rEQ}{Rload + rEQ} \bullet C_{OUT}} \qquad (4)$$

Figure 55 depicts the small signal response of the modulator when perturbing EAO and measuring the differential gain and phase from EAO to $V_{OUT}$.

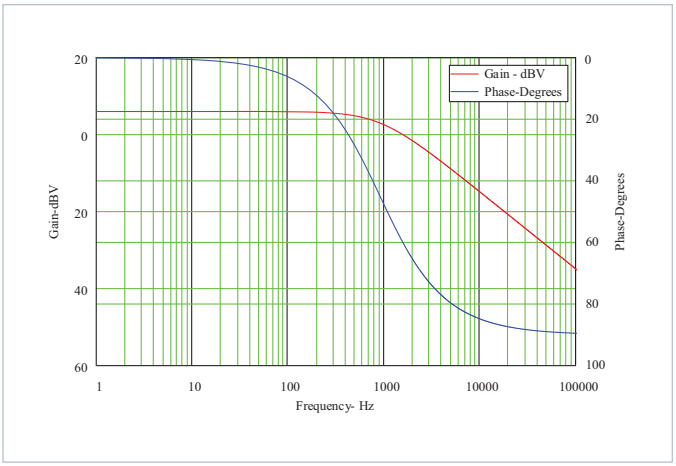



***Figure 55*** *— PI354X Control-Output Gain/Phase Example*

### Error Amplifier

The small signal model of the error amplifier and compensator is shown in Figure 56. The error amplifier is a trans-conductance amplifier (TCA). The transfer function is shown in Equation (5), where in this example R1 = 2.3k, R2 = 1k, GMeao = 5.1mS, $R_{OUT}$ = 1Meg, Chf = 56 pF, Ccomp = 4.7 nF and Rzi = 5 k. Here it is important to note that the external components are Ccomp, R1 and R2. The other components are internal to each specific model. See the data tables section "Soft Start, Tracking And Error Amplifier" for details.

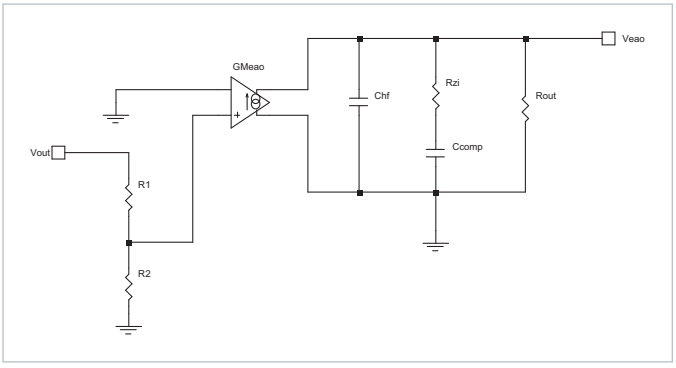



***Figure 56*** *— PI354X Error Amplifier Model*

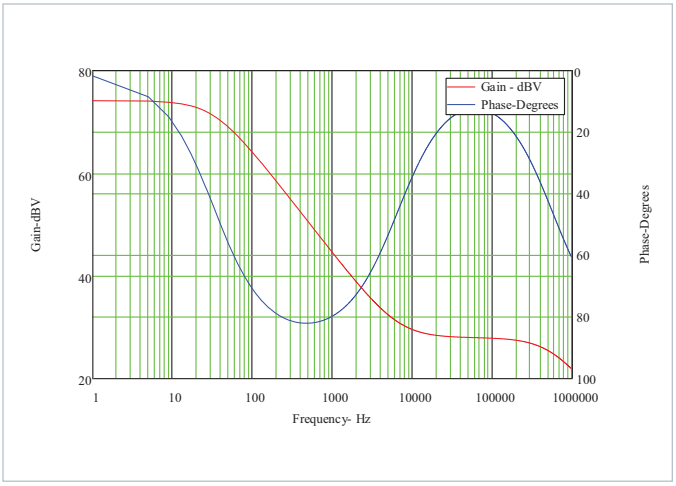



***Figure 57*** *— PI354X Input-Control Gain/Phase*

$$Ginctl(s) = GMeao \bullet \frac{R_{OUT} + s\,(Rzi \bullet Ccomp \bullet R_{OUT})}{1 + s \bullet (Ccomp + Chf) + s^2 \bullet (Chf \bullet Ccomp \bullet Rzi)} \bullet \frac{R2}{R1 + R2} \quad (5)$$

The transfer function of the error amplifier and compensator (also known as the Input To Control transfer function) reveals the response of a Type II amplifier with a low frequency pole determined by Equation (6), a zero which sets the mid-band gain determined by Equation (7) and a high frequency pole determined by Equation (8). Figure 58 shows the calculated Input To Control transfer function. Multiplying Equation (3) by Equation (5) ; described by Equation (9), results in the total loop gain (also known as the Output To Input transfer function). A graph is shown in Figure 58. The strategy is to set the zero such that the mid-band gain allows a high crossover frequency while providing maximum phase boost at crossover, with proper gain and phase margin.

$$Fplf = \frac{1}{2 \bullet \pi \bullet (Rzi + R_{OUT}) \bullet (Ccomp + Chf)} = 33\ Hz \quad (6)$$

$$Fzmb = \frac{1}{2 \bullet \pi \bullet (Rzi \,//\, R_{OUT}) \bullet Ccomp} = 6.8\ kHz \quad (7)$$

$$Fphf = \frac{Chf + Ccomp}{2 \bullet \pi \bullet (Rzi \,//\, R_{OUT}) \bullet Ccomp \bullet Chf} = 580\ kHz \quad (8)$$

$$Goutin(s) = Gco(s) \bullet Ginctl(s) \quad (9)$$

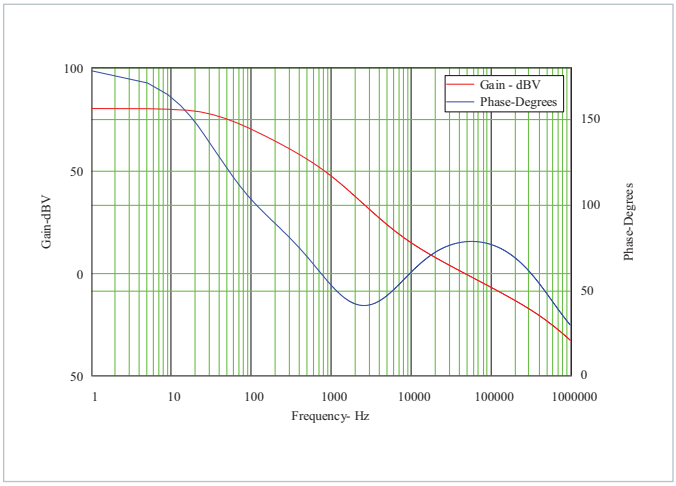



***Figure 58*** — *PI354X Output-Input Gain/Phase*

## Lighting Mode (LGH)

The Lighting (LGH) mode allows the PI354x-00 product family to be able to operate in constant current mode (CC) so that it can support a wide range of applications that require the ability to regulate current or voltage. Primary applications are LED lighting, battery / super-capacitor charging and high peak current pulse transient load applications. The PI354x-00 product family can operate in dual modes, either as a constant voltage (CV) regulator or a constant current (CC) regulator. Both modes can be utilized in a single system. The PI354x-00 family has a separate current amplifier, called LGH, and built in 100 mV lighting reference that has its output connected to the EAO pin internally. If the current through an external shunt starts to develop 100 mV at the LGH pin, the LGH amplifier will take over regulation by pulling down on the EAO output until the current is in regulation according to the designed shunt value. The LGH amplifier is a sink only trans-conductance amplifier (TCA). It does not source current. In the event of an open LED string or open current signal, the voltage loop can be set to regulate the output voltage to a safe or desired value in CV mode.

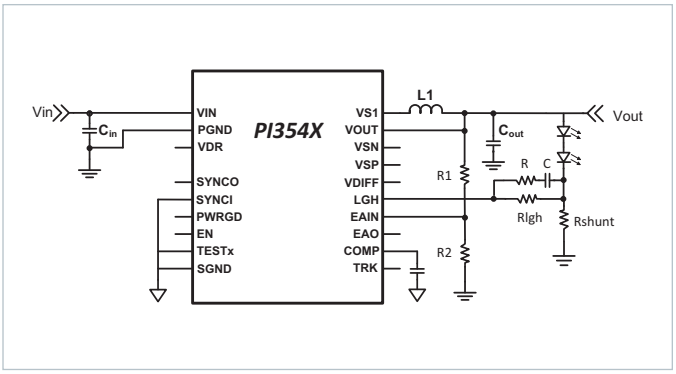



***Figure 59*** — *Lighting Configuration Using CC Mode*

When using the CC mode, it is important to set R1 and R2 appropriately to avoid voltage loop interaction with the current loop. In this case, the voltage setting at the EAIN pin should be set so that the error between it and the 1 V reference is sufficient to force the EAO to be open loop and source current always. When not using the LGH amplifier, the LGH pin should be connected to SGND.

The LGH amplifier is able to sink more current than the error amplifier can source, thus avoiding arbitration issues when transitioning back and forth from LGH mode to voltage mode. The equation for setting the source current for EAO is shown in Equation (10).

$$Ieao = (Veain - Vref) \bullet Gmea > 400\ \mu A \quad (10)$$

### LGH Amplifier Small Signal Model

A small signal model of the LGH amplifier is shown in Figure 60.

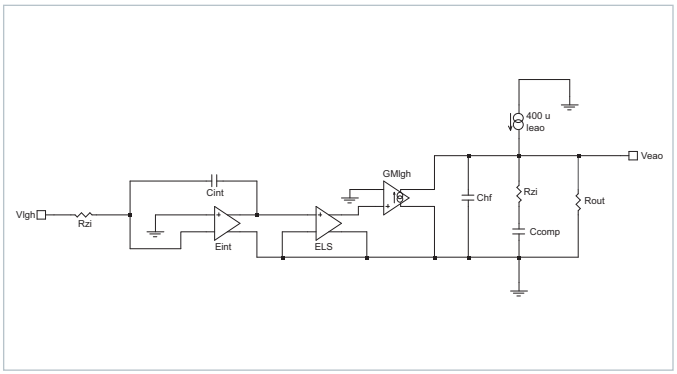



***Figure 60*** *— LGH Amplifier Small Signal Model*

The LGH amplifier consists of three distinct stages. The first is a wide bandwidth integrator stage, followed by a fixed gain level shift circuit. Finally, the level shift circuit drives a trans-conductance (TCA) amplifier with an open collector sink only output stage. Since the LGH output is internally connected to the output of the voltage error amplifier, the compensation components show up in the model and are used by both stages, depending on which one is in use. Only one stage should be in use at a time. When using LGH or if the LGH input rises above the internal reference, the voltage error amplifier acts as a 400uA current source pull up for the EAO pin.

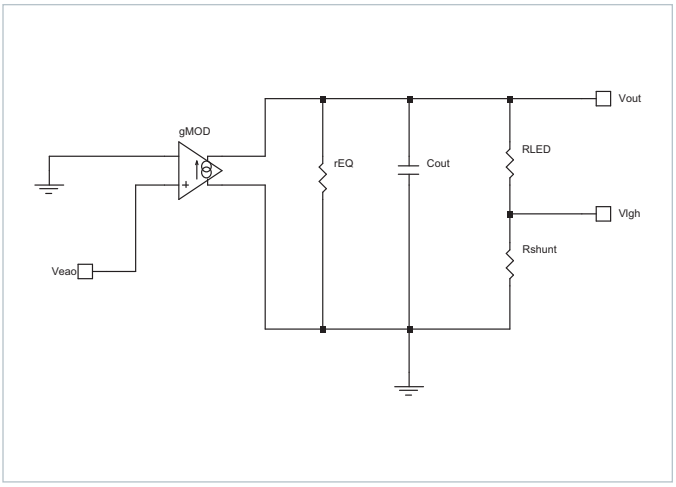



***Figure 61*** *— Lighting Application Modulator Gain Model*

Figure 61 shows a small signal model of the modulator gain when using the application circuit shown in Figure 59 with two 3.4 V high current LED's in series. RLED is the series combination of the AC resistance of each LED, which is 0.2 Ohms. Rshunt is used to sense the current through the LED string. It has a value of 0.050 Ohms in this case. The other component values were defined earlier and remain the same values. Equation (11) defines the transfer function of the modulator and Equation (12) defines the pole of transfer function. The transfer function of the LGH amplifier is defined in Equation (13). The open loop gain of Eint is 2500 and ELS = 4.4.

$$Gled(s) = gMOD \bullet (rEQ \bullet Rshunt)/((Rshunt + RLED + rEQ) + s\,(C_{OUT} \bullet rEQ \bullet RLED + Rshunt \bullet rEQ \bullet C_{OUT})) \quad (11)$$

$$Fpled = \frac{1}{2 \bullet \pi \bullet ((RLED + Rshunt))//reQ) \bullet C_{OUT}} = 1.2\ kHz \quad (12)$$

$$Glgheao(s) = Eint\,(s) = \bullet\ ELS \bullet GMlgh \bullet \frac{R_{OUT} + s\,(Rzi \bullet Ccomp \bullet R_{OUT})}{1 + s \bullet (Ccomp + Chf) + s^2 \bullet (Chf \bullet Ccomp \bullet Rzi)} \quad (13)$$

$$Fphf = \frac{Chf + Ccomp}{2 \bullet \pi \bullet (Rzi\ //\ R_{OUT}) \bullet Ccomp \bullet Chf} = 580\ kHz \quad (14)$$

The integrator pole is determined by the external input resistor Rlgh and the internal Cint, which is 20 pF. Assuming Rlgh = 100 k and Eint = 2500:

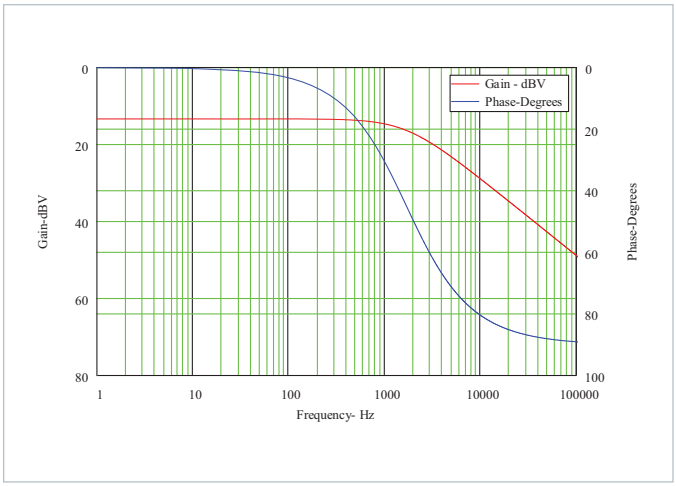



***Figure 62*** *— Gled(s) Gain/Phase Plot*

Figure 62 is the Bode plot of the Gled(s) transfer function, which in LGH mode is what needs to be compensated for by the LGH amplifier and compensator. This transfer function defines the gain and phase from the error amplifier output (EAO) to the current shunt Rshunt. Figure 65 is a plot of the transfer function Glgheao(s), which defines the gain and phase from the LGH pin (voltage across current sensing Rshunt) to EAO. As shown in Equation (13), the output is dependent on the integrator stage and the following trans-conductance stage. Figures 63 and 64 show the two individual sections that make up Equation (13) which produces Glgheao(s).

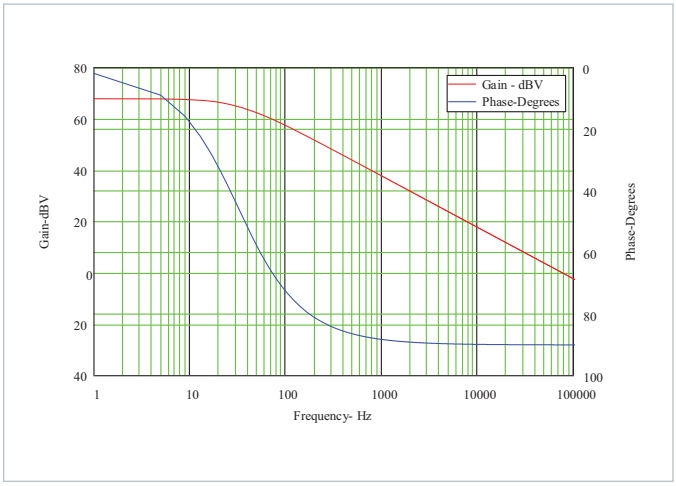



***Figure 63*** *— Eint(s) Gain/Phase Plot Rlgh = 100k*

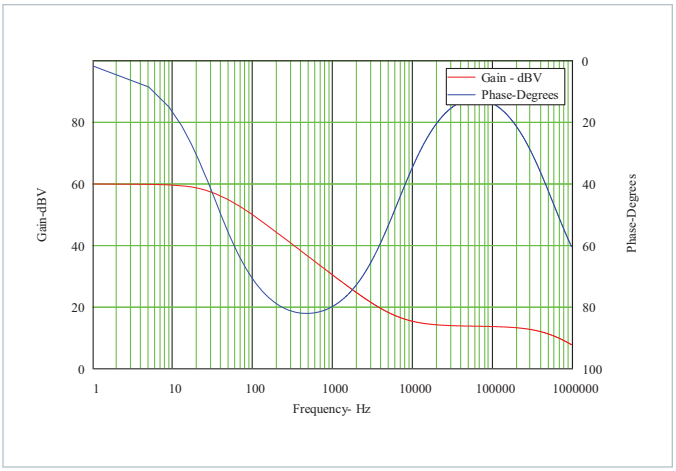



***Figure 64*** *— GMlgh(s) Gain/Phase Plot Voltage Loop Open*

The GMlgh(s) plot is from integrator to EAO with the voltage loop open and sourcing 400uA of current.

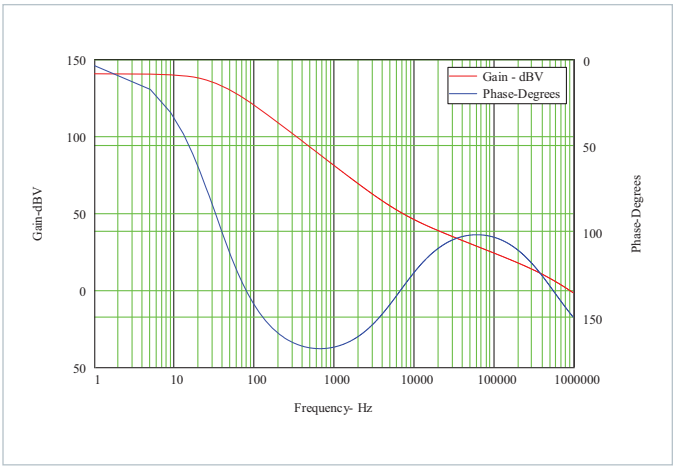



***Figure 65*** *— Glgheao(s) Gain/Phase Plot Rlgh = 100k*

When combining Figure 63 with Figure 64, it becomes clear that additional compensation is needed to have enough phase and gain margin like can be seen with the voltage loop plot. We can remedy that easily, by adding a series R-C in parallel with Rlgh as shown in the lighting application diagram in Figure 59. The capacitor will be chosen to work with Rlgh to add a zero approximately 1.2 kHz before the zero provided by the GMlgh(s) transfer function (the trans-conductance stage of the LGH amplifier). This value will be chosen to be 270 pF. The external added resistor will form a high frequency pole to roll the gain off at higher frequency. This pole will be set at approximately 120 kHz so a common 4.99 k resistor will be used. The resulting Bode plot with the new compensator of Glgheao(s) can be seen in Figure 66. Figure 67 shows the final Bode plot of the loop gain when using a lighting application with LED's operating in constant current mode. Note that it is very important to understand the AC resistance of the LED's that are being used. Please consult the LED manufacturer for details. For a series string, you should add the individual LED resistances and combine them into one lumped value to simplify the analysis.

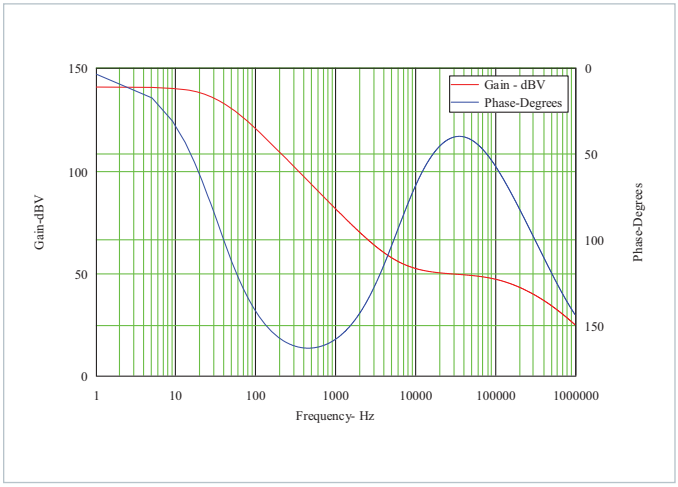



***Figure 66*** — *GMlgh(s) Gain/Phase Plot Compensated*

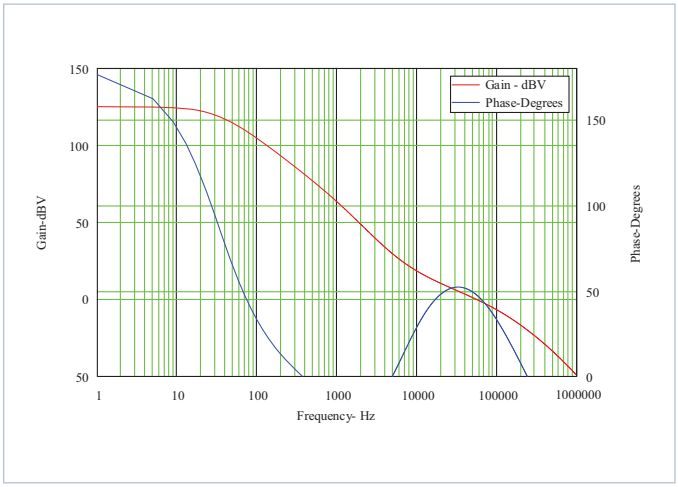



***Figure 67*** — *Lighting Application Loop Gain/Phase Plot*

## Filter Considerations

The PI354x-00 requires low impedance ceramic input capacitors (X7R/X5R or equivalent) to ensure proper start up and high frequency decoupling for the power stage. The PI354x-00 will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET(s) are conducting. During the time the MOSFET(s) are off, the input capacitors are replenished from the source. Table 4 shows the recommended input and output capacitors to be used for the PI354x-00 as well as per capacitor RMS ripple current and the input and output ripple voltages. Table 5 includes the recommended input and output ceramic capacitors.

It is very important to verify that the voltage supply source as well as the interconnecting lines are stable and do not oscillate.

**Input Filter Case 1; Inductive source and local, external, input decoupling capacitance with negligible ESR (i.e.: ceramic type):**

The voltage source impedance can be modeled as a series R(line) L(line) circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{line} > \frac{L_{line}}{(Cin_{int} + Cin_{ext}) \bullet |r\_EQin|} \quad (16)$$

$$R_{line} << |r\_EQin| \quad (17)$$

Where r_EQin can be calculated by dividing the lowest line voltage by the full load input current. It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, Equation (17). However, R_line cannot be made arbitrarily low otherwise Equation (16) is violated and the system will show instability, due to an under-damped RLC input network.

**Input Filter case 2; Inductive source and local, external input decoupling capacitance with significant RCIN_EXT ESR (i.e.: electrolytic type):**

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor Lline.

$$|r\_EQin| > R_{cin_{ext}} \quad (18)$$

$$\frac{L_{line}}{(Cin_{int} \bullet R_{cin_{ext}})} > |r\_EQin| \quad (19)$$

Notice that, the high performance ceramic capacitors CIN_INT within the PI354x-00 should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

Equation (19) shows that if the aggregate ESR is too small – for example by using very high quality input capacitors ($C_{IN\_EXT}$) – the system will be under-damped and may even become destabilized. As noted, an octave of design margin in satisfying Equation (18) should be considered the minimum.

When applying an electrolytic capacitor for input filter damping the ESR value must be chosen to avoid loss of converter efficiency and excessive power dissipation in the electrolytic capacitor.

### VDR Bias Regulator

The VDR internal bias regulator is a ZVS switching regulator that resides internal to the PI354x-00 product family. It is intended strictly for use to power the internal controller and driver circuitry. The power capability of this regulator is sized only for the PI354x-00, with adequate reserve for the application it was intended for. It may be used for as a pull-up source for open collector applications and for other very low power use with the following restrictions:

1. No direct connection is allowed. Any noise source that can disturb the VDR voltage can also affect the internal controller operation.
2. All loads must be locally de-coupled using a 0.1 µF ceramic capacitor. This capacitor must be connected to the VDR output through a series resistor no smaller than 1 k. which forms a loss pass filter and limits the total current to 5 mA.

### System Design Considerations

1. Inductive loads- As with all power electronic applications, consideration must be given to driving inductive loads that may be exposed to a fault in the system which could result in consequences beyond the scope of the power supply primary protection mechanisms. An inductive load could be a filter, fan motor or even excessively long cables. Consider an instantaneous short circuit through an un-damped inductance that occurs when the output capacitors are already at an initial condition of fully charged. The only thing that limits the current is the inductance of the short circuit and any series resistance. Even if the power supply is off at the time of the short circuit, the current could ramp up in the external inductor and store considerable energy. The release of this energy will result in considerable ringing, with the possibility of ringing nodes connected to the output voltage below ground. The system designer should plan for this by considering the use of other external circuit protection such as load switches, fuses, and transient voltage protectors. The inductive filters should be critically damped to avoid excessive ringing or damaging voltages. Adding a high current Schottky diode from the output voltage to PGND close to the PI354x-00 is recommended for these applications.
2. Low voltage operation – there is no isolation from an SELV (Safety-Extra-Low-Voltage) power system. Powering low voltage loads from input voltages as high as 60 V may require additional consideration to protect low voltage circuits from excessive voltage in the event of a short circuit from input to output. A fast TVS (transient voltage suppressor) gating an external load switch is an example of such protection.
3. Use of Lighting Mode (LGH) as a battery charger is certainly very feasible. It is fashionable to design these chargers such that the battery is always connected to it. Since the Buck topology is not isolated, shorting the input terminals or capacitors of an unpowered regulator/charger could allow damaging current flow through the body diode of the high side MOSFET that would be unprotected by a conventional input fuse. It is recommended to connect the PI354x-00 family to the battery using an active ORing device if LGH mode is used as a constant current battery charger. The same should be considered for super-capacitor applications as well.

| Device | $V_{IN}$ (V) | $I_{LOAD}$ (A) | $C_{INPUT}$ Ceramic X5R | $C_{OUTPUT}$ Ceramic X5R | $C_{INPUT}$ Ripple Current ($I_{RMS}$) | $C_{OUTPUT}$ Ripple Current ($I_{RMS}$) | Input Ripple (mVpp) | Output Ripple (mVpp) | Transient Deviation (mVpk) | Recovery Time (µs) | Load Step (A) (Slew/µs) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PI3542 | 48 | 10 | 5 x 2.2 µF 100 V | 6 x 100 µF | 0.7 | 1.32 | 416 | 47 | -/+80 | 40 | 5 (1 A/µs) |
| | | 5 | | | | | 220 | 22 | | | |
| PI3543 | 48 | 10 | 5 x 2.2 µF 100 V | 6 x 100 µF | 0.8 | 1.3 | 464 | 61.6 | -/+90 | 40 | 5 (1 A/µs) |
| | | 5 | | | | | 230 | 31 | | | |
| PI3545 | 48 | 10 | 5 x 2.2 µF 100 V | 6 x 47 µF | .88 | 1.37 | 485 | 62 | -/+150 | 40 | 5 (1 A/µs) |
| | | 5 | | | | | 245 | 32 | | | |
| PI3546 | 48 | 9 | 5 x 2.2 µF 100 V | 6 x 10 µF | 1.12 | 1.26 | 880 | 114 | -/+300 | 20 | 5 (1 A/µs) |
| | | 4.5 | | | | | 125 | 33 | | | |

***Table 3*** *— Recommended input and output capacitance*

| Murata Part Number | Description |
|---|---|
| C3225X7S1H1106M250AB | 2.2 µF 100 V 1210 X7R |
| C3225X7S1H106M250AB | 10 µF 50 V 1210 X7R |
| GRM31CR60J107ME39L | 100 µF 6.3 V 1206 X7R |
| GRM31CR61A476ME15L | 47 µF 10 V 1206 X5R |
| GRM32ER61H106MA12 | 10 µF 50 V 1210 X7R |

***Table 4*** *— Capacitor manufacturer part numbers*

## Layout Guidelines

To optimize maximum efficiency and low noise performance from a PI354x-00 design, layout considerations are necessary. Reducing trace resistance and minimizing high current loop returns along with proper component placement will contribute to optimized performance.

A typical buck converter circuit is shown in Figure 68. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

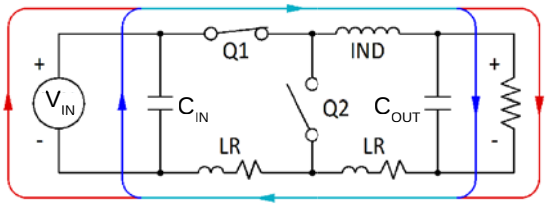



***Figure 68*** *— Typical Buck Regulator*

The path between the COUT and CIN capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on. Figure 69, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI354x-00 performance.

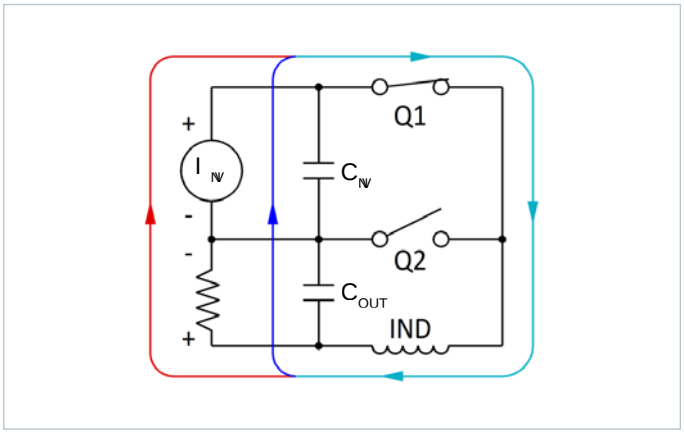



***Figure 69*** *— Current flow: Q1 closed*

When Q1 is on and Q2 is off, the majority of $C_{IN}$'s current is used to satisfy the output load and to recharge the $C_{OUT}$ capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the $C_{OUT}$ capacitor as shown in Figure 70. During this period $C_{IN}$ is also being recharged by the $V_{IN}$. Minimizing $C_{IN}$ loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the $C_{IN}$ loop and $C_{OUT}$ loop is vital to minimize switching and GND noise.

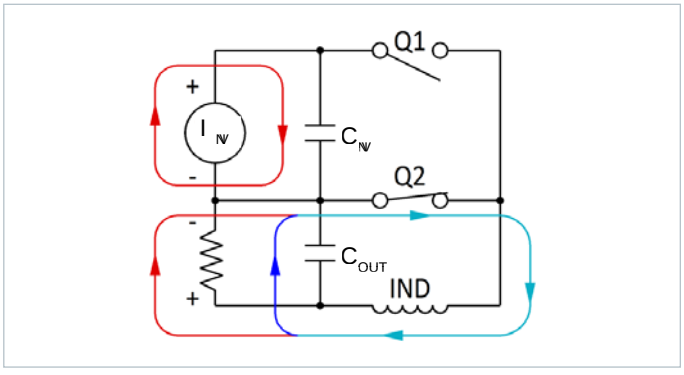



***Figure 70*** *— Current flow: Q2 closed*

The recommended component placement, shown in Figure 71, illustrates the tight path between $C_{IN}$ and $C_{OUT}$ (and $V_{IN}$ and $V_{OUT}$) for the high AC return current. This optimized layout is used on the PI354x-00 evaluation board.

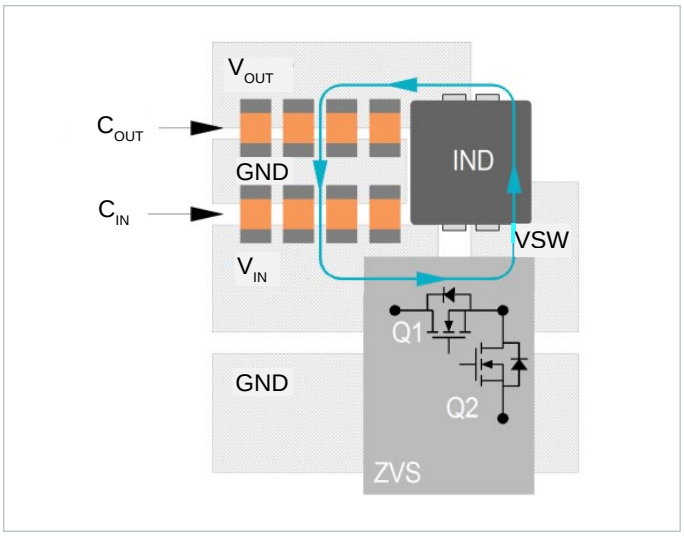



***Figure 71*** — *Recommended component placement and metal routing*

Figure 72 details the recommended receiving footprint for PI354x-00 10 mm x 10 mm package. All pads should have a final copper size of 0.55 mm x 0.55 mm, whether they are solder-mask defined or copper defined, on a 1 mm x 1 mm grid. All stencil openings are 0.45 mm when using either a 5 mil or 6 mil stencil.

## Recommended PCB Footprint and Stencil

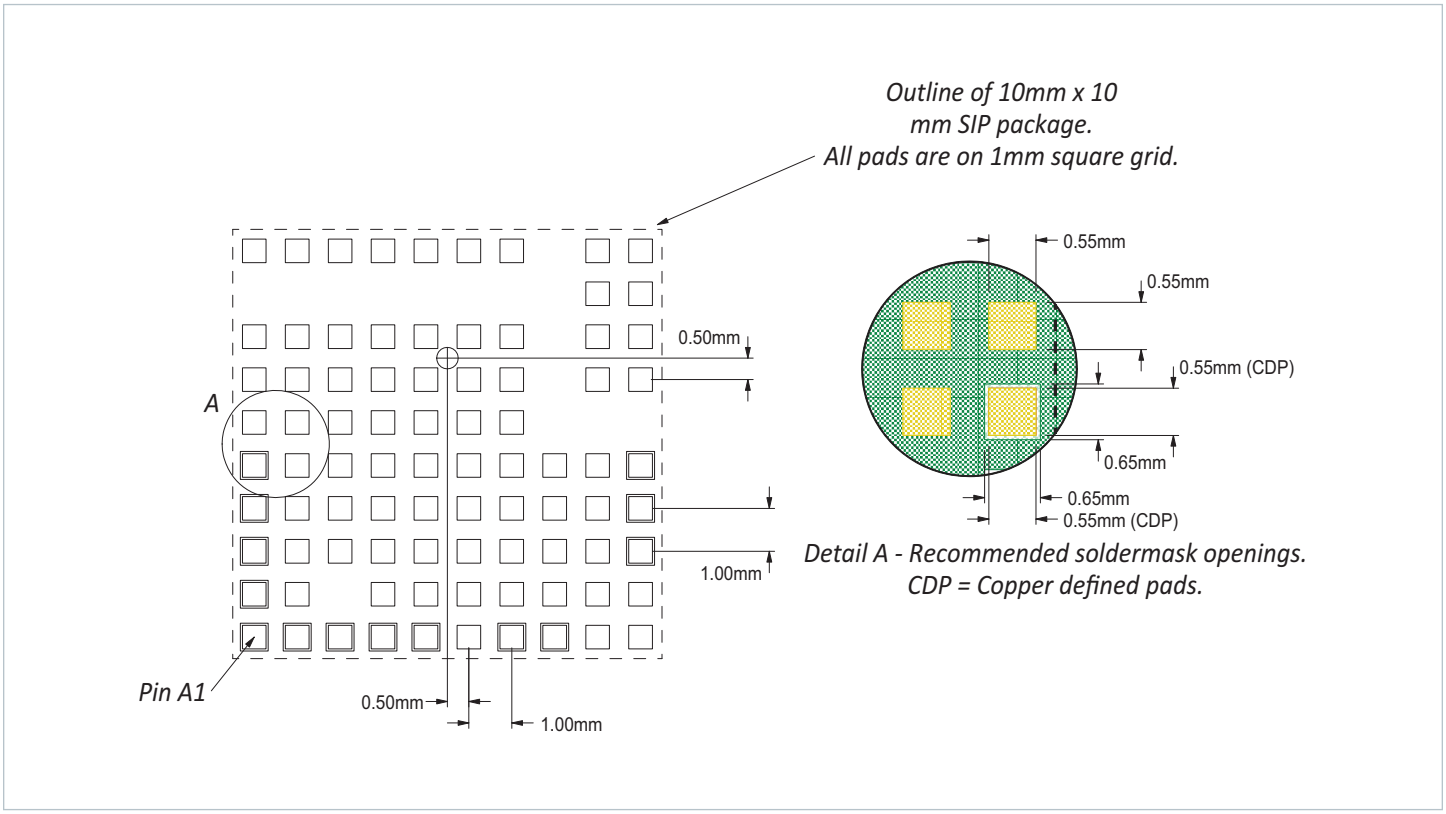
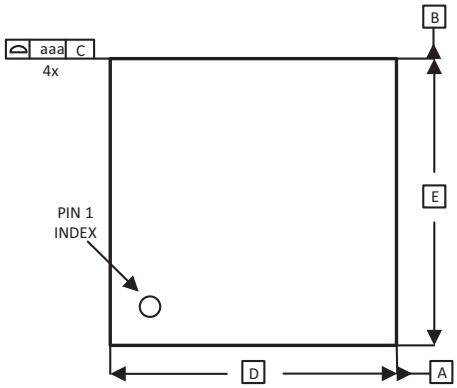
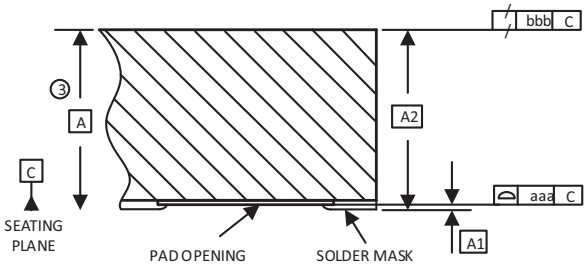



***Figure 72*** — *Recommended Receiving PCB footprint*

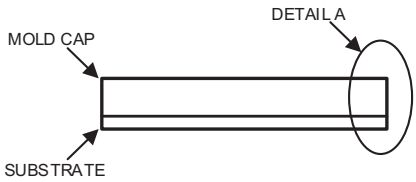
## Package Drawings



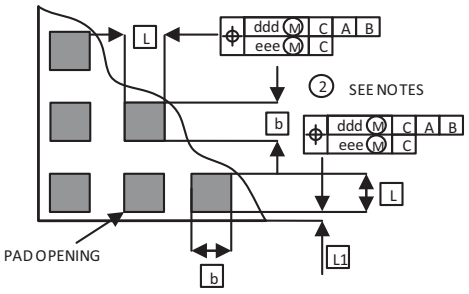

PACKAGE TOP VIEW



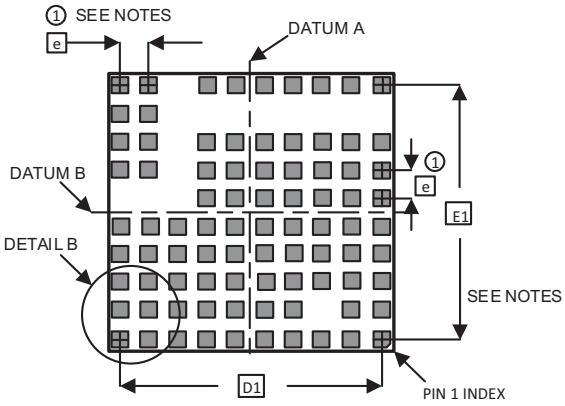

DETAIL A




PACKAGE SIDE VIEW




DETAIL B




PACKAGE BOTTOM VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 2.49 | 2.56 | 2.63 |
| A1 | – | – | 0.04 |
| A2 | – | – | 2.59 |
| b | 0.50 | 0.55 | 0.60 |
| L | 0.50 | 0.55 | 0.60 |
| D | 10.00 BSC | | |
| E | 10.00 BSC | | |
| D1 | 9.00 BSC | | |
| E1 | 9.00 BSC | | |
| e | 1.00 BSC | | |
| L1 | 0.175 | 0.225 | 0.275 |
| aaa | | | 0.10 |
| bbb | | | 0.10 |
| ccc | | | 0.08 |
| ddd | | | 0.10 |
| eee | | | 0.08 |

DIMENSIONS

NOTES

1. 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. DIMENSION 'b' APPLIES TO METALLIZED PAD OPENING.
3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
4. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
5. ALL DIMENSIONS IN MILLIMETERS.

## Revision History

| Revision | Date | Description | Page Number(s) |
|---|---|---|---|
| 1.0 - 1.1 | 05/2015 | Released Engineering format/style | n/a |
| 1.2 | 10/12/15 | Reformatted in new template | n/a |
| 1.3 | 02/19/2016 | Updated PCB Footprint | 34 |

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