# 3.3V/2.5V Step-Up/ Step-Down Charge Pump DC/DC Converter

## FEATURES

- **Step-Up/Step-Down Charge Pumps Generate Fixed 3.3V or 2.5V Outputs**
- **$V_{IN}$ Range: 1.8V to 5.5V**
- **Output Current up to 150mA**
- **Automatic Mode Switching**
- Constant Frequency (1.2MHz) Operation in Step-Up Mode
- Low Dropout Regulator Operation in Step-Down Mode
- Low No-Load Quiescent Current: $I_Q$ = 65µA
- Built-In Soft-Start Reduces Inrush Current
- Shutdown Disconnects Load from Input
- Shutdown Current < 1µA
- Short-Circuit/Thermal Protection
- Available in a 6-Lead (2mm × 2mm) DFN Package

## APPLICATIONS

- 2 AA to 2.5V
- 2-3 AA/Li-Ion to 3.3V
- Low Power Supplies for Cameras, I/O Supplies, Audio, PC Cards, Misc. Logic, etc., in a Wide Variety of Handheld Products

## DESCRIPTION

The LTC®3240-3.3/LTC3240-2.5 are step-up/step-down charge pump DC/DC converters that produce a fixed regulated output voltage of 3.3V or 2.5V over a wide input voltage range (1.8V to 5.5V).

With input voltages greater than the regulated output voltage the LTC3240 operates as a low dropout regulator. Once the input voltage drops within 100mV of the regulated output voltage the part automatically switches to step-up mode. In step-up mode the LTC3240 operates as a constant frequency (1.2MHz) doubling charge pump.

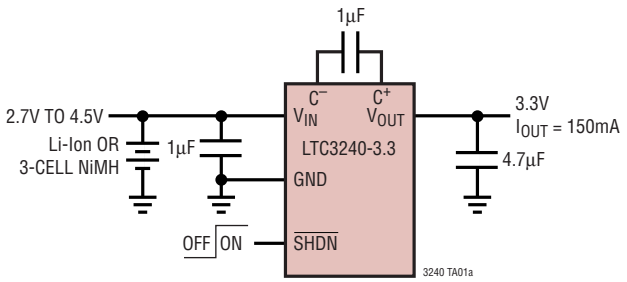
The LTC3240-3.3/LTC3240-2.5 feature low no load operating current (65µA typical) and ultralow operating current in shutdown (<1µA). Built-in soft-start circuitry prevents excessive inrush current during start-up. Thermal shutdown and current-limit circuitry allow the parts to survive a continuous short-circuit from $V_{OUT}$ to GND.

The LTC3240-3.3/LTC3240-2.5 require only three tiny external ceramic capacitors for an ultrasmall application footprint. The LTC3240-3.3/LTC3240-2.5 are available in a 6-pin (2mm × 2mm) DFN package.

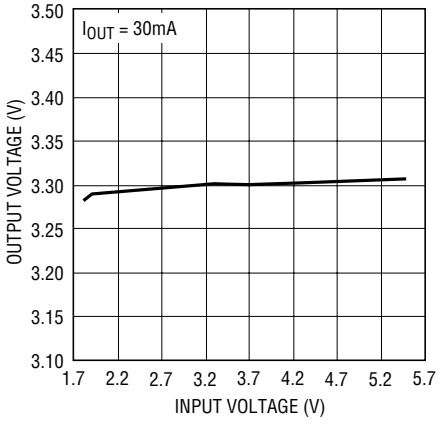
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Protected by U.S. Patents including 6411531.

## TYPICAL APPLICATION

**Li-Ion to 3.3V at Up to 150mA**




**Output Voltage vs Input Voltage (Full Range)**

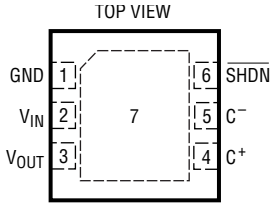


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$ to GND .....–0.3V to 6V
$V_{OUT}$ to GND .....–0.3V to 5.5V
$\overline{SHDN}$ to GND.....–0.3V to ($V_{IN}$ + 0.3V)
$V_{OUT}$ Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 2) ...–40°C to 85°C
Storage Temperature Range.....–65°C to 125°C
Maximum Junction Temperature .....125°C

## PACKAGE/ORDER INFORMATION




DC PACKAGE
6-LEAD (2mm × 2mm) PLASTIC DFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 80°C/W (NOTE 4)
EXPOSED PAD (PIN 7) IS GND, MUST BE SOLDERED TO PCB

| ORDER PART NUMBER | DC PART MARKING |
|---|---|
| LTC3240EDC-3.3 | LBXJ |
| LTC3240EDC-2.5 | LCBP |

**Order Options** Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C, $\overline{SHDN}$ = $V_{IN}$, $C_{FLY}$ = 1µF, $C_{IN}$ = 1µF, $C_{OUT}$ = 4.7µF unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage Range | | ● | 1.8 | | 5.5 | V |
| $V_{OUT}$ | Output Voltage Range<br>LTC3240-3.3 | 1.8V ≤ $V_{IN}$ ≤ 2.5V, $I_{OUT}$ < 40mA<br>2.5V ≤ $V_{IN}$ ≤ 5.5V, $I_{OUT}$ < 150mA | ●<br>● | 3.168<br>3.168 | 3.3<br>3.3 | 3.432<br>3.432 | V<br>V |
| | LTC3240-2.5 | 1.8V ≤ $V_{IN}$ ≤ 5.5V, $I_{OUT}$ < 60mA | ● | 2.4 | 2.5 | 2.6 | V |
| $I_{IN}$ | No Load Input Current | $I_{OUT}$ = 0, 1.8V ≤ $V_{IN}$ ≤ 5.5V | | | 65 | 100 | µA |
| $I_{\overline{SHDN}}$ | Shutdown Current | $\overline{SHDN}$ = 0V, $V_{OUT}$ = 0V | | | 0.1 | 1 | µA |
| η | Efficiency<br>LTC3240-3.3 | $V_{IN}$ = 2.5V, $I_{OUT}$ = 100mA<br>$V_{IN}$ = 3.7V, $I_{OUT}$ = 100mA | | | 64<br>87 | | %<br>% |
| | LTC3240-2.5 | $V_{IN}$ = 2V, $I_{OUT}$ = 50mA<br>$V_{IN}$ = 3V, $I_{OUT}$ = 50mA | | | 63<br>83 | | %<br>% |
| $V_{IH}$ | $\overline{SHDN}$ Input High Voltage | 1.8V ≤ $V_{IN}$ ≤ 5.5V | ● | 1.2 | | | V |
| $V_{IL}$ | $\overline{SHDN}$ Input Low Voltage | 1.8V ≤ $V_{IN}$ ≤ 5.5V | ● | | | 0.4 | V |
| $I_{IH}$ | $\overline{SHDN}$ Input Current | $V_{\overline{SHDN}}$ = $V_{IN}$ = 5.5V | ● | –1 | | 1 | µA |
| $I_{IL}$ | $\overline{SHDN}$ Input Current | $V_{\overline{SHDN}}$ = 0V | ● | –1 | | 1 | µA |
| $I_{LIM}$ | Output Current Limit | $V_{IN}$ = 3.7V, $V_{OUT}$ = 0V Step-Down Mode<br>$V_{IN}$ = 2.4V, $V_{OUT}$ = 0V Step-Up Mode | | | 450<br>270 | | mA<br>mA |
| $t_{ON}$ | $V_{OUT}$ Turn-On Time | From the Rising Edge of $\overline{SHDN}$ to 90% of $V_{OUT}$<br>$V_{IN}$ = 2.5V, $R_{LOAD}$ = 66Ω<br>$V_{IN}$ = 3.7V, $R_{LOAD}$ = 66Ω | | | <br>0.5<br>0.4 | | <br>ms<br>ms |
| **Step-Up Mode** | | | | | | | |
| $I_{BURST}$ | Burst Mode Threshold | $V_{IN}$ = 2.4V | | | 15 | | mA |
| $V_{RIPPLE}$ | Output Ripple | $I_{OUT}$ = 100mA, $V_{OUT}$ = 2.5V or 3.3V | | | 20 | | $mV_{P-P}$ |
| $f_{OSC}$ | Switching Frequency | $V_{IN}$ = 2.4V | ● | 0.6 | 1.2 | 1.8 | MHz |
| $V_{RIPPLE(BURST)}$ | Burst Mode® Output Ripple | $V_{IN}$ = 2.4V | | | 20 | | $mV_{P-P}$ |

Burst Mode is a registered trademark of Linear Technology Corporation.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C, $\overline{SHDN}$ = $V_{IN}$, $C_{FLY}$ = 1µF, $C_{IN}$ = 1µF, $C_{OUT}$ = 4.7µF unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $R_{OL}$ | Effective Open-Loop Output Resistance | Doubler Mode | | | | |
| | LTC3240-3.3 | $V_{IN}$ = 1.8V, $V_{OUT}$ = 3V | | 7.5 | | Ω |
| | LTC3240-2.5 | $V_{IN}$ = 1.8V, $V_{OUT}$ = 2.25V | | 8.0 | | Ω |
| | (Note 3) | | | | | |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3240-3.3/LTC3240-2.5 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

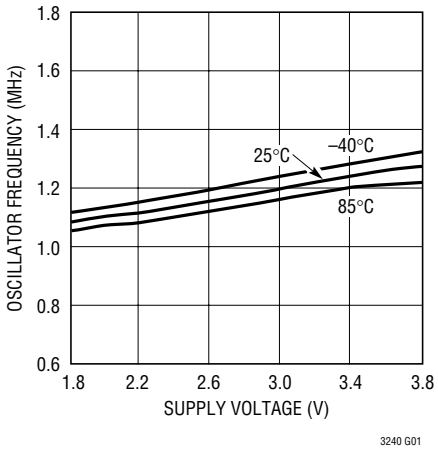
**Note 3:** $R_{OL} \equiv (2V_{IN} - V_{OUT})/I_{OUT}$

**Note 4:** Failure to solder the exposed backside of the package to a PCB ground plane will result in a thermal resistance much higher than 80°C/W.

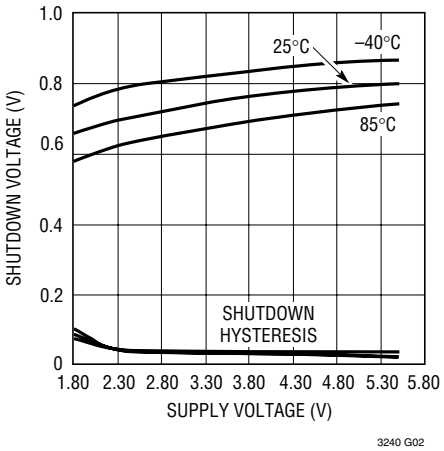
## TYPICAL PERFORMANCE CHARACTERISTICS

**($T_A$ = 25°C, $C_{FLY}$ = $C_{IN}$ = 1µF, $C_{OUT}$ = 4.7µF unless otherwise noted)**

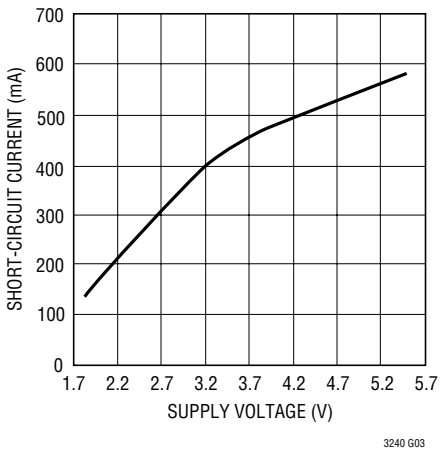
**Oscillator Frequency vs Supply Voltage (Doubler Mode)**



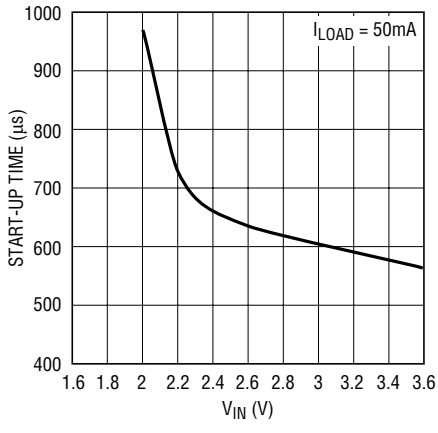

**$\overline{SHDN}$ Threshold Voltage vs Supply Voltage**



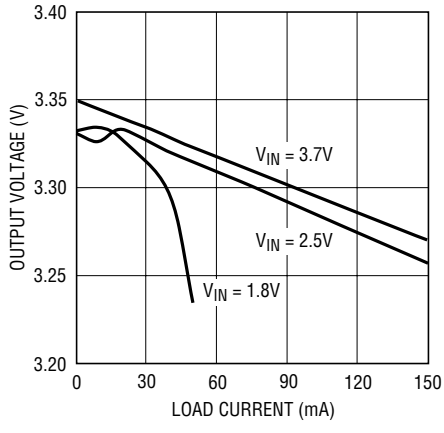

**Short-Circuit Current vs Supply Voltage**



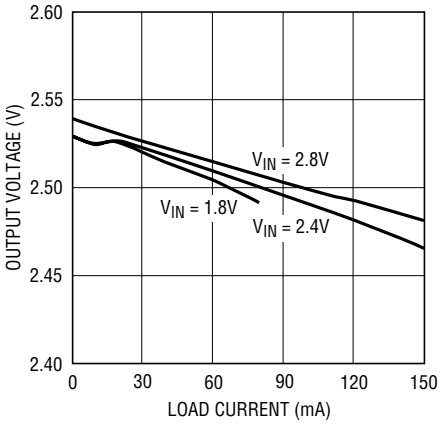

**Start-Up Time vs Supply Voltage**




**Load Regulation (LTC3240-3.3)**

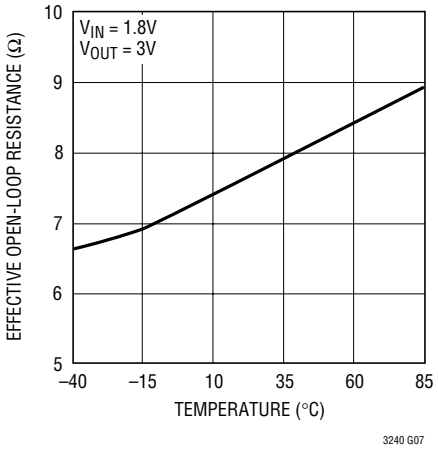



**Load Regulation (LTC3240-2.5)**

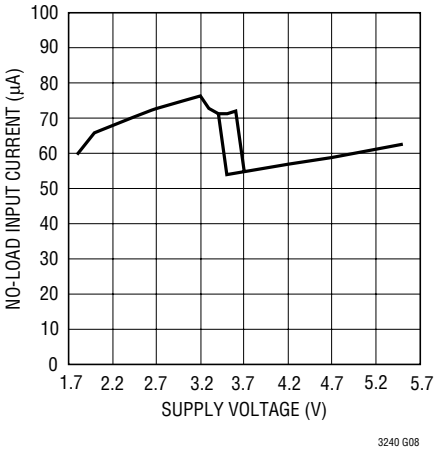


## TYPICAL PERFORMANCE CHARACTERISTICS ($T_A$ = 25°C, $C_{FLY}$ = $C_{IN}$ = 1µF, $C_{OUT}$ = 4.7µF unless otherwise noted)

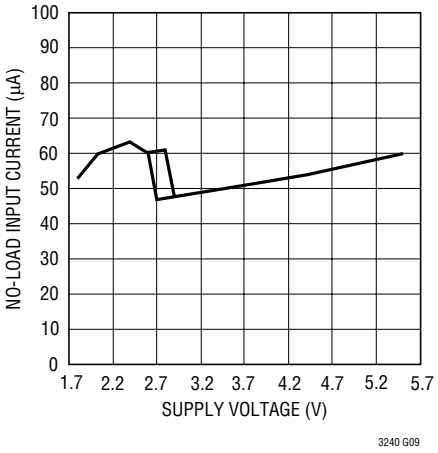
### Effective Open-Loop Resistance vs Temperature (LTC3240-3.3)



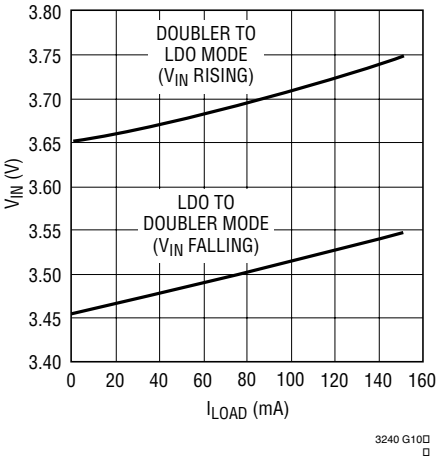

### No-Load Input Current vs Supply Voltage (LTC3240-3.3)



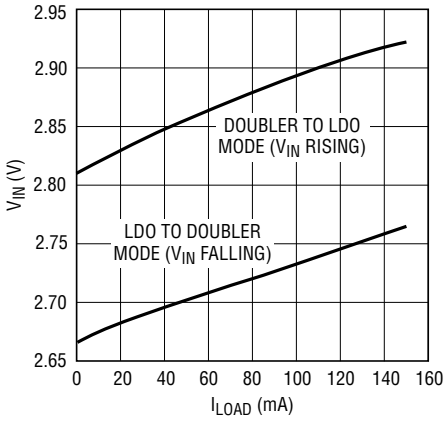

### No-Load Input Current vs Supply Voltage (LTC3240-2.5)



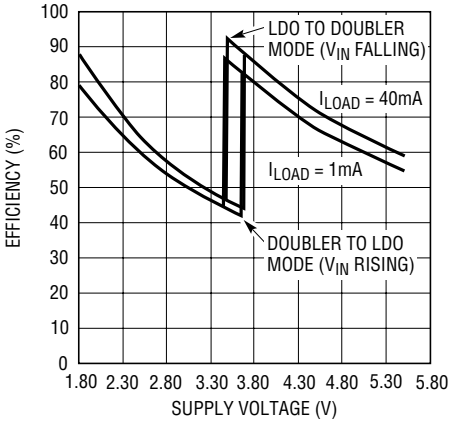

### Mode Switch Threshold vs Load Current (LTC3240-3.3)



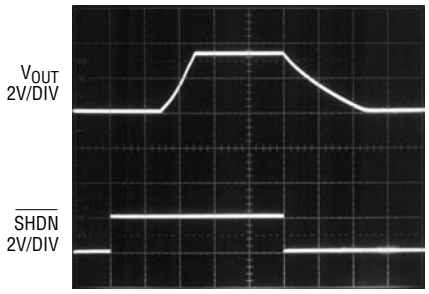

### Mode Switch Threshold vs Load Current (LTC3240-2.5)



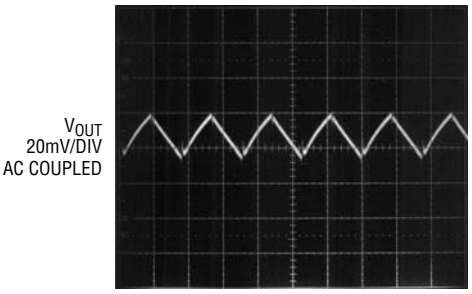

### Efficiency vs Supply Voltage (LTC3240-3.3)




### $V_{OUT}$ Soft-Start (LTC3240-3.3)



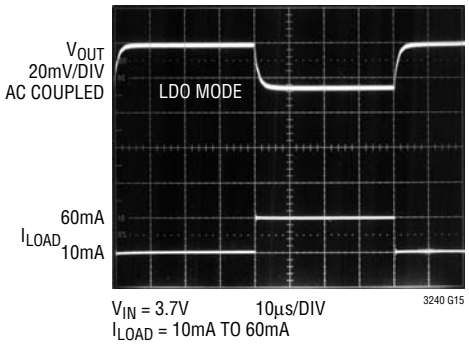

### Output Noise/Ripple (LTC3240-3.3)



## TYPICAL PERFORMANCE CHARACTERISTICS

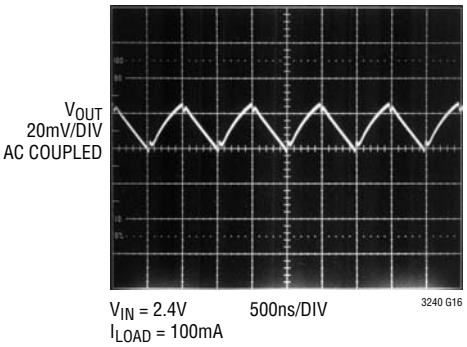
($T_A$ = 25°C, $C_{FLY}$ = $C_{IN}$ = 1µF, $C_{OUT}$ = 4.7µF unless otherwise noted)

**Load Transient Response (LTC3240-3.3)**



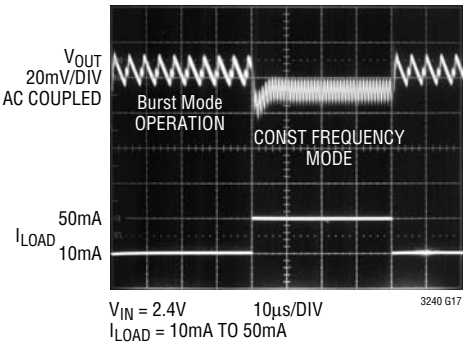

$V_{IN}$ = 3.7V 10µs/DIV
$I_{LOAD}$ = 10mA TO 60mA

**Output Noise/Ripple (LTC3240-2.5)**




$V_{IN}$ = 2.4V 500ns/DIV
$I_{LOAD}$ = 100mA

**Load Transient Response (LTC3240-2.5)**




$V_{IN}$ = 2.4V 10µs/DIV
$I_{LOAD}$ = 10mA TO 50mA

## PIN FUNCTIONS

**GND (Pin 1):** Ground. This pin should be tied to a ground plane for best performance.

**$V_{IN}$ (Pin 2):** Input Supply Voltage. $V_{IN}$ should be bypassed with a 1µF or greater, low ESR ceramic capacitor.

**$V_{OUT}$ (Pin 3):** Regulated Output Voltage. $V_{OUT}$ should be bypassed with a 4.7µF or greater, low ESR ceramic capacitor as close to the pin as possible for best performance.

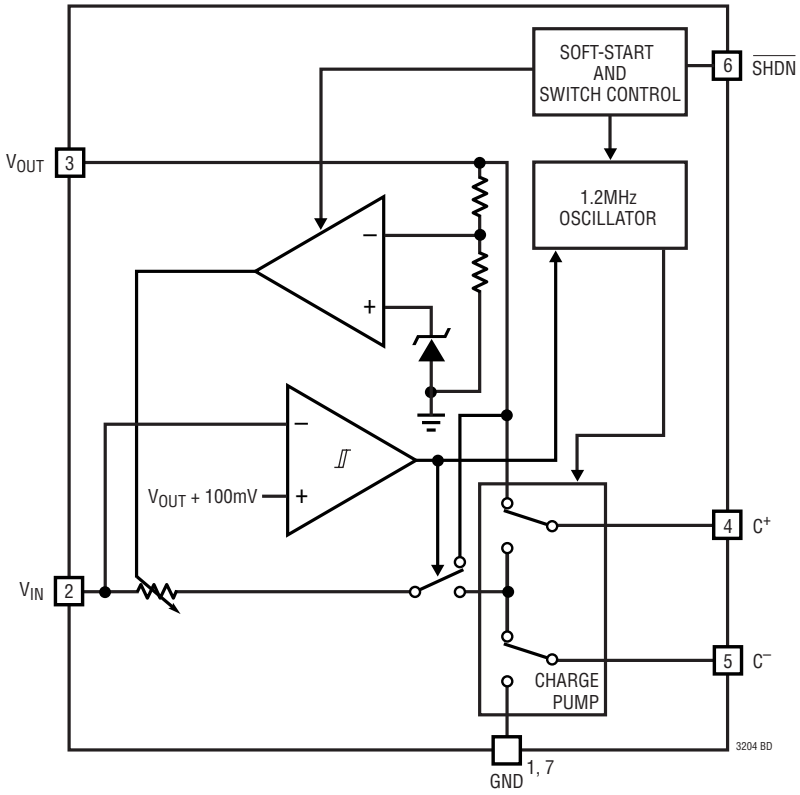
**$C^+$ (Pin 4):** Flying Capacitor Positive Terminal.

**$C^-$ (Pin 5):** Flying Capacitor Negative Terminal.

**$\overline{SHDN}$ (Pin 6):** Active Low Shutdown Input. A low on $\overline{SHDN}$ disables the LTC3240-3.3/LTC3240-2.5. This pin is a high impedance CMOS input pin which must be driven with valid logic levels. This pin must not be allowed to float.

**Exposed Pad (Pin 7):** Ground. The exposed pad must be soldered to PCB ground to provide electrical contact and optimum thermal performance.

## BLOCK DIAGRAM



## OPERATION (Refer to the Block Diagram)

The LTC3240 is a step-up/step-down charge pump DC/DC converter. For $V_{IN}$ greater than $V_{OUT}$ by about 100mV it operates as a low dropout regulator. Once $V_{IN}$ drops to within 100mV of $V_{OUT}$, the part automatically switches into charge pump mode to boost $V_{IN}$ to the regulated output voltage. Regulation is achieved by sensing the output voltage through an internal resistor divider and modulating the charge pump output current based on the error signal.

In the charge pump mode a 2-phase nonoverlapping clock activates the charge pump switches. The flying capacitor is charged from $V_{IN}$ on the first phase of the clock. On the second phase of the clock it is stacked in series with $V_{IN}$ and connected to $V_{OUT}$. This sequence of charging and discharging the flying capacitor continues at a free running frequency of 1.2MHz (typ).

### Shutdown Mode

In shutdown mode, all circuitry is turned off and the LTC3240 draws only leakage current from the $V_{IN}$ supply. Furthermore, $V_{OUT}$ is disconnected from $V_{IN}$. The $\overline{SHDN}$ pin is a CMOS input with a threshold voltage of approximately 0.8V. The LTC3240 is in shutdown when a logic low is applied to the $\overline{SHDN}$ pin. Since the $\overline{SHDN}$ pin is a high impedance CMOS input, it should never be allowed to float. To ensure that its state is defined, it must always be driven with a valid logic level.

Since the output voltage of this device can go above the input voltage, circuitry is required to control the state of the converter even in shutdown. This circuitry will draw an input current of 5μA in shutdown. However, this current is eliminated when the output voltage ($V_{OUT}$) drops to less than approximately 0.8V.

### Burst Mode Operation

The LTC3240 provides automatic Burst Mode operation while operating as a charge pump, to increase efficiency of the power converter at light loads. Burst Mode operation is initiated if the output load current falls below an internally programmed threshold. Once Burst Mode operation is initiated, the part shuts down the internal oscillator to reduce the switching losses, and goes into a low current state. This state is referred to as the sleep state in which the IC consumes only about 65μA from the input. When the output voltage droops enough to overcome the burst comparator hysteresis, the part wakes up and commences normal fixed frequency operation recharging the output capacitor. If the output load is still less than the Burst Mode threshold the part will re-enter sleep state. This Burst Mode threshold varies with $V_{IN}$, $V_{OUT}$ and the choice of output storage capacitor.

### Soft-Start

The LTC3240 has built-in soft-start circuitry to prevent excessive current flow during start-up. The soft-start is achieved by internal circuitry that slowly ramps the amount of current available to the output storage capacitor from zero to a value of 300mA over a period of approximately 2ms. The soft-start circuitry is reset in the event of a commanded shutdown or thermal shutdown.

### Short-Circuit/Thermal Protection

The LTC3240 has built-in short-circuit current limit as well as overtemperature protection. During a short-circuit condition, the part automatically limits its output current to approximately 300mA. If the junction temperature exceeds approximately 160°C the thermal shutdown circuitry shuts down current delivery to the output. Once the junction temperature drops back to approximately 150°C current delivery to the output is resumed. The LTC3240 will cycle in and out of thermal shutdown indefinitely without latch-up or damage until the short-circuit condition on $V_{OUT}$ is removed. Long term overstress (i.e. operation at junction temperatures above 125°C) should be avoided as it reduces the lifetime of the part and can result in degraded performance.

## APPLICATIONS INFORMATION

### Power Efficiency

During LDO operation, the power efficiency (η) of the LTC3240 is given by:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet I_{OUT}} = \frac{V_{OUT}}{V_{IN}}$$

At moderate to high output power, the quiescent current of the LTC3240 is negligible and the expression above is valid. For example, the measured efficiency of LTC3240-3.3, with $V_{IN}$ = 3.7V, $I_{OUT}$ = 100mA and $V_{OUT}$ regulating to 3.3V is 87% which is in close agreement with the theoretical value of 89%.

During charge pump operation, the power efficiency (η) of the LTC3240 is similar to that of a linear regulator with an effective input voltage of twice the actual input voltage. This occurs because the input current for a voltage doubling charge pump is approximately twice the output current. In an ideal regulating voltage doubler the power efficiency is given by:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet 2I_{OUT}} = \frac{V_{OUT}}{2V_{IN}}$$

At moderate to high output power, the switching losses and the quiescent current of the LTC3240 are negligible and the expression above is valid. For example, the measured efficiency of LTC3240-3.3 with $V_{IN}$ = 2.5V, $I_{OUT}$ = 100mA and $V_{OUT}$ regulating to 3.3V is 64% which is in close agreement with the theoretical value of 66%.

### Effective Open-Loop Output Resistance ($R_{OL}$)

The effective open-loop output resistance ($R_{OL}$) of a charge pump is a very important parameter which determines the strength of the charge pump. The value of this parameter depends on many factors such as the oscillator frequency ($f_{OSC}$), value of the flying capacitor ($C_{FLY}$), the nonoverlap time, the internal switch resistances ($R_S$), and the ESR of the external capacitors. A first order approximation for $R_{OL}$ is given below:

$$R_{OL} \cong 2 \sum_{S=1\,TO\,4} R_S + \frac{1}{f_{OSC} \bullet C_{FLY}}$$

For the LTC3240 in charge pump mode, the maximum available output current and voltage can be calculated from the effective open-loop output resistance, $R_{OL}$, and the effective output voltage, $2V_{IN(MIN)}$.

From Figure 1, the available current is given by:

$$I_{OUT} = \frac{2V_{IN} - V_{OUT}}{R_{OL}}$$

Typical $R_{OL}$ values as a function of temperature are shown in Figure 2.

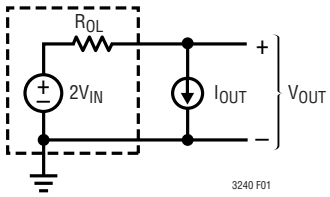



**Figure 1. Equivalent Open-Loop Circuit**

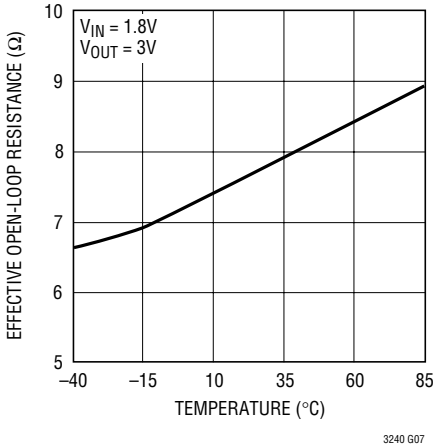



**Figure 2. Typical $R_{OL}$ vs Temperature**

### $V_{IN}$, $V_{OUT}$ Capacitor Selection

The style and value of capacitors used with the LTC3240 determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum start-up time.

To reduce noise and ripple, it is recommended that low ESR (<0.1Ω) ceramic capacitors be used for both $C_{IN}$ and $C_{OUT}$. $C_{IN}$ should be 1µF or greater while $C_{OUT}$ should be 4.7µF or greater. Tantalum and aluminum capacitors are not recommended because of their high ESR.

## APPLICATIONS INFORMATION

In charge pump mode the value of $C_{OUT}$ directly controls the amount of output ripple for a given load current. Increasing the size of $C_{OUT}$ will reduce the output ripple at the expense of higher minimum turn-on time. The peak-to-peak output ripple is approximately given by the expression:

$$V_{RIPPLE(P-P)} \cong \frac{I_{OUT}}{2f_{OSC} \bullet C_{OUT}}$$

where $f_{OSC}$ is the oscillator frequency (typically 1.2MHz) and $C_{OUT}$ is the value of the output capacitor.

Also, the value and style of the output capacitor can significantly affect the stability of the LTC3240. As shown in the Block Diagram, the LTC3240 uses a linear control loop to adjust the strength of the charge pump to match the current required at the output. The error signal of this loop is stored directly on the output storage capacitor. This output capacitor also serves to form the dominant pole of the control loop. To prevent ringing or instability on the LTC3240, it is important to maintain at least 2µF of capacitance over all conditions.

Excessive ESR on the output capacitor can degrade the loop stability of the LTC3240. The closed-loop output resistance of the LTC3240 is designed to be 0.5Ω. For a 100mA load current change, the output voltage will change by about 50mV. If the output capacitor has 0.5Ω or more of ESR, the closed-loop frequency response will cease to roll off in a simple one-pole fashion and poor load transient response or instability could result. Ceramic capacitors typically have exceptional ESR performance and combined with a tight board layout should yield very good stability and load transient performance.

Just as the value of $C_{OUT}$ controls the amount of output ripple, the value of $C_{IN}$ controls the amount of ripple present at the input pin ($V_{IN}$) in charge pump mode. The input current to the LTC3240 is relatively constant during the input charging phase and the output charging phase but drops to zero during the nonoverlap times. Since the nonoverlap time is small (~25ns), these missing notches result in a small perturbation on the input power supply line. A higher ESR capacitor such as tantalum will have higher input noise than a low ESR ceramic capacitor. Therefore, ceramic capacitors are again recommended for their exceptional ESR performance.

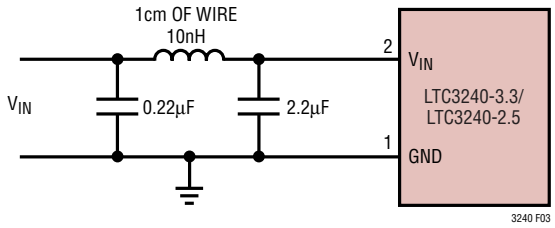



**Figure 3. 10nH Inductor Used for Additional Input Noise Reduction**

Further input noise reduction can be achieved by powering the LTC3240 through a very small series inductor as shown in Figure 3. A 10nH inductor will reject the fast current notches, thereby presenting a nearly constant current load to the input power supply. For economy, the 10nH inductor can be fabricated on the PC board with about 1cm (0.4") of PC board trace.

### Flying Capacitor Selection

*Warning: A polarized capacitor such as tantalum or aluminum should never be used for the flying capacitor since its voltage can reverse upon start-up of the LTC3240. Low ESR ceramic capacitors should always be used for the flying capacitor.*

The flying capacitor controls the strength of the charge pump. A 1µF or greater ceramic capacitor is suggested for the flying capacitor. For the LTC3240-3.3 operating at an input voltage in the range $1.8V \le V_{IN} \le 2.5V$, it is necessary to have at least 0.5µF of capacitance for the flying capacitor in order to achieve the maximum rated current of 40mA.

For very light load applications, the flying capacitor may be reduced to save space or cost. From the first order approximation of $R_{OL}$ in the "Effective Open-Loop Output Resistance" section, the theoretical minimum output resistance of a voltage doubling charge pump can be expressed by the following equation:

$$R_{OL(MIN)} = \frac{2V_{IN} - V_{OUT}}{I_{OUT}} \cong \frac{1}{f_{OSC} \bullet C_{FLY}}$$

where $f_{OSC}$ is the switching frequency (1.2MHz) and $C_{FLY}$ is the value of the flying capacitor. The charge pump will typically be weaker than the theoretical limit due

## APPLICATIONS INFORMATION

to additional switch resistance. However, for very light load applications, the above expression can be used as a guideline in determining a starting capacitor value.

### Ceramic Capacitors

Ceramic capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a capacitor made of X5R or X7R material will retain most of its capacitance from –40°C to 85°C whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range. Z5U and Y5V capacitors may also have a poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than discussing the specified capacitance value. For example, a 4.7µF 10V Y5V ceramic capacitor in a 0805 case only retains 25% of its rated capacitance over temperature with a 3.3V bias, while a 4.7µF 10V X5R ceramic capacitor will retain 80% of its rated capacitance over the same conditions. The capacitor manufacturer's data sheet should be consulted to ensure the desired capacitance at all temperatures and voltages.

Below is a list of ceramic capacitor manufacturers and how to contact them:

| | |
|---|---|
| AVX | www.avxcorp.com |
| Kemet | www.kemet.com |
| Murata | www.murata.com |
| Taiyo Yuden | www.t-yuden.com |
| Vishay | www.vishay.com |
| TDK | www.component.tdk.com |

### Layout Considerations

Due to the high switching frequency and high transient currents produced by LTC3240, careful board layout is necessary for optimum performance. A true ground plane and short connections to all the external capacitors will improve performance and ensure proper regulation under all conditions. Figure 4 shows an example layout for the LTC3240.

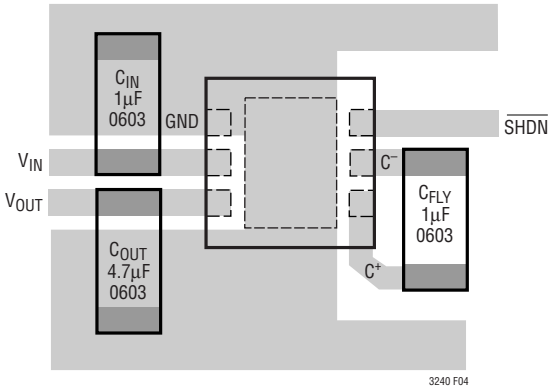



**Figure 4. Recommended Layout**

### Thermal Management

For higher input voltages and maximum output current, there can be substantial power dissipation in the LTC3240. If the junction temperature increases above approximately 160°C, the thermal shutdown circuitry will automatically deactivate the output. To reduce the maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting GND (Pin 1) and the Exposed Pad of the DFN package to a ground plane under the device on two layers of the PC board can reduce the thermal resistance of the package and PC board considerably.

### Derating Power at High Temperatures

To prevent an overtemperature condition in high power applications, Figure 5 should be used to determine the maximum combination of ambient temperature and power dissipation.

The power dissipated in the LTC3240 should always fall under the line shown for a given ambient temperature. The power dissipation of the LTC3240 in step-up mode is given by the expression:

$$P_D = (2V_{IN} – V_{OUT}) \bullet I_{OUT}$$

The power dissipation in step-down mode is given by:

$$P_D = (V_{IN} – V_{OUT}) \bullet I_{OUT}$$

## APPLICATIONS INFORMATION

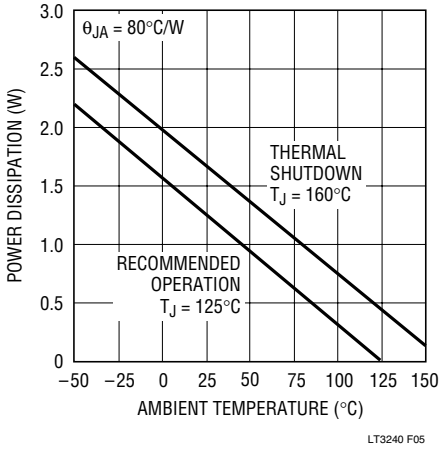


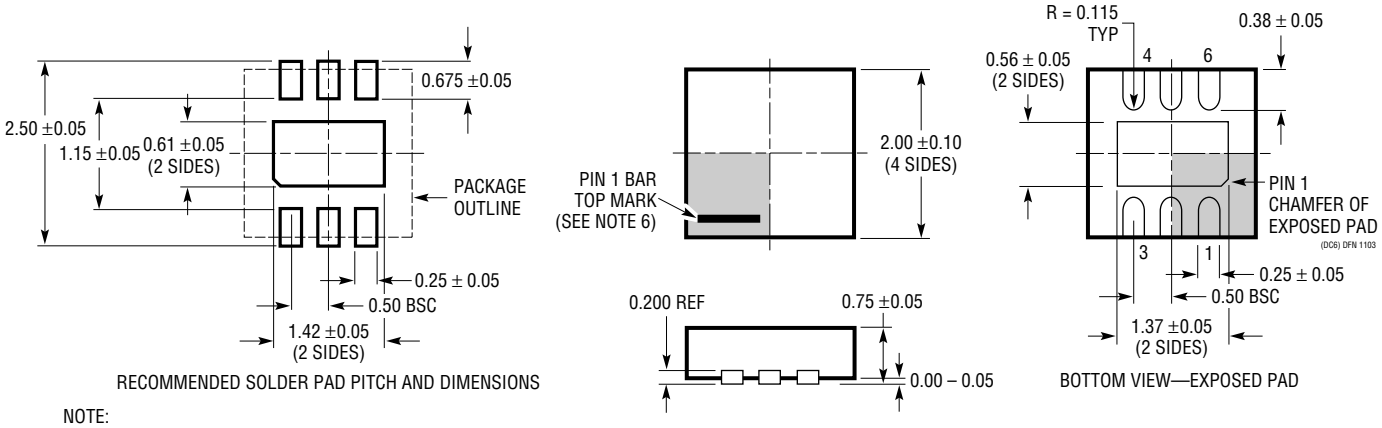

**Figure 5. Maximum Power Dissipation vs Ambient Temperature**

This derating curve assumes a maximum thermal resistance, $\theta_{JA}$, of 80°C/W for the 2 × 2 DFN package. This can be achieved from a printed circuit board layout with a solid ground plane and a good connection to the ground pins of LTC3240 and the Exposed Pad of the DFN package.

It is recommended that the LTC3240 be operated in the region corresponding to $T_J \leq 125°C$ for continuous operation as shown in Figure 5. Short term operation may be acceptable for $125°C \leq T_J \leq 160°C$ but long term operation in this region should be avoided as it may reduce the life of the part or cause degraded performance. For $T_J \geq 160°C$, the part will be in thermal shutdown.

## PACKAGE DESCRIPTION

**DC Package**
**6-Lead Plastic DFN (2mm × 2mm)**
(Reference LTC DWG # 05-08-1703)




NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WCCD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

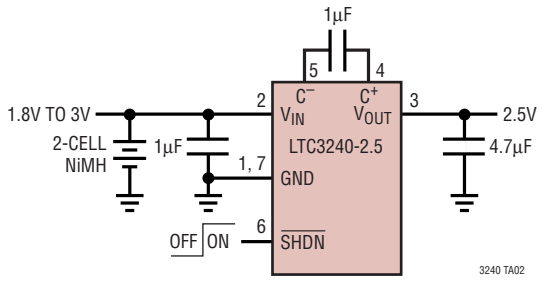


LINEAR TECHNOLOGY

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## TYPICAL APPLICATION

**2.5V Output from 2-Cell NiMH**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1751-3.3/LTC1751-5 | 100mA, 800kHz Regulated Doubler | $V_{IN}$: 2V to 5V, $V_{OUT(MAX)}$ = 3.3V/5V, $I_Q$ = 20µA, $I_{SD}$ < 2µA, MS8 Package |
| LTC1983-3/LTC1983-5 | 100mA, 900kHz Regulated Inverter | $V_{IN}$: 3.3V to 5.5V, $V_{OUT(MAX)}$ = –3V/–5V, $I_Q$ = 25µA, $I_{SD}$ < 2µA, ThinSOT™ Package |
| LTC3200-5 | 100mA, 2MHz Low Noise, Doubler/White LED Driver | $V_{IN}$: 2.7V to 4.5V, $V_{OUT(MAX)}$ = 5V, $I_Q$ = 3.5mA, $I_{SD}$ < 1µA, ThinSOT Package |
| LTC3202 | 125mA, 1.5MHz Low Noise, Fractional White LED Driver | $V_{IN}$: 2.7V to 4.5V, $V_{OUT(MAX)}$ = 5.5V, $I_Q$ = 2.5mA, $I_{SD}$ < 1µA, DFN, MS Packages |
| LTC3204-3.3<br>LTC3204B-3.3<br>LTC3204-5<br>LTC3204B-5 | Low Noise, Regulated Charge Pumps in (2mm × 2mm) DFN Package | $V_{IN}$: 1.8V to 4.5V (LTC3204B-3.3), 2.7V to 5.5V (LTC3204B-5), $I_Q$ = 48µA, "B" Version Without Burst Mode Operation, 6-Lead (2mm × 2mm) DFN Package |
| LTC3440 | 600mA ($I_{OUT}$) 2MHz Synchronous Buck-Boost DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, $I_Q$ = 25µA, $I_{SD}$ ≤ 1µA, 10-Lead MS Package |
| LTC3441 | High Current Micropower 1MHz Synchronous Buck-Boost DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, $I_Q$ = 25µA, $I_{SD}$ ≤ 1µA, DFN Package |
| LTC3443 | High Current Micropower 600kHz Synchronous Buck-Boost DC/DC Converter | 96% Efficiency, $V_{IN}$: 2.4V to 5.5V, $V_{OUT(MIN)}$ = 2.4V, $I_Q$ = 28µA, $I_{SD}$ < 1µA, DFN Package |

ThinSOT is a trademark of Linear Technology Coorporation


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