AKD4128A-A

AK4128A-A Evaluation Board Rev.0

GENERAL DESCRIPTION

The AKD4128A-A is an evaluation board for AK4128A, the digital sample rate converter. The AKD4128A-A has the digital audio interface and can achieve the interface with digital audio system via optical or coaxial connector.

■ **Ordering guide**

AKD4128A-A --- AK4128A Evaluation Board

FUNCTION

- **DIR/DIT with optical or coaxial input/output**
- **10pin Header for AKM AD/DA evaluation board**

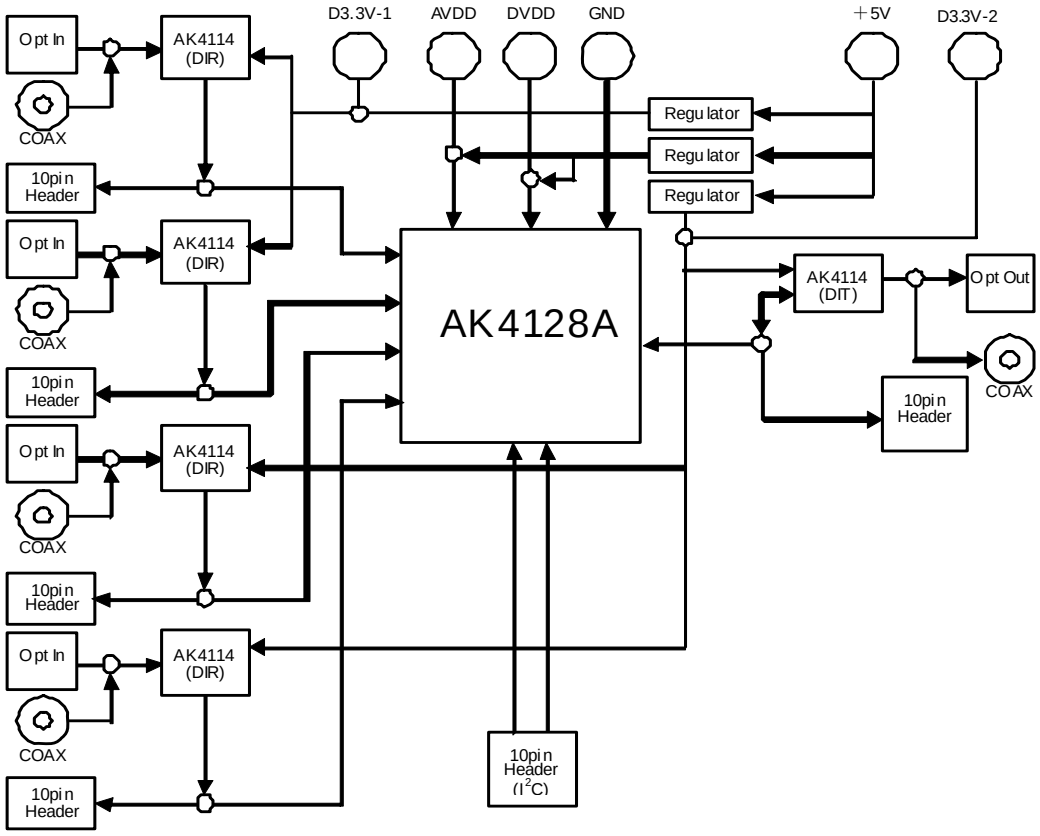


Figure 1. AKD4128A-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

1) Set up the power supply lines.

Name of jack	Color of jack	Typ Voltage	Used for	Open / Connect	Default Setting
+5V	Orange	+5V	Regulator T1,T2,T3: AVDD and DVDD of AK4128A, AK4114, Digital Logic	Should be always connected When default setting.	+5V
AVDD	Red	+3.3V	AVDD of AK4128A	Should be always connected when AVDD of AK4128A is not supplied from regulator T1. In this case “JP1” is set to “AVDD” side.	Open
DVDD	Red	+3.3V	DVDD of AK4128A	Should be always connected when DVDD of AK4128A is not supplied from regulator T1. In this case “JP2” is set to “DVDD” side.	Open
D3.3V-1	Red	+3.3V	AK4114, Digital Logic	Should be always connected when AK4114 and Digital Logic is not supplied from regulator T2. In this case “JP3” is set to “D3.3V-1” side.	Open
D3.3V-2	Red	+3.3V	AK4114, Digital Logic	Should be always connected when AK4114 and Digital Logic is not supplied from regulator T3. In this case “JP4” is set to “D3.3V-2” side.	Open
GND	Black	0V	Ground	Should be always connected	GND

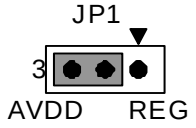
Table 1. Set up the power supply lines

Each supply line should be distributed from the power supply unit.

2) Set up the jumper pin of power supply unit.

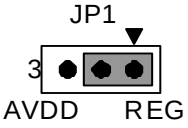
(1).Setup the AVDD of AK4128A.

a).When using AVDD jack.



AVDD-SEL

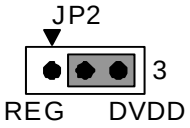
b).When using Regulator.



AVDD-SEL

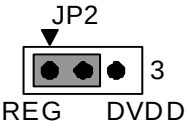
(2).Setup the DVDD of AK4128A.

a).When using DVDD jack.



DVDD-SEL

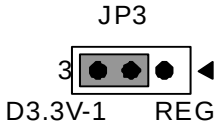
b).When using Regulator.



DVDD-SEL

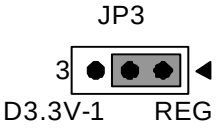
(3).Setup the D3.3V-1(AK4114 and Digital Logic).

a).When using D3.3V-1 jack.



D3.3V-1 SEL

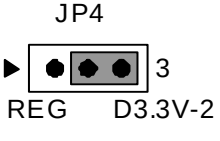
b).When using Regulator.



D3.3V-1 SEL

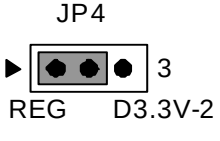
(4). Setup the D3.3V-2(AK4114 and Digital Logic).

a).When using D3.3V-2 jack.



D3.3V-2 SEL

b).When using Regulator.



D3.3V-2 SEL

3) Set up the evaluation mode, jumper pins. (See the followings.)
(1). Setting for Input port
(1)-1. When using DIR function of AK4114 (U2,U3,U4 and U5)
(1)-2. When using all clocks are fed through the 10pin port
(2). Setting for Output port
(2)-1. When using DIT function of AK4114 (U6)
(2)-2. When using all clocks are fed through the 10pin port(PORT5).
(3). Other jumper pins setup.

4) Power on.
The AK4128A should be reset once bringing SW2 (PDN) “L” upon power-up.

■ **Set up the evaluation mode, jumper pins.**

(1). Setting for Input port

(1)-1. When using DIR function of AK4114 (U2,U3,U4 and U5)

When using J1-4(COAX) and PORT6-9(OPT), nothing should be connected to PORT1-4.

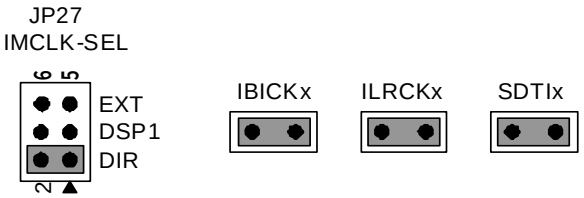
(1)-1-1. Setup the RX.

(a) Select to Optical jack (Default) (b) Select to BNC jack

* "x" contains a number (1 - 4).

(1)-1-2. Setup the IBICK1-4, ILRCK1-4 and SDTI1-4.

When using J1-4(COAX) and PORT6-9(OPT), nothing should be connected to PORT1-4.

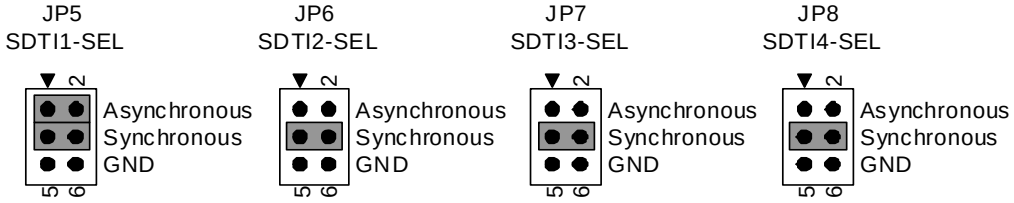


* "x" contains a number (1 - 4).

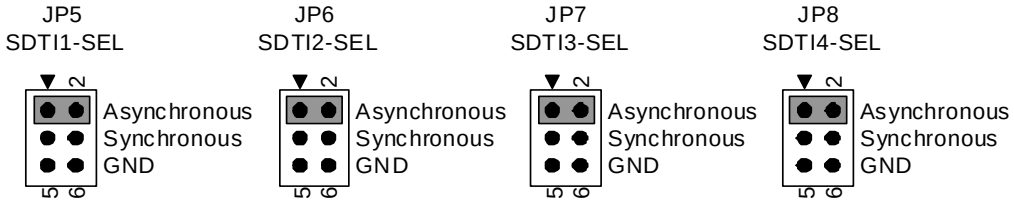
(1)-1-3. Setup the SDTI1, SDTI2, SDTI3 and SDTI4.

Select to input signal for SDTI1, SDTI2, SDTI3 and SDTI4 of AK4128A(U1).

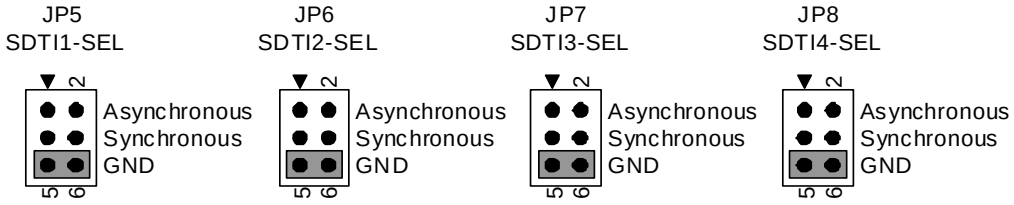
(a). When using "Synchronous Mode" (INAS pin = "L"). (Default)



(b).When using "Asynchronous Mode" (INAS pin = "H").



(c). Connect to GND.



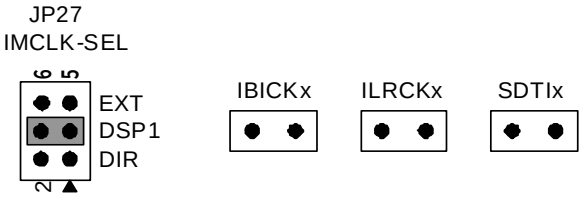
(1)-2. When using all clocks are fed through the 10pin port

(1)-2-1. Setup the RX.

When using PORT1-4, nothing should be connected to J1-4 (COAX) and PORT6-9 (OPT).

(1)-2-2. Setup the IBICK1-4, ILRCK1-4 and SDTI1-4.

When using PORT1-4, nothing should be connected to J1-4 (COAX) and PORT6-9 (OPT).

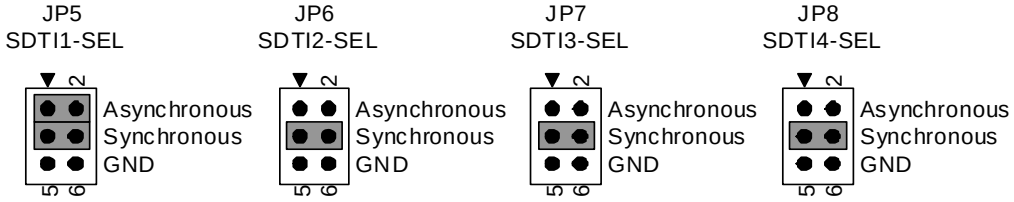


* "x" contains a number (1 - 4).

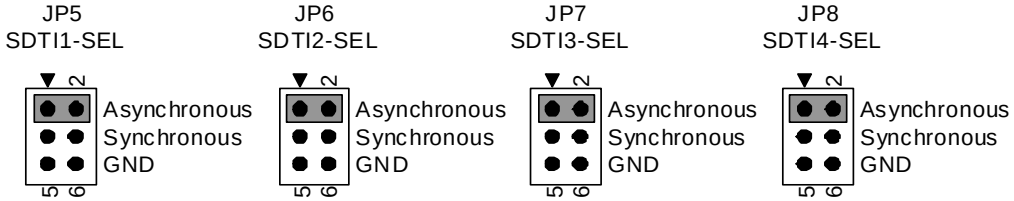
(1)-2-3. Setup the SDTI1, SDTI2, SDTI3 and SDTI4.

Select to input signal for SDTI1, SDTI2, SDTI3 and SDTI4 of AK4128A(U1).

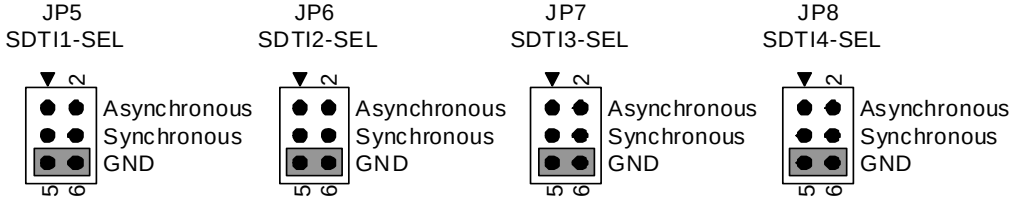
(a). When using "Synchronous Mode" (INAS pin = "L"). (Default)



(b).When using "Asynchronous Mode" (INAS pin = "H").



(c). Connect to GND.

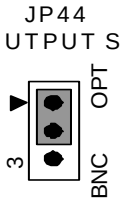


(2). Setting for Output port

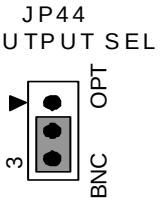
(2)-1. When using DIT function of AK4114 (U6)

(2)-1-1. Setup the TX.

(a) Select to Optical jack (Default)



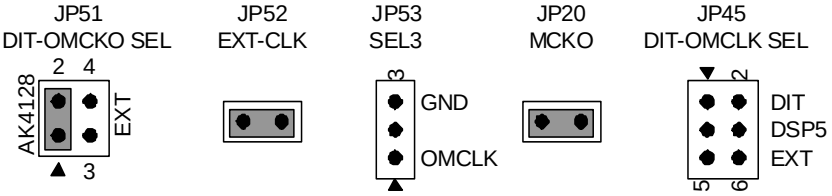
(b) Select to BNC jack



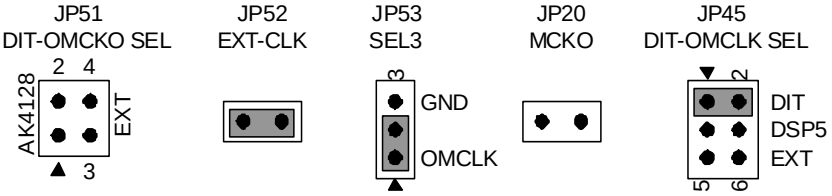
(2)-1-2. Setup the TXI.

Select to input signal for XTI/OMCLK pin of AK4128A(U1) and XTI pin of AK4114(U6).

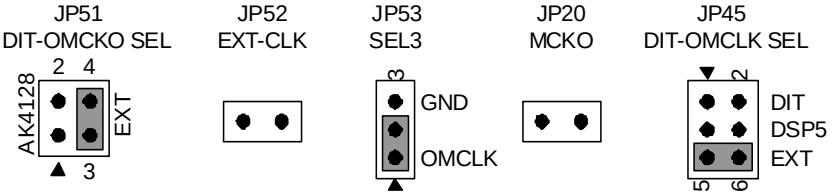
(a) When using X'Tal(X1). In this case, X'Tal(X2) is "open".



(b) When using X'Tal(X2). In this case, X'Tal(X1) is "open".

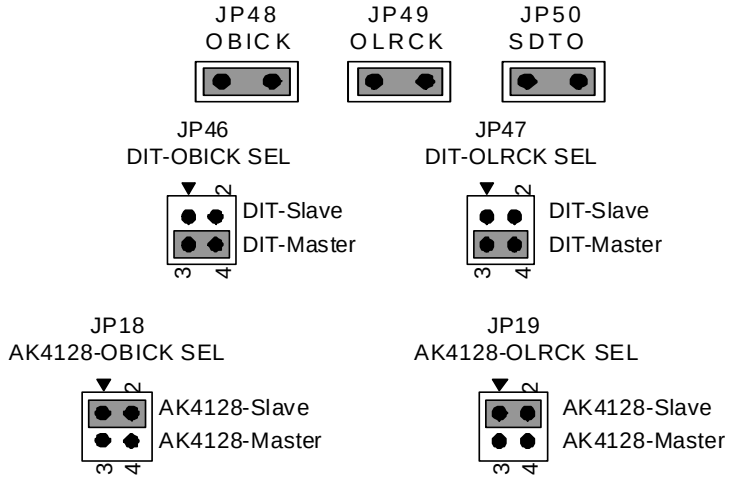


(c) When using J8(EXT-CLK). In this case, X'Tal(X1 and X2) is "open".

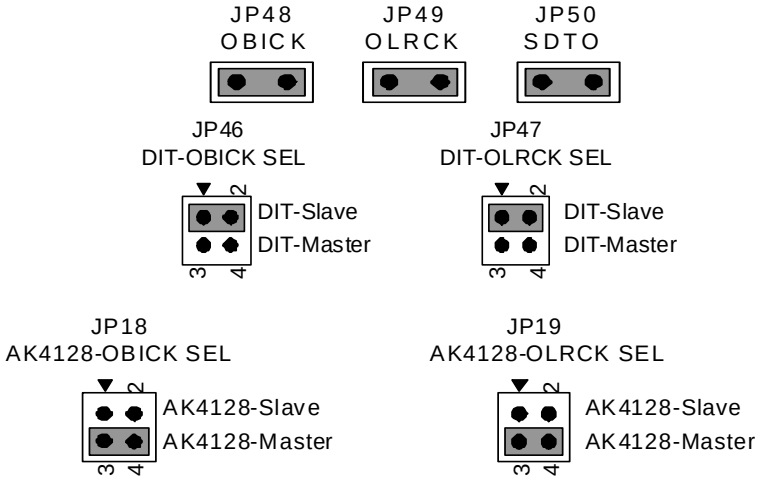


(2)-1-3. Setup the OBICK, OLRCK and SDTO.

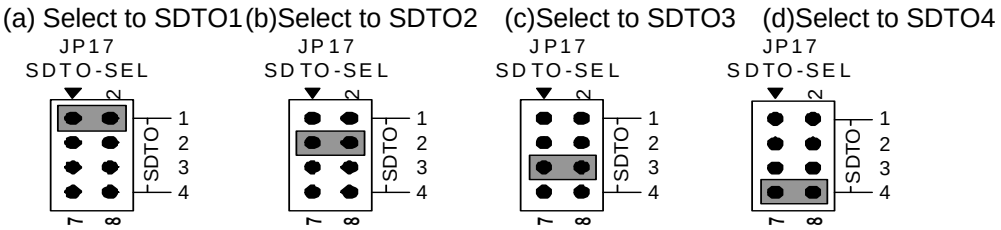
(2)-1-3-1.When using OBICK, OLRCK of AK4114(U6), and SDTO of AK4128A(U1).



(2)-1-3-2.When using OBICK, OLRCK and SDTO of AK4128A(U1).



(2)-1-4. Selection of SDTO1, SDTO2, SDTO3 and SDTO4.



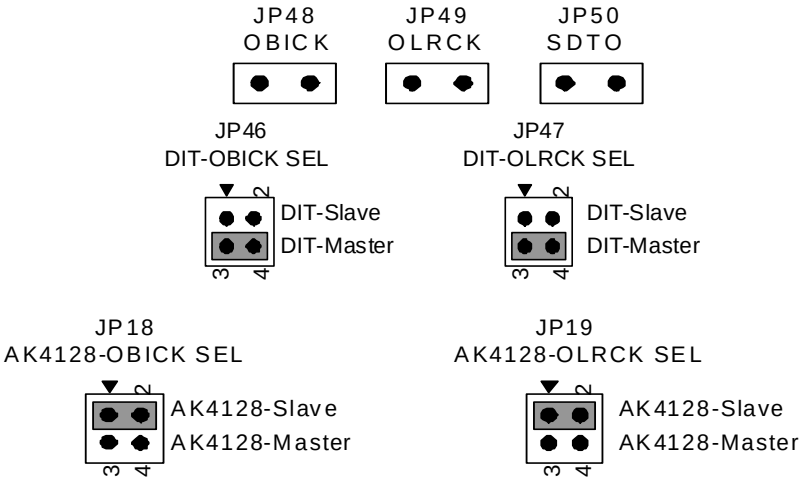
(2)-2. When using all clocks are fed through the 10pin port(PORT5).

(2)-2-1.Setup TX.

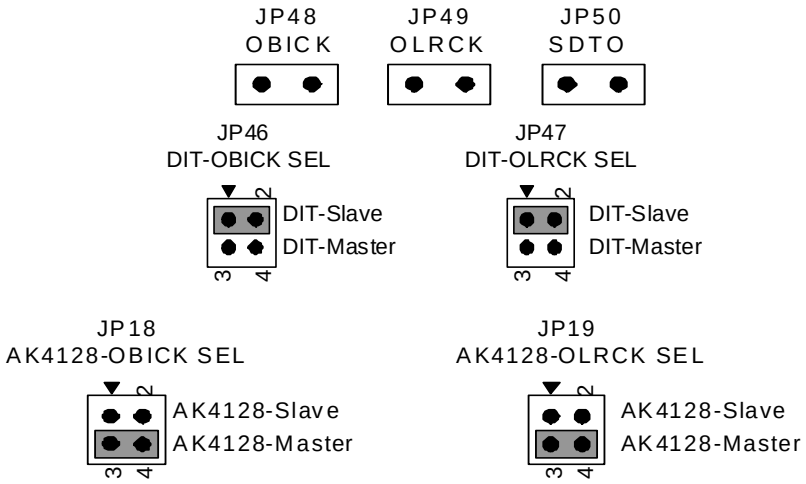
As Optical connector:PORT10(OPT) and BNC connector:J5(COAX) are not used, please don't connect anything.

(2)-2-2. Setup the OBICK, OLRCK and SDTO.

(2)-2-2-1. When using OBICK and OLRCK of 10pin port, and SDTO of AK4128A(U1).



(2)-2-2-2. When using OBICK, OLRCK and SDTO of AK4128A(U1).



(2)-2-2-3. Selection of SDTO1, SDTO2, SDTO3 and SDTO4.

(3). Other jumper pins setup.

[JP9 (SEL1)]：The selection of input signal to IMCLK pin.
IMCLK ：Connect to MCLK signal of DIR or 10 pin PORT. (Default)
GND ：Connect to GND

[JP10 (ILRCK2-SEL)]：The selection of input signal to ILRCK2 pin.
ILRCK2：Connect to LRCK2 signal of DIR or 10 pin PORT. (Default)
GND ：Connect to GND

[JP11 (ILRCK3-SEL)]：The selection of input signal to ILRCK3 pin.
ILRCK3：Connect to LRCK3 signal of DIR or 10 pin PORT. (Default)
GND ：Connect to GND

[JP12 (IBICK3-SEL)]：The selection of input signal to IBICK3 pin.
IBICK3：Connect to BICK3 signal of DIR or 10 pin PORT. (Default)
GND ：Connect to GND

[JP13 (ILRCK4-SEL)]：The selection of input signal to ILRCK4 pin.
ILRCK4：Connect to LRCK4 signal of DIR or 10 pin PORT. (Default)
GND ：Connect to GND

[JP14 (IBICK4-SEL)]：The selection of input signal to IBICK4 pin.
IBICK4 ：Connect to BICK4 signal of DIR or 10 pin PORT. (Default)
GND ：Connect to GND

[JP15 (SEL2)]：The selection of input signal to INAS pin.
INAS ：Connect to INAS signal (Default)
GND ：Connect to GND

[JP16 (UNLOCK)]：The selection of connection to UNLOCK pin and LE1.
OPEN ：Unconnection.
SHORT：Connection. (Default)

[JP21 (TST0)]：The selection of connection to TST0 pin and SW17(TST0).
OPEN ：Unconnection.
SHORT：Connection. (Default)

[JP22 (TST1)]：The selection of connection to TST1 pin and SW3(TST1).
OPEN ：Unconnection.
SHORT：Connection. (Default)

[JP23 (TST2)]：The selection of connection to TST2 pin and SW3(TST2).
OPEN ：Unconnection.
SHORT：Connection. (Default)

[JP24 (SEL4)]：The selection of input signal to SDA pin.
SDA ：Connect to SDA signal of 10 pin PORT(PORT11). (Default)
GND ：Connect to GND

[JP25 (TST3)]：The selection of connection to TST3 pin and SW17(TST3).
OPEN ：Unconnection.
SHORT：Connection. (Default)

[JP31 (EXT-CLK)]：The selection of J7(EXT-CLK) connector.
OPEN ：J7(EXT-CLK) connector is use.
SHORT：J7(EXT-CLK) connector is not use. (Default)
* If “JP31(EXT-CLK)” is set to “OPEN”, JP27 is set to “EXT”.

■ Setup the DIP SW.

(1). Setup the AK4128A(U1).

(1)-1. SW3 setting

Upper-side is “H” and lower-side is “L”.

SW3 No.	Name	ON (“H”)	OFF (“L”)	Default
1	IDIF2	Audio Interface Format Setting for Input PORT Refer to Table 3		L
2	IDIF1			H
3	IDIF0			L
4	SPB	Serial Control Mode	Parallel Control Mode	L
5	TST1	TEST Pin Fixed to ”L”		L
6	TST2			L
7	SMSEMI	Semi-auto Mode	Manual Mode	L
8	CAD0	Chip Address 0 bit=”1”	Chip Address 0 bit=”0”	L

Table 2. SW3 Setting

Mode	IDIF2 pin	IDIF1 pin	IDIF0 pin	SDTI1-4 Format	IBICK Freq	
0	L	L	L	16bit, LSB justified	≥ 32FSI	
1	L	L	H	20bit, LSB justified	≥ 40FSI	
2	L	H	L	24bit, MSB justified	≥ 48FSI	(Default)
3	L	H	H	24/16bit, I^2S Compatible	≥ 48FSI or 32FSI	
4	H	L	L	24bit, LSB justified	≥ 48FSI	
5	H	L	H	Reserved		
6	H	H	H			

Table 3. AK4128A Audio Interface Format Setting for Input PORT

(1)-2. SW3 setting

Upper-side is “H” and lower-side is “L”.

SW4 No.	Name	ON (“H”)	OFF (“L”)	Default
1	OBIT1	Output PORT Audio Interface Format Setting 2 Refer to Table 6		H
2	OBIT0			H
3	TDM	TDM mode	Stereo mode	L
4	CM2	Clock Select or Mode Select pin for Output PORT Refer to Table 7		H
5	CM1			L
6	CM0			L
7	ODIF1	Output PORT Audio Interface Format Setting 1 Refer to Table 5		H
8	ODIF0			L

Table4. SW4 Setting

Mode	TDM pin	ODIF1 pin	ODIF0 pin	SDTO1-4 Format	
0	L	L	L	LSB justified	
1		L	H	(Reserved)	
2		H	L	MSB justified	(Default)
3		H	H	I^2S Compatible	
4	H	L	L	(Reserved)	
5		L	H		
6		H	L	TDM256 mode 24bit MSB justified	
7		H	H	TDM256 mode 24bit I^2S Compatible	

Table 5. Output PORT Audio Interface Format Setting 1

Mode	TDM pin	Master / Slave setting	OBIT1 pin	OBIT0 pin	SDTO 1-4	OLRCK	OBICK	OBICK Frequency		
								MSB justified, I^2S	LSB justified	
0	L	Slave (CM2-0 = “HLL” or “HHL”)	L	L	16bit	Input	Input	≥ 32FSO	64FSO	
1			L	H	18bit			≥ 36FSO		
2			H	L	20bit			≥ 40FSO		
3			H	H	24bit			≥ 48FSO		(Default)
4		Master (Not CM2-0 = “HLL”/“HHL”)	L	L	16bit	Output	Output	64FSO		
5			L	H	18bit					
6			H	L	20bit					
7			H	H	24bit					
8	H	Slave (CM2-0 = “HLL” or “HHL”)	*	*	TDM256 mode 24bit	Input	Input	256FSO		
9										
10										
11										
12		Master (Not CM2-0 = “HLL”/“HHL”)	*	*	TDM256 mode 24bit	Output	Output	256FSO		
13										
14										
15										

Table 6. Output PORT Audio Interface Format Setting 2

Mode	CM2 pin	CM1 pin	CM0 pin	Master / Slave	OMCLK/XTI Input	MCKO Output	FSO	
0	L	L	L	Master	256FSO	256FSO	8k ~ 108kHz	
1	L	L	H	Master	384FSO	384FSO	8k ~ 96kHz	
2	L	H	L	Master	512FSO	512FSO	8k ~ 54kHz	
3	L	H	H	Master	768FSO	768FSO	8k ~ 48kHz	
4	H	L	L	Slave	In External Clock Mode, 1.024MHz~36.864MHz. In X'tal Mode, X'tal oscillation frequency.	OMCLK Input Clock	8k ~ 216kHz	(Default)
5	H	L	H	Master	128FSO	128FSO	8k ~ 216kHz	
6	H	H	L	Slave (Bypass)	Not used. (note)	IMCLK Input Clock	8k ~ 216kHz	
7	H	H	H					

Table 7. Output PORT Master/Slave/Bypass Mode Control Setting

(1)-3. SW5 setting

Upper-side is "H" and lower-side is "L".

SW4 No.	Name	ON ("H")	OFF ("L")	Default
1	INAS	Asynchronous mode	Synchronous mode	L
2	DITHER	Dither ON	Dither OFF	L
3	SMT1	Soft Mute Timer Setting Refer to Table 9		L
4	SMT0			L
5	DEM0	De-emphasis Filter Setting Refer to Table 10		H
6	DEM1			L
7	PM2	Channel Mode Setting Refer to Table 11		H
8	PM1			L

Table 8. SW5 Setting

SMT1pin	SMT0 pin	Period	FSO=48kHz	FSO=96kHz	FSO=192kHz	
L	L	1024/fso	21.3ms	10.7ms	5.3ms	(Default)
L	H	2048/fso	42.7ms	21.3ms	10.7ms	
H	L	4096/fso	85.3ms	42.7ms	21.3ms	
H	H	8192/fso	170.7ms	85.3ms	42.7ms	

Table 9. Soft Mute Cycle Setting

DEM1pin	DEM0 pin	Mode(SDTI1-4)	
L	L	44.1kHz	
L	H	OFF	(Default)
H	L	48kHz	
H	H	32kHz	

Table 10. De-emphasis Filter Setting

PM2 pin	PM1 pin	PDN pin	Mode	X'tal Oscillator	XTI pin	XTO pin	MCKO pin	
L	L	L	6-channel mode	Power-down	Pull down to VSS2-5	Hi-z	Hi-z	
L	L	H			Input			
L	H	L	4-channel mode	Power-down	Pull down to VSS2-5	Hi-z		
L	H	H			Input			
H	L	L	8-channel mode	Power-down	Pull down to VSS2-5	Hi-z	L	
H	L	H		Normal operation	Input	Output	Normal operation	(Default)
H	H	L	Not available	-	-	-	-	
H	H	H		-	-	-	-	

Table 11. Channel Mode Setting

(1)-4. SW17 setting

Upper-side is "H" and lower-side is "L".

SW17 No.	Name	ON ("H")	OFF ("L")	Default
1	TST3	TEST Pin		L
2	TST0	Fixed to "L"		L

Table 12. SW17 Setting

(2). Setup the AK4114 (U2,U3,U4,U5,U6)

(2)-1. SW6(U2), SW7(U3), SW8(U4), SW9(U5) setting.

Upper-side is "H" and lower-side is "L".

SW6 No.	Name	ON ("H")	OFF ("L")	Default
1	DIR1-OCKS1	Master Clock Frequency Setting		H
2	DIR1-OCKS0	Refer to Table 17		L
3	DIR1-DIF0	24bit, I^2S Compatible	24bit, Left justified	L

Table 13. SW6 Setting

SW7 No.	Name	ON ("H")	OFF ("L")	Default
1	DIR2-OCKS1	Master Clock Frequency Setting		H
2	DIR2-OCKS0	Refer to Table 17		L
3	DIR2-DIF0	24bit, I^2S Compatible	24bit, Left justified	L

Table 14. SW7 Setting

SW8 No.	Name	ON ("H")	OFF ("L")	Default
1	DIR3-OCKS1	Master Clock Frequency Setting		H
2	DIR3-OCKS0	Refer to Table 17		L
3	DIR3-DIF0	24bit, I^2S Compatible	24bit, Left justified	L

Table 15. SW8 Setting

SW9 No.	Name	ON ("H")	OFF ("L")	Default
1	DIR4-OCKS1	Master Clock Frequency Setting		H
2	DIR4-OCKS0	Refer to Table 17		L
3	DIR4-DIF0	24bit, I^2S Compatible	24bit, Left justified	L

Table 16. SW9 Setting

Mode	OCKS1 pin	OCKS0 pin	MCKO1	fs (max)	
0	L	L	256fs	96 kHz	
1	L	H	256fs	96 kHz	
2	H	L	512fs	48 kHz	(Default)
3	H	H	128fs	192 kHz	

Table 17. Master Clock Frequency Setting

(2)-2. SW16(U6) setting.

Upper-side is "H" and lower-side is "L".

SW16 No.	Name	ON ("H")	OFF ("L")	Default
1	DIT-OCKS1	Master Clock Frequency Setting Refer to Table 19		H
2	DIT-OCKS0			L
3	DIT-DIF2	Audio Interface Format Setting Refer to Table 20		H
4	DIT-DIF1			L
5	DIT-DIF0			L

Table 18. Master Clock Frequency Setting

Mode	OCKS1 pin	OCKS0 pin	MCKO1	fs (max)	
0	L	L	256fs	96 kHz	
1	L	H	256fs	96 kHz	
2	H	L	512fs	48 kHz	(Default)
3	H	H	128fs	192 kHz	

Table 19. Master Clock Frequency Setting

Mode	DIF2 pin	DIF1 pin	DIF0 pin	DAUX Format	LRCK		BICK		
						I/O		I/O	
0	L	L	L	24bit, Left justified	H/L	O	64fs	O	
1	L	L	H	24bit, Left justified	H/L	O	64fs	O	
2	L	H	L	24bit, Left justified	H/L	O	64fs	O	
3	L	H	H	24bit, Left justified	H/L	O	64fs	O	
4	H	L	L	24bit, Left justified	H/L	O	64fs	O	(Default)
5	H	L	H	24bit, I^2S Compatible	L/H	O	64fs	O	
6	H	H	L	24bit, Left justified	H/L	I	64-128fs	I	
7	H	H	H	24bit, I^2S Compatible	L/H	I	64-128fs	I	

Table 20. Audio Interface format Setting

■ The function of the toggle SW

Upper-side is “H” and lower-side is “L”.

[SW1] (AK4128-SMUTE) : Soft mute of AK4128A.
When using Soft mute function, SW1 is “H”.

[SW2] (AK4128-PDN) : Resets the AK4128A. Keep “H” during normal operation.
The AK4128A should be resets once bringing “L” upon power-up.

[SW10] (DIR1-PDN) : Resets the AK4114 (U2). Keep “H” during normal operation.
The AK4114 (U2) should be resets once bringing “L” upon power-up.
Keep “L” when AK4114 (U2) is not used.

[SW11] (DIR2-PDN) : Resets the AK4114 (U3). Keep “H” during normal operation.
The AK4114 (U3) should be resets once bringing “L” upon power-up.
Keep “L” when AK4114 (U3) is not used.

[SW12] (DIR3-PDN) : Resets the AK4114 (U4). Keep “H” during normal operation.
The AK4114 (U4) should be resets once bringing “L” upon power-up.
Keep “L” when AK4114 (U4) is not used.

[SW13] (DIR4-PDN) : Resets the AK4114 (U5). Keep “H” during normal operation.
The AK4114 (U5) should be resets once bringing “L” upon power-up.
Keep “L” when AK4114 (U5) is not used.

[SW14] (DIT-PDN) : Resets the AK4114 (U6). Keep “H” during normal operation.
The AK4114 (U6) should be resets once bringing “L” upon power-up.
Keep “L” when AK4114 (U6) is not used.

■ Indication for LED

[LE1] (UNLOCK) : Monitor UNLOCK pin of the AK4128A (U1).
LED turns on when PDN pin = “L”.

■ Serial Control

The AK4128A can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT1 (CTRL) with PC by 10 wire flat cable packed with the AKD4128A-A.

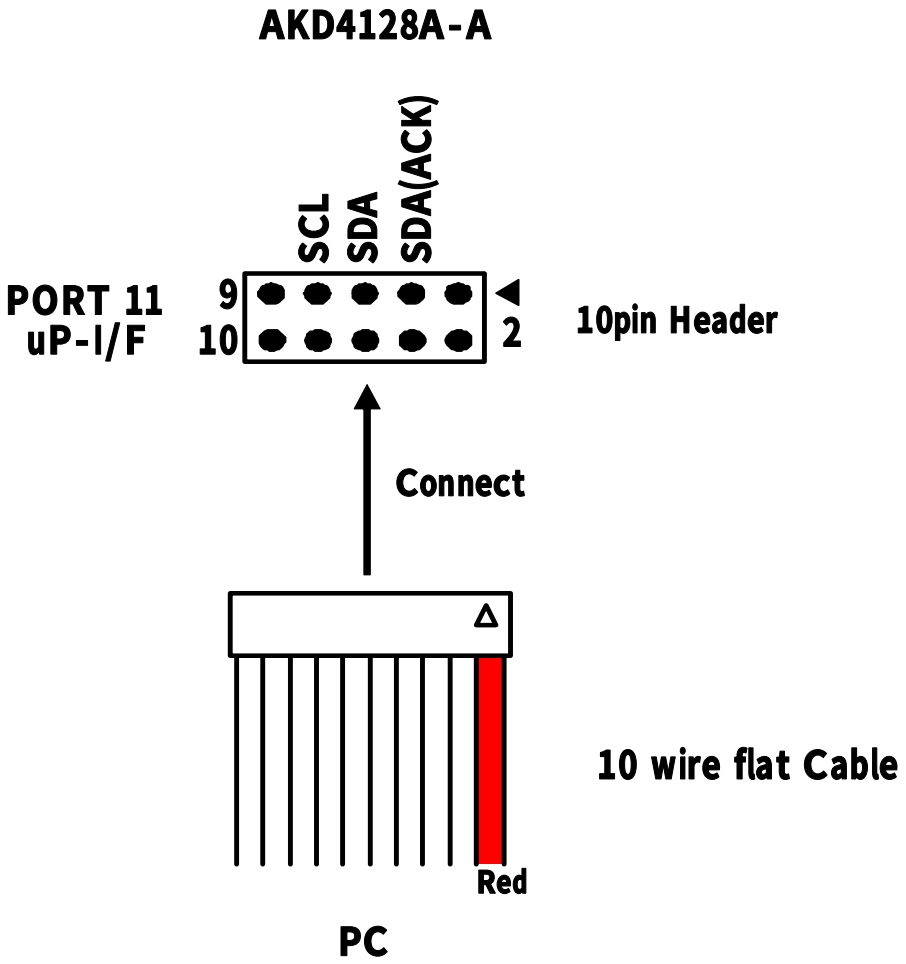


Figure 1. Connection of 10 wire flat cable

Control Soft Manual

■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an IBM PC/AT compatible PC by a 10wire flat cable. Be aware of the direction of the 10pin header. When running this control soft on the Windows 2000/XP, the driver which is included in the CD must be installed. Refer to the "Driver Control Install Manual for AKM Device Control Software" for installing the driver. When running this control soft on the windows 95/98/ME, driver installing is not necessary. This control soft does not support the Windows NT.
3. Proceed evaluation by following the process below.

■Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” for details of each dialog box setting.

1. [Port Reset] : For when connecting to USB I/F board (AKDUSBIF-A)
   Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-A).
2. [Write Default] : Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.
3. [All Write] : Executing write commands for all registers displayed.
4. [All Read] : Executing read commands for all registers displayed.
5. [Save] : Saving current register settings to a file.
6. [Load] : Executing data write from a saved file.
7. [All Req Write] : “All Req Write” dialog box is popped up.
8. [Data R/W] : “Data R/W” dialog box is popped up.
9. [Sequence] : “Sequence” dialog box is popped up.
10. [Sequence(File)] : “Sequence(File)” dialog box is popped up.
11. [Read] : Reading current register settings and display on to the Register area (on the right of the main window).
    This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.

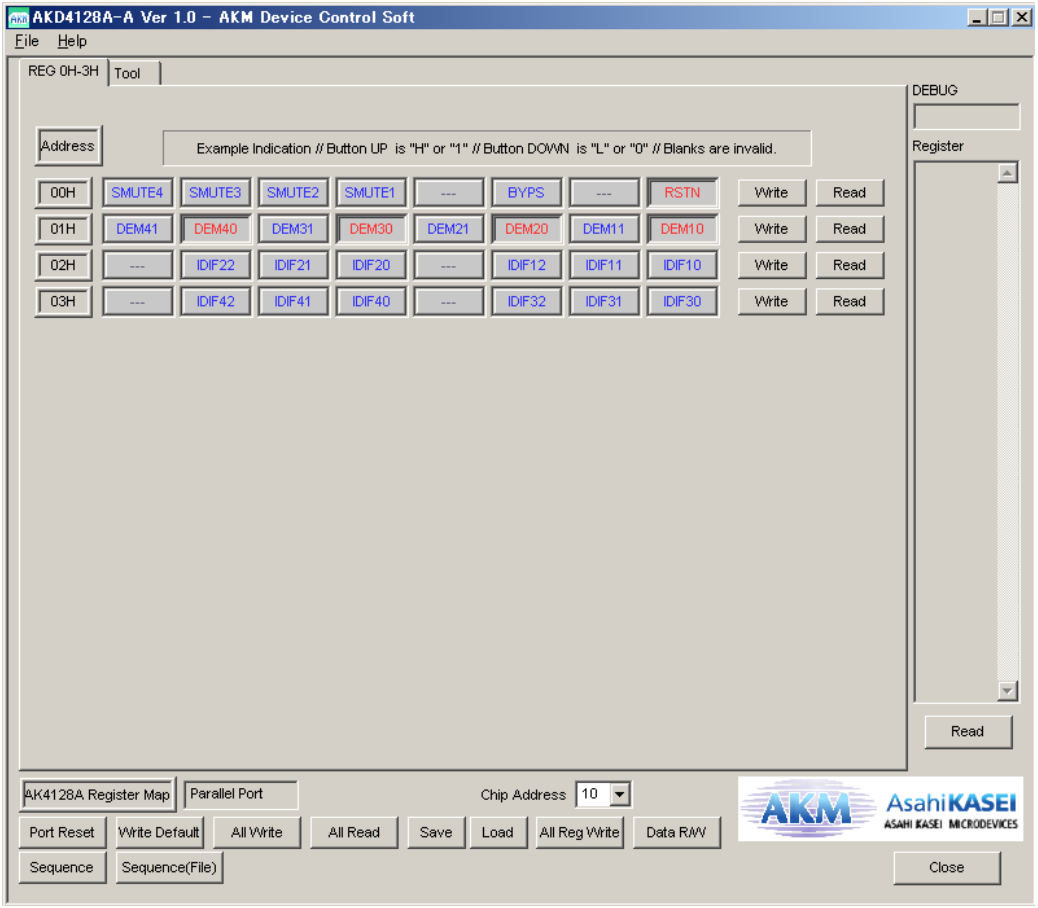


Figure 3. Window of [FUNCTION]

■Dialog Boxes

[All Req Write]

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.

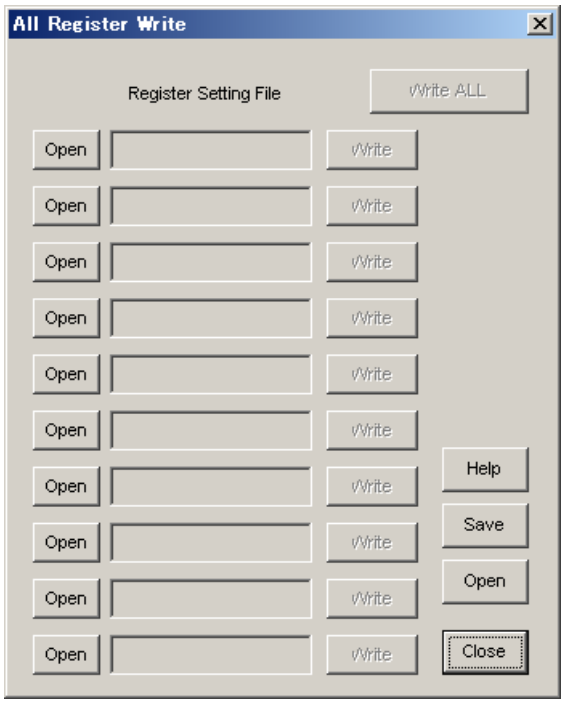


Figure 4. Window of [All Reg Write]

[Open (left)]	: Selecting a register setting file (*.akr).
[Write]	: Executing register writing.
[Write All]	: Executing all register writings. Writings are executed in descending order.
[Help]	: Help window is popped up.
[Save]	: Saving the register setting file assignment. The file name is "*.mar".
[Open (right)]	: Opening a saved register setting file assignment "*. mar".
[Close]	: Closing the dialog box and finish the process.

*Operating Suggestions

(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mar" should be stored in the same folder.

(2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

[Data R/W]

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.

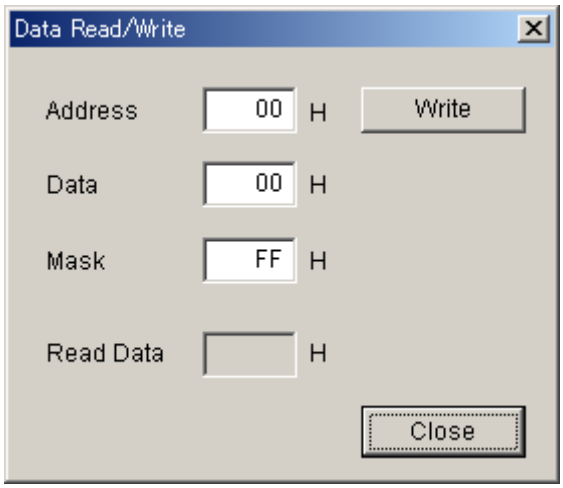


Figure 5. Window of [Data R/W]

Address Box : Input data address in hexadecimal numbers for data writing.
Data Box : Input data in hexadecimal numbers.
Mask Box : Input mask data in hexadecimal numbers.
This is “AND” processed input data.

[Write] : Writing to the address specified by “Address” box.
[Close] : Closing the dialog box and finish the process.
Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

[Sequence]

Click [Sequence] button to open register sequence setting dialog box.
Register sequence can be set in this dialog box.

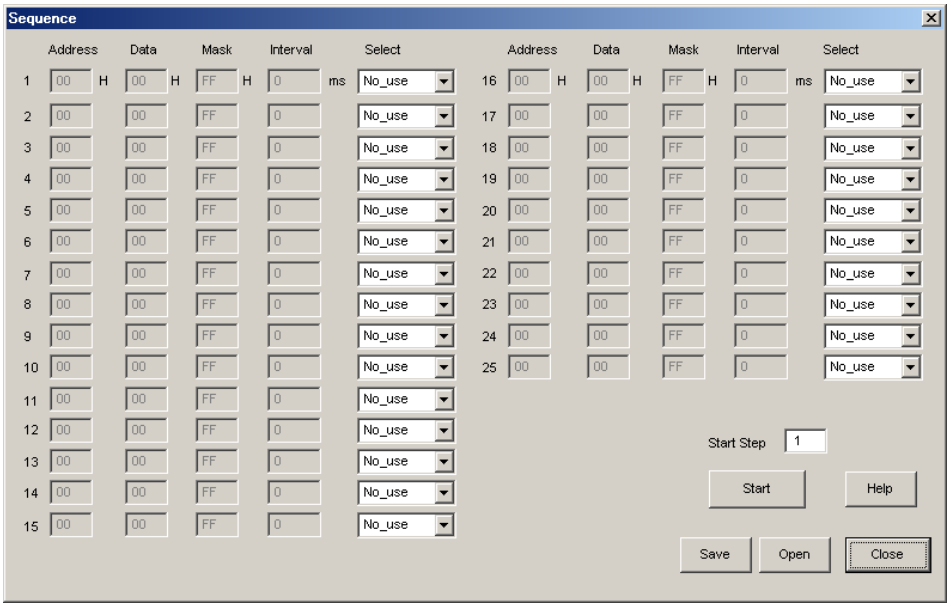


Figure 6. Window of [Sequence]

Sequence Setting

Set register sequence by following process bellow.

(1)Select a command

Use [Select] pull-down box to choose commands.
Corresponding boxes will be valid.

< Select Pull-down menu >

- · No_use : Not using this address
- · Register : Register writing
- · Reg(Mask) : Register writing (Masked)
- · Interval : Taking an interval
- · Stop : Pausing the sequence
- · End : Finishing the sequence

(2)Input sequence

[Address] : Data address
[Data] : Writing data
[Mask] : Mask
[Data] box data is ANDed with [Mask] box data. This is the actual writing data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.
[Interval] : Interval time

Valid boxes for each process command are shown bellow.

· No_use : None
· Register : [Address], [Data], [Interval]
· Reg(Mask) : [Address], [Data], [Mask], [Interval]
· Interval : [Interval]
· Stop : None
· End : None

Control Buttons

The function of Control Button is shown bellow.

[Start] : Executing the sequence
[Help] : Opening a help window
[Save] : Saving sequence settings as a file. The file name is "*.aks".
[Open] : Opening a sequence setting file "*.aks".
[Close] : Closing the dialog box and finish the process.

Stop of the sequence

When "Stop" is selected in the sequence, processing is paused and it starts again when [Start] button is clicked. Restarting step number is shown in the "Start Step" box. When finishing the process until the end of sequence, "Start Step" will return to "1".

The sequence can be started from any step by writing the step number to the "Start Step" box.
Write "1" to the "Start Step" box and click [Start] button, when restarting the process from the beginning.

[Sequence(File)]

Click [Sequence(File)] button to open sequence setting file dialog box.
Those files saved in the "Sequence setting dialog" can be applied in this dialog.

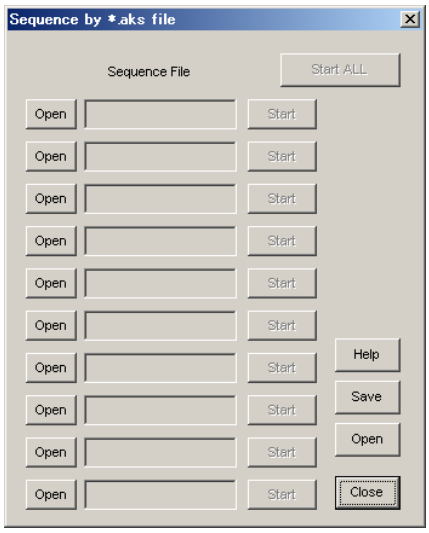


Figure 7. Window of [Sequence(File)]

[Open (left)] : Opening a sequence setting file (*.aks).
[Start] : Executing the sequence setting.
[Start All] : Executing all sequence settings.
Sequences are executed in descending order.
[Help] : Pop up the help window.
[Save] : Saving sequence setting file assignment. The file name is "*.mas".
[Open(right)] : Opening a saved sequence setting file assignment "*. mas".
[Close] : Closing the dialog box and finish the process.

*Operating Suggestions

(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mas" should be stored in the same folder.
(2) When "Stop" is selected in the sequence the process will be paused and a pop-up message will appear. Click "OK" to continue the process.

Figure 8. Window of [Sequence Pause]

1. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

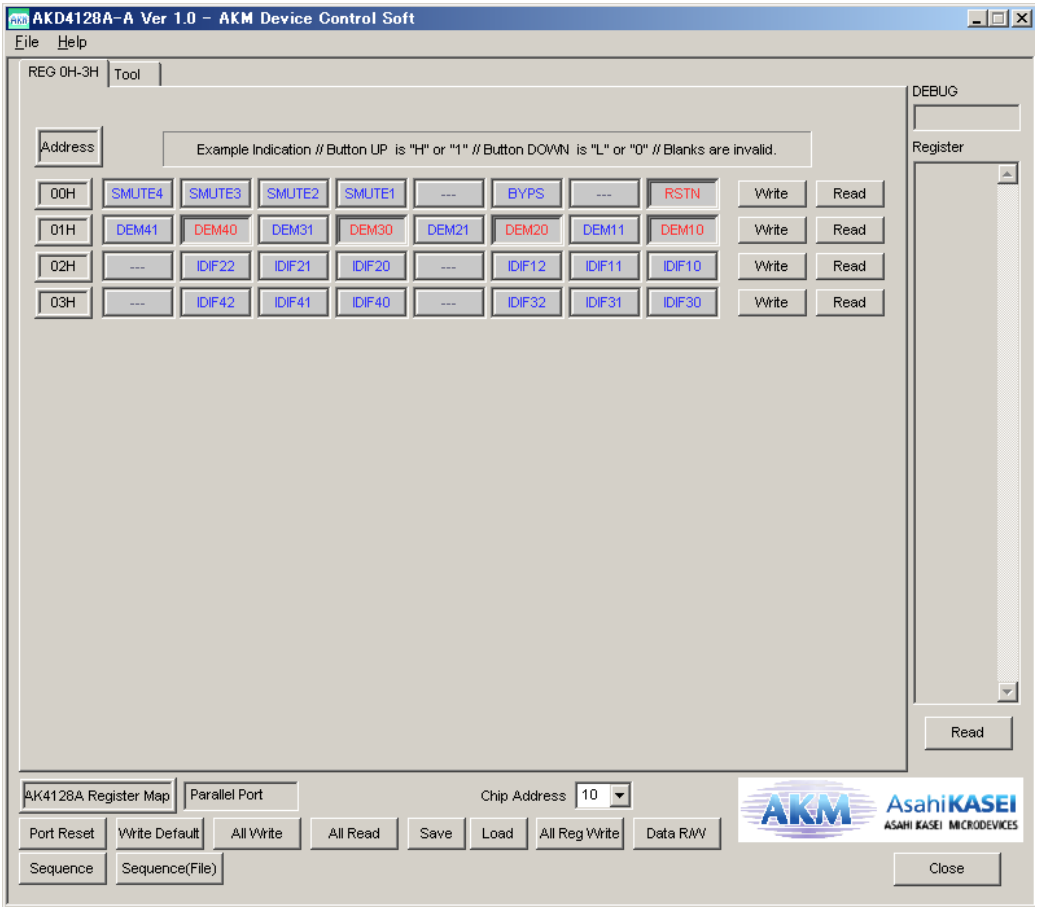


Figure 9. Window of [REG]

[Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or ”0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

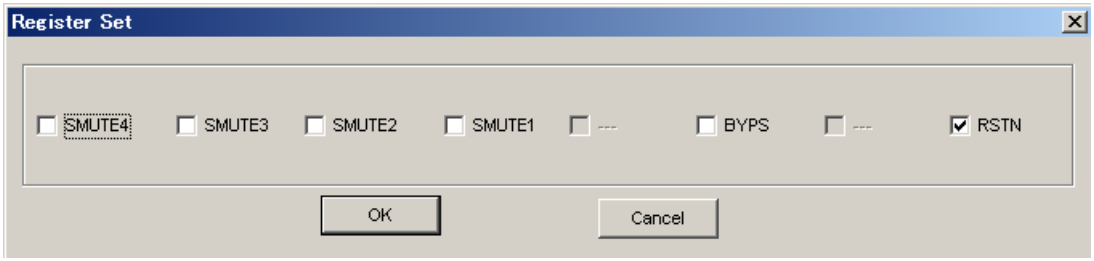


Figure 10. Window of [Register Set]

[Read]: Data Read

Click [Read] button located on the right of the each corresponded address to execute register reading.

After register reading, the display will be updated regarding to the register status.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Please be aware that button statuses will be changed by Read command.

2.[Tool]: Testing Tools

This tab screen is for evaluation testing tool.
Click buttons for each testing tool.

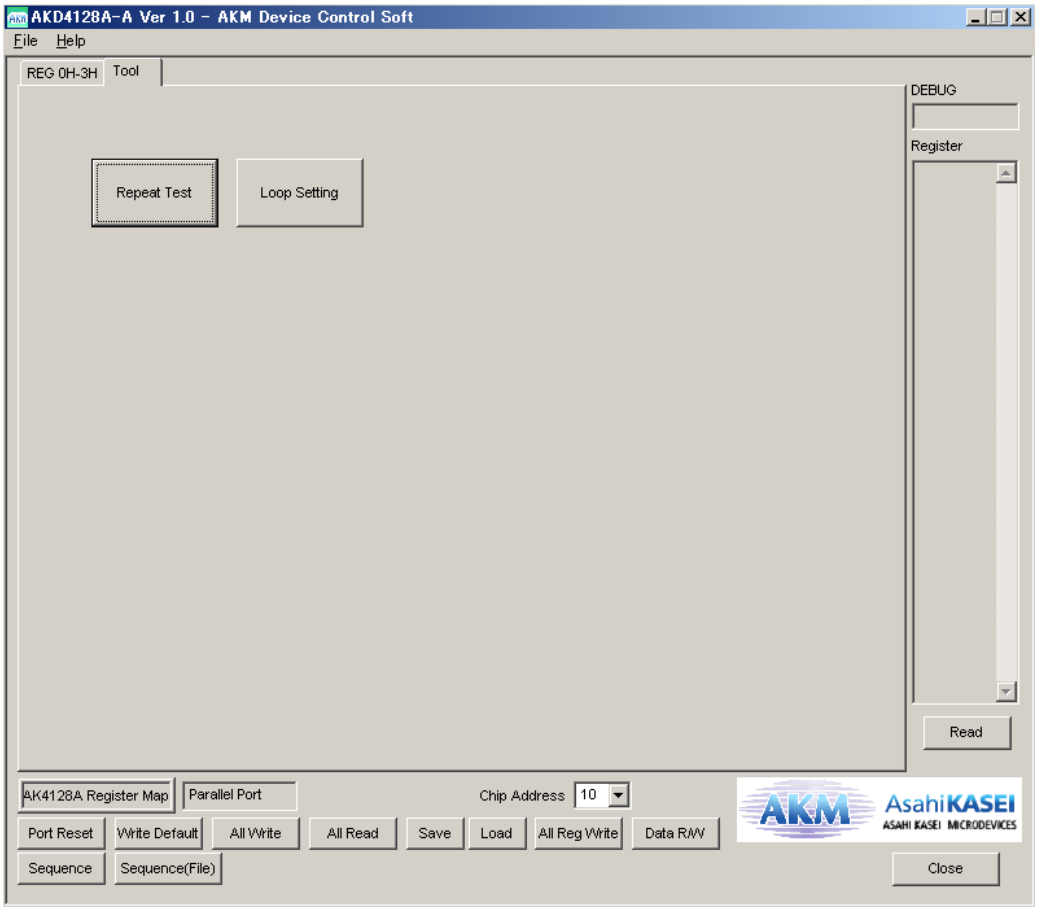


Figure 11. Window of [Tool]

[Repeat Test]: Repeat Test Dialog

Click [Repeat Test] button to open repeat test setting dialog box.

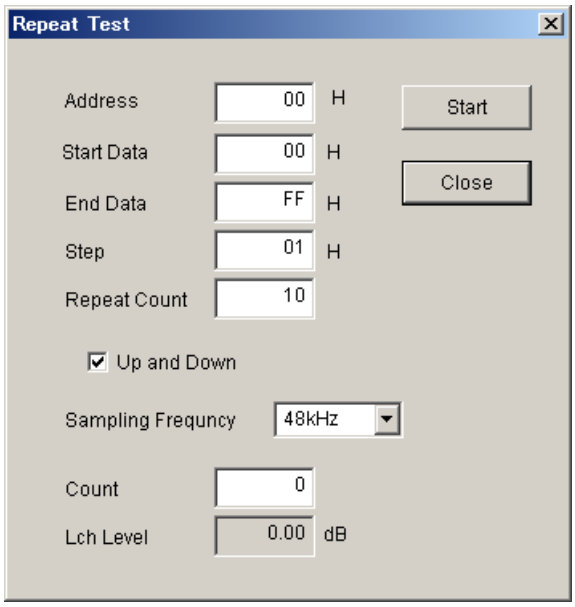


Figure 12. Window of [Repeat Test]

[Loop Setting]: Loop Setting Dialog

Click [Loop Setting] button to open loop setting dialog box.

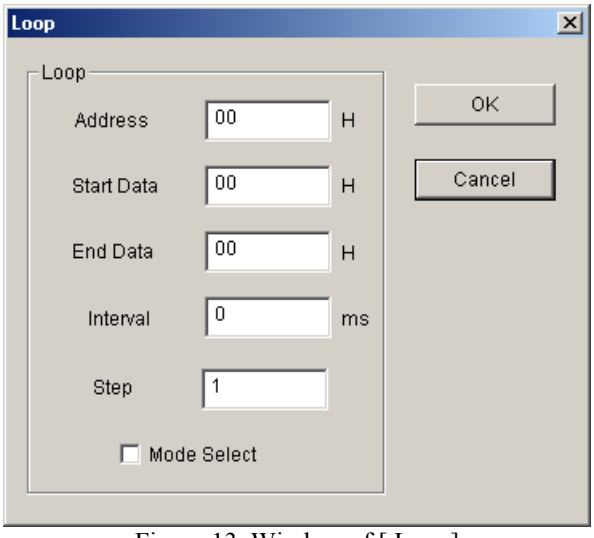


Figure 13. Window of [Loop]

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision, System Two Cascade
- Power Supply : AVDD=DVDD=3.3V
- Band width : 20Hz ~ FSO/2
- INAS pin : "L" (Synchronous Mode)
- OMCLK/XTI Input : Use X'Tal (X1)
- Output PORT : Slave Mode
- Temperature : Room

[Measurement Result]

SRC Characteristics	SDTO1		SDTO2		SDTO3		SDTO4		Unit
	Lch	Rch	Lch	Rch	Lch	Rch	Lch	Rch	
THD+N (Input = 1kHz, 0dBFS)									
FSO/FSI = 44.1kHz/48kHz	130.4	130.4	130.3	130.3	130.4	130.4	130.4	130.4	dB
FSO/FSI = 48kHz/44.1kHz	125.0	125.0	125.0	125.0	125.1	125.1	125.1	125.1	dB
FSO/FSI = 48kHz/192kHz	133.3	133.4	133.5	133.3	133.3	133.4	133.4	133.5	dB
FSO/FSI = 192kHz/48kHz	124.9	124.9	124.7	124.9	124.9	124.9	124.9	124.9	dB
Worst Case (FSO/FSI = 32kHz/176.4kHz)	130.4	130.4	130.3	130.3	130.4	130.4	130.4	130.4	dB
Dynamic Range (Input = 1kHz, –60dBFS)									
FSO/FSI = 44.1kHz/48kHz	136.5	136.5	136.7	136.7	136.7	136.9	136.8	136.8	dB
FSO/FSI = 48kHz/44.1kHz	136.7	136.8	136.6	136.7	136.6	136.8	136.8	136.9	dB
FSO/FSI = 48kHz/192kHz	136.3	136.5	136.4	136.3	136.3	136.3	136.4	136.4	dB
FSO/FSI = 192kHz/48kHz	132.6	132.6	132.7	132.7	132.6	132.7	132.7	132.7	dB
Worst Case(FSO/FSI = 48kHz/32kHz)	136.2	136.5	136.3	136.3	136.5	136.5	136.2	136.3	dB
Dynamic Range (Input = 1kHz, –60dBFS, A-weighted)									
FSO/FSI = 44.1kHz/48kHz	140.2	140.4	140.2	140.1	140.1	140.1	140.2	140.2	dB

[Plots]

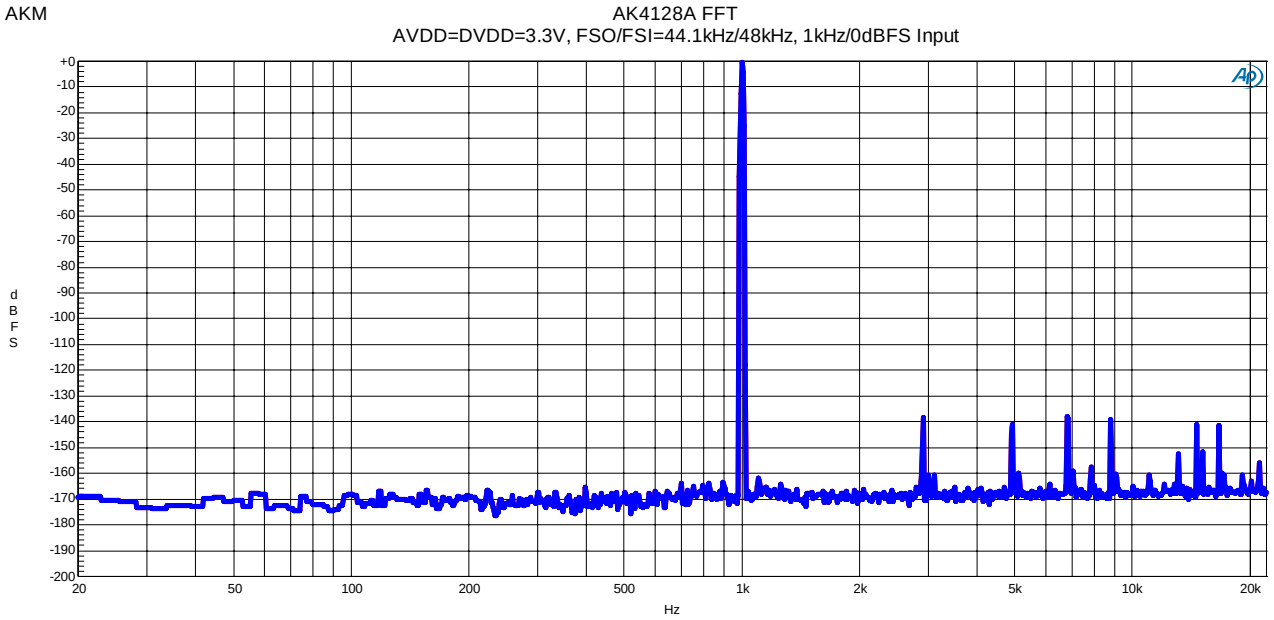


Figure 14. FFT Plot (Input = 0dBFS)

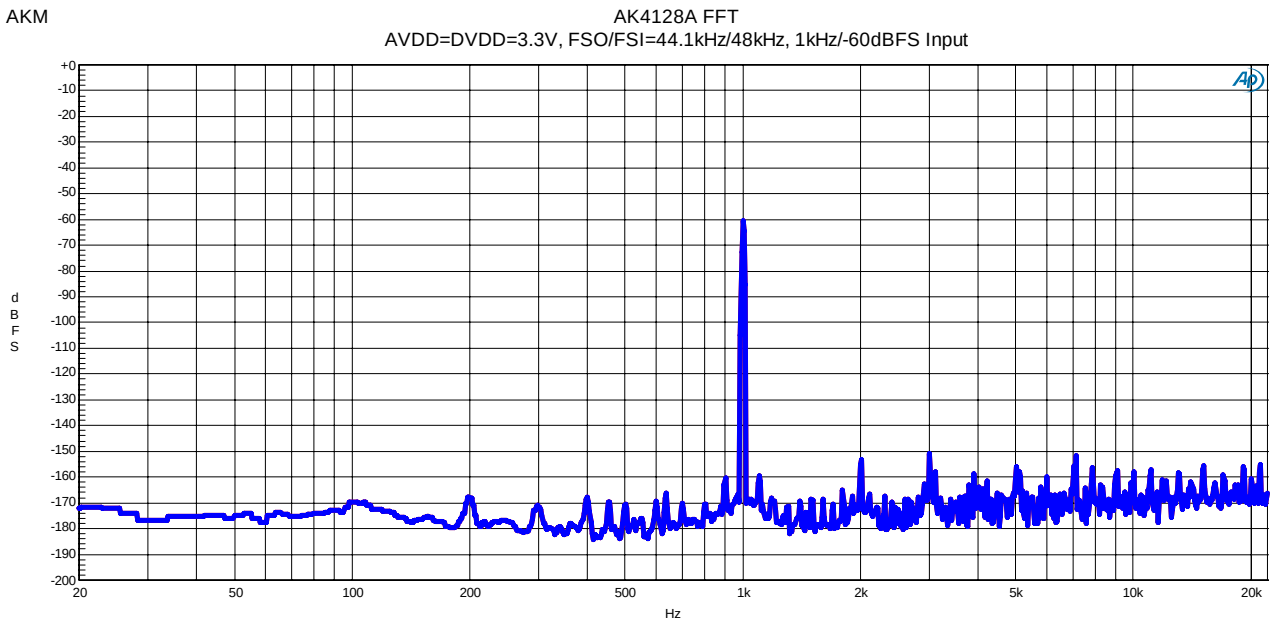


Figure 15. FFT Plot (Input = -60dBFS)

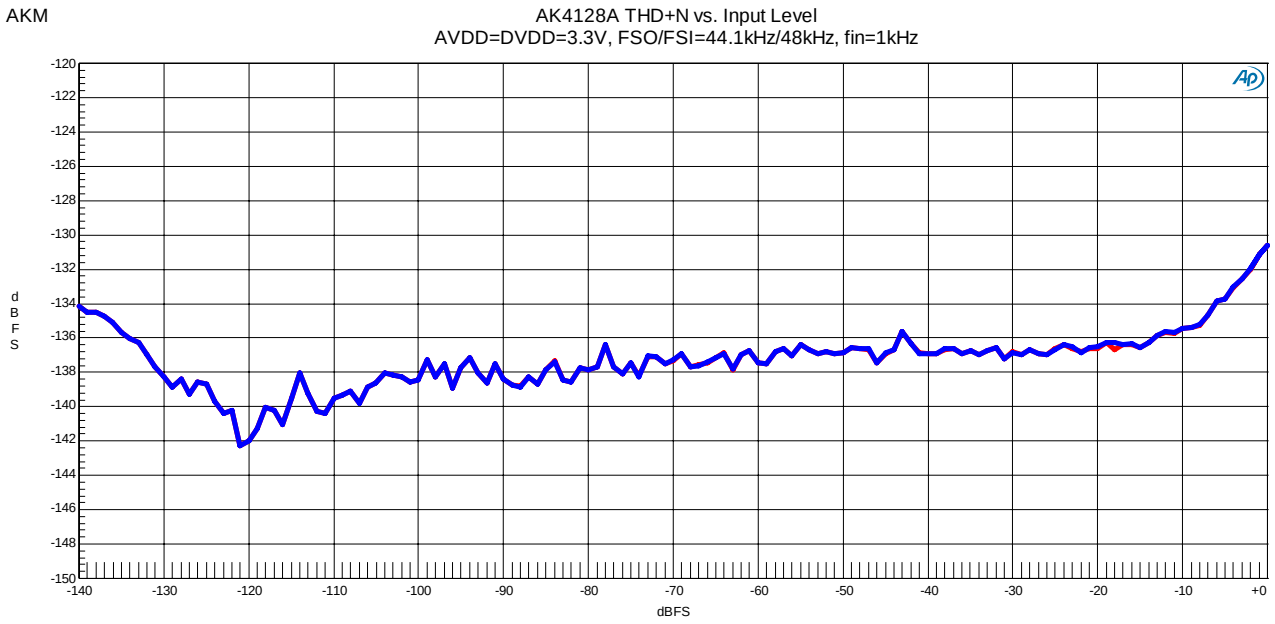


Figure 16. THD+N vs. Input Level

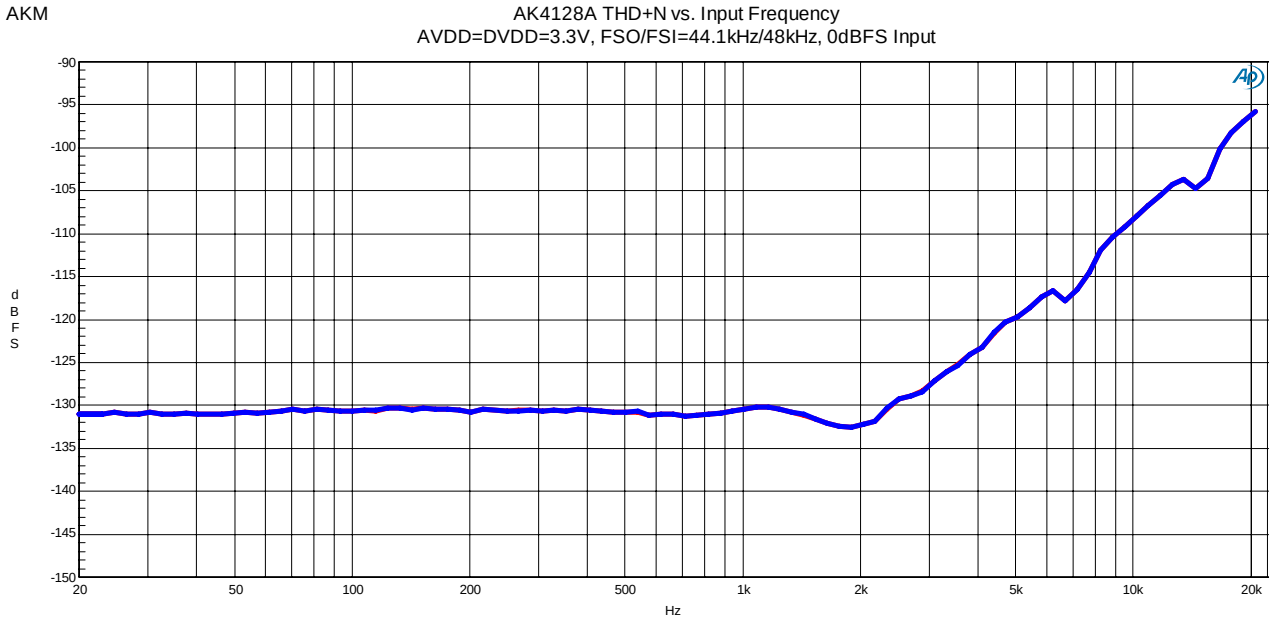


Figure 17. THD+N vs. Input Frequency (Input = 0dBFS)

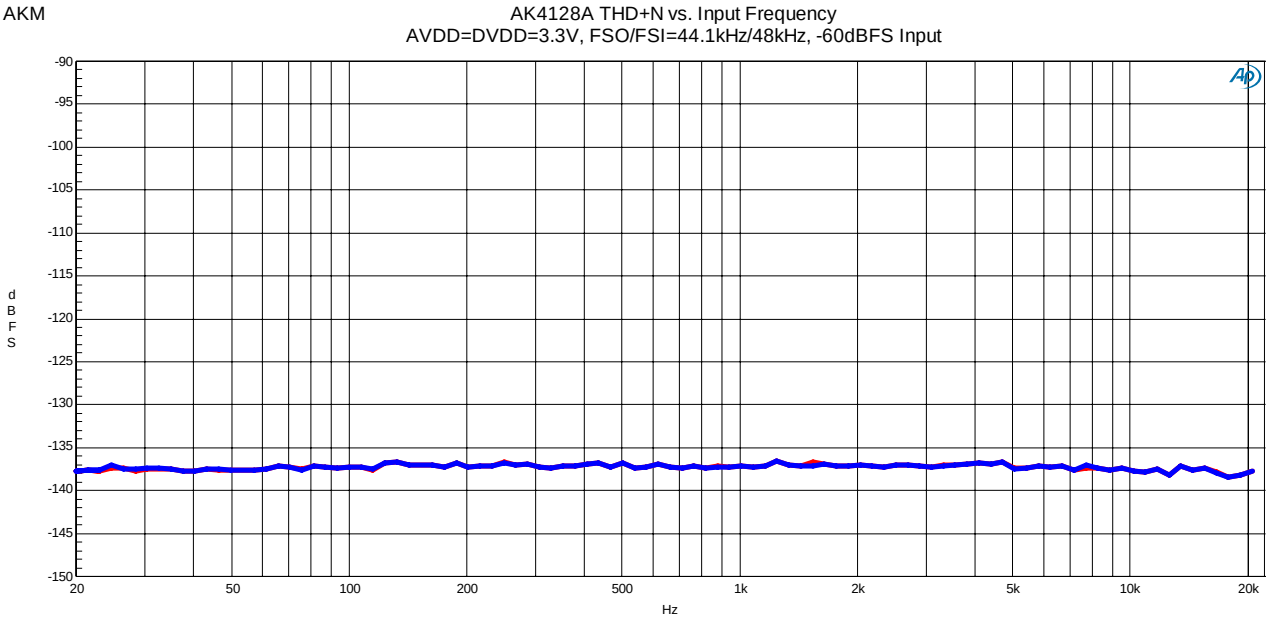


Figure 18. THD+N vs. Input Frequency (Input = -60dBFS)

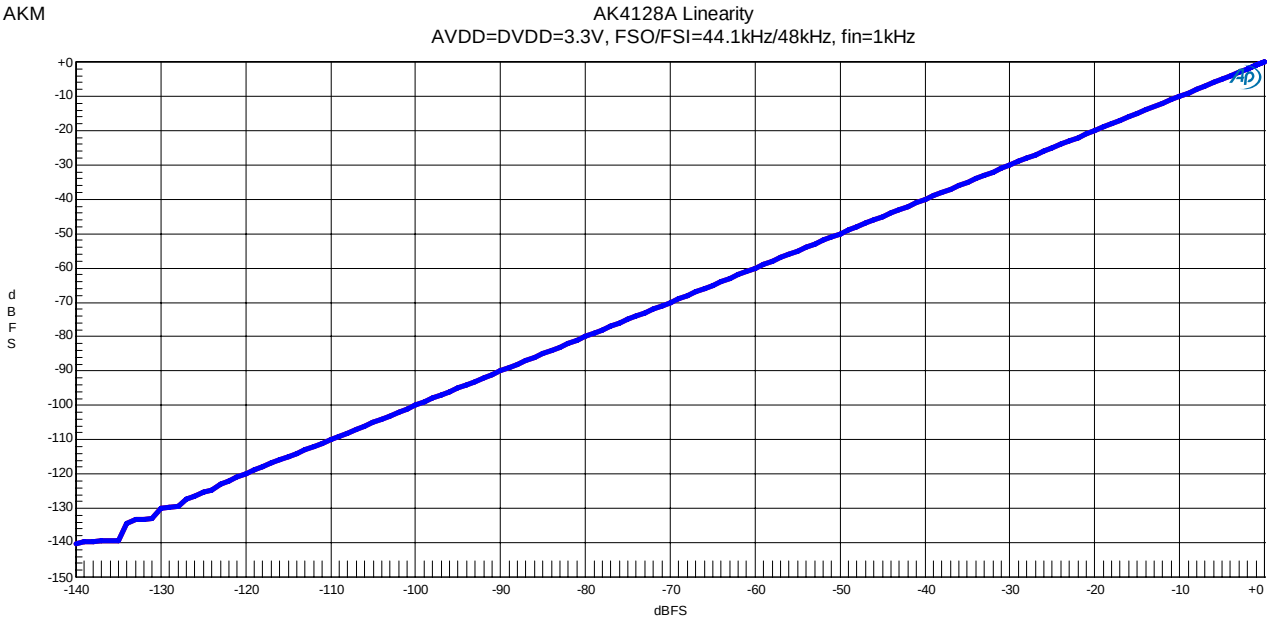


Figure 19. Linearity

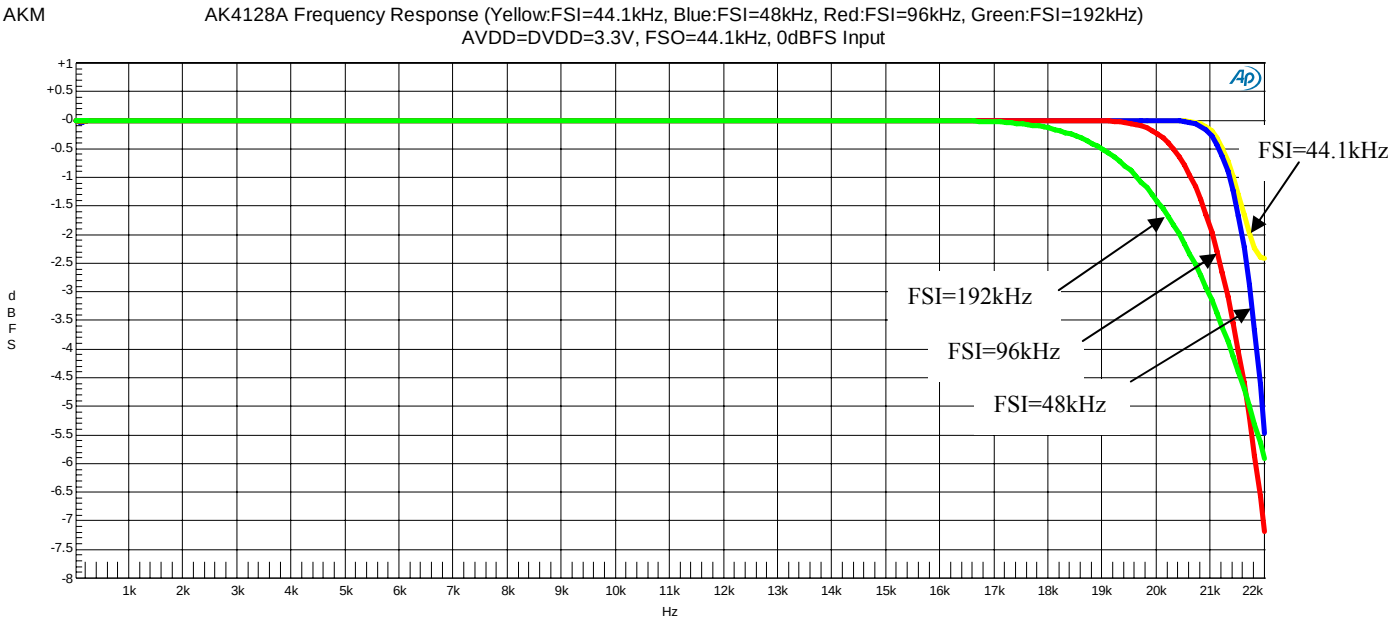


Figure 20. Frequency Response (FSO=44.1kHz)

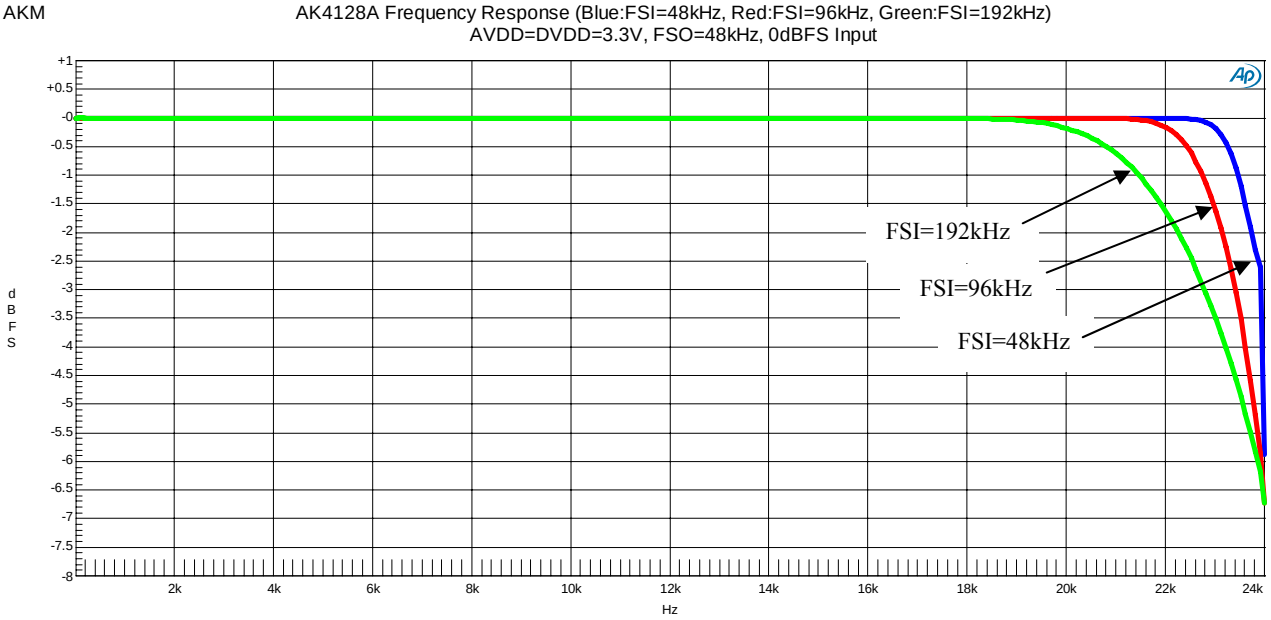
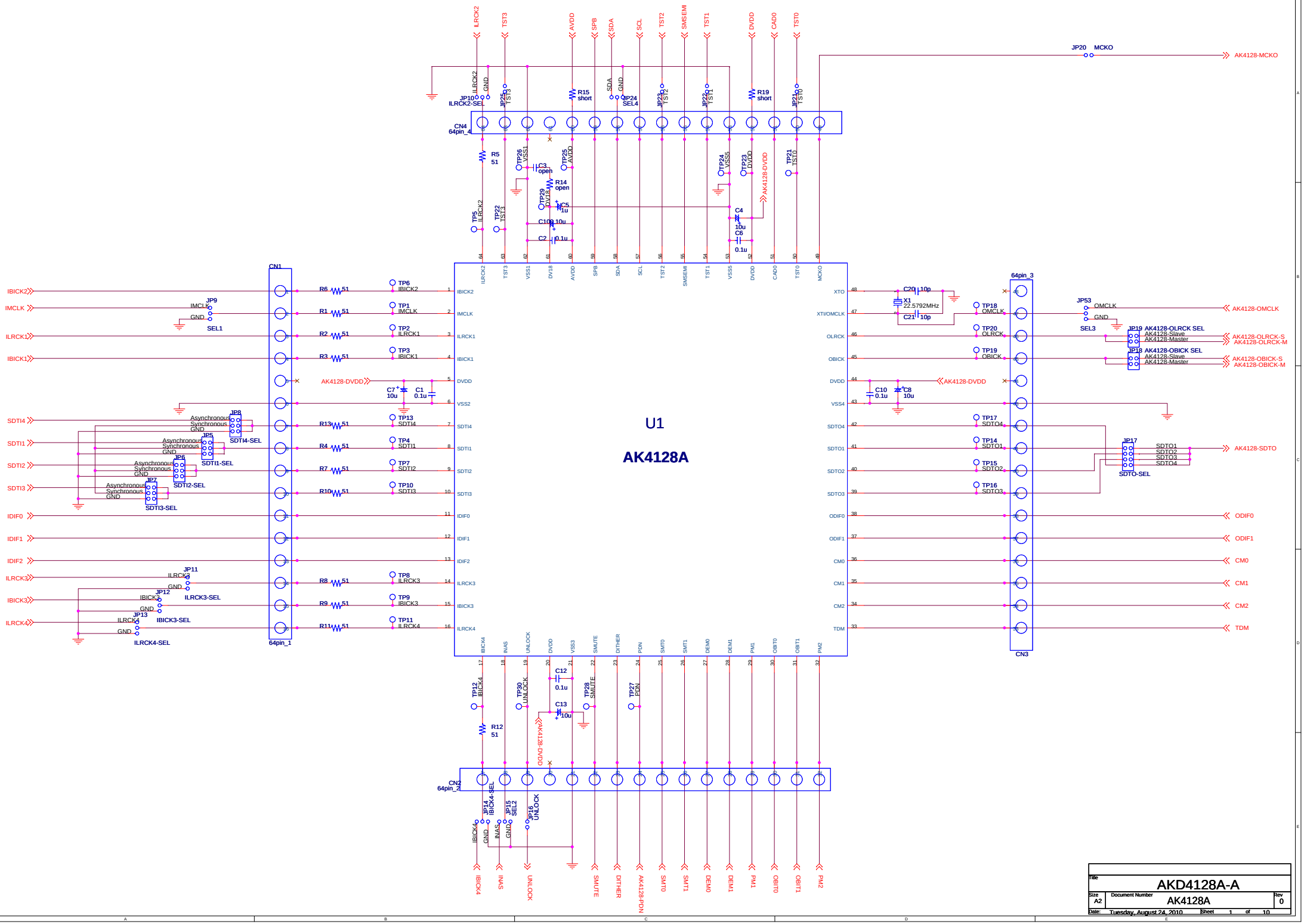


Figure 21. Frequency Response (FSO=48kHz

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Page	Contents
10/08/24	KM104300	0	First edition	-	
10/09/30	KM104301	0	Addition	33-37	Measurement Results and Plots were added.


U1
AK4128A
CN1
64pin_1
CN2
64pin_2
CN3
64pin_3
CN4
64pin_4
ILRCK2
TST3
AVDD
SPB
SDA
SCL
TST2
SMSEMI
TST1
DVDD
CAD0
TST0
MCKO
XTO
XTI/OMCLK
OLRCK
OBICK
VSS4
SDTO4
SDTO1
SDTO2
SDTO3
CM0
CM1
CM2
TDM
IBICK4
INAS
UNLOCK
VSS3
SMUTE
DITHER
PDN
SMT0
SMT1
DEM0
DEM1
PM1
OBIT0
OBIT1
PM2
DV18
VSS1
VSS5
IBICK2
IMCLK
ILRCK1
IBICK1
DVDD
VSS2
SDTI4
SDTI1
SDTI2
SDTI3
IDIF0
IDIF1
IDIF2
ILRCK3
IBICK3
ILRCK4
JP10 ILRCK2-SEL
JP24 SEL4
JP20 MCKO
AK4128-MCKO
AK4128-DVDD
JP9 IMCLK
SEL1
JP53 OMCLK
SEL3
JP19 AK4128-OLRCK SEL
JP18 AK4128-OBICK SEL
AK4128-OLRCK-S
AK4128-OLRCK-M
AK4128-OBICK-S
AK4128-OBICK-M
JP8 SDTI4-SEL
JP5 SDTI1-SEL
JP6 SDTI2-SEL
JP7 SDTI3-SEL
JP17 SDTO-SEL
AK4128-SDTO
JP11 ILRCK3
JP12 IBICK3
ILRCK3-SEL
IBICK3-SEL
JP13 ILRCK4
ILRCK4-SEL
JP14 IBICK4-SEL
JP15 SEL2
JP16 UNLOCK
ODIF0
ODIF1
CM0
CM1
CM2
TDM
R15 short
R19 short
R5 51
R14 open
C3 open
C4 10u
C5 1u
C6 0.1u
C10 0.1u
C8 10u
C20 10p
C21 10p
X1 22.5792MHz
C7 10u
C1 0.1u
C12 0.1u
C13 10u
C100 10u
C2 0.1u
R6 51
R1 51
R2 51
R3 51
R13 51
R4 51
R7 51
R10 51
R8 51
R9 51
R11 51
R12 51
TP1 IMCLK
TP2 ILRCK1
TP3 IBICK1
TP4 SDTI1
TP7 SDTI2
TP10 SDTI3
TP8 ILRCK3
TP9 IBICK3
TP11 ILRCK4
TP13 SDTI4
TP6 IBICK2
TP5 ILRCK2
TP22 TST3
TP26 VSS1
TP25 AVDD
TP29 DV18
TP24 VSS5
TP23 DVDD
TP21 TST0
TP18 OMCLK
TP20 OLRCK
TP19 OBICK
TP17 SDTO4
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TP15 SDTO2
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TP12 IBICK4
TP30 UNLOCK
TP28 SMUTE
TP27 PDN
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AKD4128A-A
Size A2
Document Number
AK4128A
Rev 0
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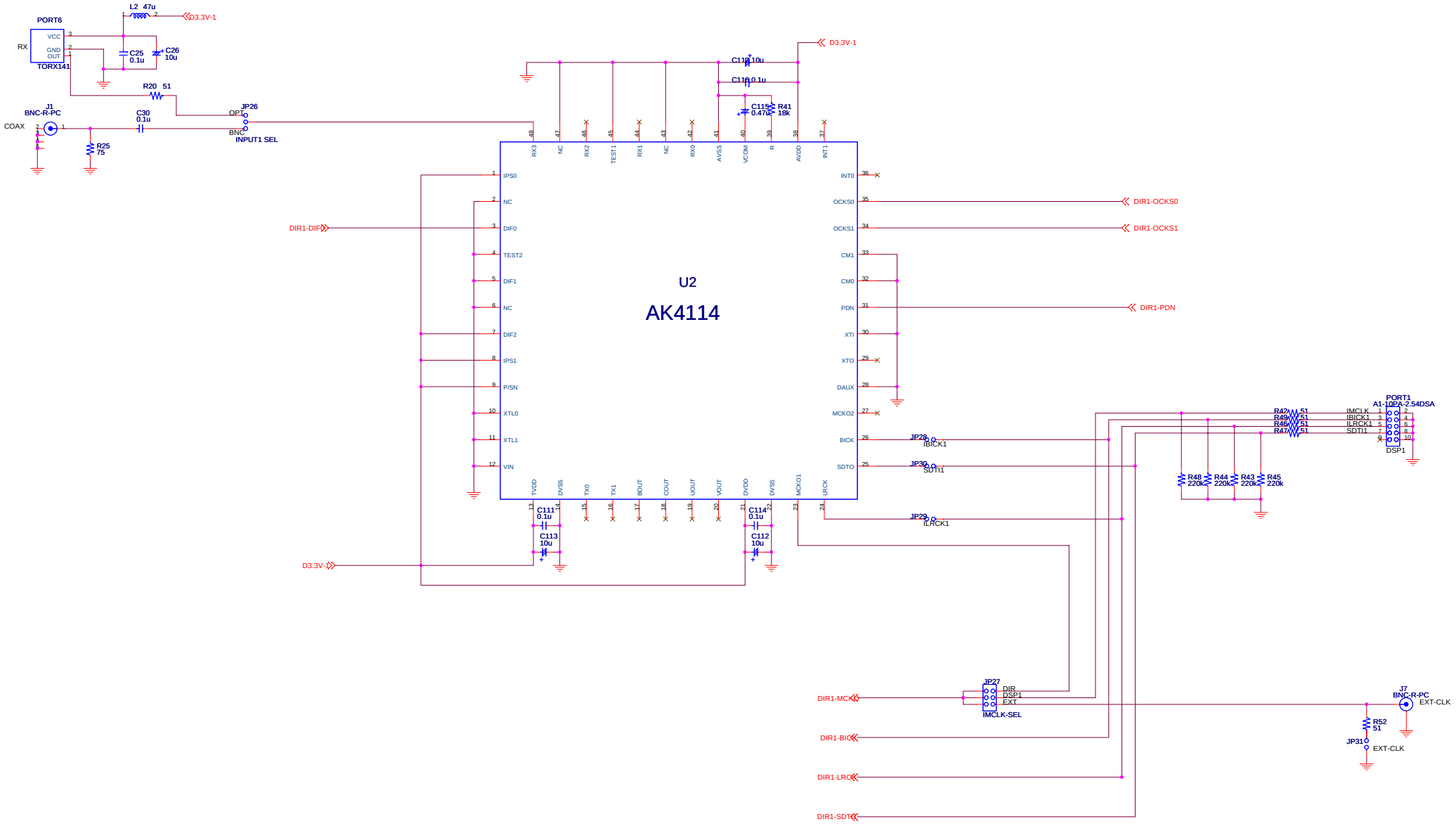

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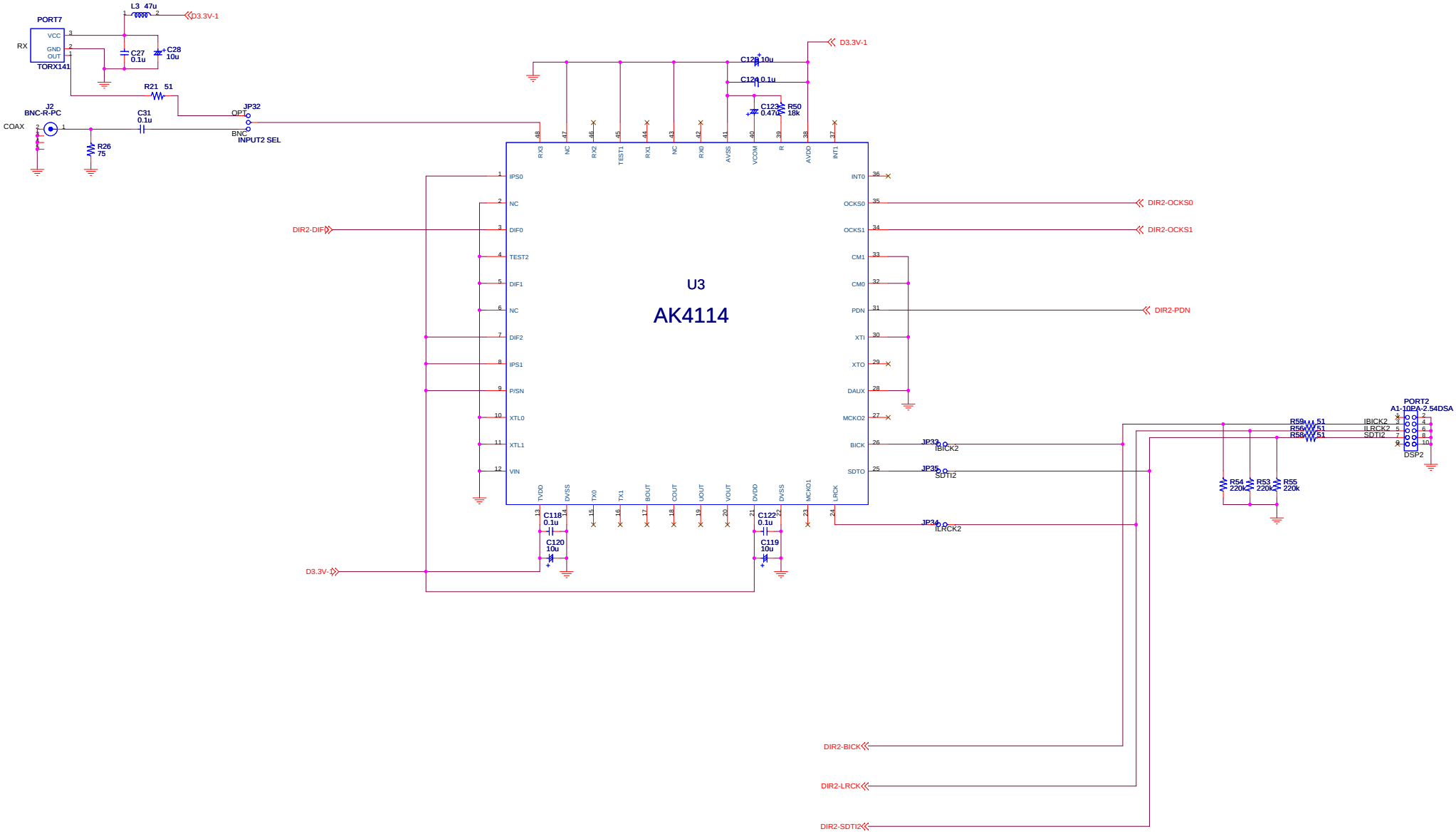

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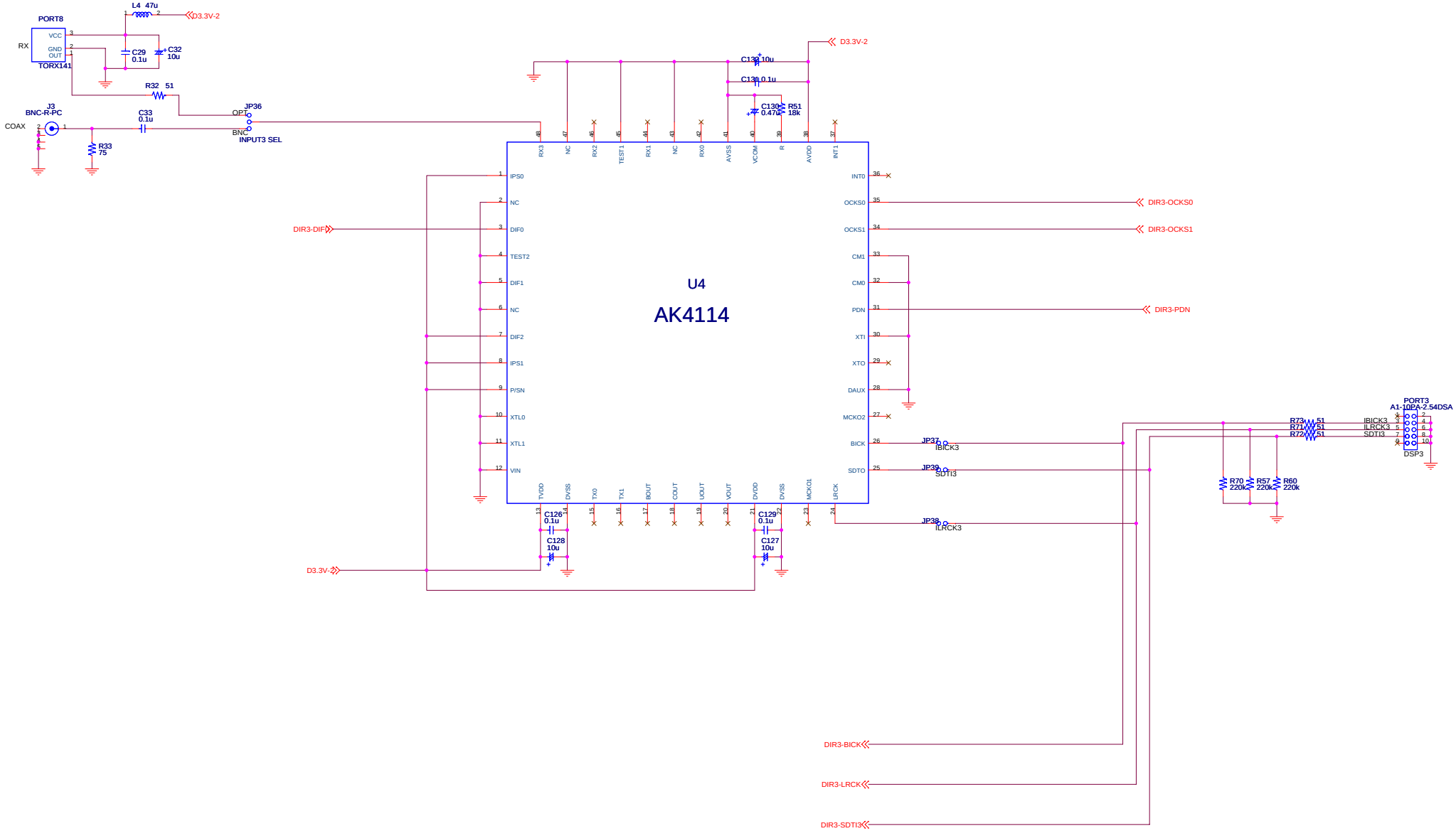

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Size A2	Document Number DIR3		Rev 0
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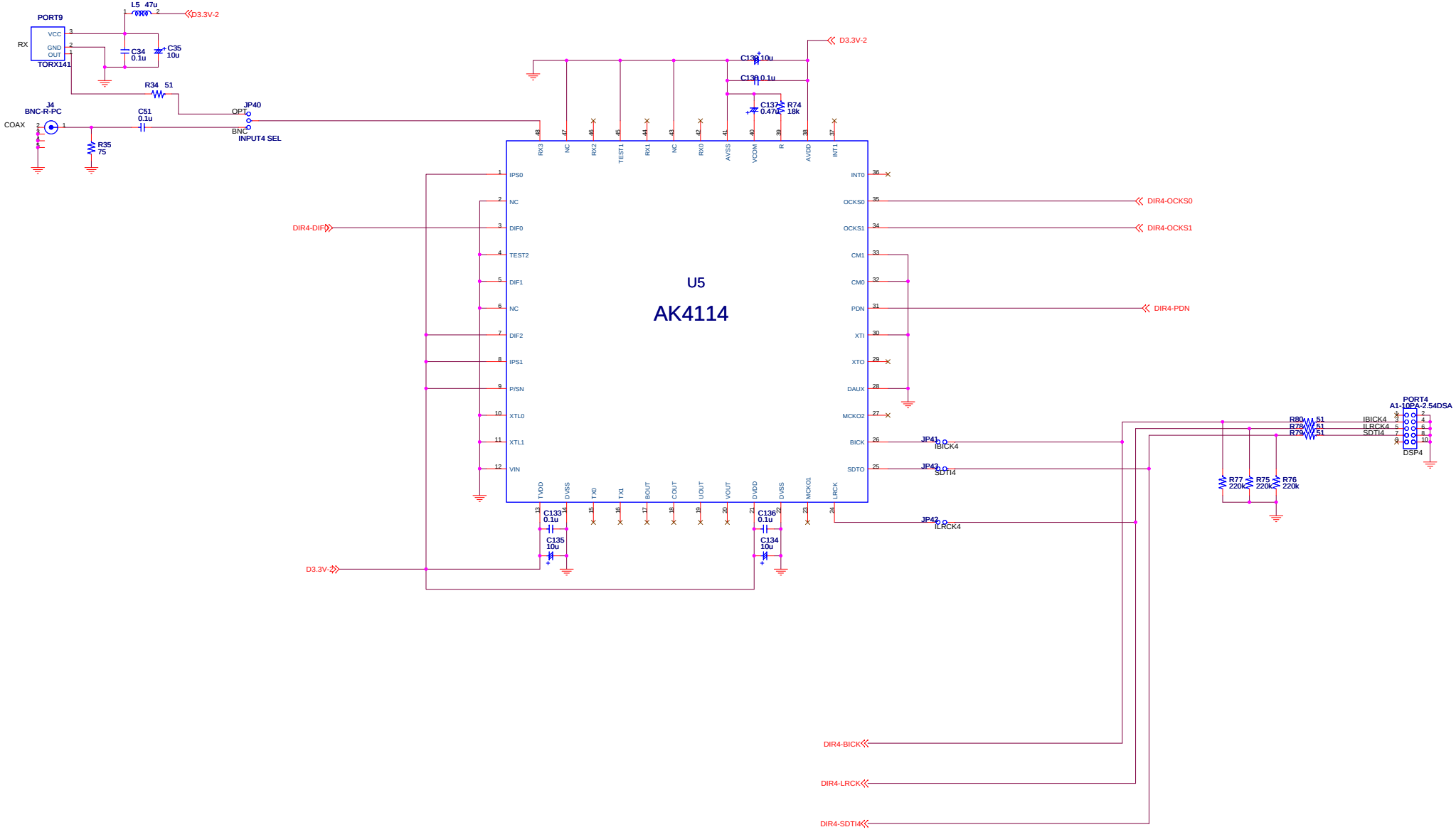

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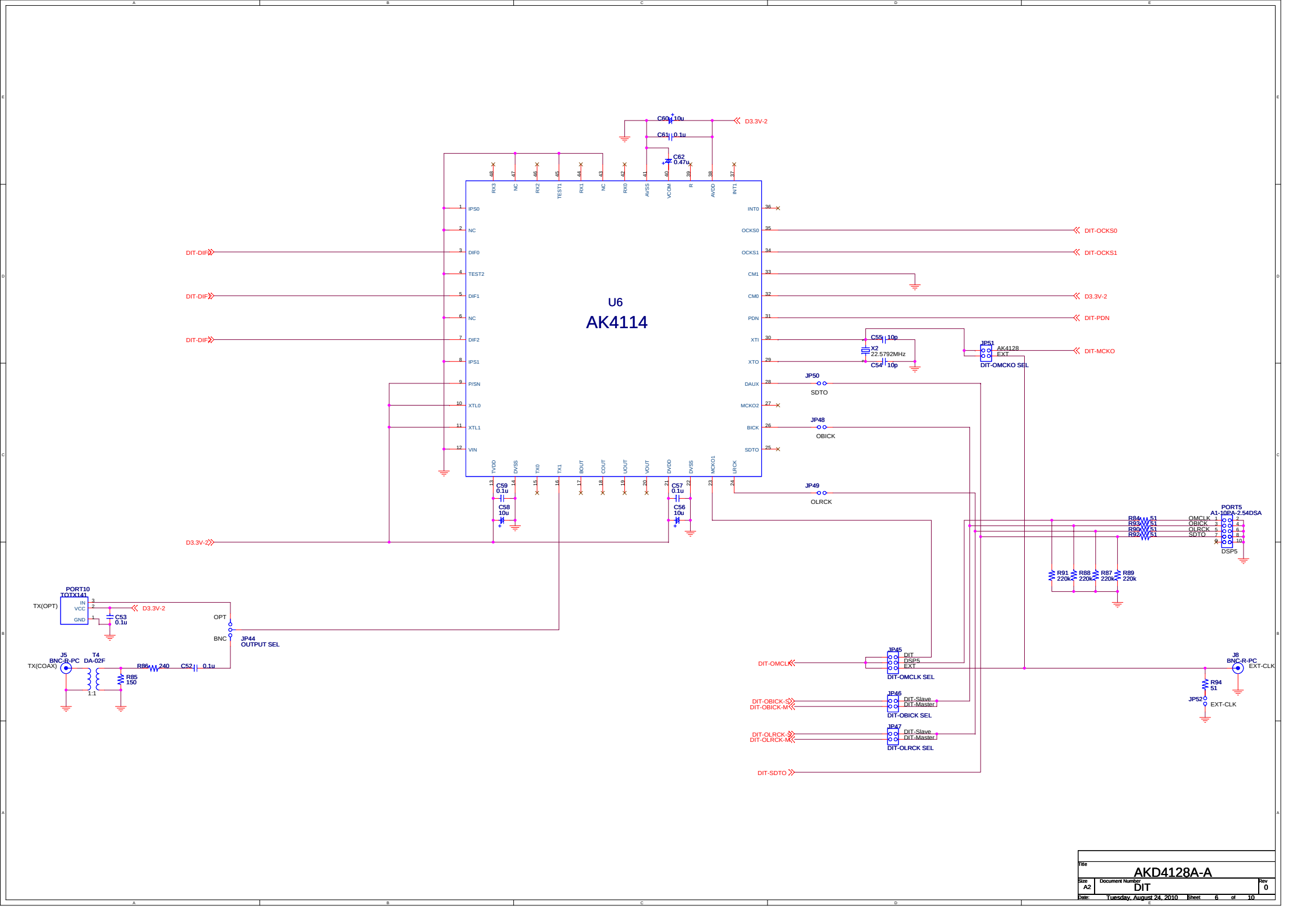

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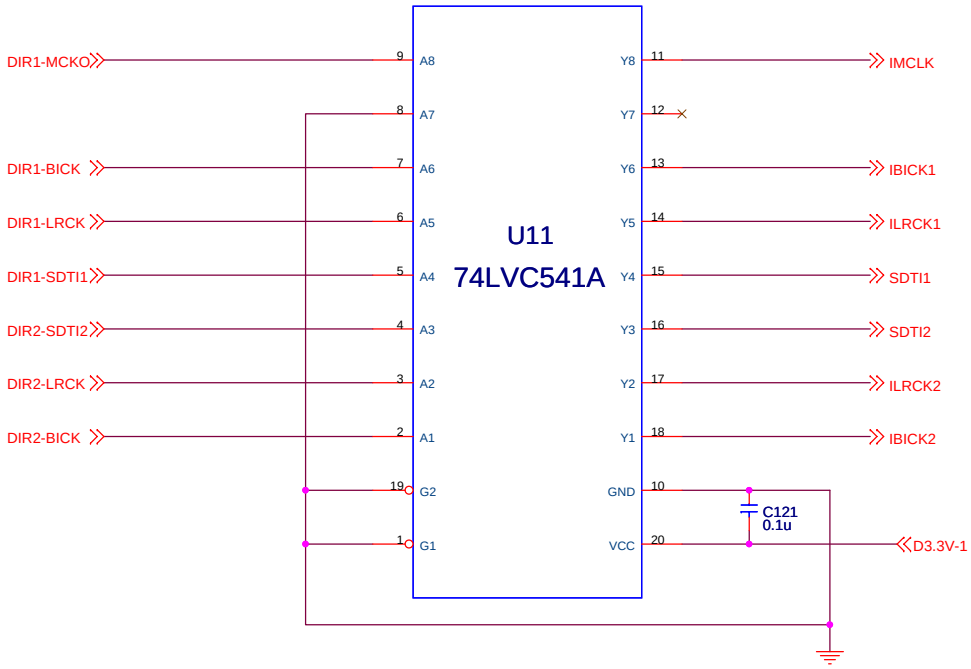

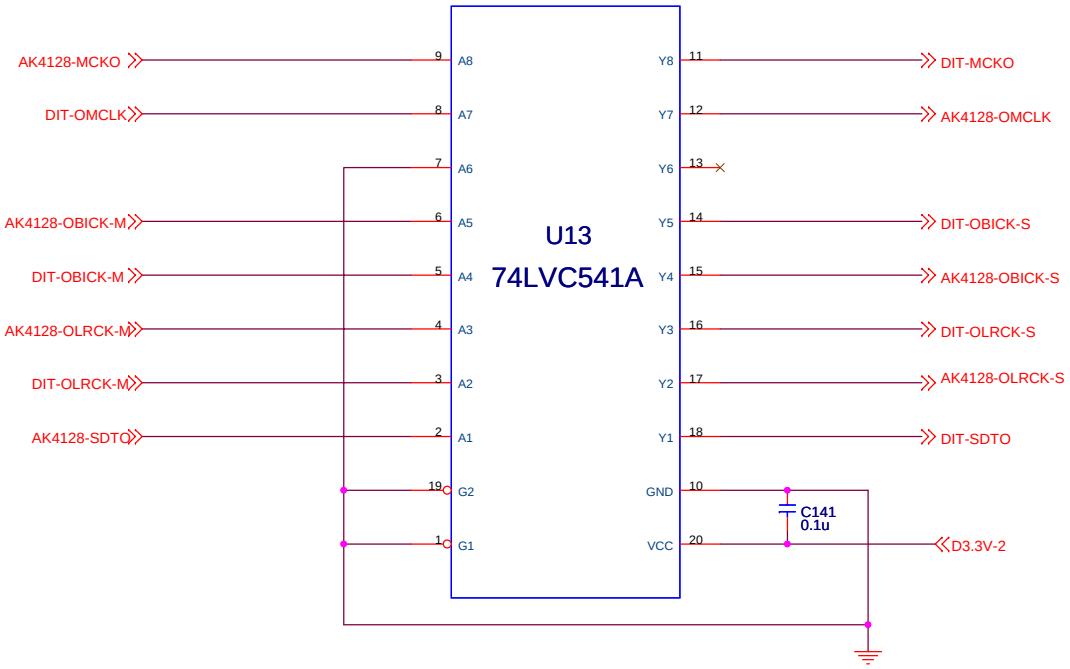

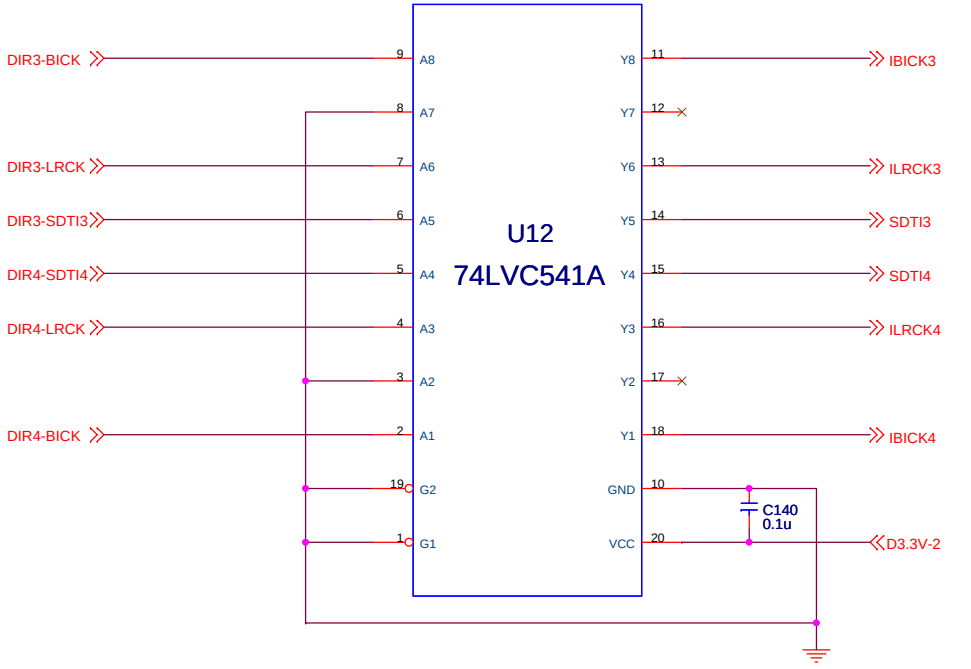

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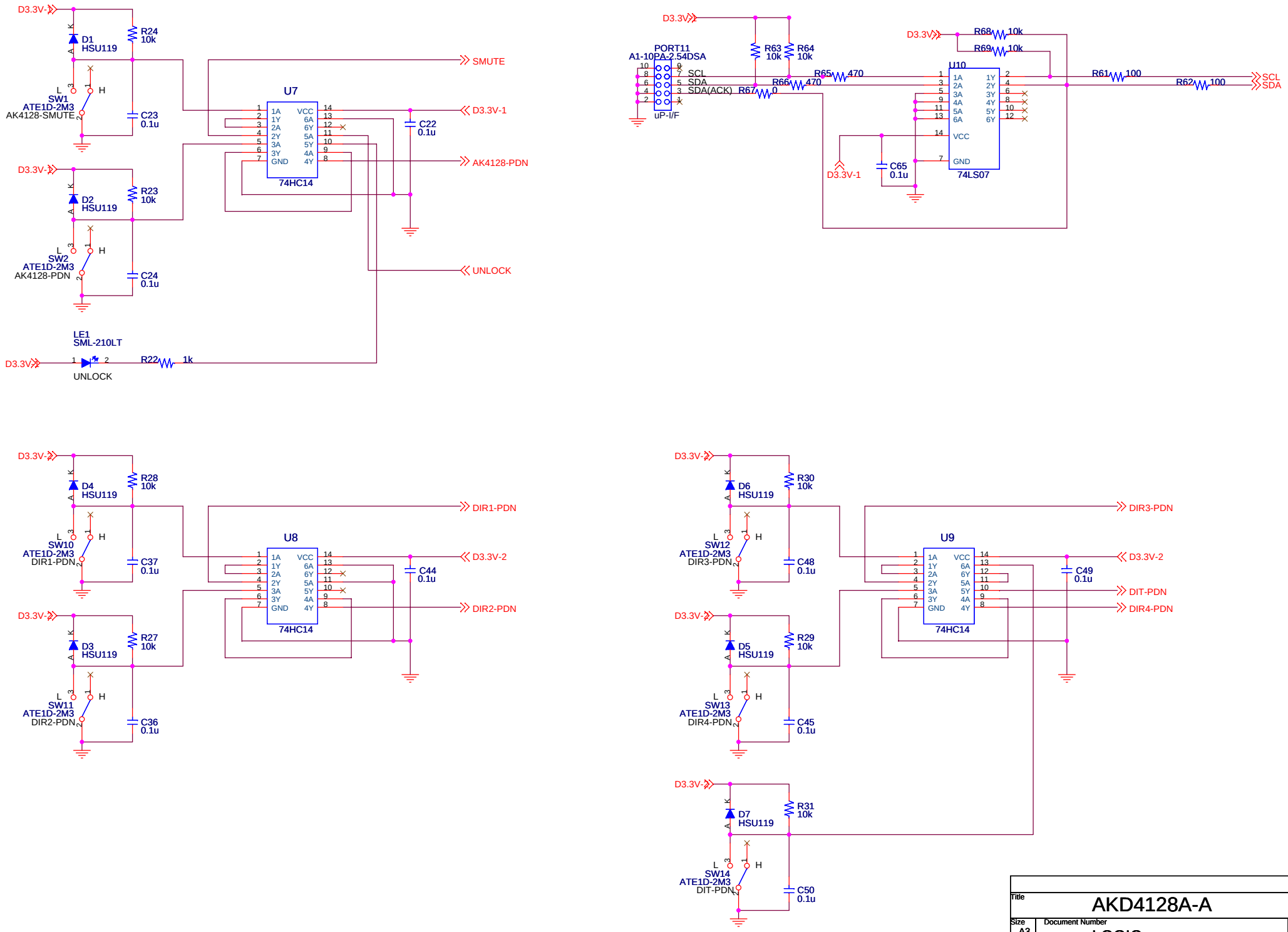

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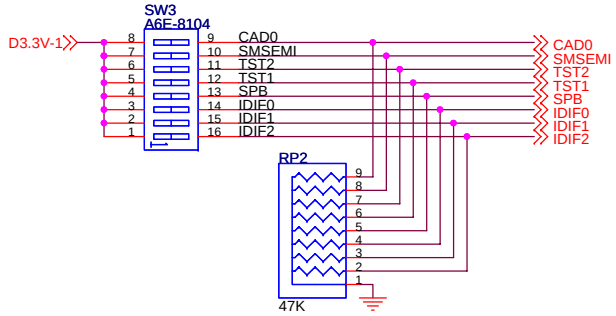

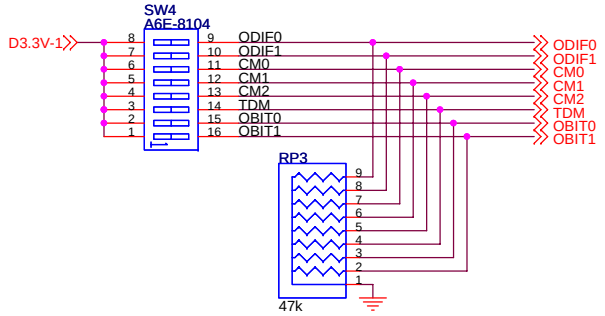

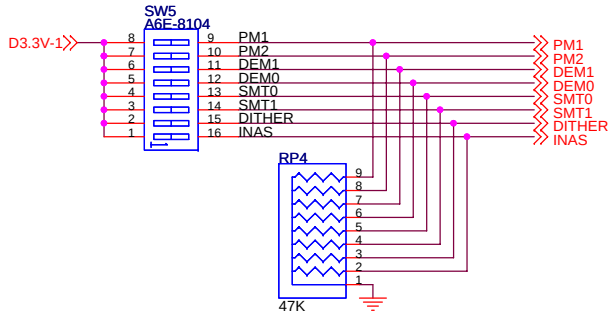

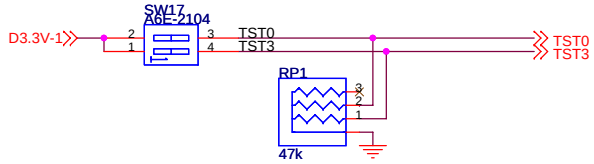

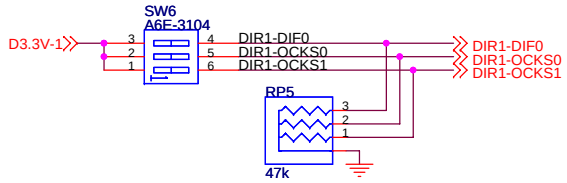

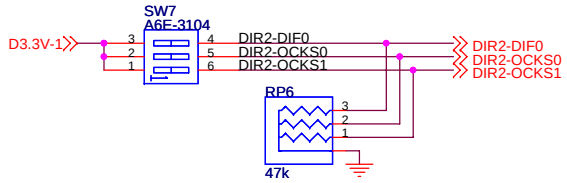

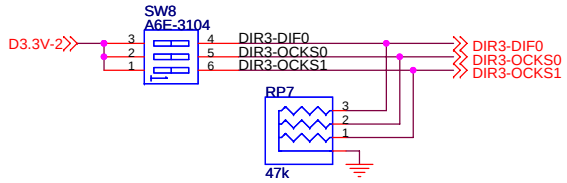

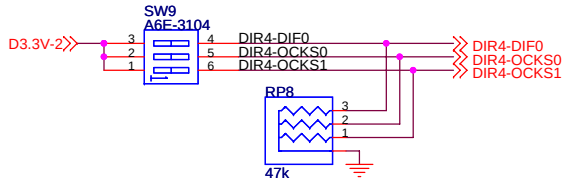

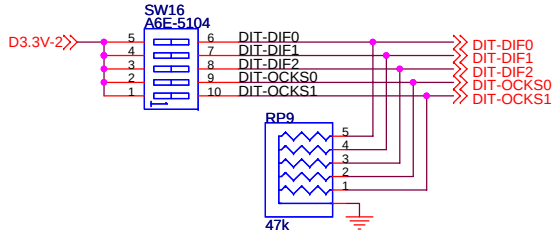

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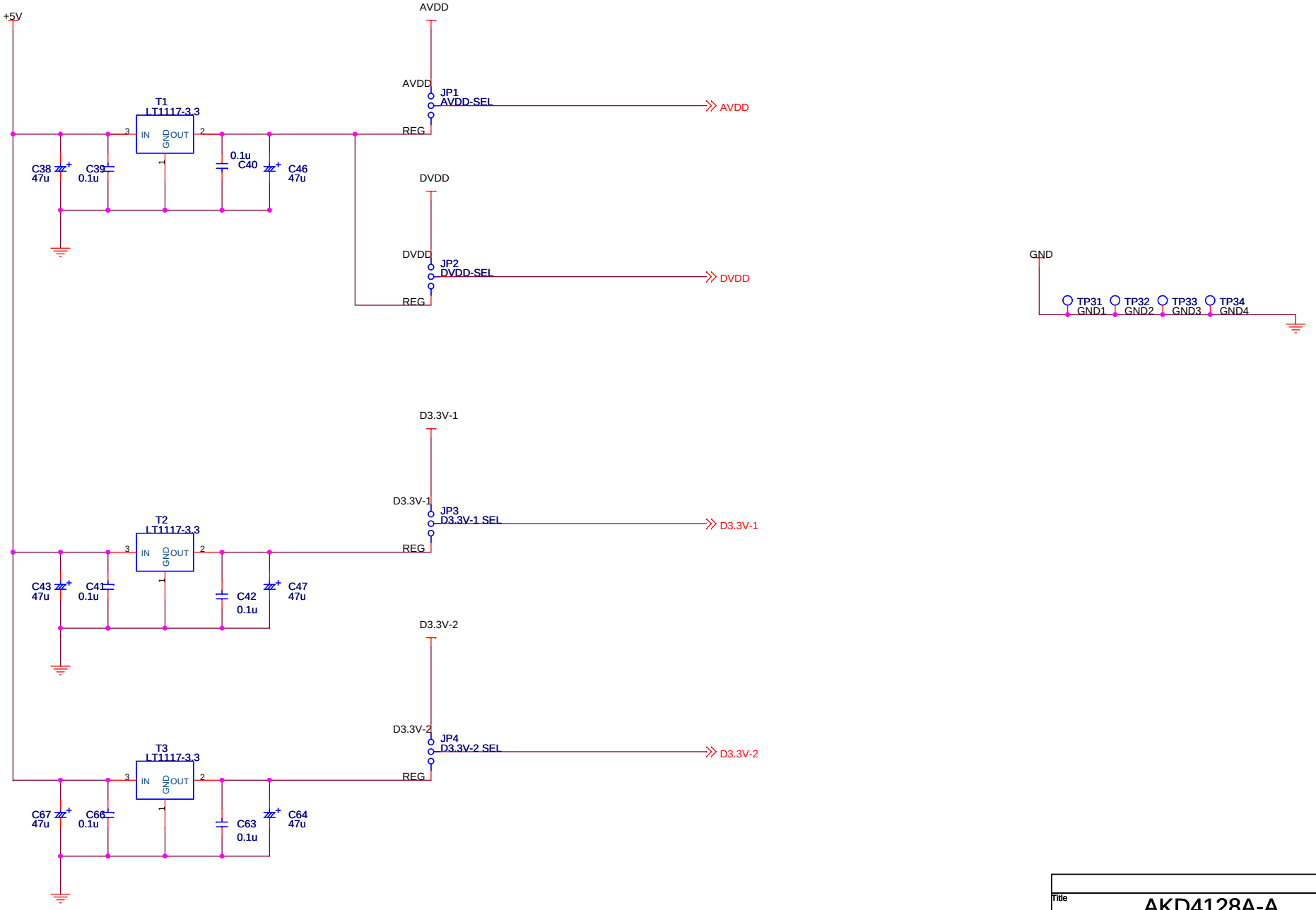

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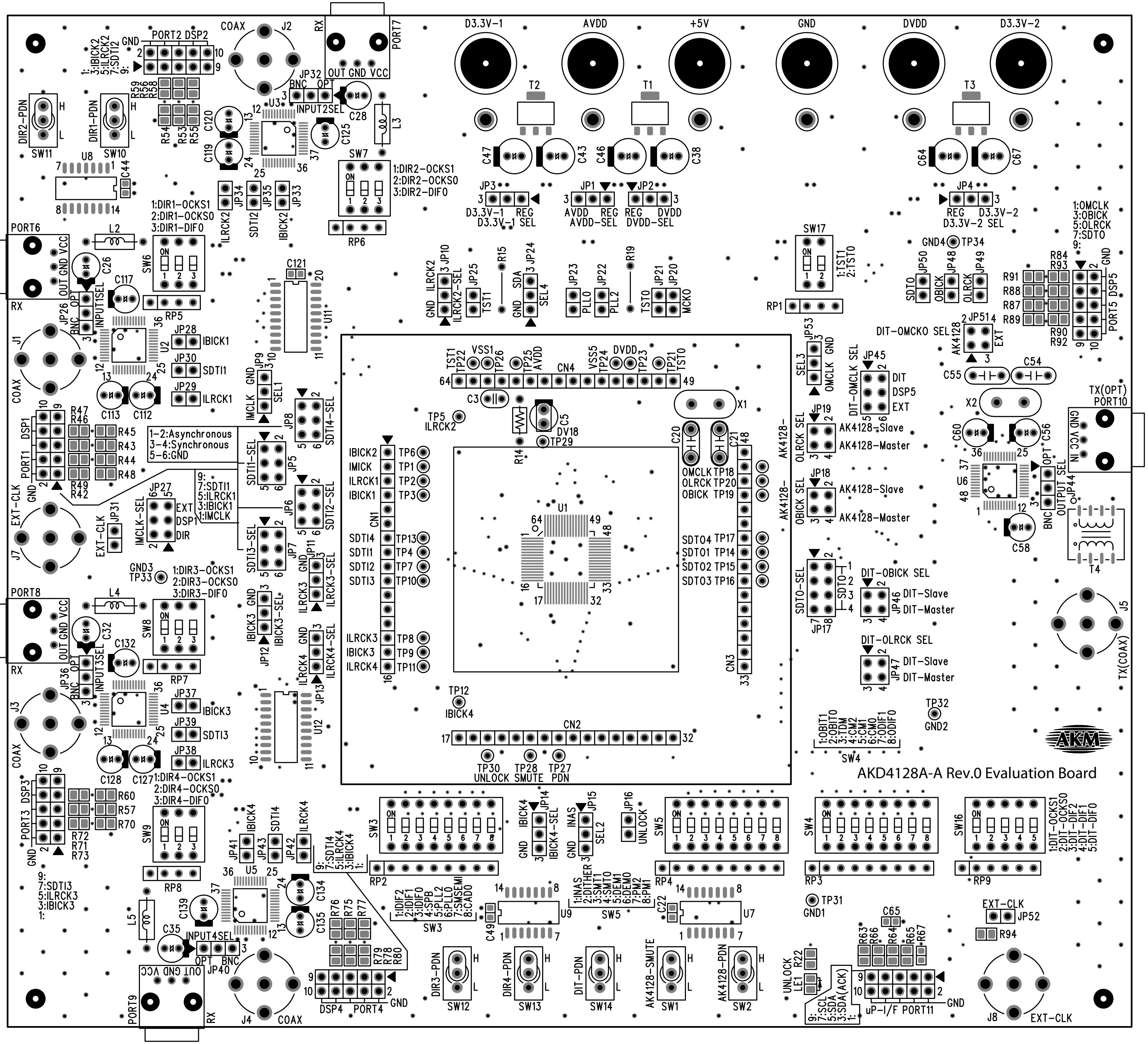
部品面シルク図



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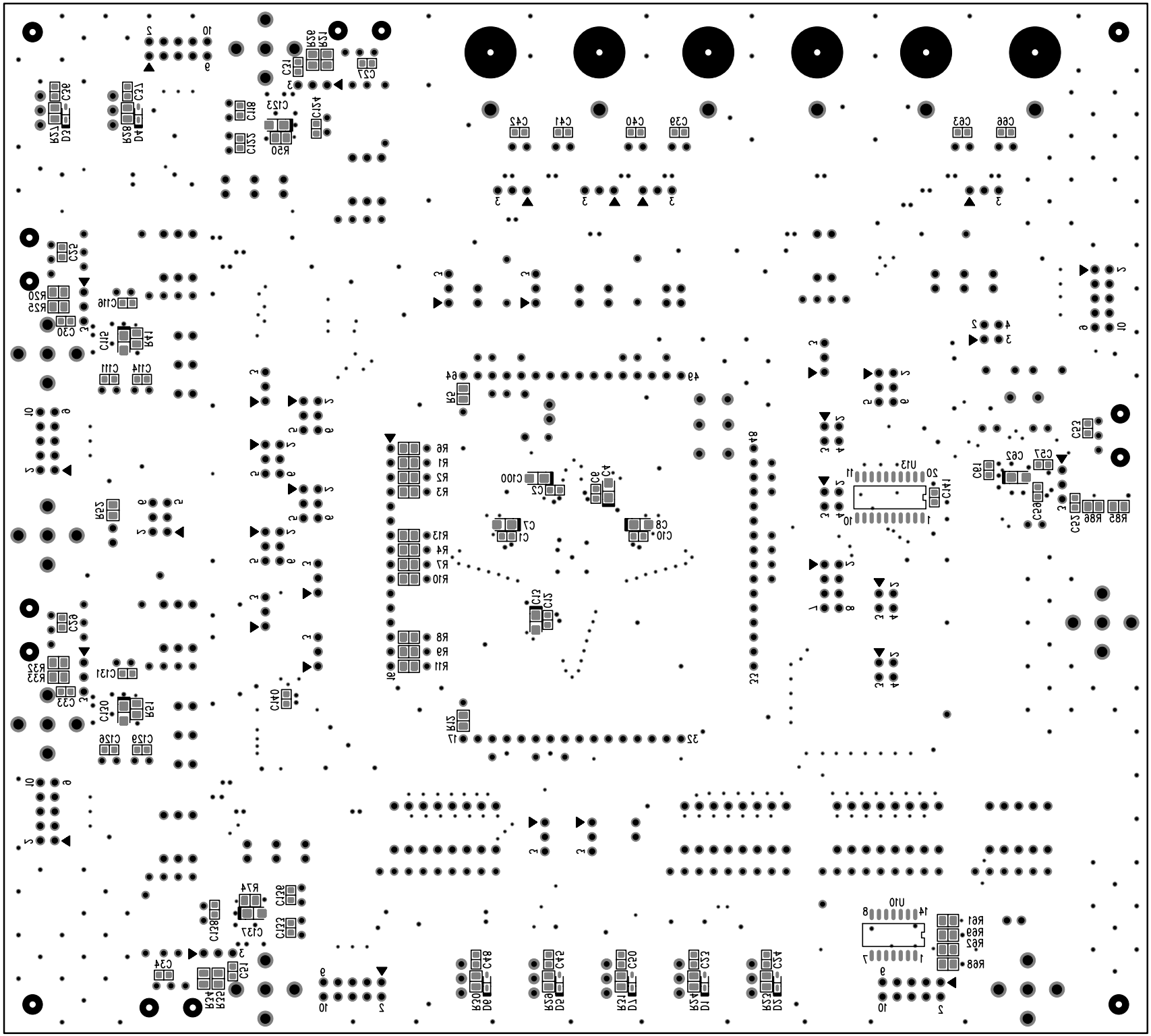
半田面シルク図



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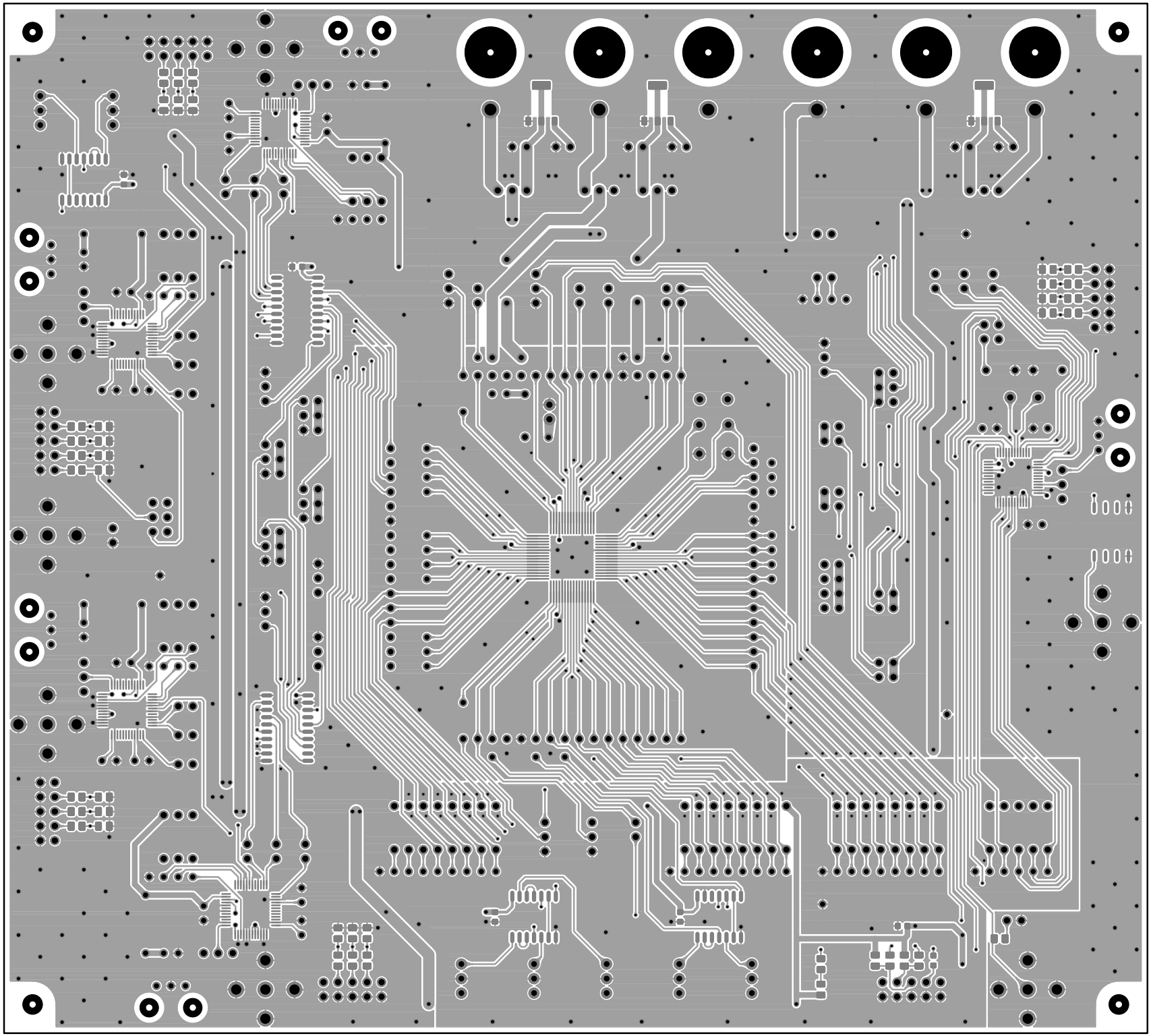
部品面パターン図



AK4128A-A Rev.0
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