LX1708

15+15W Stereo Filterless Class-D Amplifier

PRODUCTION DATA SHEET

DESCRIPTION

The LX1708 is part of a new generation of fully integrated stereo class-D amplifiers from Microsemi. This CMOS audio amplifier is optimized for highly efficient operation and minimum system cost. The stereo BTL (Bridge-tied-load) configuration uses 3-level PWM modulation. This allows eliminating the LC filter to reduce the system cost and simplify the system design. The LX1708 outputs 15W into each of two channels with better than 85% efficiency.

The part features on–board H-bridge output stages with low RDSON. External bootstrap capacitors are all that is required to provide the gate drive to the all-NFET output stage since on-board bootstrap diodes are provided.

The LX1708 also features Mute and Standby modes, over-current protection, POP-free turn-on and turn-off, under-voltage lockout, over-voltage protection, and over-temperature protection.

The LX1708 is offered in a small footprint, low profile surface mountable 32-pin Micro Lead Quad Package (MLPQ) in 7mm x 7 mm.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

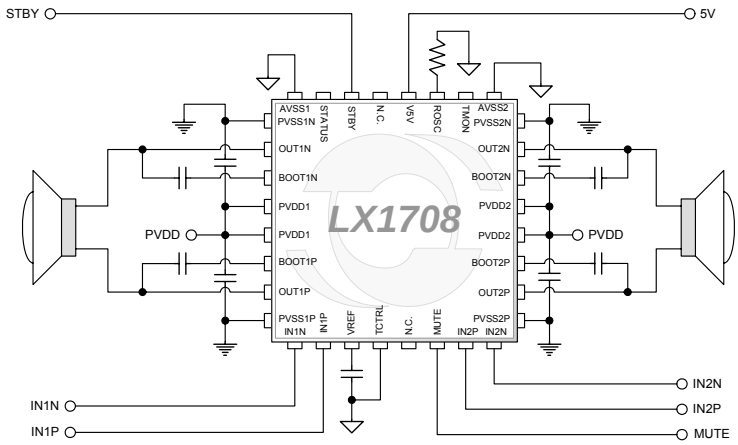
KEY FEATURES

- Filter Free Operation
- 15W +15W Output Power @ 4Ω load: THD+N < 1%
- High Efficiency > 85%
- Full Audio Bandwidth: 20Hz to 20KHz
- Low Distortion < 0.15% @ 30% Max Power, 1KHz
- High Signal-to-Noise Ratio: 90dB
- Wide Supply Voltage Range 5.0V ~ 15V
- Low Quiescent Current < 30mA
- Turn ON/OFF POP Free
- Standby / Mute Feature
- Built-in Under Voltage Lockout
- Thermal Protection
- Short Circuit Protection

APPLICATIONS

- LCD TV
- Car Navigation
- Computer:
- Portable Sound System

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)	LQ Plastic MLPQ 32-Pin 7mmx7mm RoHS Compliant / Pb-free
-40 to 85	**LX1708ILQ**

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1708ILQ-TR)

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ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (PVDD) ..... -0.3V to 16.5V
Supply Voltage (V5V) ..... -0.3 to 6V
STBY to VSS.....-0.3V to V5V + 0.3V
IN1P/M, IN2P/M .....-0.3V to V5V +0.3V
Maximum Operating Junction Temperature ..... 150°C
Storage Temperature Range.....-65°C to 150°C
Package Peak Temp. for Solder Reflow (40 seconds maximum exposure) ... 260°C (+0 -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

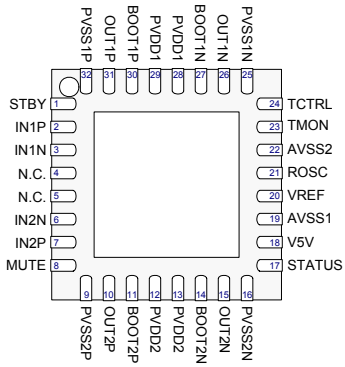
THERMAL DATA

LQ **Plastic MLPQ 32-Pin 7mm x 7mm**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	15.5°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUT



LQ PACKAGE
(Top View)

Pb-free 100% Matte Tin Lead Finish

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FUNCTIONAL PIN DESCRIPTION

Name		# Of Pins	Description
PVSS1P PVSS1N PVSS2P PVSS2N	Power Ground	4	Power Ground for the two H-bridge output drivers.
PVDD1 PVDD2	Power Supply	4	Power Supply for the two H-bridge output drivers. Operating voltage is from 4.5 up to 15V. Current draw will be up to 3.2A at 2X15W into 8ohms or up to 4.5A at 2X15W into 4 ohms. These are peak currents when the part is run at maximum rated power on both channels.
V5V	Power Supply	1	Analog Power Supply for the analog signal processing section. Operating voltage is from 4.5 up to 5.5V.
AVSS1 AVSS2	Analog Ground	2	Analog Ground for the analog signal processing section. Should be at the same voltage as PVSS. Also used to bias the substrate.
IN1N IN1P IN2N IN2P	Analog Input	4	Differential analog audio inputs for each channel. The common mode voltage will be set by the LX1708 to around 2.25V.
OUT1N OUT1P OUT2N OUT2P	Digital Output	4	Differential high power audio outputs for each channel. Each output will swing between PVDD and PVSS. These outputs are driven by an on-chip H-bridge output driver which uses low Rdson NFETs.
BOOT1N BOOT1P BOOT2N BOOT2P	Digital Output	4	Bootstrap voltage pins which provide the high voltage needed to drive the upper NFET. A bootstrap capacitor should be placed between the respective output and these pins.
VREF	Analog Output	1	2.25V reference voltage which serves as a local “GND” reference. An external compensation capacitor of at least 1uF should be connected between this pin and AVSS.
MUTE	CMOS Input	1	Logic level control which mutes the audio signal when high. This will be a four level pin to allow testing of the low gain mode as follows: From 0 to ¼ of V5V, the gain will be normal. From ¼ of V5V to ½ of V5V, the gain will be low Above ½ of V5V, the gain will be muted.
STBY	CMOS Input	1	Logic level control which places the chip into sleep mode when high. The logic threshold will be at ½ of V5V.
STATUS	CMOS Output	1	Digital monitoring pin which is used to flag internal fault states. This pin will be synchronized with the internal clock to prevent glitches. See the STATUS flag table for a summary of which conditions will force this pin to go high.
ROSC	Analog Input	1	Frequency control pin. A resistor between this pin and GND will set the oscillation frequency for the Class-D modulator.
TCTRL	CMOS Input	1	Test purpose only, Connect to AVSS1
TMON	Analog I/O	1	Test purpose only, left open.
N.C.		2	No Connect

The STATUS pin will go under any of the following conditions:

- STBY is high. This indicates that the chip is in “stand-by” mode.
- V5V is below the UVLO threshold. The outputs will be forced into the low state.
- PVDD is below the PVDD UVLO threshold. The outputs will be forced into the low state.
- PVDD is above the over-voltage threshold which is about 17.8V. The outputs will be forced into the low state.
- The die temperature is above about 140°C. This indicates that the part has gone in to gain foldback.
- A short circuit at the output has caused the output devices to shut off due to excessive temperature.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature -40°C ≤ T_A ≤ 85°C except where otherwise noted and the following test conditions: P_{VDD} = 12V, P_{VSS} = A_{VSS} = 0V, V5V = 5V, R_{OSC} = 25KΩ

Parameter	Symbol	Test Conditions	LX1708			Units
			Min	Typ	Max	
OSCILLATOR						
Oscillator Frequency	F_{OSC}	Varies with ROSC resistor value, value shown is for default conditions. R = 25K		300		KHz
Temperature Stability		T_A = 0°C to 70°C		5		%
		T_A = -40°C to 125°C		8		%
POWER SUPPLY						
Supply Voltage	PVDD		5.0	12	15	V
UVLO	PVDD	Start-up Voltage		4.50	4.90	V
UVLO Hysteresis	PVDD			500		mV
+5V Supply	V5V		4.5		5.5	V
UVLO	V5V	Start-up Voltage		4.25	4.50	V
UVLO Hysteresis	V5V			250		mV
Stand-By Current	I_{QQ}	For PVDD, STBY high		10	50	µA
Operating Current	I_{QQ}	For PVDD, STBY low, Mute high		10	30	mA
Stand-By Current	I_{QQ}5V5	For 5V5, STBY high		10		µA
Operating Current	IQQ5V5	For 5V5, STBY low, Mute high		7	15	mA
Power Supply Rejection Ratio	PSRR	For PVDD	55			dB
Reference Voltage[1]	VREF	C bypass = 1µF		2.25		V
GAIN						
Stage Gain @ 0dB Volume	G	f = 1KHz		20		V/V
Mute Gain @ minimum volume	G_{MUTE}	Mute active, Input shorted		0.01		V/V
OFFSET						
Output DC Offset	V_{OFF}	Measured Differentially. OUT1- to OUT1+ OUT2- to OUT2+		100		mV
INPUT STAGE						
Input Resistance	R_{IN}			22		KΩ
Common Mode Voltage	V_{CM}			2.25		V
OUTPUT STAGE						
MOSFET On Resistance	R_{DSON}	IDS = 200mA		280		mΩ
THERMAL						
Thermal Shut Off Junction Temperature				150		°C
Hystersis				25		°C
MUTE / STBY / MASTER						
MUTE Threshold		Mute Mode		V5V/2		V
STBY Threshold				V5V/2		V
STBY To Output Enable		After Power on Reset Pulse, Not Quick Mode		16384		Clocks
Power On Reset Delay			0.20	0.30	3.8	mS

Note 1: Not ATE Tested

Note: Functionality over the -40°C to +85°C operating range is assured by design characterization and correlation.

Caution: Power Up/Down Sequencing

Power-on: Apply V5V w/STBY=V5V. Then apply PVDD. Then bring STBY low.

Power-off: Bring STBY high such that STBY=V5V. Then shut off PVDD. Then shut off V5V.

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SYSTEM MODULE CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature -40°C ≤ TA ≤ 85°C except where otherwise noted and the following test conditions: P_{VDD} = 12V, P_{VSS} = A_{VSS} = 0V, V5V = 5V, R_{OSC} = 25KΩ, R_L = 4Ω.

Parameter		Symbol	Test Conditions	LX1708 Min	LX1708 Typ	LX1708 Max	Units
AUDIO CHARACTERISTICS							
Output Power Stereo		P_O	THD+N < 1%		12		W
			THD+N <10%		15		
Total Harmonic Distortion Stereo		THD+N	P_{OUT} = 50% of Maximum Power, FIN = 1KHz with diodes		0.2		%
			P_{OUT} = 50% of Maximum Power, FIN = 1KHz No diodes		0.7		
			P_{OUT} = 1W, FIN = 20Hz~20KHz		0.4		
Power Efficiency			P_{OUT} = Max, THD+N < 1%		90		%
Channel Crosstalk		V_{XTALK}	P_{OUT} = 1W, F = 1KHz		-60		dB
Audio Bandwidth		BW	P_{OUT} = 1W, F = 20-20KHz			3	dB
Stage Gain Stereo	High		V_{IN} = 200mV_{RMS}, F = 20Hz~20KHz		20		V/V
	Low		V_{IN} = 2V_{RMS}, F = 20Hz~20Khz		0.01		
Mute Output		V_{MUTE}	Input short, system muted, stereo		-60		dB
Signal to Noise Ratio		SNR	FIN = 1KHz @ 20Hz-20KHz non A-weighted		90		dB
Output Noise Floor		V_N	Input short, non A-weighted @ 20Hz-20KHz		200		μV_{RMS}
Common Mode Rejection Ratio		CMRR		55			dB
Output Short Circuit Protection		T_{SENSE}	Thermal Shutdown Mode		150		°C

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SIMPLIFIED BLOCK DIAGRAM

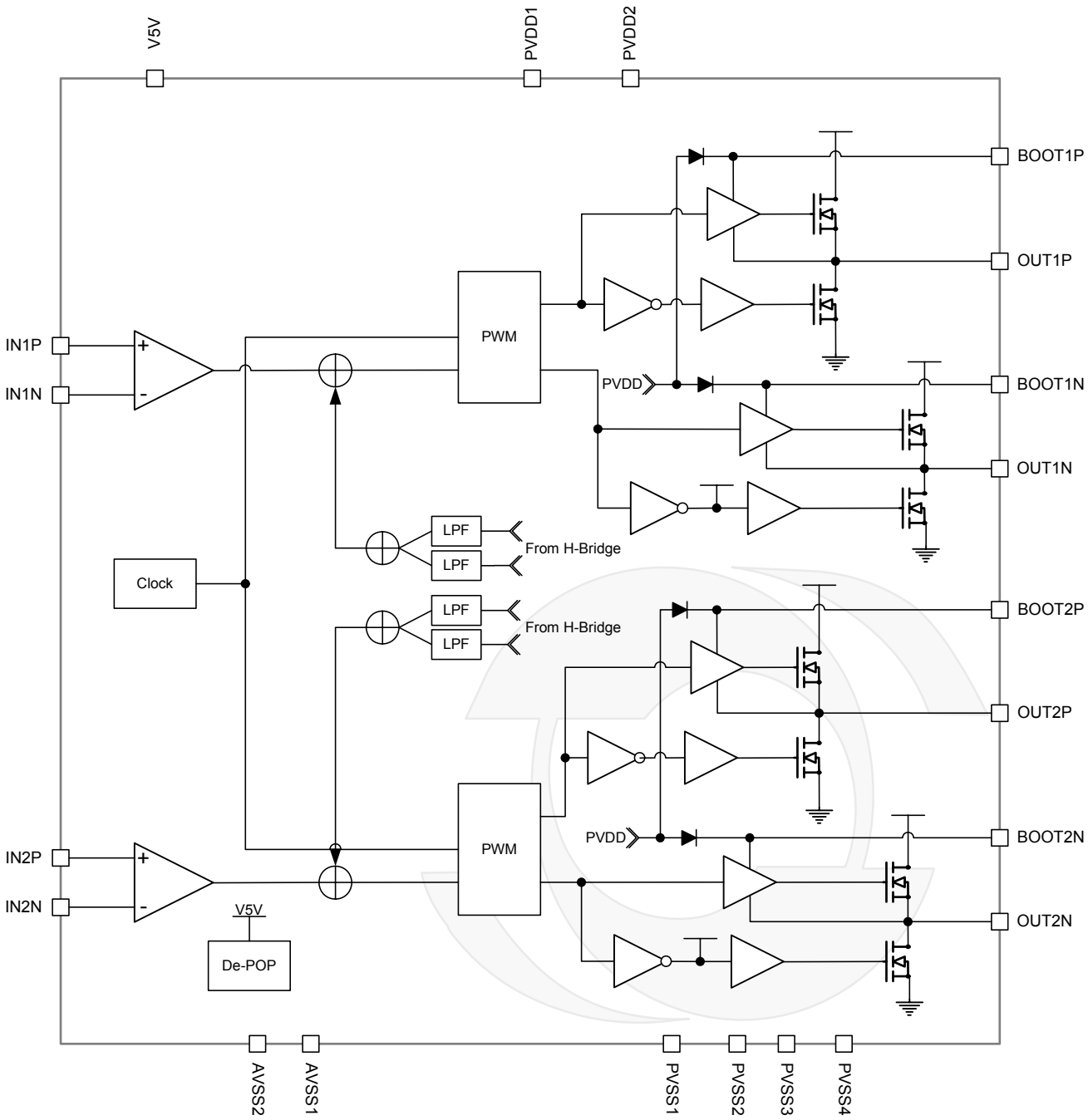


Figure 1 – Simplified Block Diagram

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TEST SYSTEM SET-UP

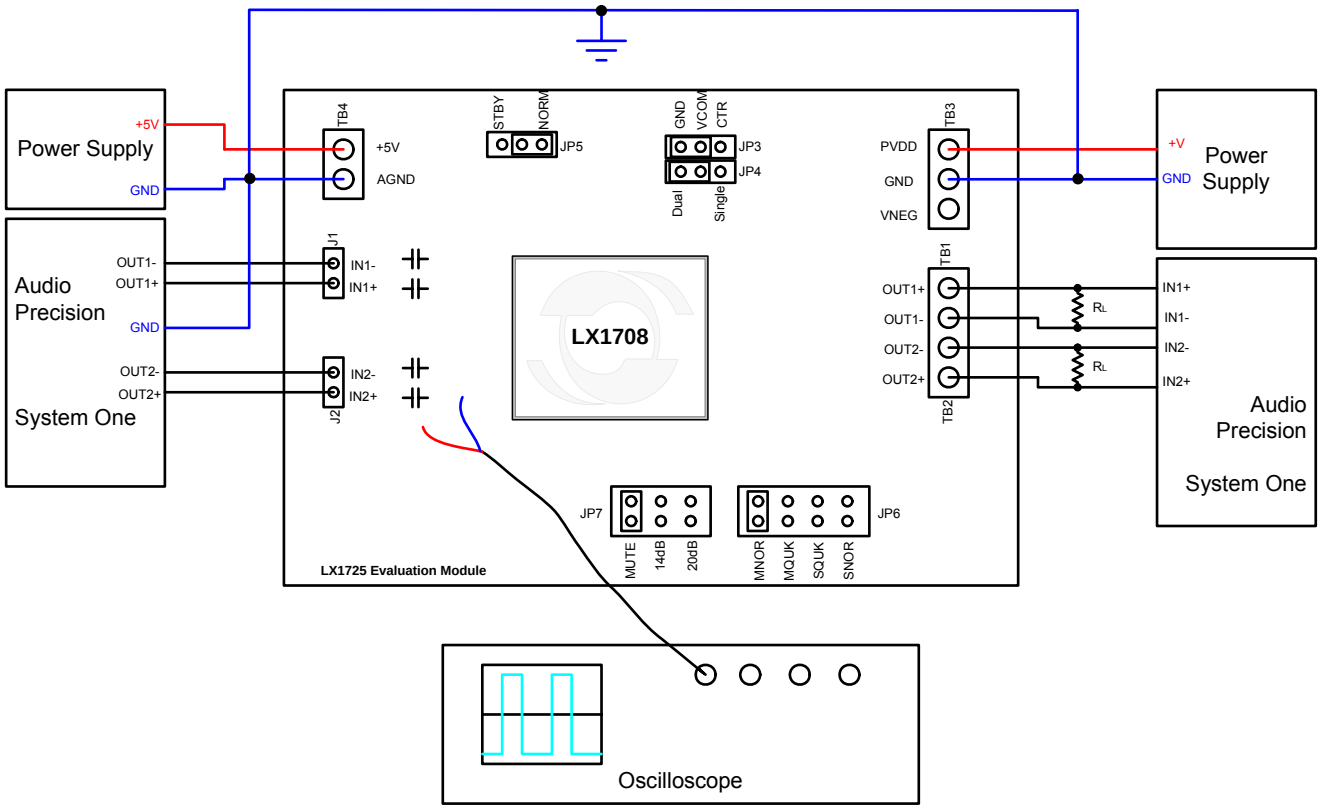
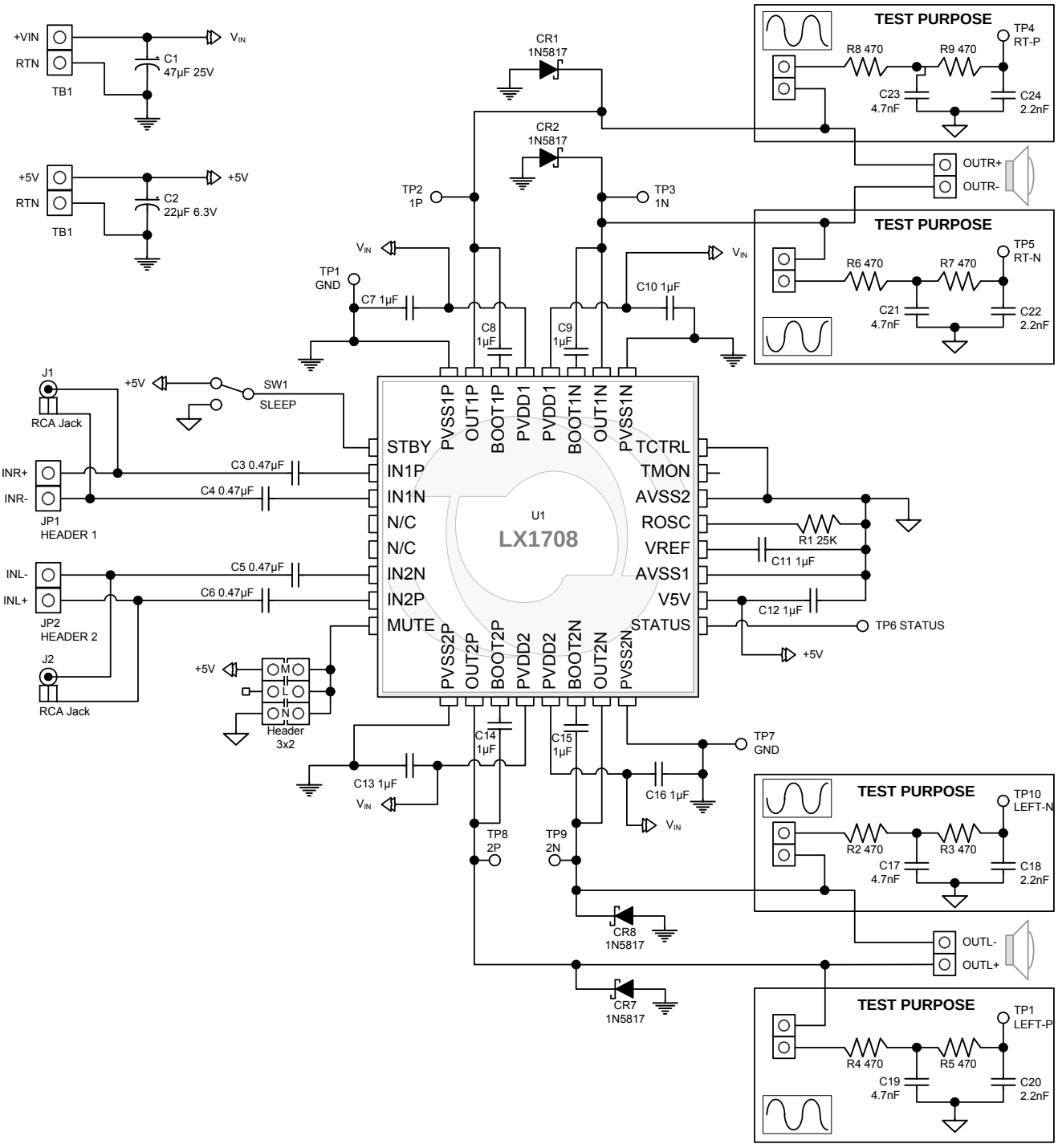


Figure 2 – System Test Set-up Diagram

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APPLICATION CIRCUITS



Note 1: CR1, CR2, CR7, CR8 can be used for lower distortion performance.

Figure 3 – Typical Application

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FUNCTIONAL DESCRIPTION

FILTERLESS CLASS-D MODULATION

The LX1708 drives each output between PVDD and PVSS using an all-NFET, bootstrapped, H-bridge driver for each channel. High efficiency is obtained by forcing all transistors to operate either completely on or completely off as required for a true class-D amplifier. The entire signal path from input to output is differential to reject any sources of common-mode noise or distortion. Even the triangle wave operates differentially. Filterless class-D modulation operates such that with no input signal, the outputs switch at 300KHz and are in-phase with each other. Because the two signals are identical, the differential signal to the speaker is zero. As a direct result, there is no requirement for a low-pass LC filter to present a high impedance at the modulation frequency. This allows a cheaper and simpler audio amplifier to be designed . As the input signal goes positive, the duty cycle to the positive output increases while the duty cycle of the negative output decreases. This produces a net positive current flow into the load. A negative signal reduces the positive output duty cycles and increases the negative output duty cycle. The differential signal actually appears at twice the modulation frequency and alternates between +PVDD, 0, and –PVDD which allows the parasitic inductance of the load to effectively filter the switching signal so that only the audio band portion remains.

Because each speaker is driven by an in-phase signal, the common mode voltage to the speaker switches at the full PVDD amplitude at 300KHz. This is a possible source of EMI radiation. Typically, a ferrite bead is placed with a small common-mode filter capacitor to reduce EMI generation by filtering the edges of the output signals.

NOISE-FREE TURN-ON AND OFF

Noise-free turn-on and off is accomplished by carefully sequencing the signal path when the amplifier is enabled or disabled. Prior to turn-on, the outputs are initially both at PVSS so there is no differential signal. The internal error amplifier is held in a reset condition so that the internal loop compensation components are “ready to go”. When the outputs begin to toggle, the audio signal path is muted for about 1.6mS. Following that time, the internal mute signal is de-asserted and the audio input signal is allowed to drive the pulse-width–modulator which then adjusts the output duty cycle as necessary to drive the speaker. At turn-off, the internal mute signal is asserted to silence the input audio signal. The outputs continue switching in this muted condition for about 0.6mS prior to being pulled low. Once the outputs are forced low, the error amplifier is reset so that the part is ready to being a new power-up sequence. This scheme basically limits the pop noise at turn-on or off to be no larger than the differential offset voltage of the error amplifier.

AC-COUPLING AND BOOTSTRAP CAPACITORS

Input AC-coupling capacitors should be used to block any input DC and low frequency components below the desired low frequency corner. Since the input resistance to the LX1708 is 25Kohms, a 20Hz low frequency corner can be achieved with a 0.32µF AC-coupling capacitor. 1µF bootstrap capacitors are required at each output to supply the gate drive voltage for the upper level NFET in each half-bridge.

THERMAL OVERLOAD PROTECTION

The LX1708 protects itself by monitoring its operating temperature in two different ways. A general thermal protection scheme monitors the overall die temperature. Above 140°C, the amplifier gain is reduced by 6dB so that the audio signal is still amplified, but the on-chip power dissipation is halved. When the die temperature then goes below 110°C, the amplifier gain is restored. Above 150°C, the LX1708 forces all outputs to PVSS so that no power is dissipated until the chip cools down to 110°C.

A dynamic thermal protection scheme operates by placing temperature sensors near each of the output devices. When a differential temperature rise of about 60°C occurs above the core die temperature, which indicates a local short circuit condition, the outputs are disabled to protect the part. This provides short circuit protection for differential shorts and shorts to ground. Since the outputs go low to PVSS, shorts to PVDD are NOT protected.

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APPLICATION NOTE/PCB DESIGN GUIDLINE

OSCILLATOR

The value of R1 decides the switching frequency, smaller value gives the system faster switching. See Figure 4, SW Frequency vs. R1

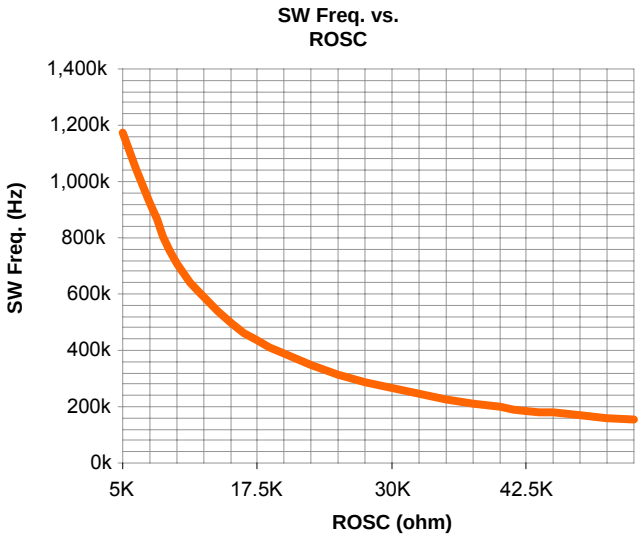


Figure 4 – SW Frequency vs. R1

BOOTSTRAP CAPACITORS

C8, C9, C14, and C15 are bootstrap capacitors for internal NMOSFETs gate drive voltage, they work together with internal diodes to boost the PVDD voltage doubled, over the threshold voltage of VGS. If BOOT1P, BOOT1N, BOOT2P, and BOOT2N are probed, 2x PVDD voltages on the PWM waveform will be observed. Those capacitors should be placed as close to the IC as possible.

BYPASSING CAPACITORS

C7, C10, C11, C12, C13, and C16 are bypassing capacitors for input supplies and internal reference voltage (2.5V), nominal value is 1µF. These capacitors should be placed as close to the IC as possible also, to guarantee low ripples and noise.

PCB DESIGN GUIDELINES

One of the key efforts in implementing the MLP package on a pc board is the design of the land pattern. The MLP has rectangular metallized terminals exposed on the bottom surface of the package body. Electrical and mechanical connection between the component and the pc board is made by screen printing solder paste on the pc board and then reflowing the paste after placement. To guarantee reliable solder joints it is essential to design the land pattern to the MLP terminal pattern, exposed PAD, and Thermal PAD via. There are two basic designs for PCB land pads for the MLP: Copper Defined style (also known as Non Solder Mask Defined (NSMD)) and the Solder Mask Defined style (SMD). The industry has had some debate on the merits of both styles and although Microsemi recommends the Copper Defined style land pad (NSMD). Both styles are acceptable for use with the MLP package. NSMD pads are recommended over SMD pads due to the tighter tolerance on copper etching than solder masking. NSDM by definition also provides a larger copper pad area and allows the solder to anchor to the edges of the copper pads thus providing improved solder joint reliability.

EXPOSED PAD PCB DESIGN

The construction of the Exposed Pad MLP enables enhanced thermal and electrical characteristics. In order to take full advantage of this feature the exposed pad must be physically connected to the PCB substrate with solder. The exposed pad is internally connected to the die substrate potential which is VNEG so it is very important that the PCB substrate potential be connected to VNEG as well.

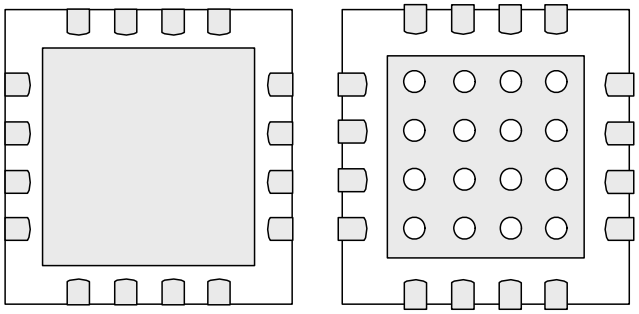
The thermal pad (D2th) should be greater than D2 of the MLP whenever possible; however adequate clearance (Cpl > 0.15mm) must be met to prevent solder bridging. If this clearance cannot be met, then D2th should be reduced in area. The formula would be: D2TH > D2 only if D2TH < Gmin – (2 x Cpl).

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APPLICATION NOTE/PCB DESIGN GUIDLINE (CONTINUED)

THERMAL PAD VIA DESIGN

There are two types of on-board thermal PAD designs: one is using thermal vias to sink the heat to the other layer with metal traces. Based on the Jedec Specification (JESD 51-5) the thermal vias should be designed like Figure 5. Another one is the no via thermal PAD which is using the same copper PAD as heat sink, this type of thermal PAD is good for a two layer board, since the bottom side is filled with all other kinds of trace also, it's hard to use the whole plane for the heat sink. But you still can use vias to sink the heat to the bottom layer by the metal traces, then layout a NMSD on which a metal heat sink is put to sink the heat to the air.



Micro Lead Quad Package Land Pattern | Land Pattern for Four Layer Board with Vias

Figure 5 – Comparison of land pattern theory

The LX1708 is supplied in an MLPQ – 7mm x 7mm, 32 pin package. θ_{JA} = 15.5°C/W for the package by itself in still air. When running at a continuous 20W output power, the on-chip power dissipation will be 3.5W assuming 85% efficiency. With no reduction in the thermal resistance, the die temperature will rise 103 about ambient. θ_{JC} is about 4° C/W. if the exposed pad is properly connected to a heat sink, then the temperature rise will be reduced to around 16°C under these conditions. So the via type thermal PAD is suggested.

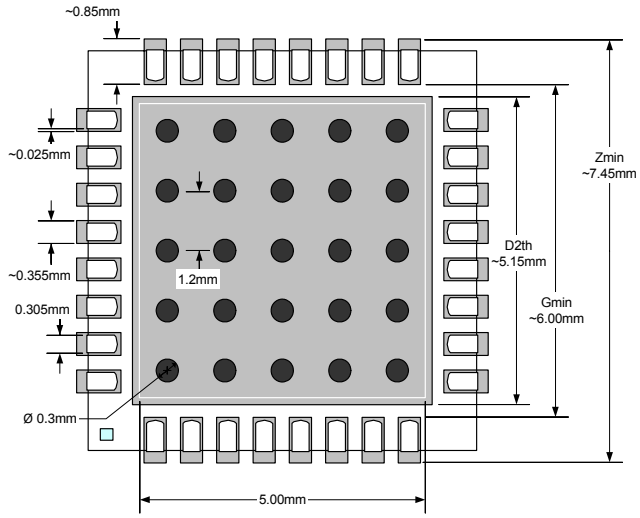


Figure 6 – Recommended Land Pad with Vias for LQ32 ($7mm^2$)

Zmin=D + aaa+ 2(0.2)
(where pkg body tolerance aaa=0.15)
(where 0.2 is outer pad extension)
Gmin=D-2(Lmax)-2(0.05)
(where 0.05 is inner pad extension)
(Lmax=0.05 for this example)
D2th max = Gmin-2(CpL)
(where CpL=0.2)

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PRINTED CIRCUIT BOARD FOR THE LXE1708

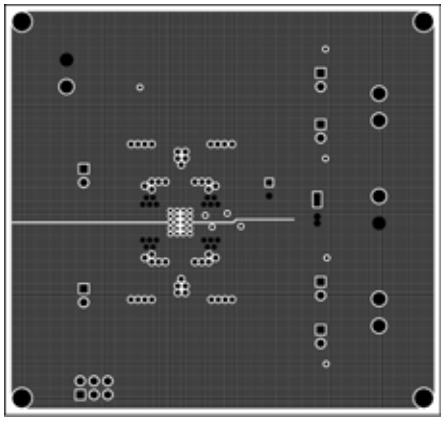


Figure 7 – Inner Layer 1

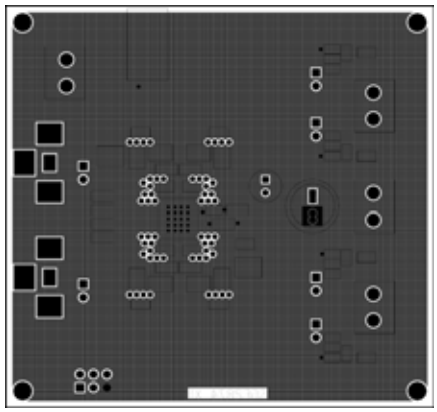


Figure 8 – Bottom Layer

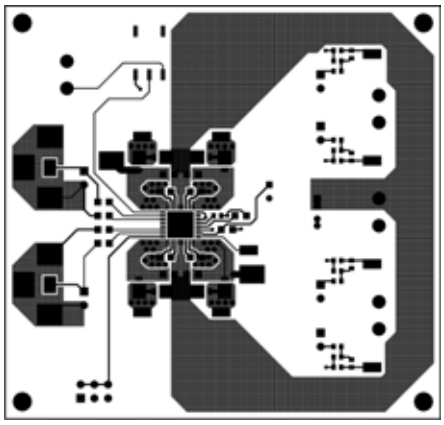


Figure 9 – Top Layer

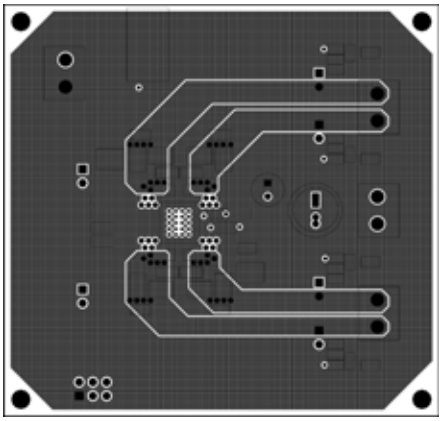


Figure 10 – Inner Layer 2

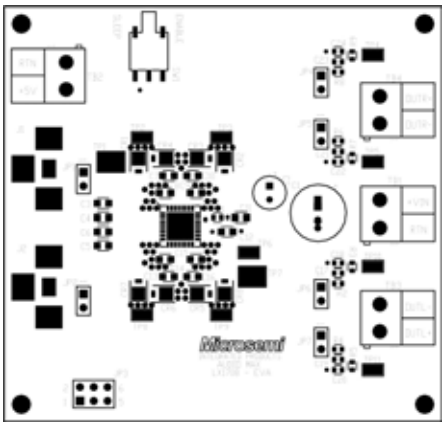


Figure 11 – Top Component Layer

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LX1708 EVAL KIT BILL OF MATERIALS

MISCELLANEOUS COMPONENTS

Line Item	Part Description	Manufacturer & Part #		Case	Reference Designators	Qty
1	Microsemi IC Controller LX1708 Class-D Audio Amplifier	MICROSEMI	LX1708ILQ	MLPQ-32	U1	1
2	Diode, Schottky	MICROSEMI	UPS5817	Powermite	CR1, CR2, CR7, CR8	N/U
3	Jack, PCB Mount, RCA	KEYSTONE	901		J1, J2	2
4	Header, 2 Position Vertical	3M	929450-01-02-1		JP1 – JP7	6
5	Header, 3 Position, 2 Row Vertical 0.1" Centers	3M			JP3	1
6	Switch, SPDT, PCB Mount Subminiature	C&K	GT11MSAKE		SW1	1
7	Terminal Block, 2 Position	BLOCKMASTER	301-021-1000		TB1, TB2, TB3, TB4	4
8	Terminal, Compact, Test Point	KEYSTONE	5016	SMT	TP1, TP7	2
9	Terminal, Subminiature,	KEYSTONE	5015	SMT	TP2, TP3, TP4, TP5, TP6, TP8, TP9, TP10, TP11	9
10	PCB, LX1708 Evaluation Board	MICROSEMI	SGE2874-X1			

CAPACITORS

Line Item	Part Description	Manufacturer & Part #		Case	Reference Designators	Qty
11	Capacitor, Elect., 47µF, 35V, 20%, KS Type	PANASONIC	ECEA1VKS470i	Thru	C1	1
12	Capacitor, Elect., 22µF, 10V, 20%, KS Type	PANASONIC	ECEA1AkS220i	Thru	C2	1
13	Capacitor, Ceramic, .47µF, 16V, 10%	PANASONIC	ECJ2YB1C474K	0805	C3, C4, C5, C6	4
14	Capacitor, Ceramic, X5R, 1µF, 25V, 10%,	PANASONIC	ECJ-2FB1E105K	0805	C7, C8, C9, C10, C11, C12, C13, C14, C15, C16	10
15	Capacitor, Ceramic, 4700pF, 50V, 10%,	PANASONIC	ECJ-1VB1H472K	0603	C17, C19, C21, C23	4
16	Capacitor, Ceramic, 2200pF, 50V, 10%	PANASONIC	ECJ-1VB1H222K	0603	C18, C20, C22, C24	4

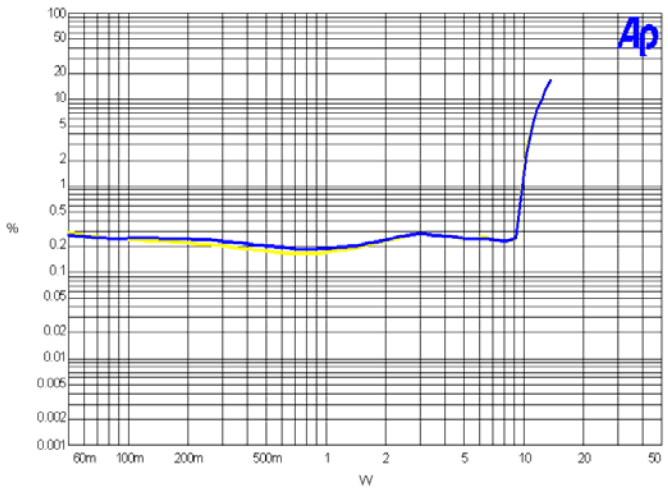
RESISTORS

Line Item	Part Description	Manufacturer & Part #		Case	Reference Designators	Qty
17	Resistor, 25.5K Ohm, 1/10W, 1%	PANASONIC	ERJ3EKF2552V	0603	R1	1
18	Resistor 470 Ohm, 1/10W, 5%	PANASONIC	ERJ3GSYJ471	0603	R2, R3, R4, R5, R6, R7, R8, R9	8

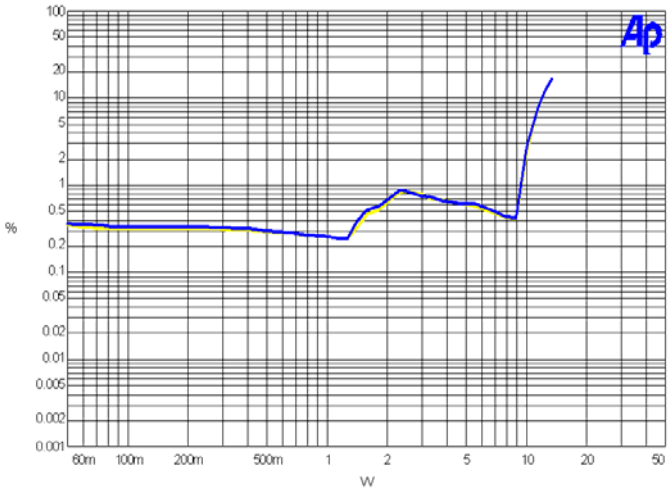
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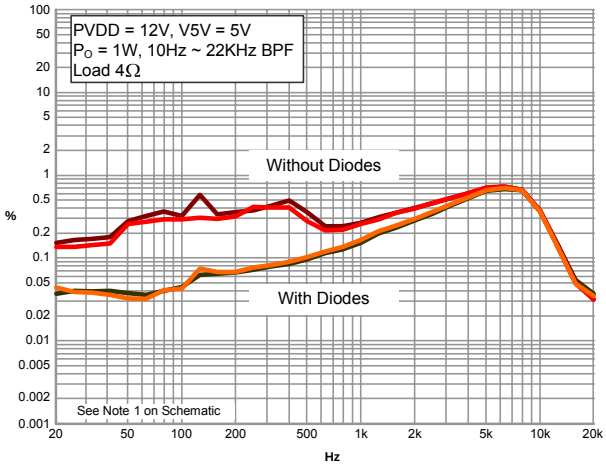
THD VS PWR @ 4 OHM WITH DIODES



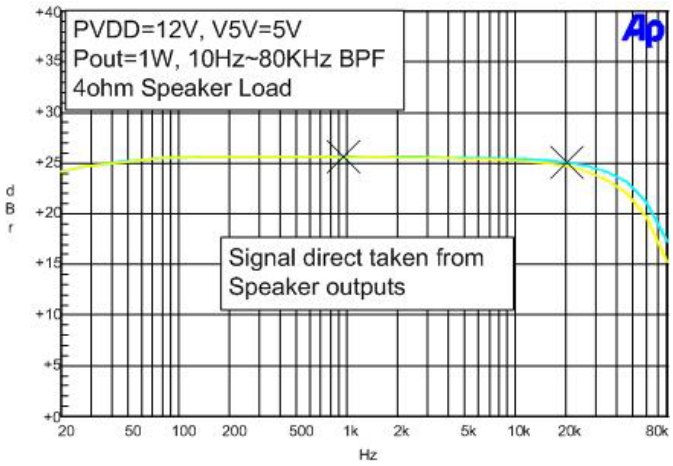
THD VS PWR @ 4 OHM NO DIODES



THD+N VS. FREQUENCY



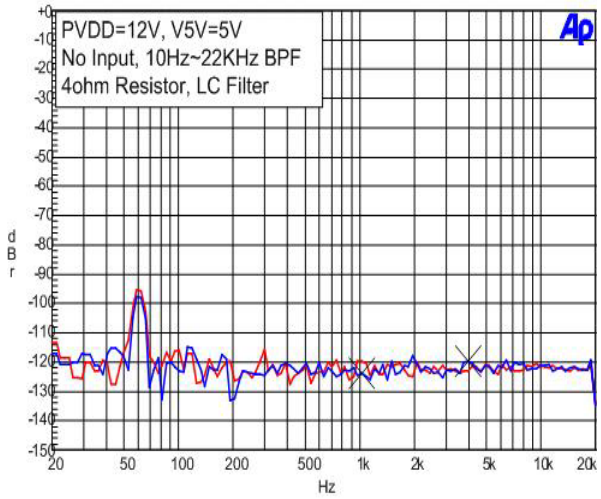
GAIN RESPONSE



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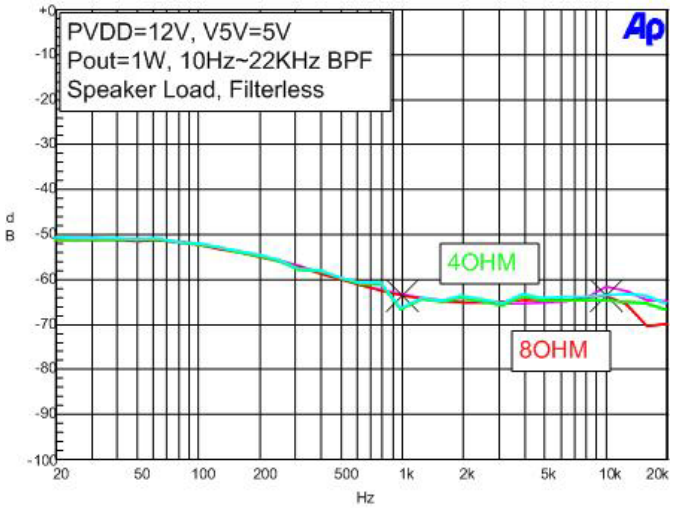
NOISE FLOOR & SIGNAL-TO-NOISE RATIO



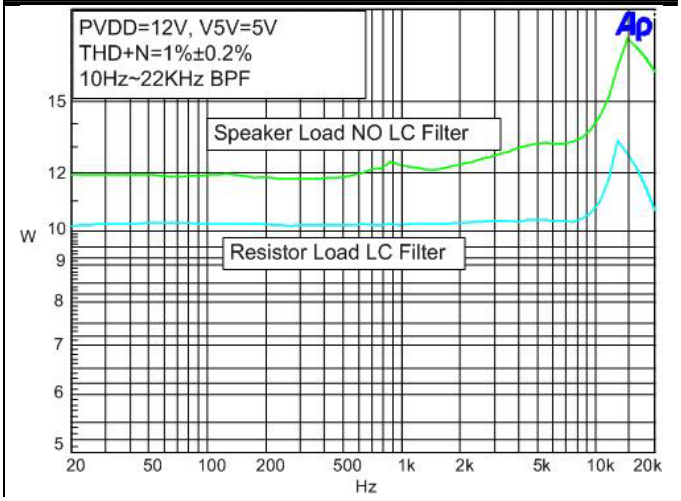
Noise Floor w/out A-Weighted:
245uVrms, -89.2dB @0dB=7Vrms (12W, THD+N<1%)

Noise Floor w/ A-Weighted:
125uVrms, -95dB @0dB=7Vrms (12W, THD+N<1%)

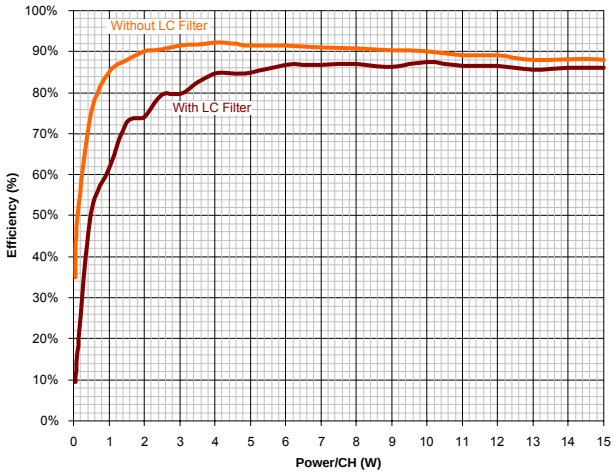
CHANNEL CROSSTALK



OUTPUT POWER BANDWIDTH @ 1% THD



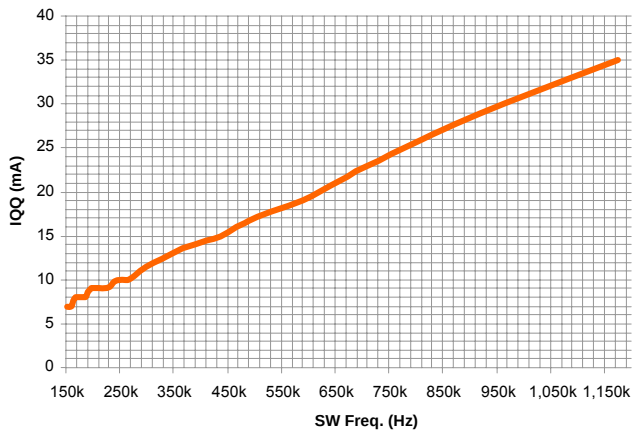
EFFICIENCY @ 4 OHM LOAD



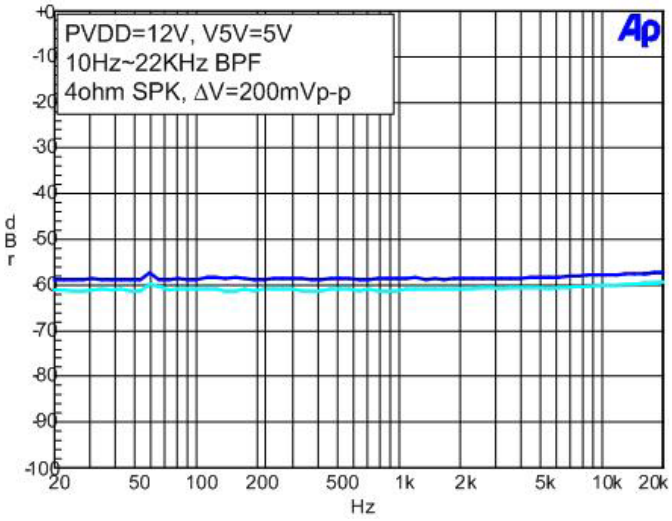
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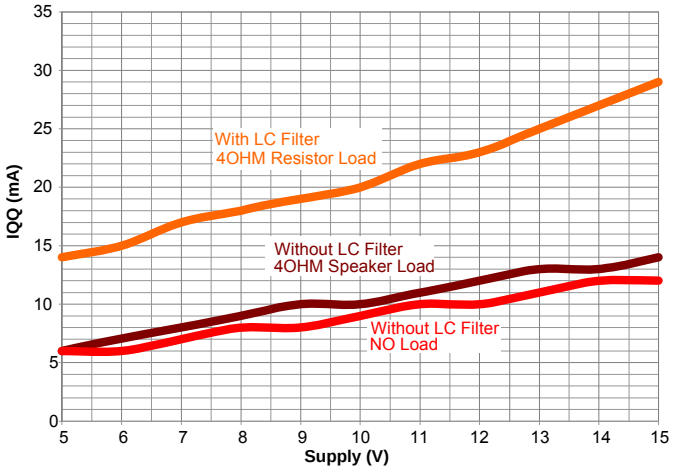
IQQ VS. FREQUENCY



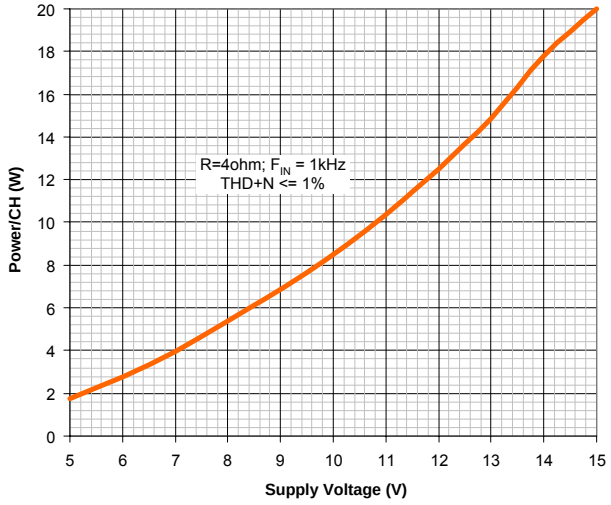
PSRR (AC)



IQQ VS. SUPPLY



POWER VS. SUPPLY VOLTAGE

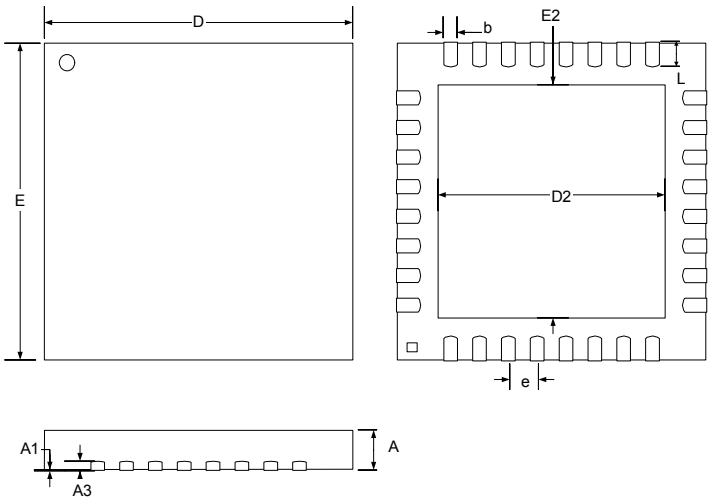


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PACKAGE DIMENSIONS

LQ 32-Pin MLPQ Plastic (7x7mm EP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.25 REF		0.010	
b	0.23	0.38	0.009	0.015
D	7.00 BSC		0.276 BSC	
D2	5.00	5.25	0.197	0.207
E	7.00 BSC		0.276 BSC	
E2	5.00	5.25	0.197	0.207
e	0.65 BSC		0.026	
L	0.45	0.65	0.018	0.026

Note:
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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