10 MHz, 20 V/µs, G = 1, 10, 100, 1000 *i*CMOS Programmable Gain Instrumentation Amplifier

Data Sheet **AD8253**

FEATURES

Small package: 10-lead MSOP
Programmable gains: 1, 10, 100, 1000
Digital or pin-programmable gain setting
Wide supply: ±5 V to ±15 V
Excellent dc performance
- **High CMRR: 100 dB (minimum), G = 100**
- **Low gain drift: 10 ppm/°C (maximum)**
- **Low offset drift: 1.2 µV/°C (maximum), G = 1000**

Excellent ac performance
- **Fast settling time: 780 ns to 0.001% (maximum)**
- **High slew rate: 20 V/µs (minimum)**
- **Low distortion: −110 dB THD at 1 kHz,10 V swing**
- **High CMRR over frequency: 100 dB to 20 kHz (minimum)**
- **Low noise: 10 nV/√Hz, G = 1000 (maximum)**
- **Low power: 4 mA**

APPLICATIONS

Data acquisition
Biomedical analysis
Test and measurement

GENERAL DESCRIPTION

The AD8253 is an instrumentation amplifier with digitally programmable gains that has gigaohm (GΩ) input impedance, low output noise, and low distortion, making it suitable for interfacing with sensors and driving high sample rate analog-to-digital converters (ADCs).

It has a high bandwidth of 10 MHz, low THD of −110 dB, and fast settling time of 780 ns (maximum) to 0.001%. Offset drift and gain drift are guaranteed to 1.2 µV/°C and 10 ppm/°C, respectively, for G = 1000. In addition to its wide input common voltage range, it boasts a high common-mode rejection of 100 dB at G = 1000 from dc to 20 kHz. The combination of precision dc performance coupled with high speed capabilities makes the AD8253 an excellent candidate for data acquisition. Furthermore, this monolithic solution simplifies design and manufacturing and boosts performance of instrumentation by maintaining a tight match of internal resistors and amplifiers.

The AD8253 user interface consists of a parallel port that allows users to set the gain in one of two different ways (see Figure 1 for the functional block diagram). A 2-bit word sent via a bus can be latched using the $\overline{WR}$ input. An alternative is to use transparent gain mode, where the state of logic levels at the gain port determines the gain.

FUNCTIONAL BLOCK DIAGRAM

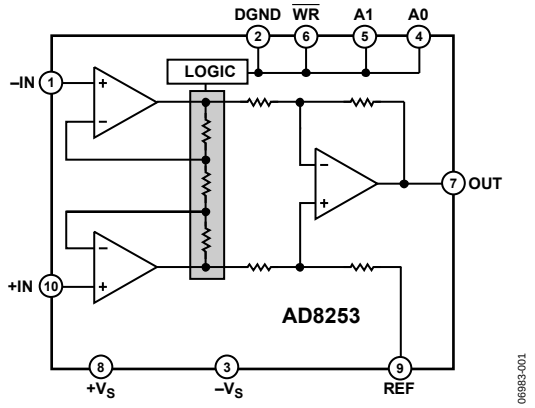


Figure 1.

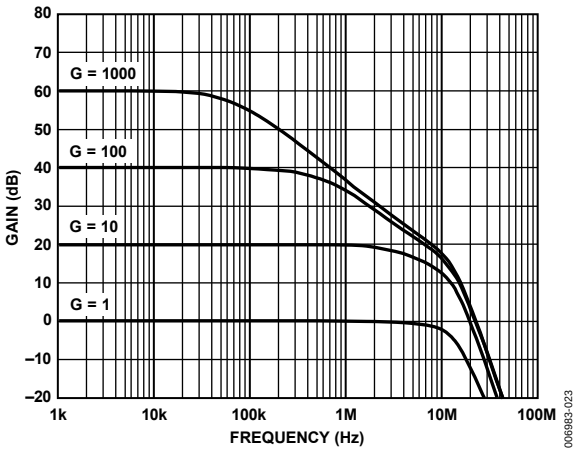


Figure 2. Gain vs. Frequency

Table 1. Instrumentation Amplifiers by Category

General Purpose	Zero Drift	Mil Grade	Low Power	High Speed PGA
AD8220[1]	AD8231[1]	AD620	AD627[1]	AD8250
AD8221	AD8553[1]	AD621	AD623[1]	AD8251
AD8222	AD8555[1]	AD524	AD8223[1]	AD8253
AD8224[1]	AD8556[1]	AD526		
AD8228	AD8557[1]	AD624		

[1] Rail-to-rail output.

The AD8253 is available in a 10-lead MSOP package and is specified over the −40°C to +85°C temperature range, making it an excellent solution for applications where size and packing density are important considerations.

Rev. B **Document Feedback**
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REVISION HISTORY

10/12—Rev. A to Rev. B

Changed Digital Input Voltage Low Maximum Parameter from 1.2 V to 2.1 V and Changed Digital Input Voltage High Typical Parameter from 1.5 V to 2.8 V ... 4
Updated Outline Dimensions ... 23

8/08—Rev. 0 to Rev. A

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7/08—Revision 0: Initial Version

SPECIFICATIONS

$+V_S$ = +15 V, $-V_S$ = −15 V, V_{REF} = 0 V @ T_A = 25°C, G = 1, R_L = 2 kΩ, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR to 60 Hz with 1 kΩ Source Imbalance	+IN = −IN = −10 V to +10 V				
G = 1		80	100		dB
G = 10		96	120		dB
G = 100		100	120		dB
G = 1000		100	120		dB
CMRR to 20 kHz[1]	+IN = −IN = −10 V to +10 V				
G = 1		80			dB
G = 10		96			dB
G = 100		100			dB
G = 1000		100			dB
NOISE					
Voltage Noise, 1 kHz, RTI					
G = 1				45	nV/√Hz
G = 10				12	nV/√Hz
G = 100				11	nV/√Hz
G = 1000				10	nV/√Hz
0.1 Hz to 10 Hz, RTI					
G = 1				2.5	µV p-p
G = 10				1	µV p-p
G = 100				0.5	µV p-p
G = 1000				0.5	µV p-p
Current Noise, 1 kHz			5		pA/√Hz
Current Noise, 0.1 Hz to 10 Hz			60		pA p-p
VOLTAGE OFFSET					
Offset RTI V_{OS}	G = 1, 10, 100, 1000			±150 + 900/G	µV
Over Temperature	T = −40°C to +85°C			±210 + 900/G	µV
Average TC	T = −40°C to +85°C			±1.2 + 5/G	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±5 V to ±15 V			±5 + 25/G	µV/V
INPUT CURRENT					
Input Bias Current			5	50	nA
Over Temperature[2]	T = −40°C to +85°C	40		60	nA
Average TC	T = −40°C to +85°C			400	pA/°C
Input Offset Current			5	40	nA
Over Temperature	T = −40°C to +85°C			40	nA
Average TC	T = −40°C to +85°C			160	pA/°C
DYNAMIC RESPONSE					
Small-Signal −3 dB Bandwidth					
G = 1		10			MHz
G = 10		4			MHz
G = 100		550			kHz
G = 1000		60			kHz
Settling Time 0.01%	ΔOUT = 10 V step				
G = 1				700	ns
G = 10				680	ns
G = 100				1.5	µs
G = 1000				14	µs

Parameter	Conditions	Min	Typ	Max	Unit
Settling Time 0.001%	ΔOUT = 10 V step				
G = 1				780	ns
G = 10				880	ns
G =100				1.8	µs
G = 1000				1.8	µs
Slew Rate					
G = 1		20			V/µs
G = 10		20			V/µs
G = 100		12			V/µs
G = 1000		2			V/µs
Total Harmonic Distortion + Noise	f = 1 kHz, R_L = 10 kΩ, ±10 V, G = 1, 10 Hz to 22 kHz band-pass filter		−110		dB
GAIN					
Gain Range	G = 1, 10, 100, 1000	1		1000	V/V
Gain Error	OUT = ±10 V				
G = 1				0.03	%
G = 10, 100, 1000				0.04	%
Gain Nonlinearity	OUT = −10 V to +10 V				
G = 1	R_L = 10 kΩ, 2 kΩ, 600 Ω			5	ppm
G = 10	R_L = 10 kΩ, 2 kΩ, 600 Ω			3	ppm
G = 100	R_L = 10 kΩ, 2 kΩ, 600 Ω			18	ppm
G = 1000	R_L = 10 kΩ, 2 kΩ, 600 Ω			110	ppm
Gain vs. Temperature	All gains		3	10	ppm/°C
INPUT					
Input Impedance					
Differential			4‖1.25		GΩ‖pF
Common Mode			1‖5		GΩ‖pF
Input Operating Voltage Range	V_S = ±5 V to ±15 V	$-V_S$ + 1		$+V_S$ − 1.5	V
Over Temperature[3]	T = −40°C to +85°C	$-V_S$ + 1.2		$+V_S$ − 1.7	V
OUTPUT					
Output Swing		−13.7		+13.6	V
Over Temperature[4]	T = −40°C to +85°C	−13.7		+13.6	V
Short-Circuit Current			37		mA
REFERENCE INPUT					
R_{IN}			20		kΩ
I_{IN}	+IN, −IN, REF = 0			1	µA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output			1 ± 0.0001		V/V
DIGITAL LOGIC					
Digital Ground Voltage, DGND	Referred to GND	$-V_S$ + 4.25	0	$+V_S$ − 2.7	V
Digital Input Voltage Low	Referred to GND	DGND		2.1	V
Digital Input Voltage High	Referred to GND	2.8		$+V_S$	V
Digital Input Current			1		µA
Gain Switching Time[5]				325	ns
t_{SU}	See Figure 3 timing diagram	15			ns
t_{HD}		30			ns
$t_{\overline{WR}\text{-LOW}}$		20			ns
$t_{\overline{WR}\text{-HIGH}}$		15			ns

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		±5		±15	V
Quiescent Current, $+I_S$			4.6	5.3	mA
Quiescent Current, $-I_S$			4.5	5.3	mA
Over Temperature	T = −40°C to +85°C			6	mA
TEMPERATURE RANGE					
Specified Performance		−40		+85	°C

[1] See Figure 20 for CMRR vs. frequency for more information on typical performance over frequency.
[2] Input bias current over temperature: minimum at hot and maximum at cold.
[3] See Figure 30 for input voltage limit vs. supply voltage and temperature.
[4] See Figure 32, Figure 33, and Figure 34 for output voltage swing vs. supply voltage and temperature for various loads.
[5] Add time for the output to slew and settle to calculate the total time for a gain change.

TIMING DIAGRAM

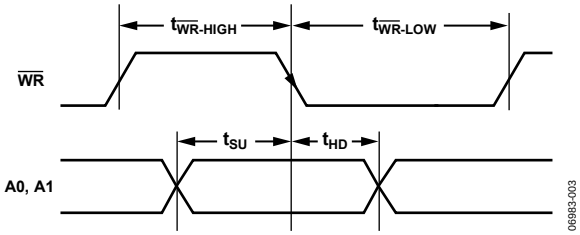


Figure 3. Timing Diagram for Latched Gain Mode (See the Timing for Latched Gain Mode Section)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±17 V
Power Dissipation	See Figure 4
Output Short-Circuit Current	Indefinite[1]
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Digital Logic Inputs	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range[2]	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	140°C
θ_{JA} (4-Layer JEDEC Standard Board)	112°C/W
Package Glass Transition Temperature	140°C

[1] Assumes the load is referenced to midsupply.
[2] Temperature for specified performance is −40°C to +85°C. For performance to +125°C, see the Typical Performance Characteristics section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8253 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 140°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8253. Exceeding a junction temperature of 140°C for an extended period can result in changes in silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), the ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature is calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some of which is dissipated in the load ($V_{OUT} \times I_{OUT}$).

The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, the worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces through holes, ground, and power planes reduces the θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature on a 4-layer JEDEC standard board.

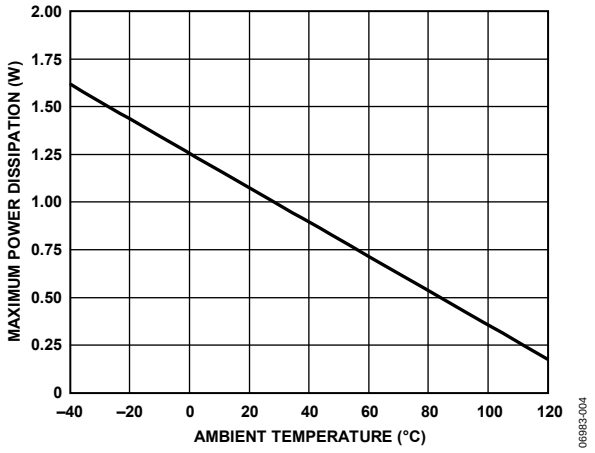


Figure 4. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

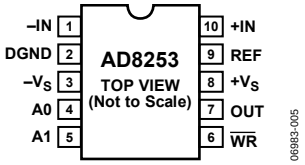


Figure 5. 10-Lead MSOP (RM-10) Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Inverting Input Terminal. True differential input.
2	DGND	Digital Ground.
3	$-V_S$	Negative Supply Terminal.
4	A0	Gain Setting Pin (LSB).
5	A1	Gain Setting Pin (MSB).
6	$\overline{WR}$	Write Enable.
7	OUT	Output Terminal.
8	$+V_S$	Positive Supply Terminal.
9	REF	Reference Voltage Terminal.
10	+IN	Noninverting Input Terminal. True differential input.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A @ 25°C, $+V_S$ = +15 V, $-V_S$ = −15 V, R_L = 10 kΩ, unless otherwise noted.

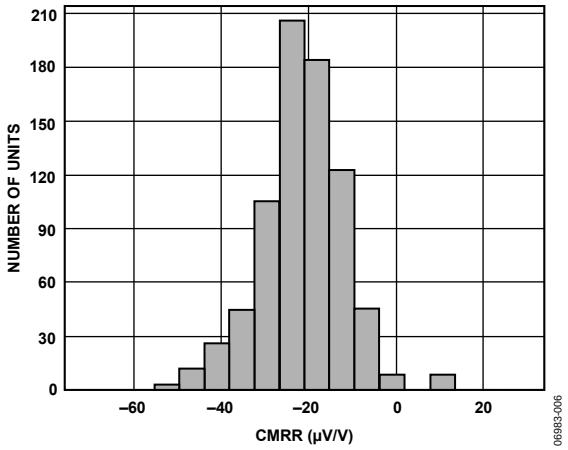


Figure 6. Typical Distribution of CMRR, G = 1

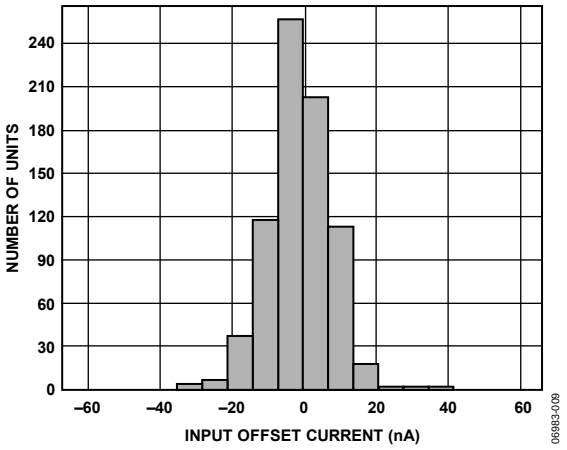


Figure 9. Typical Distribution of Input Offset Current

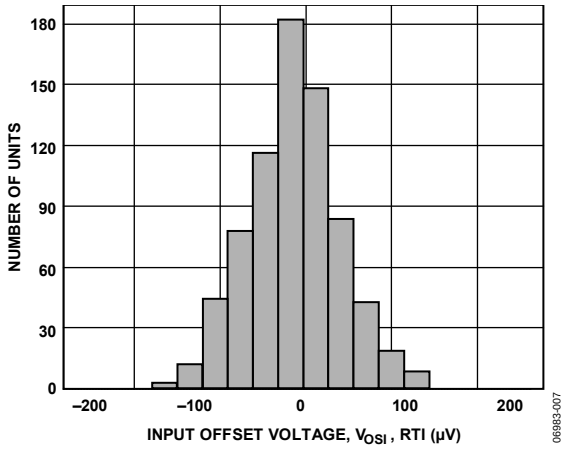


Figure 7. Typical Distribution of Offset Voltage, V_{OSI}

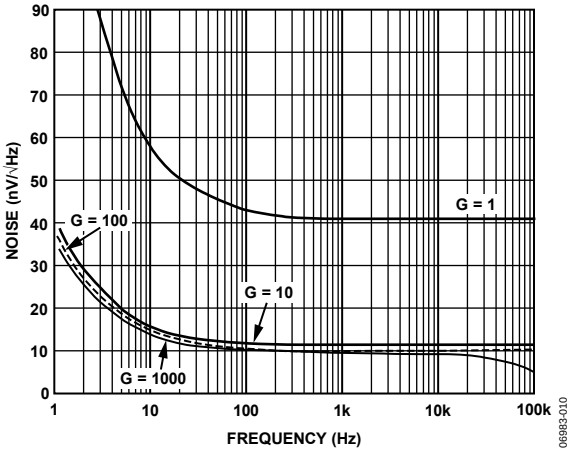


Figure 10. Voltage Spectral Density Noise vs. Frequency

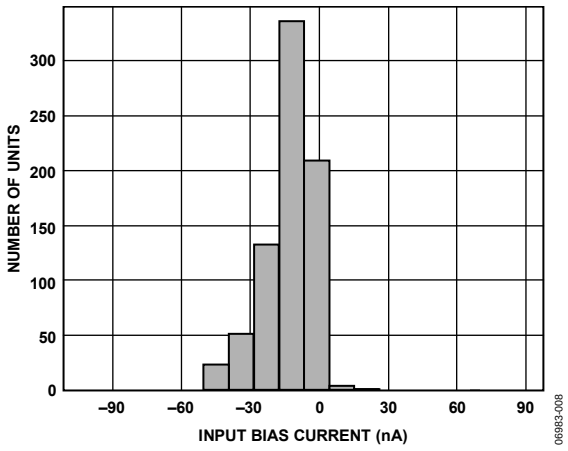


Figure 8. Typical Distribution of Input Bias Current

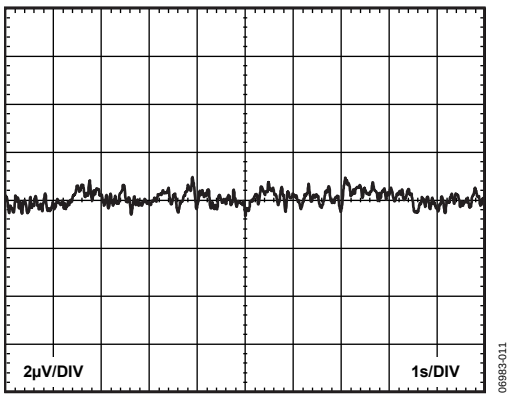


Figure 11. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 1

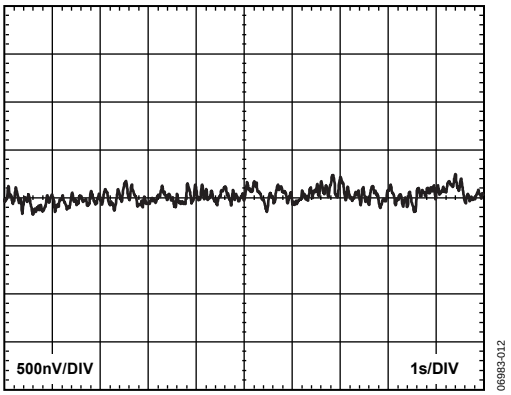


Figure 12. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 1000

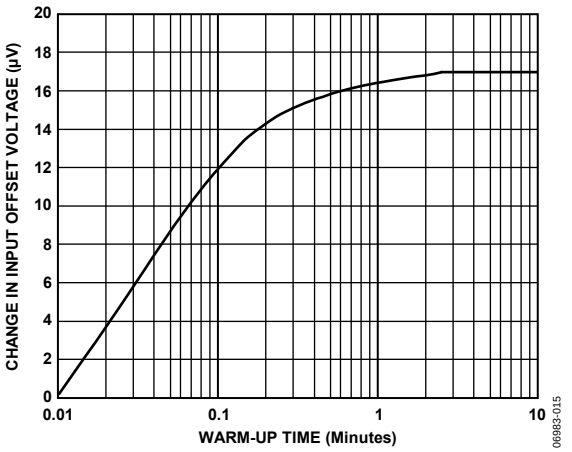


Figure 15. Change in Input Offset Voltage vs. Warm-Up Time, G = 1000

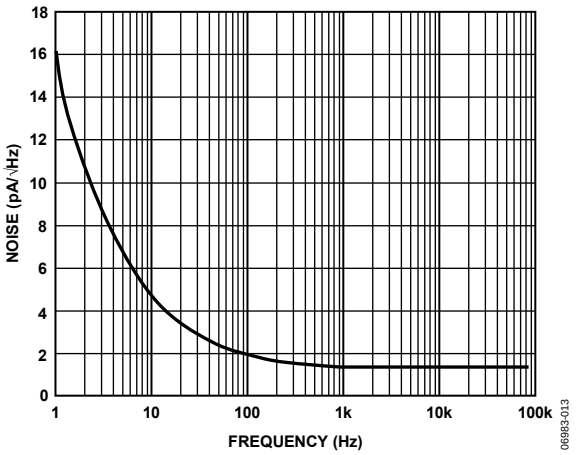


Figure 13. Current Noise Spectral Density vs. Frequency

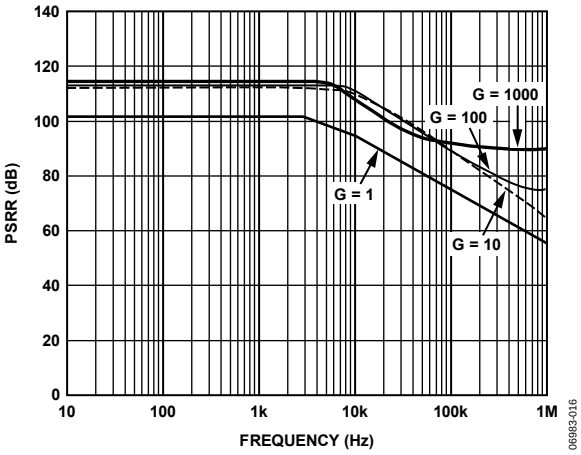


Figure 16. Positive PSRR vs. Frequency, RTI

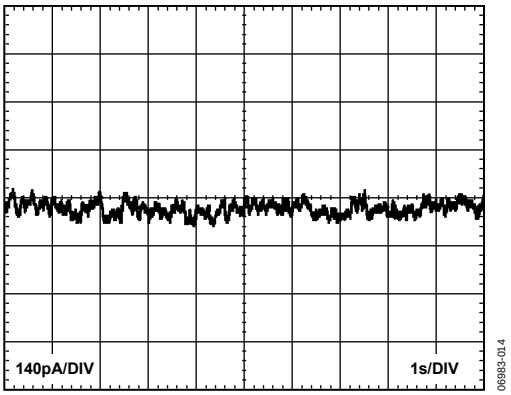


Figure 14. 0.1 Hz to 10 Hz Current Noise

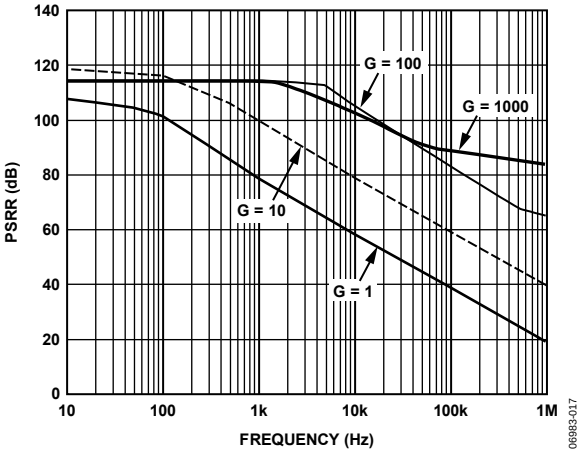


Figure 17. Negative PSRR vs. Frequency, RTI

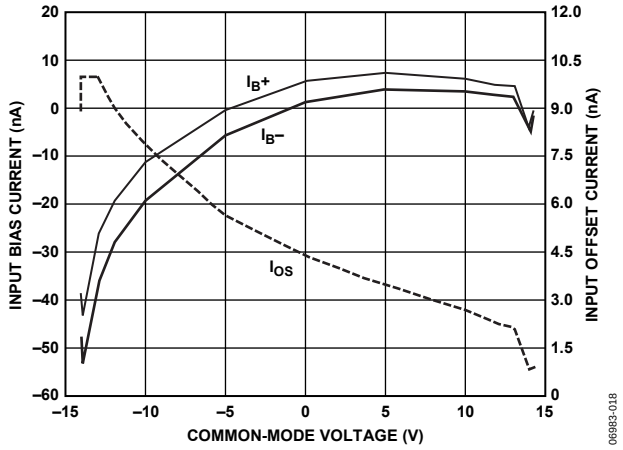


Figure 18. Input Bias Current and Offset Current vs. Common-Mode Voltage

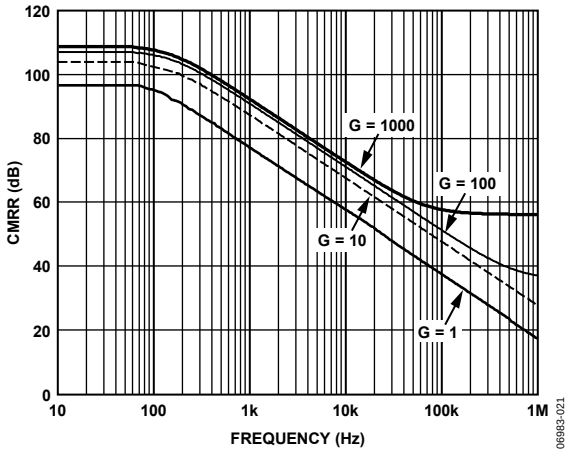


Figure 21. CMRR vs. Frequency, 1 kΩ Source Imbalance

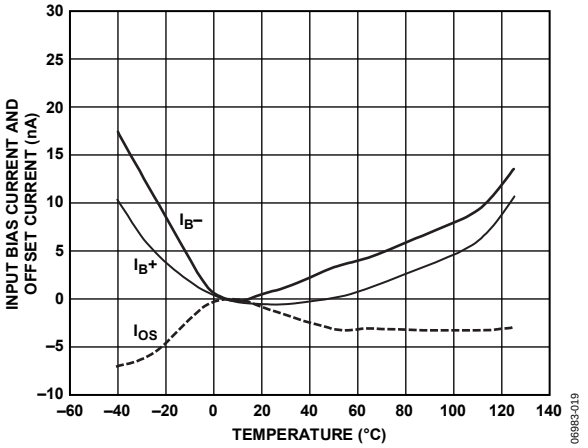


Figure 19. Input Bias Current and Offset Current vs. Temperature

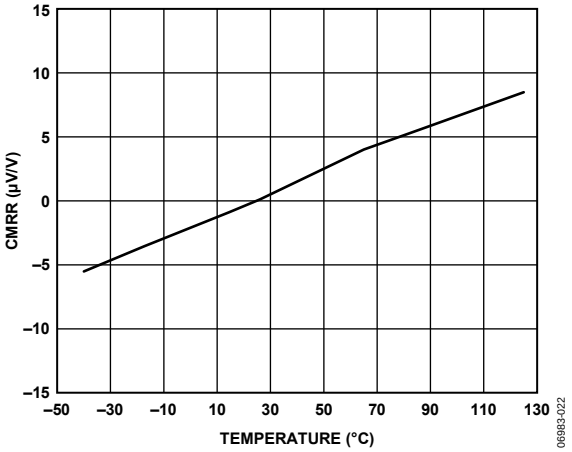


Figure 22. CMRR vs. Temperature, G = 1

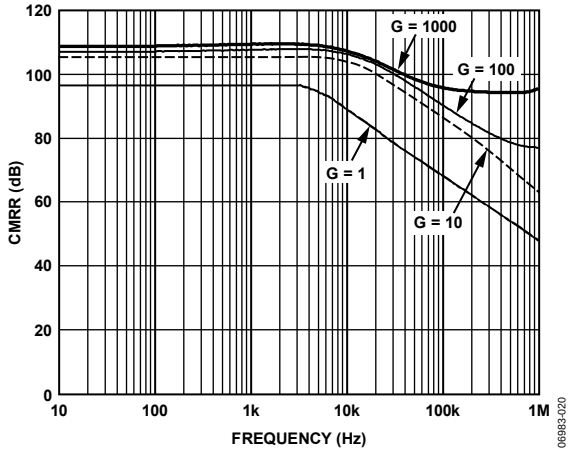


Figure 20. CMRR vs. Frequency

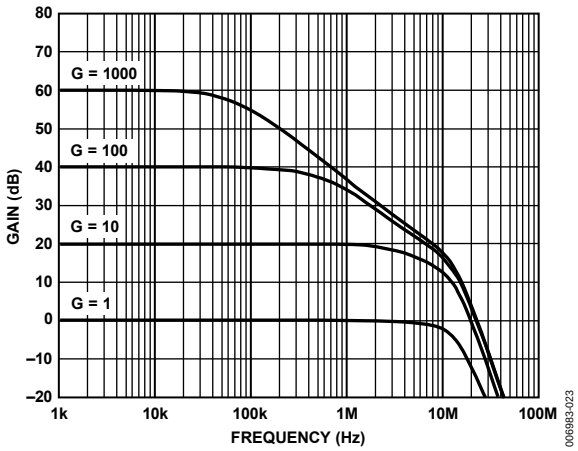


Figure 23. Gain vs. Frequency

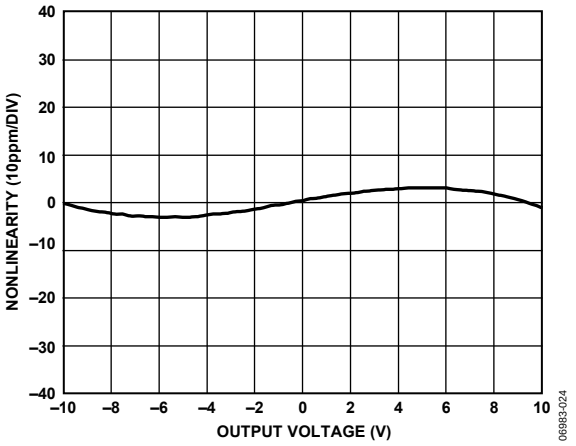


Figure 24. Gain Nonlinearity, G = 1, R_L = 10 kΩ, 2 kΩ, 600 Ω

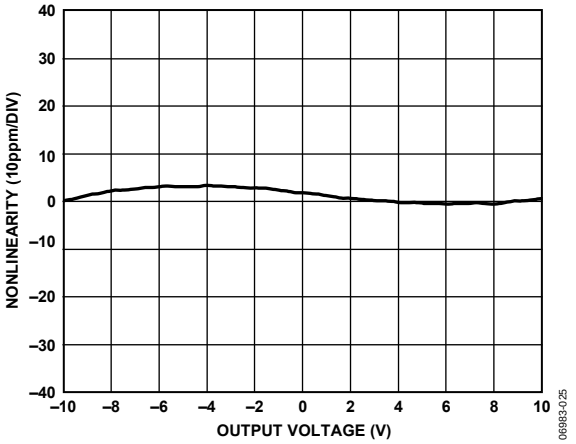


Figure 25. Gain Nonlinearity, G = 10, R_L = 10 kΩ, 2 kΩ, 600 Ω

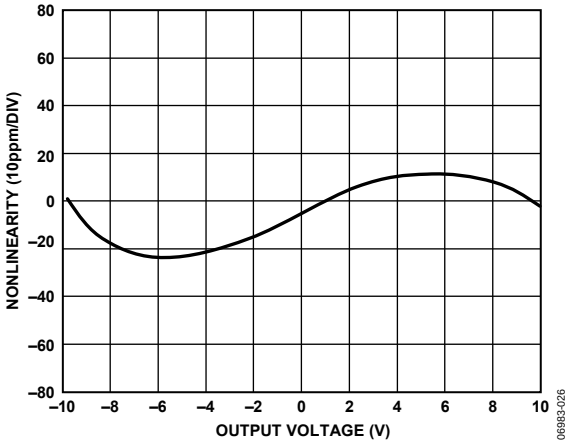


Figure 26. Gain Nonlinearity, G = 100, R_L = 10 kΩ, 2 kΩ, 600 Ω

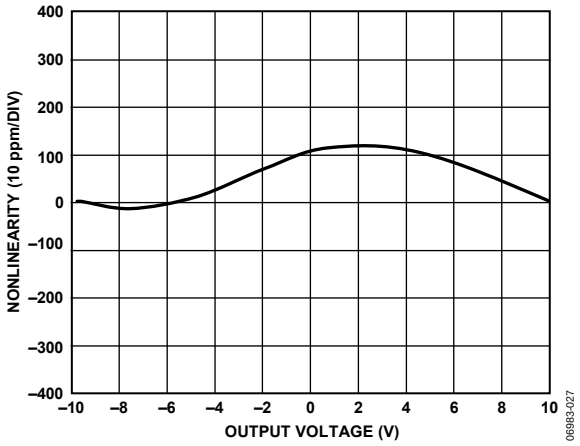


Figure 27. Gain Nonlinearity, G = 1000, R_L = 10 kΩ, 2 kΩ, 600 Ω

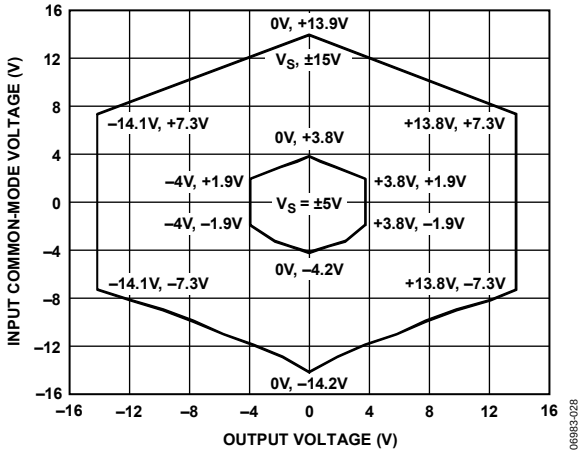


Figure 28. Input Common-Mode Voltage Range vs. Output Voltage, G = 1

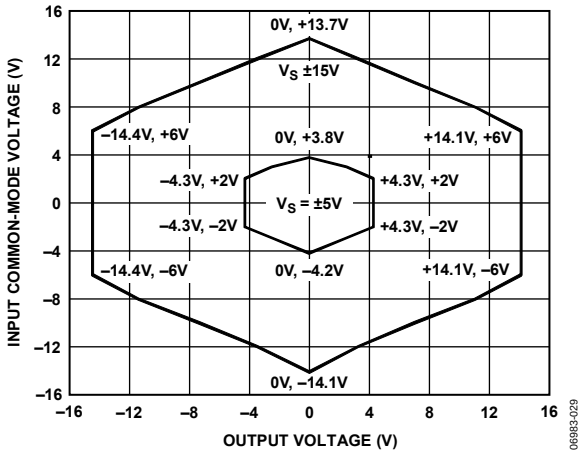


Figure 29. Input Common-Mode Voltage Range vs. Output Voltage, G = 1000

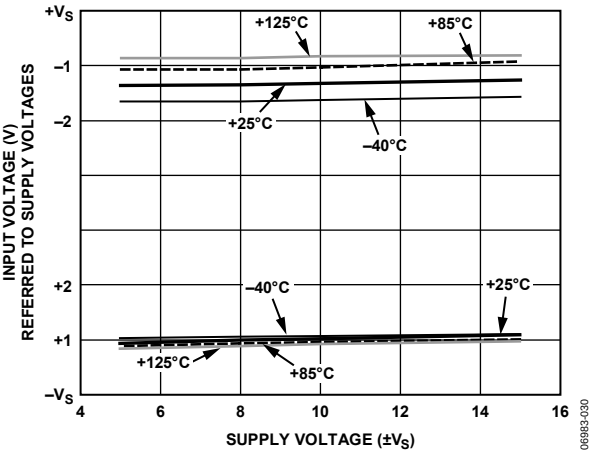


Figure 30. Input Voltage Limit vs. Supply Voltage, G = 1, V_{REF} = 0 V, R_L = 10 kΩ

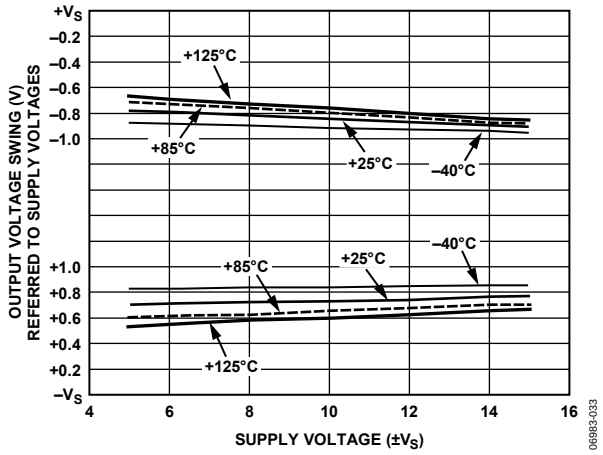


Figure 33. Output Voltage Swing vs. Supply Voltage, G =1000, R_L = 10 kΩ

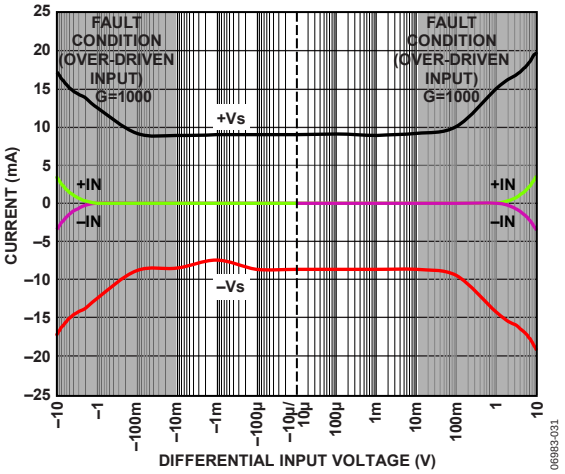


Figure 31. Fault Current Draw vs. Input Voltage, G = 1000, R_L = 10 kΩ

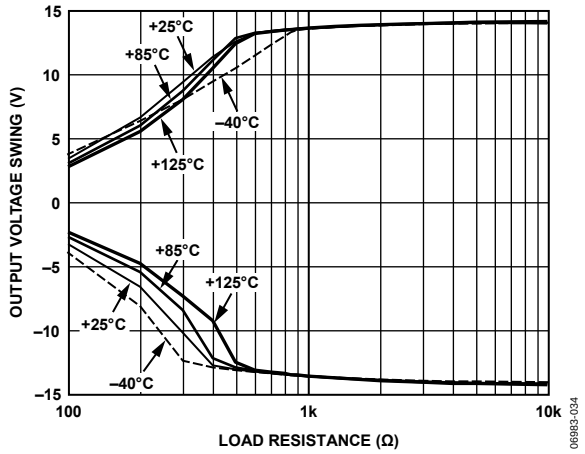


Figure 34. Output Voltage Swing vs. Load Resistance

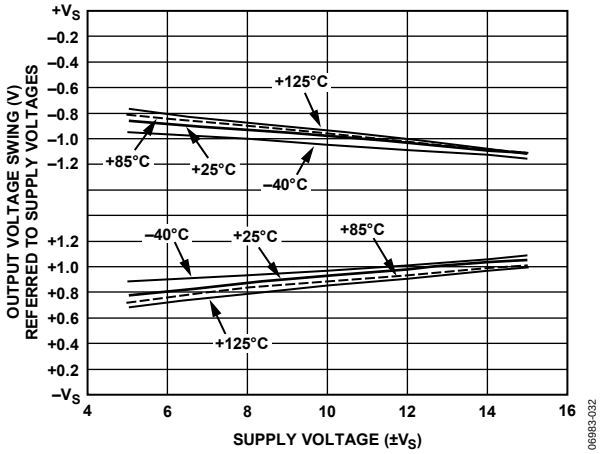


Figure 32. Output Voltage Swing vs. Supply Voltage, G = 1000, R_L = 2 kΩ

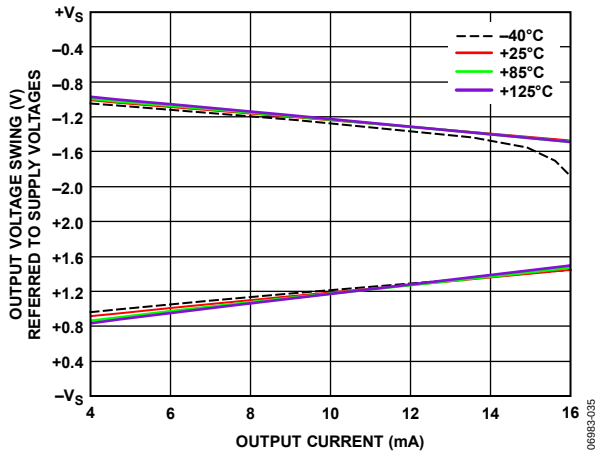


Figure 35. Output Voltage Swing vs. Output Current

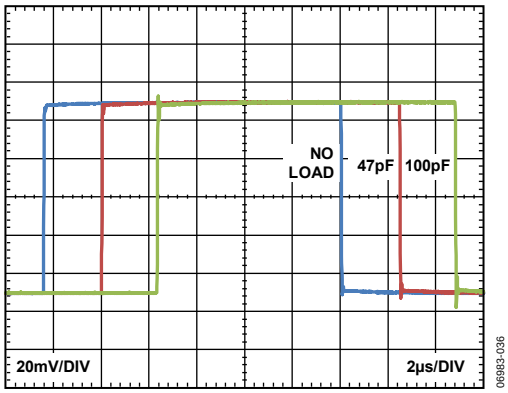


Figure 36. Small-Signal Pulse Response for Various Capacitive Loads, G = 1

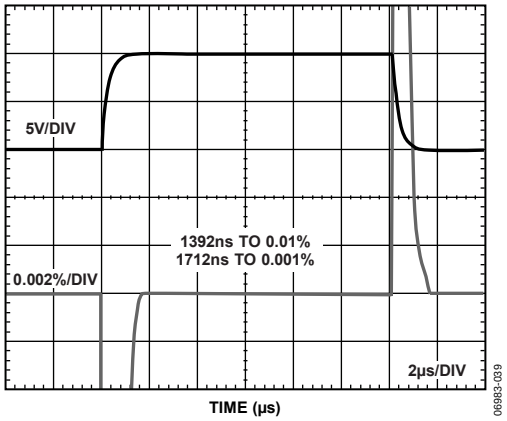


Figure 39. Large-Signal Pulse Response and Settling Time, G = 100, R_L = 10 kΩ

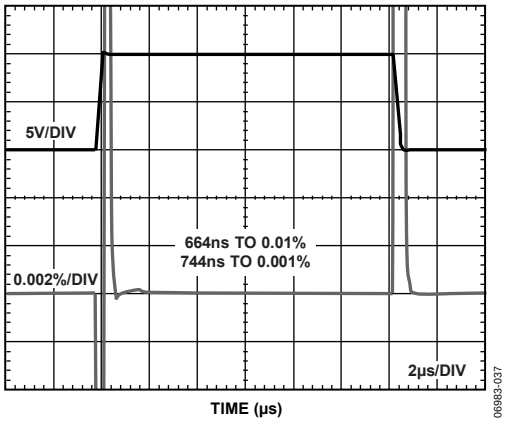


Figure 37. Large-Signal Pulse Response and Settling Time, G = 1, R_L = 10 kΩ

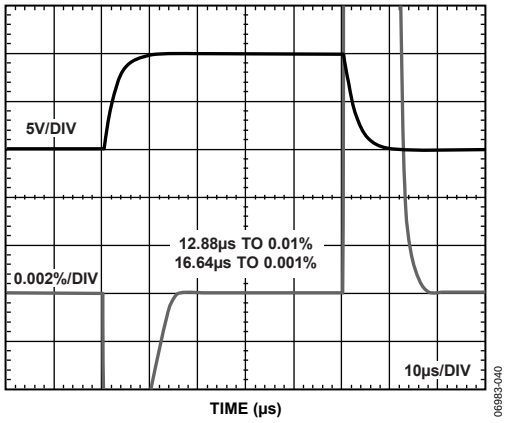


Figure 40. Large-Signal Pulse Response and Settling Time, G = 1000, R_L = 10 kΩ

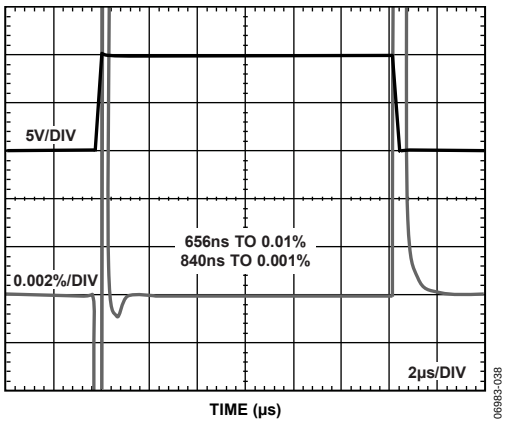


Figure 38. Large-Signal Pulse Response and Settling Time, G = 10, R_L = 10 kΩ

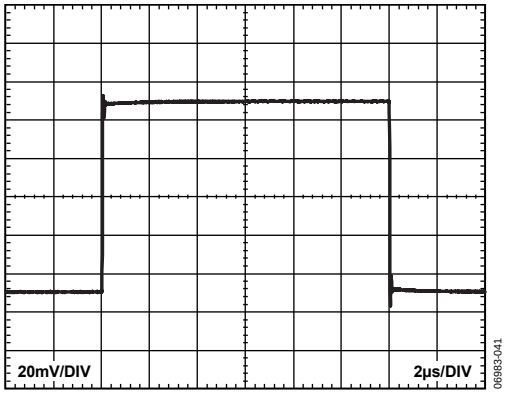


Figure 41. Small-Signal Response, G = 1, R_L = 2 kΩ, C_L = 100

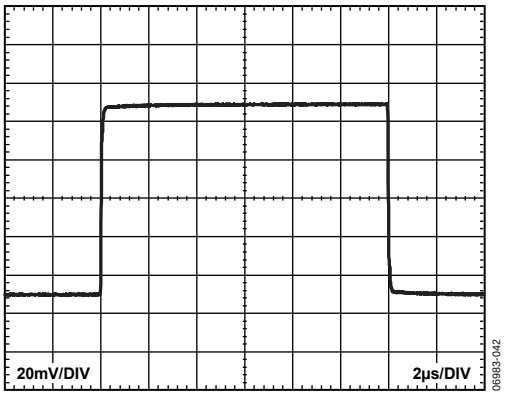


Figure 42. Small-Signal Response,
$G = 10$, $R_L = 2\ k\Omega$, $C_L = 100\ pF$

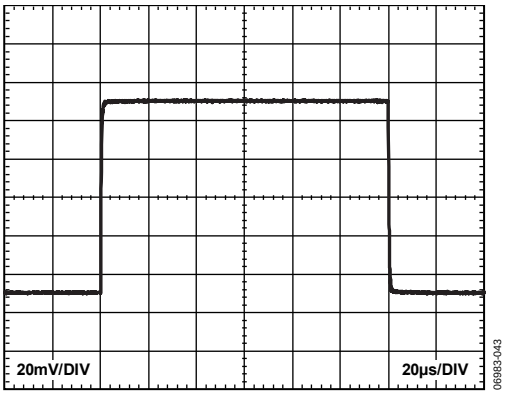


Figure 43. Small-Signal Response,
$G = 100$, $R_L = 2\ k\Omega$, $C_L = 100\ pF$

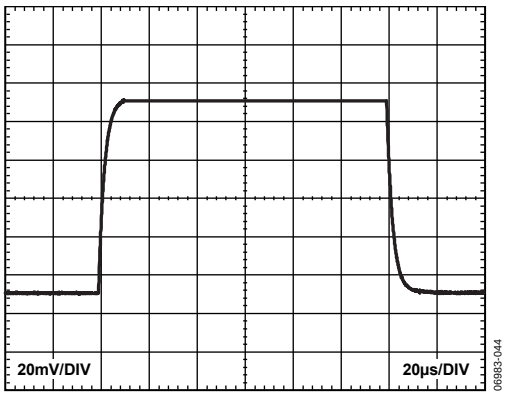


Figure 44. Small-Signal Response, $G = 1000$, $R_L = 2\ k\Omega$, $C_L = 100\ pF$

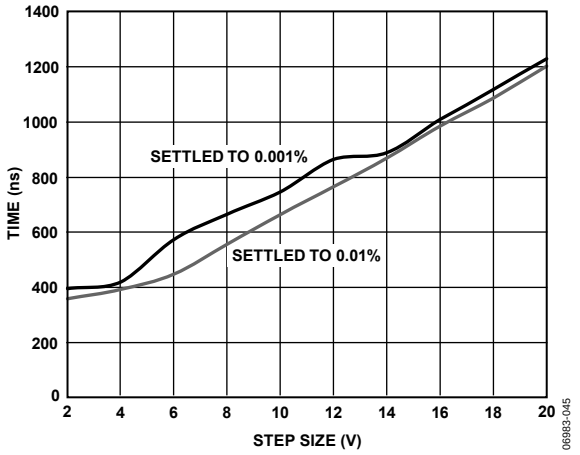


Figure 45. Settling Time vs. Step Size, $G = 1$, $R_L = 10\ k\Omega$

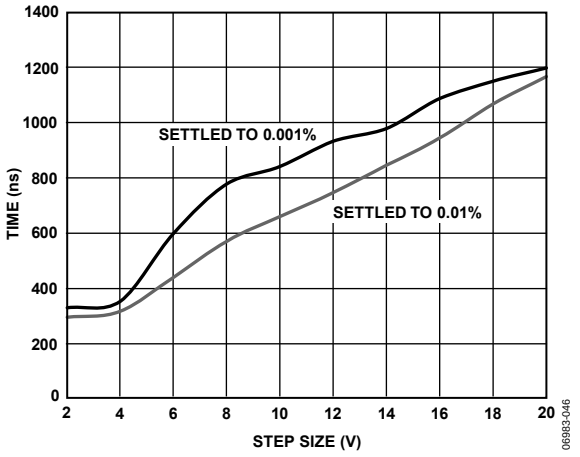


Figure 46. Settling Time vs. Step Size, $G = 10$, $R_L = 10\ k\Omega$

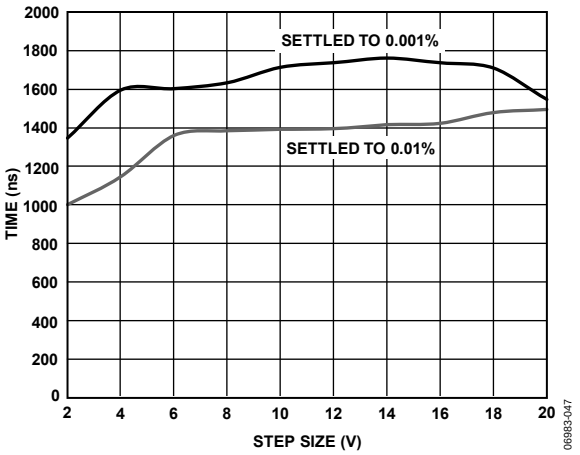


Figure 47. Settling Time vs. Step Size, $G = 100$, $R_L = 10\ k\Omega$

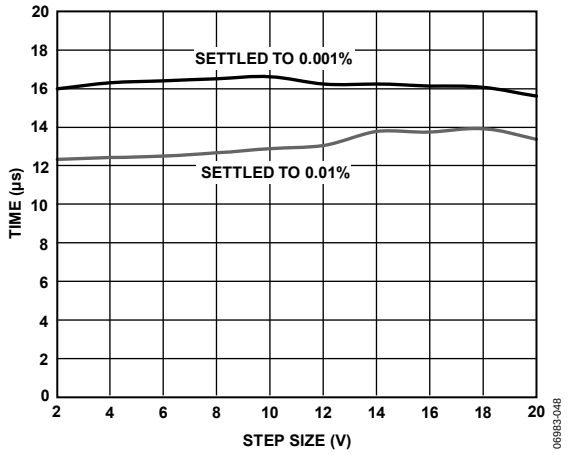


Figure 48. Settling Time vs. Step Size, G = 1000, R_L = 10 kΩ

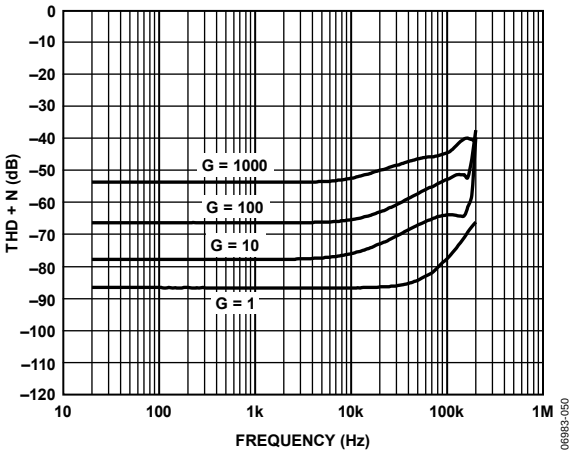


Figure 50. Total Harmonic Distortion vs. Frequency, 10 Hz to 500 kHz Band-Pass Filter, 2 kΩ Load

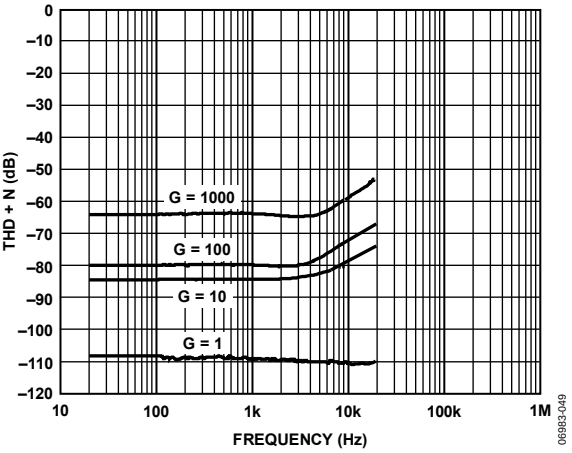


Figure 49. Total Harmonic Distortion vs. Frequency, 10 Hz to 22 kHz Band-Pass Filter, 2 kΩ Load

THEORY OF OPERATION

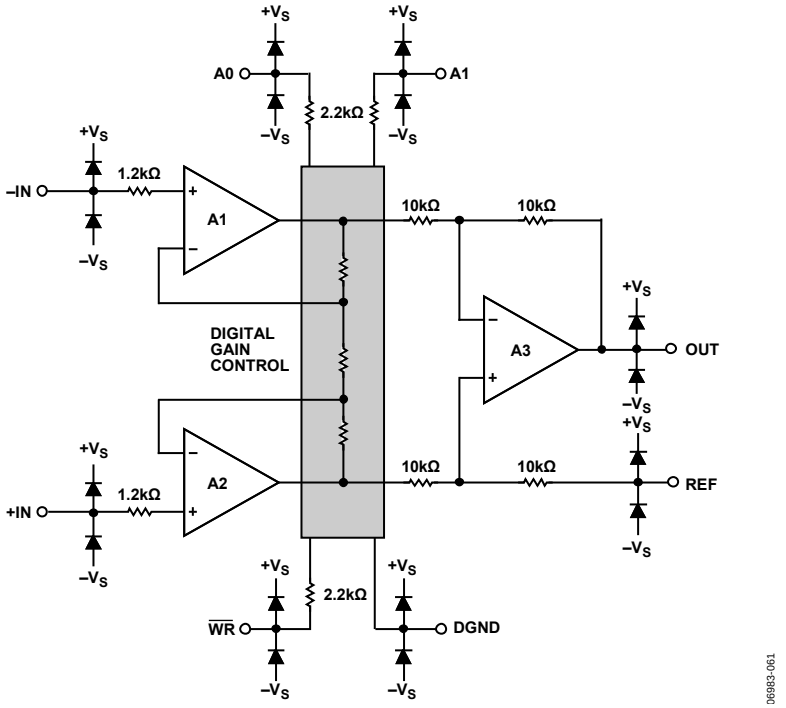


Figure 51. Simplified Schematic

The AD8253 is a monolithic instrumentation amplifier based on the classic 3-op-amp topology, as shown in Figure 51. It is fabricated on the Analog Devices, Inc., proprietary *i*CMOS® process that provides precision linear performance and a robust digital interface. A parallel interface allows users to digitally program gains of 1, 10, 100, and 1000. Gain control is achieved by switching resistors in an internal precision resistor array (as shown in Figure 51).

All internal amplifiers employ distortion cancellation circuitry and achieve high linearity and ultralow THD. Laser-trimmed resistors allow for a maximum gain error of less than 0.03% for G = 1 and a minimum CMRR of 100 dB for G = 1000. A pinout optimized for high CMRR over frequency enables the AD8253 to offer a guaranteed minimum CMRR over frequency of 80 dB at 20 kHz (G = 1). The balanced input reduces the parasitics that in the past had adversely affected CMRR performance.

GAIN SELECTION

This section describes how to configure the AD8253 for basic operation. Logic low and logic high voltage limits are listed in the Specifications section. Typically, logic low is 0 V and logic high is 5 V; both voltages are measured with respect to DGND. Refer to the specifications table (Table 2) for the permissible voltage range of DGND. The gain of the AD8253 can be set using two methods: transparent gain mode and latched gain mode. Regardless of the mode, pull-up or pull-down resistors should be used to provide a well-defined voltage at the A0 and A1 pins.

Transparent Gain Mode

The easiest way to set the gain is to program it directly via a logic high or logic low voltage applied to A0 and A1. Figure 52 shows an example of this gain setting method, referred to throughout the data sheet as transparent gain mode. Tie $\overline{WR}$ to the negative supply to engage transparent gain mode. In this mode, any change in voltage applied to A0 and A1 from logic low to logic high, or vice versa, immediately results in a gain change. Table 5 is the truth table for transparent gain mode, and Figure 52 shows the AD8253 configured in transparent gain mode.

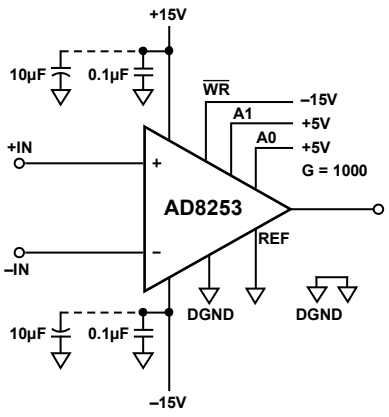


Figure 52. Transparent Gain Mode, A0 and A1 = High, G = 1000

Table 5. Truth Table Logic Levels for Transparent Gain Mode

$\overline{WR}$	A1	A0	Gain
$-V_S$	Low	Low	1
$-V_S$	Low	High	10
$-V_S$	High	Low	100
$-V_S$	High	High	1000

Latched Gain Mode

Some applications have multiple programmable devices such as multiplexers or other programmable gain instrumentation amplifiers on the same PCB. In such cases, devices can share a data bus. The gain of the AD8253 can be set using $\overline{WR}$ as a latch, allowing other devices to share A0 and A1. Figure 53 shows a schematic using this method, known as latched gain mode. The AD8253 is in this mode when $\overline{WR}$ is held at logic high or logic low, typically 5 V and 0 V, respectively. The voltages on A0 and A1 are read on the downward edge of the $\overline{WR}$ signal as it transitions from logic high to logic low. This latches in the logic levels on A0 and A1, resulting in a gain change. See the truth table listing in Table 6 for more on these gain changes.

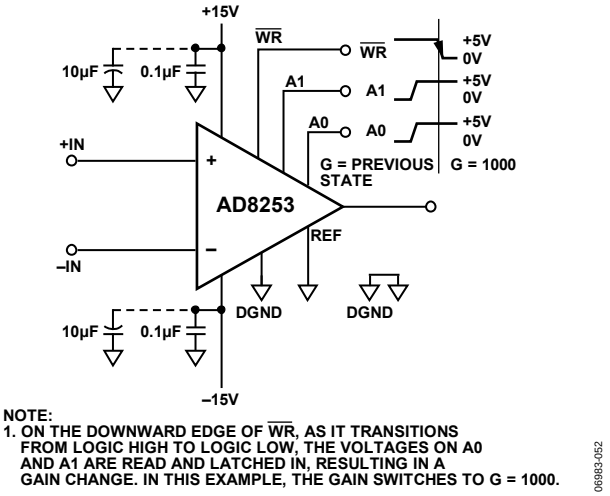


Figure 53. Latched Gain Mode, G = 1000

Table 6. Truth Table Logic Levels for Latched Gain Mode

$\overline{WR}$	A1	A0	Gain
High to Low	Low	Low	Change to 1
High to Low	Low	High	Change to 10
High to Low	High	Low	Change to 100
High to Low	High	High	Change to 1000
Low to Low	X[1]	X[1]	No change
Low to High	X[1]	X[1]	No change
High to High	X[1]	X[1]	No change

[1] X = don't care.

On power-up, the AD8253 defaults to a gain of 1 when in latched gain mode. In contrast, if the AD8253 is configured in transparent gain mode, it starts at the gain indicated by the voltage levels on A0 and A1 on power-up.

Timing for Latched Gain Mode

In latched gain mode, logic levels at A0 and A1 must be held for a minimum setup time, t_{SU}, before the downward edge of $\overline{WR}$ latches in the gain. Similarly, they must be held for a minimum hold time, t_{HD}, after the downward edge of $\overline{WR}$ to ensure that the gain is latched in correctly. After t_{HD}, A0 and A1 may change logic levels, but the gain does not change until the next downward edge of $\overline{WR}$. The minimum duration that $\overline{WR}$ can be held high is $t_{\overline{WR}\text{-HIGH}}$, and $t_{\overline{WR}\text{-LOW}}$ is the minimum duration that $\overline{WR}$ can be held low. Digital timing specifications are listed in Table 2. The time required for a gain change is dominated by the settling time of the amplifier. A timing diagram is shown in Figure 54.

When sharing a data bus with other devices, logic levels applied to those devices can potentially feed through to the output of the AD8253. Feedthrough can be minimized by decreasing the edge rate of the logic signals. Furthermore, careful layout of the PCB also reduces coupling between the digital and analog portions of the board.

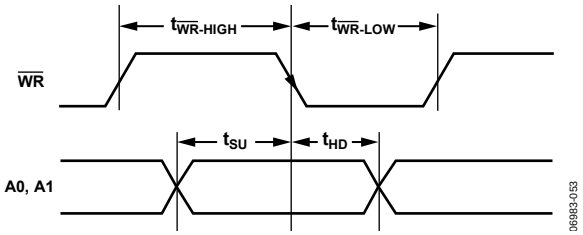


Figure 54. Timing Diagram for Latched Gain Mode

POWER SUPPLY REGULATION AND BYPASSING

The AD8253 has high PSRR. However, for optimal performance, a stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. As in all linear circuits, bypass capacitors must be used to decouple the amplifier.

Place a 0.1 µF capacitor close to each supply pin. A 10 µF tantalum capacitor can be used farther away from the part (see Figure 55) and, in most cases, it can be shared by other precision integrated circuits.

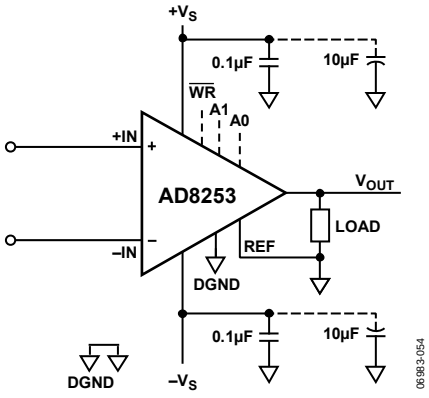


Figure 55. Supply Decoupling, REF, and Output Referred to Ground

INPUT BIAS CURRENT RETURN PATH

The AD8253 input bias current must have a return path to its local analog ground. When the source, such as a thermocouple, cannot provide a return current path, one should be created (see Figure 56).

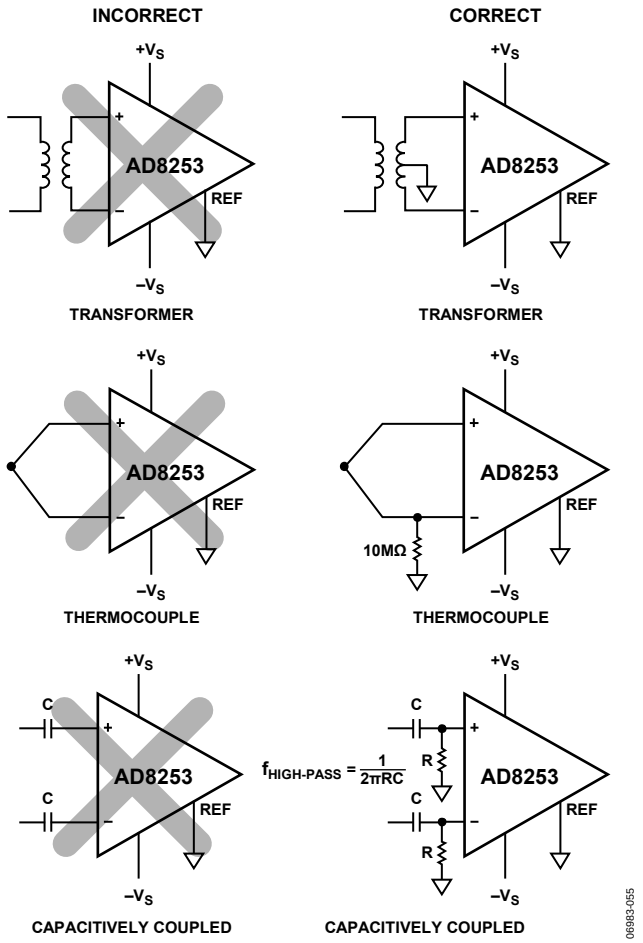


Figure 56. Creating an I_{BIAS} Path

INPUT PROTECTION

All terminals of the AD8253 are protected against ESD. An external resistor should be used in series with each of the inputs to limit current for voltages greater than 0.5 V beyond either supply rail. In such a case, the AD8253 safely handles a continuous 6 mA current at room temperature. For applications where the AD8253 encounters extreme overload voltages, external series resistors and low leakage diode clamps such as BAV199Ls, FJH1100s, or SP720s should be used.

REFERENCE TERMINAL

The reference terminal, REF, is at one end of a 10 kΩ resistor (see Figure 51). The instrumentation amplifier output is referenced to the voltage on the REF terminal; this is useful when the output signal needs to be offset to voltages other than its local analog ground. For example, a voltage source can be tied to the REF pin to level shift the output so that the AD8253 can interface with a single-supply ADC. The allowable reference voltage range is a function of the gain, common-mode input, and supply voltages. The REF pin should not exceed either $+V_S$ or $-V_S$ by more than 0.5 V.

For best performance, especially in cases where the output is not measured with respect to the REF terminal, source impedance to the REF terminal should be kept low because parasitic resistance can adversely affect CMRR and gain accuracy.

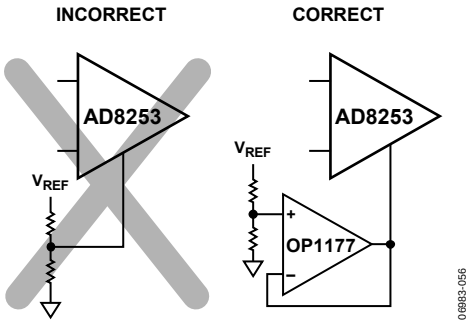


Figure 57. Driving the Reference Pin

COMMON-MODE INPUT VOLTAGE RANGE

The 3-op-amp architecture of the AD8253 applies gain and then removes the common-mode voltage. Therefore, internal nodes in the AD8253 experience a combination of both the gained signal and the common-mode signal. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not. Figure 28 and Figure 29 show the allowable common-mode input voltage ranges for various output voltages, supply voltages, and gains.

LAYOUT

Grounding

In mixed-signal circuits, low level analog signals need to be isolated from the noisy digital environment. Designing with the AD8253 is no exception. Its supply voltages are referenced to an analog ground. Its digital circuit is referenced to a digital ground. Although it is convenient to tie both grounds to a single ground plane, the current traveling through the ground wires and PC board can cause an error. Therefore, use separate analog and digital ground planes. Only at one point, star ground, should analog and digital ground meet.

The output voltage of the AD8253 develops with respect to the potential on the reference terminal. Take care to tie REF to the appropriate local analog ground or to connect it to a voltage that is referenced to the local analog ground.

Coupling Noise

To prevent coupling noise onto the AD8253, follow these guidelines:

- Do not run digital lines under the device.
- Run the analog ground plane under the AD8253.
- Shield fast-switching signals with digital ground to avoid radiating noise to other sections of the board, and never run them near analog signal paths.
- Avoid crossover of digital and analog signals.
- Connect digital and analog ground at one point only (typically under the ADC).
- Power supply lines should use large traces to ensure a low impedance path. Decoupling is necessary; follow the guidelines listed in the Power Supply Regulation and Bypassing section.

Common-Mode Rejection

The AD8253 has high CMRR over frequency, giving it greater immunity to disturbances, such as line noise and its associated harmonics, in contrast to typical in amps whose CMRR falls off around 200 Hz. They often need common-mode filters at the inputs to compensate for this shortcoming. The AD8253 is able to reject CMRR over a greater frequency range, reducing the need for input common-mode filtering.

Careful board layout maximizes system performance. To maintain high CMRR over frequency, lay out the input traces symmetrically. Ensure that the traces maintain resistive and capacitive balance; this holds for additional PCB metal layers under the input pins and traces. Source resistance and capacitance should be placed as close to the inputs as possible. Should a trace cross the inputs (from another layer), it should be routed perpendicular to the input traces.

RF INTERFERENCE

RF rectification is often a problem when amplifiers are used in applications where there are strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 58. The filter limits the input signal bandwidth according to the following relationship:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10\ C_C$.

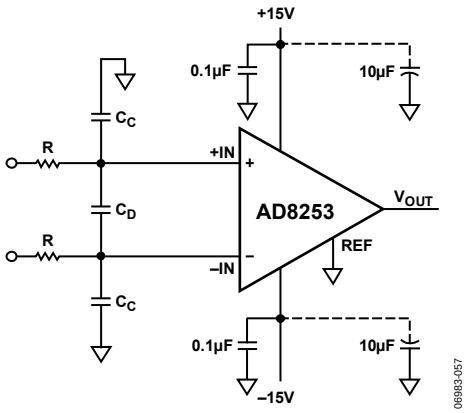


Figure 58. RFI Suppression

Values of R and C_C should be chosen to minimize RFI. Mismatch between the R × C_C at the positive input and the R × C_C at negative input degrades the CMRR of the AD8253. By using a value of C_D that is 10 times larger than the value of C_C, the effect of the mismatch is reduced and performance is improved.

DRIVING AN ANALOG-TO-DIGITAL CONVERTER

An instrumentation amplifier is often used in front of an analog-to-digital converter to provide CMRR. Usually, instrumentation amplifiers require a buffer to drive an ADC. However, the low output noise, low distortion, and low settle time of the AD8253 make it an excellent ADC driver.

In this example, a 1 nF capacitor and a 49.9 Ω resistor create an antialiasing filter for the AD7612. The 1 nF capacitor also serves to store and deliver necessary charge to the switched capacitor input of the ADC. The 49.9 Ω series resistor reduces the burden of the 1 nF load from the amplifier and isolates it from the kickback current injected from the switched capacitor input of the AD7612. Selecting too small a resistor improves the correlation between the voltage at the output of the AD8253 and the voltage at the input of the AD7612 but may destabilize the AD8253. A trade-off must be made between selecting a resistor small enough to maintain accuracy and large enough to maintain stability.

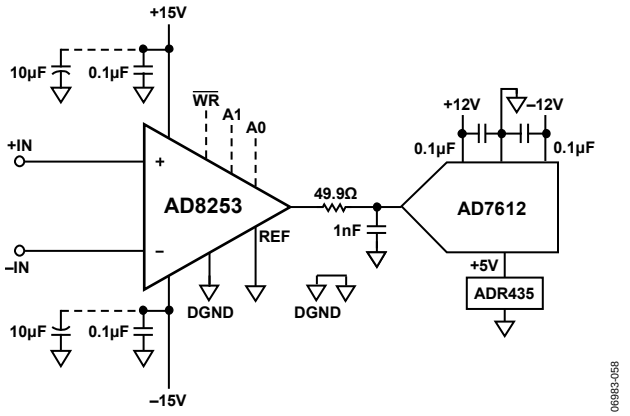


Figure 59. Driving an ADC

APPLICATIONS INFORMATION

DIFFERENTIAL OUTPUT

In certain applications, it is necessary to create a differential signal. High resolution analog-to-digital converters often require a differential input. In other cases, transmission over a long distance can require differential signals for better immunity to interference.

Figure 61 shows how to configure the AD8253 to output a differential signal. An op amp, the AD8675, is used in an inverting topology to create a differential voltage. V_{REF} sets the output midpoint according to the equation shown in the figure. Errors from the op amp are common to both outputs and are thus common mode. Likewise, errors from using mismatched resistors cause a common-mode dc offset error. Such errors are rejected in differential signal processing by differential input ADCs or instrumentation amplifiers.

When using this circuit to drive a differential ADC, V_{REF} can be set using a resistor divider from the ADC reference to make the output ratiometric with the ADC.

SETTING GAINS WITH A MICROCONTROLLER

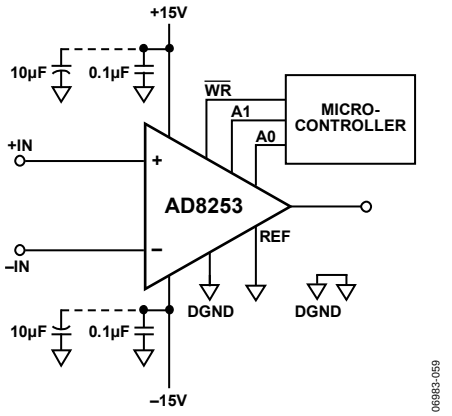


Figure 60. Programming Gain Using a Microcontroller

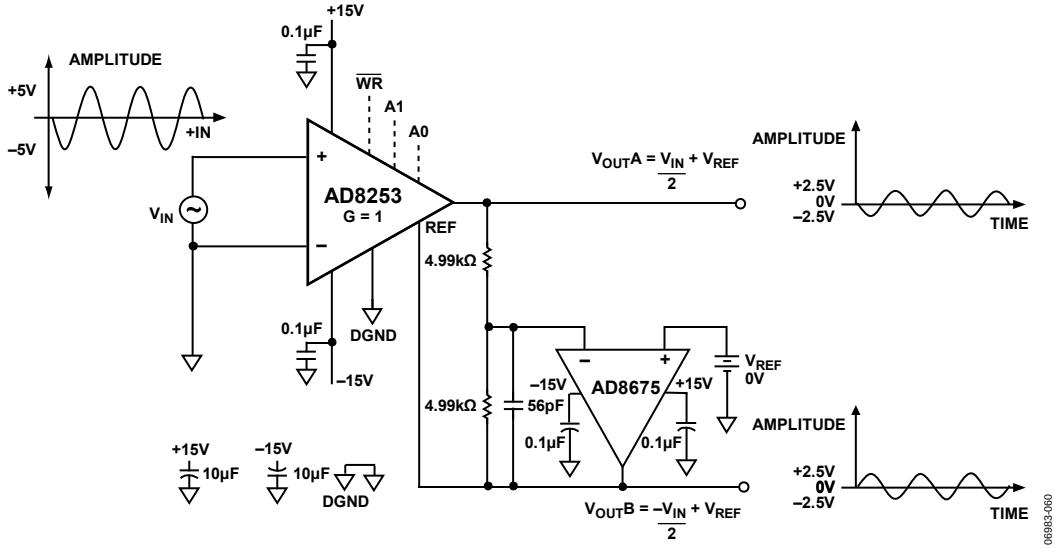


Figure 61. Differential Output with Level Shift

DATA ACQUISITION

The AD8253 makes an excellent instrumentation amplifier for use in data acquisition systems. Its wide bandwidth, low distortion, low settling time, and low noise enable it to condition signals in front of a variety of 16-bit ADCs.

Figure 63 shows the AD825x as part of a total data acquisition system. The quick slew rate of the AD8253 allows it to condition rapidly changing signals from the multiplexed inputs. An FPGA controls the AD7612, AD8253, and ADG1209. In addition, mechanical switches and jumpers allow users to pin strap the gains when in transparent gain mode.

This system achieved −116 dB of THD at 1 kHz and a signal-to-noise ratio of 91 dB during testing, as shown in Figure 62.

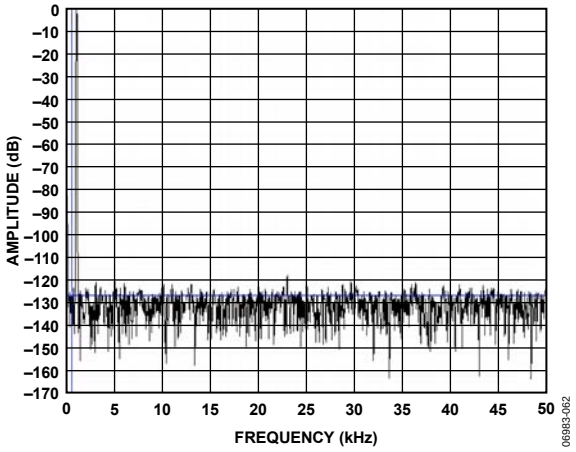


Figure 62. FFT of the AD825x in a Total Data Acquisition System Using the AD8253 1 kHz Signal

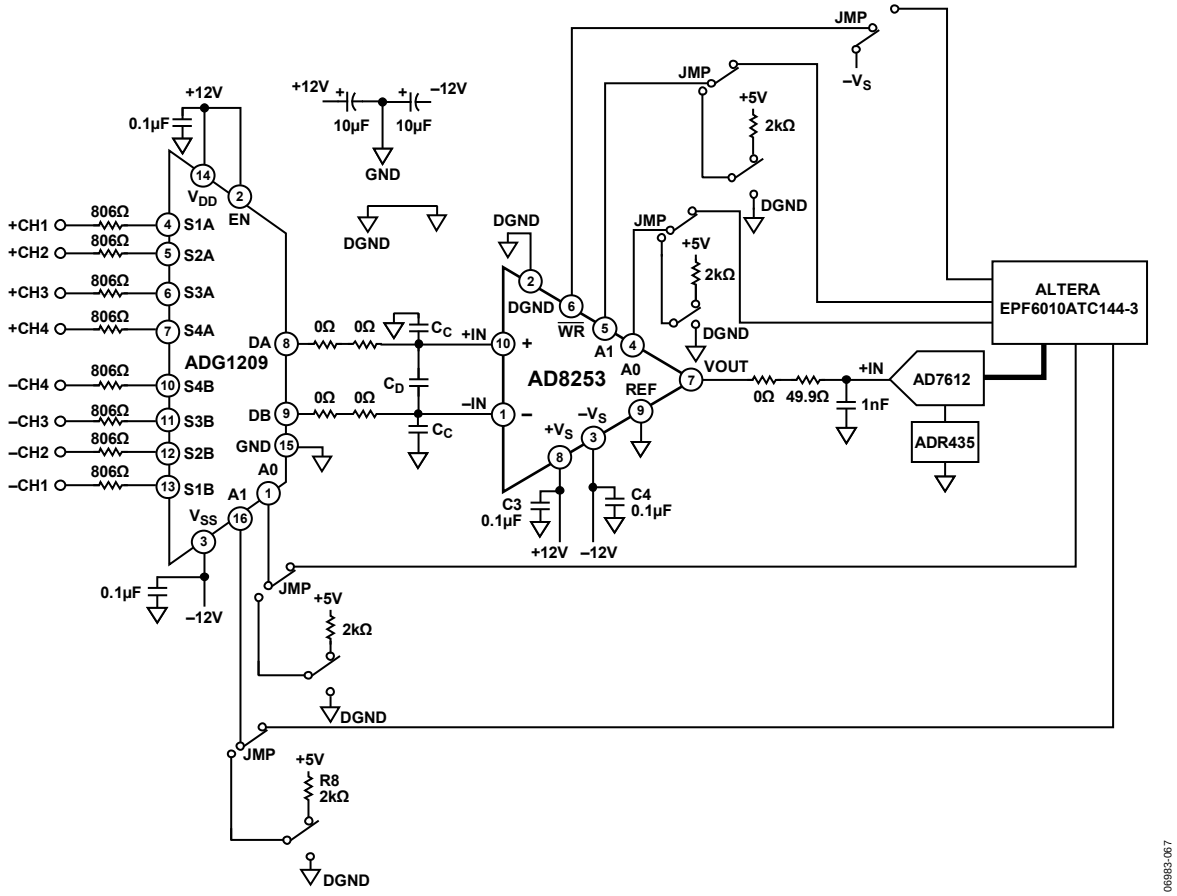


Figure 63. Schematic of ADG1209, AD8253, and AD7612 Used with the AD825x in a Total Data Acquisition System

OUTLINE DIMENSIONS

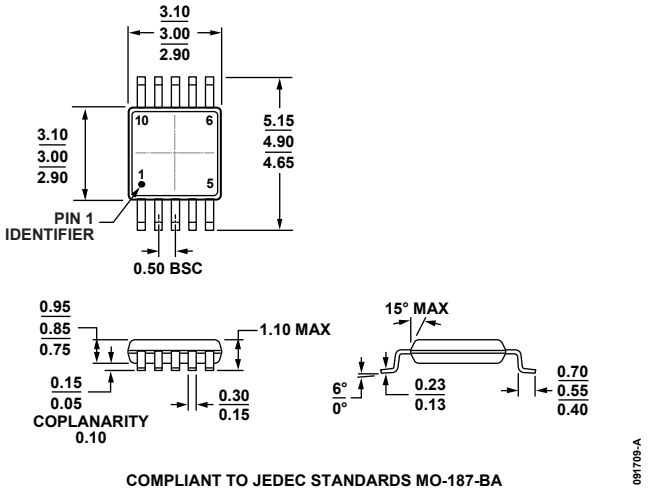


Figure 64. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8253ARMZ	–40°C to +85°C	10-Lead MSOP	RM-10	Y0K
AD8253ARMZ-RL	–40°C to +85°C	10-Lead MSOP	RM-10	Y0K
AD8253ARMZ-R7	–40°C to +85°C	10-Lead MSOP	RM-10	Y0K
AD8253-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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