

# M320x Series

9x14 mm, 3.3/2.5/1.8 Volt, PECL/LVDS/CML, VCXO



- Featuring *QiK Chip™* Technology
- Superior Jitter Performance (comparable to SAW based)
- APR of  $\pm 50$  or  $\pm 100$ ppm over industrial temperature range
- Frequencies from 150 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

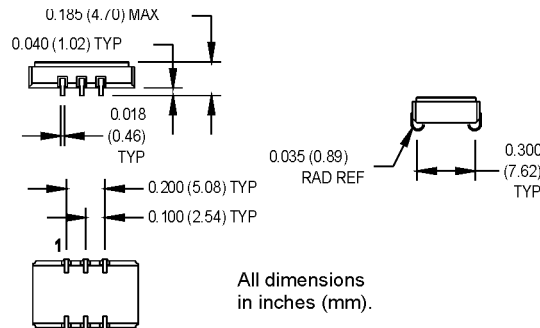
## Phase Lock Loop Applications:

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

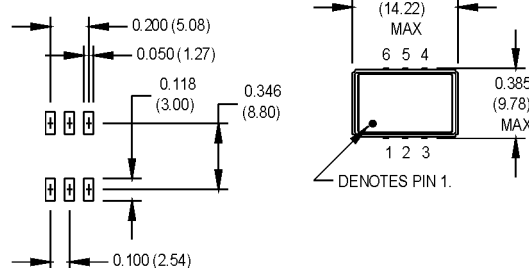
## Ordering Information

|                                      | M320 | 0 | 6 | A | G | P | J | 00.0000 | MHz |
|--------------------------------------|------|---|---|---|---|---|---|---------|-----|
| Product Series                       |      |   |   |   |   |   |   |         |     |
| Supply Voltage                       |      |   |   |   |   |   |   |         |     |
| 0: 3.3 V                             |      |   |   |   |   |   |   |         |     |
| 1: 2.5 V                             |      |   |   |   |   |   |   |         |     |
| 2: 1.8 V                             |      |   |   |   |   |   |   |         |     |
| Temperature Range                    |      |   |   |   |   |   |   |         |     |
| 2: -40°C to +85°C (see note 1)       |      |   |   |   |   |   |   |         |     |
| 6: -20°C to +70°C                    |      |   |   |   |   |   |   |         |     |
| Absolute Pull Range (APR)            |      |   |   |   |   |   |   |         |     |
| A: $\pm 50$ ppm                      |      |   |   |   |   |   |   |         |     |
| B: $\pm 100$ ppm                     |      |   |   |   |   |   |   |         |     |
| Enable/Disable                       |      |   |   |   |   |   |   |         |     |
| G: Complementary Enable High (Pad 2) |      |   |   |   |   |   |   |         |     |
| M: Complementary Enable Low (Pad 2)  |      |   |   |   |   |   |   |         |     |
| U: Complementary Output              |      |   |   |   |   |   |   |         |     |
| Logic Type                           |      |   |   |   |   |   |   |         |     |
| P: PECL                              |      |   |   |   |   |   |   |         |     |
| L: LVDS                              |      |   |   |   |   |   |   |         |     |
| M: CML                               |      |   |   |   |   |   |   |         |     |
| Package/Lead Configuration           |      |   |   |   |   |   |   |         |     |
| J: 9x14 mm J-lead                    |      |   |   |   |   |   |   |         |     |
| Frequency (customer specified)       |      |   |   |   |   |   |   |         |     |

Pin1: Voltage Control  
Pin2: Enable/Disable (or N/C)  
Pin3: Ground  
Pin4: Output Q (PECL, LVDS, CML)  
Pin5: Output  $\bar{Q}$  (PECL, LVDS, CML)  
Pin6: Vcc



## SUGGESTED SOLDER PAD LAYOUT



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Revision: 8-16-06

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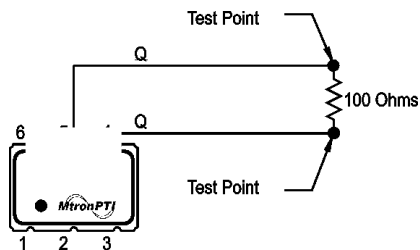
| PARAMETER                    | Symbol                         | Min.                                                                                                 | Typ.       | Max.                   | Units  | Condition/Notes                                  |
|------------------------------|--------------------------------|------------------------------------------------------------------------------------------------------|------------|------------------------|--------|--------------------------------------------------|
| Frequency Range              | F                              | 150                                                                                                  |            | 1400                   | MHz    | See Note 2                                       |
| Operating Temperature        | T <sub>A</sub>                 | (See ordering information)                                                                           |            |                        |        | See Note 1                                       |
| Storage Temperature          | T <sub>S</sub>                 | -55                                                                                                  |            | +125                   | °C     |                                                  |
| Frequency Stability          | ΔF/F                           |                                                                                                      | ±25        |                        | ppm    |                                                  |
| Aging                        |                                |                                                                                                      |            |                        |        |                                                  |
| 1st Year                     |                                | -3                                                                                                   |            | +3                     | ppm    |                                                  |
| Thereafter (per year)        |                                | -1                                                                                                   |            | +1                     | ppm    |                                                  |
| Pullability/APR              |                                | (See ordering information)                                                                           |            |                        |        | See Note 3                                       |
| Control Voltage              | V <sub>c</sub>                 | 0.18                                                                                                 | 0.90       | 1.62                   | V      | @ 1.8V V <sub>cc</sub>                           |
|                              |                                | 0.25                                                                                                 | 1.25       | 2.25                   | V      | @ 2.5V V <sub>cc</sub>                           |
|                              |                                | 0.30                                                                                                 | 1.65       | 3.0                    | V      | @ 3.3V V <sub>cc</sub>                           |
| Linearity                    |                                |                                                                                                      | 1          | 5                      | %      | Positive Monotonic                               |
| Modulation Bandwidth         | f <sub>m</sub>                 | 20                                                                                                   |            |                        | KHz    | -3 dB bandwidth                                  |
| Input Impedance              | Z <sub>in</sub>                | 500k                                                                                                 | 1M         |                        | Ohms   | @ DC                                             |
| Supply Voltage               | V <sub>cc</sub>                | 1.71                                                                                                 | 1.8        | 1.89                   | V      |                                                  |
|                              |                                | 2.375                                                                                                | 2.5        | 2.625                  | V      |                                                  |
|                              |                                | 3.135                                                                                                | 3.3        | 3.465                  | V      |                                                  |
| Input Current                | I <sub>cc</sub>                |                                                                                                      |            | 125                    | mA     | PECL/LVDS/CML                                    |
| Load                         |                                | 50 Ohms to (V <sub>cc</sub> - 2) V <sub>dc</sub><br>100 Ohm differential load                        |            |                        |        | See Note 4<br>PECL Waveform<br>LVDS/CML Waveform |
| Symmetry (Duty Cycle)        |                                | 45                                                                                                   |            | 55                     | %      | @ 50% of waveform                                |
| Output Skew                  |                                |                                                                                                      | TBD        |                        |        |                                                  |
| Differential Voltage         |                                | 350                                                                                                  | 425<br>TBD | 500                    | mVppd  | LVDS<br>CML                                      |
| Common Mode Output Voltage   | V <sub>cm</sub>                |                                                                                                      | 1.2        |                        | V      | LVDS                                             |
| Logic "1" Level              | V <sub>oh</sub>                | V <sub>cc</sub> - 1.02                                                                               |            |                        | V      | LVPECL                                           |
| Logic "0" Level              | V <sub>ol</sub>                |                                                                                                      |            | V <sub>cc</sub> - 1.63 | V      | LVPECL                                           |
| Rise/Fall Time               | T <sub>r</sub> /T <sub>f</sub> |                                                                                                      | 0.23       | 0.50                   | ns     | @ 20/80% LVPECL                                  |
| Enable Function              |                                | 80% V <sub>cc</sub> min. or N/C: output active<br>20% V <sub>cc</sub> max: output disables to high-Z |            |                        |        | Output Option G                                  |
|                              |                                | 20% V <sub>cc</sub> max: output active<br>80% V <sub>cc</sub> min: output disables to high-Z         |            |                        |        | Output Option M                                  |
| Start up Time                |                                |                                                                                                      | 10         |                        | ms     |                                                  |
| Phase Jitter<br>@ 622.08 MHz | φ <sub>J</sub>                 |                                                                                                      | 0.50       |                        | ps RMS | Integrated 12 kHz – 20 MHz                       |

Note 1: If the device is powered up below -20°C and then the ambient temperature rises 105°C during normal operation, the output will be interrupted for approximately 2-3 ms. A correction is in process and will be available Q1 2007

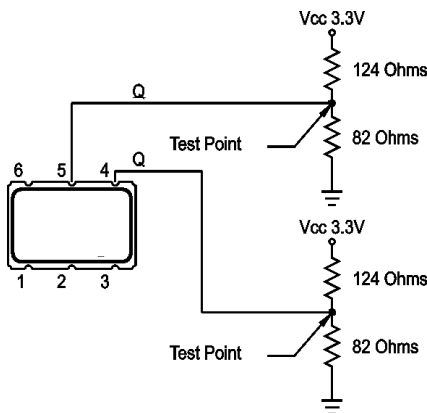
Note 2: Contact factory for exact frequency availability over 945 MHz.

Note 3: APR specification is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.

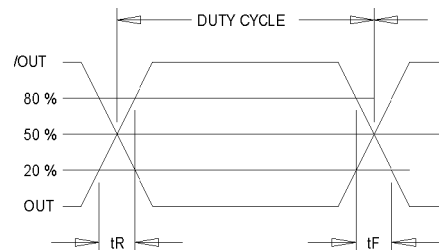
Note 4: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.



LVDS Load Circuit



3.3V LVPECL Load Circuit



Output Waveform: LVDS/CML/PECL

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