WM8742

24-bit 192 kHz DAC with Advanced Digital Filtering

DESCRIPTION

The WM8742 is a very high performance stereo DAC designed for audio applications such as professional recording systems, A/V receivers and high specification CD, DVD and home theatre systems. The device supports PCM data input word lengths from 16 to 32-bits and sampling rates up to 192kHz. The WM8742 also supports DSD bit-stream data format, in both direct DSD and PCM-converted DSD modes.

The WM8742 includes fine resolution volume and soft mute control, digital de-emphasis and a range of advanced digital filter responses, followed by a digital interpolation filter, multi-bit sigma delta modulator and stereo DAC. The architecture optimises the linearity of the DAC and provides maximum insensitivity to clock jitter.

The digital filters include several selectable roll-off and performance characteristics. The user can select between standard sharp or slow roll-off responses. In addition, the WM8742 includes a selection of advanced digital filter characteristics including non-half band filters and minimum phase filters.

This flexibility provides a range of benefits, such as significantly reduced pre-ringing and minimal group delay. The internal digital filters can also be by-passed and the WM8742 used with an external digital filter.

The WM8742 supports two connection schemes for audio DAC control. The 2/3 wire serial control interface provides access to all features. A range of features can also be accessed by hardware control interface.

The WM8742 is available in a convenient 28-SSOP package, and is pin compatible with the WM8740 and WM8741.

FEATURES

- Advanced Ultra High Performance Multi-bit Sigma-Delta Architecture
  - 126dB SNR ('A'-weighted mono @ 48kHz)
  - 123dB SNR ('A'-weighted stereo @ 48kHz)
  - 121dB SNR (non-weighted stereo @ 48kHz)
  - -100dB THD @ 48kHz
  - Differential analogue voltage outputs
  - High tolerance to clock jitter
- PCM Mode
  - Sampling frequency: 32kHz to 192kHz
  - Input data word length support: 16 to 32-bit
  - Supports all standard audio interface formats
  - Selectable advanced digital filter responses
    - Includes linear/minimum phase and range of tailored characteristics
    - Enables low pre-ringing, minimal latency
  - Optional interface to industry standard external filters
  - Digital volume control in 0.125dB steps with soft ramp and soft mute
  - Anti-clipping mode to prevent distortion even with input signals recorded up to 0dB
  - Selectable de-emphasis support
  - Zero Flag output
- DSD Mode
  - DSD bit-stream support for SACD applications
  - Support for normal or phase modulated bit-streams
  - Direct or PCM converted DSD paths (DSD Plus)
  - DSD mute
- Hardware or software control modes:
  - 2 and 3 wire serial control interface support
- Pin compatible with WM8740 and WM8741
- 4.5V to 5.5V analogue, 3.15V to 3.6V digital supply operation
- 28-lead SSOP Package

APPLICATIONS

- Professional audio systems
- CD, DVD, SACD audio
- Home theatre systems
- A/V receivers

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BLOCK DIAGRAM

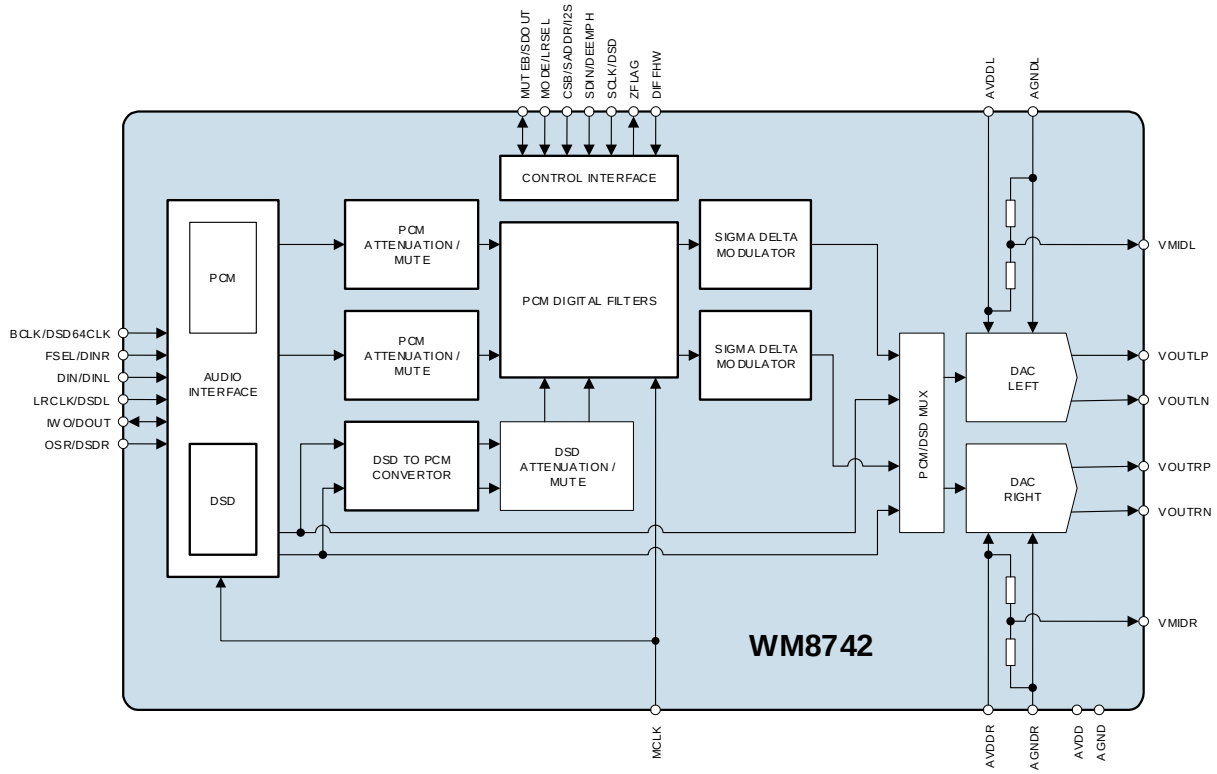
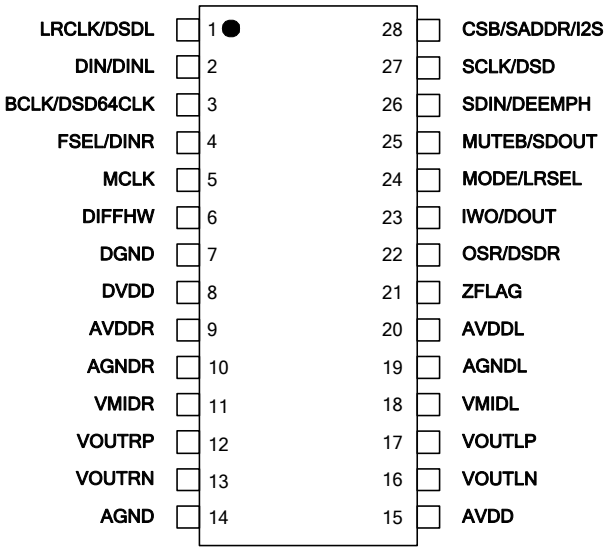


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PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	PEAK SOLDERING TEMPERATURE
WM8742GEDS/V	-0° to +70°C	28-lead SSOP (Pb-free)	260˚C
WM8742GEDS/RV	-0° to +70°C	28-lead SSOP (Pb-free, tape and reel)	260˚C

Note:

Reel Quantity = 2,000

PIN DESCRIPTION (SOFTWARE CONTROL MODE)

PIN	NAME	TYPE	DESCRIPTION		
			PCM MODE	8FS PCM MODE	DSD MODES
1	LRCLK / DSDL	Digital input	Audio interface left/right clock input	Audio interface left/right clock input	DSD left audio data in
2	DIN / DINL	Digital input	Audio interface data input	Audio interface left data input	Unused
3	BCLK / DSD64CLK	Digital input	Audio interface bit clock input	Audio interface bit clock input	64fs system clock input
4	FSEL / DINR	Digital input Tri-level	Unused	Audio interface right data input	Unused
5	MCLK	Digital input	Master clock input	Master clock input	Unused
6	DIFFHW	Digital input Internal pull-down	Differential mono mode selection 0 = normal operation 1 = differential mono mode	Differential mono mode selection 0 = normal operation 1 = differential mono mode	Differential mono mode selection 0 = normal operation 1 = differential mono mode
7	DGND	Supply	Digital ground	Digital ground	Digital ground
8	DVDD	Supply	Digital supply	Digital supply	Digital supply
9	AVDDR	Analogue Input	Right analogue positive reference	Right analogue positive reference	Right analogue positive reference
10	AGNDR	Analogue Input	Right analogue negative reference	Right analogue negative reference	Right analogue negative reference
11	VMIDR	Analogue Output	Right analogue midrail decoupling pin	Right analogue midrail decoupling pin	Right analogue midrail decoupling pin
12	VOUTRP	Analogue Output	Right DAC positive output	Right DAC positive output	Right DAC positive output
13	VOUTRN	Analogue Output	Right DAC negative output	Right DAC negative output	Right DAC negative output
14	AGND	Supply	Analogue ground	Analogue ground	Analogue ground
15	AVDD	Supply	Analogue supply	Analogue supply	Analogue supply
16	VOUTLN	Analogue Output	Left DAC negative output	Left DAC negative output	Left DAC negative output
17	VOUTLP	Analogue Output	Left DAC positive output	Left DAC positive output	Left DAC positive output
18	VMIDL	Analogue Output	Left analogue midrail decoupling pin	Left analogue midrail decoupling pin	Left analogue midrail decoupling pin
19	AGNDL	Analogue Input	Left analogue negative reference	Left analogue negative reference	Left analogue negative reference
20	AVDDL	Analogue Input	Left analogue positive reference	Left analogue positive reference	Left analogue positive reference
21	ZFLAG	Digital Output	Zero flag output	Zero flag output	Zero flag output
22	OSR/DSDR	Digital input Tri-level	Unused	Unused	DSD right audio data in
23	IWO / DOUT	Digital input/output	Buffered audio interface data output	Unused	Unused

PIN	NAME	TYPE	DESCRIPTION		
			PCM MODE	8FS PCM MODE	DSD MODES
24	MODE / LRSEL	Digital input, tri-level	When DIFFHW=0: 0 = hardware mode 1 = 3-wire software mode Z = 2-wire software mode When DIFFHW=1: 0 = left channel mono 1 = right channel mono	When DIFFHW=0: 0 = hardware mode 1 = 3-wire software mode Z = 2-wire software mode When DIFFHW=1: 0 = left channel mono 1 = right channel mono	When DIFFHW=0: 0 = hardware mode 1 = 3-wire software mode Z = 2-wire software mode When DIFFHW=1: 0 = left channel mono 1 = right channel mono
25	MUTEB / SDOUT	Digital input or output: Internal pull-up	Softmute Control 0 = mute active 1 = normal operation NOTE: In 3-wire mode only, this pin may be used as a buffered control interface data output	Softmute Control 0 = mute active 1 = normal operation	Softute Control 0 = mute active 1 = normal operation NOTE: In DSD Direct mode this is an analogue mute
26	SDIN / DEEMPH	Digital input Tri-level	Serial control interface data input	Serial control interface data input	Serial control interface data input
27	SCLK / DSD	Digital input	Serial control interface clock input	Serial control interface clock input	Serial control interface clock input
28	CSB / SADDR / I^2S	Digital input	3-wire mode: serial control interface latch 2-wire mode: device address select	3-wire mode: serial control interface latch 2-wire mode: device address select	3-wire mode: serial control interface latch 2-wire mode: device address select

Notes:

1. Undefined inputs should be connected to DVDD or DGND
2. Tri-level pins which require the 'Z' state to be selected should be left floating (open)

PIN DESCRIPTION (HARDWARE CONTROL MODE)

PIN	NAME	TYPE	DESCRIPTION	
			PCM MODE	DSD DIRECT MODE
1	LRCLK / DSDL	Digital input	Audio interface left/right clock input	DSD left audio data in
2	DIN / DINL	Digital input	Audio interface data input	Unused
3	BCLK / DSD64CLK	Digital input	Audio interface bit clock input	64fs system clock input
4	FSEL / DINR	Digital input Tri-level	Selects between one of three digital filters – see Table 50	Unused
5	MCLK	Digital input	Master clock input	Unused
6	DIFFHW	Digital input Internal pull-down	Differential mono mode selection 0 = normal operation 1 = differential mono mode	Differential mono mode selection 0 = normal operation 1 = differential mono mode
7	DGND	Supply	Digital ground	Digital ground
8	DVDD	Supply	Digital supply	Digital supply
9	AVDDR	Analogue Input	Right analogue positive reference	Right analogue positive reference
10	AGNDR	Analogue Input	Right analogue negative reference	Right analogue negative reference
11	VMIDR	Analogue Output	Right analogue midrail decoupling pin	Right analogue midrail decoupling pin
12	VOUTRP	Analogue Output	Right DAC positive output	Right DAC positive output
13	VOUTRN	Analogue Output	Right DAC negative output	Right DAC negative output
14	AGND	Supply	Analogue ground	Analogue ground
15	AVDD	Supply	Analogue supply	Analogue supply
16	VOUTLN	Analogue Output	Left DAC negative output	Left DAC negative output
17	VOUTLP	Analogue Output	Left DAC positive output	Left DAC positive output
18	VMIDL	Analogue Output	Left analogue midrail decoupling pin	Left analogue midrail decoupling pin
19	AGNDL	Analogue Input	Left analogue negative reference	Left analogue negative reference
20	AVDDL	Analogue Input	Left analogue positive reference	Left analogue positive reference
21	ZFLAG	Digital Output	Zero flag output	Unused
22	OSR/DSDR	Digital input Tri-level	Controls internal oversampling rate: 0 = low rate Z = medium rate 1 = high rate	DSD right audio data in
23	IWO / DOUT	Digital input/output	Controls audio interface wordlength – see Table 46	Unused

PIN	NAME	TYPE	DESCRIPTION	
			PCM MODE	DSD DIRECT MODE
24	MODE / LRSEL	Digital input, tri-level	When DIFFHW=0: 0 = hardware mode 1 = 3-wire software mode Z = 2-wire software mode When DIFFHW=1: 0 = left channel mono 1 = right channel mono	When DIFFHW=0: 0 = hardware mode 1 = 3-wire software mode Z = 2-wire software mode When DIFFHW=1: 0 = left channel mono 1 = right channel mono
25	MUTEB / SDOUT	Digital input or output: Internal pull-up	Softmute Control 0 = mute active 1 = normal operation	Analogue Mute Control 0 = mute active 1 = normal operation
26	SDIN / DEEMPH	Digital input Tri-level	De-emphasis Control 0 = normal operation 1 = de-emphasis applied Z = anti-clipping digital filter mode	Unused
27	SCLK / DSD	Digital input	HW Mode Select: 0 = PCM 1 = DSD Direct	HW Mode Select: 0 = PCM 1 = DSD Direct
28	CSB / SADDR / I^2S	Digital input	Controls audio interface format – see Table 46	Unused

Notes:

1. Undefined inputs should be connected to DVDD or DGND
2. Tri-level pins who require the 'Z' state to be selected should be left floating (open)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Digital supply voltage, DVDD	-0.3V	+4.5V
Analogue supply voltage, AVDD	-0.3V	+7V
Voltage range digital inputs	DGND - 0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND - 0.3V	AVDD + 0.3V
Master Clock Frequency		38.462MHz
Operating temperature range, T_A	-0°C	+70°C
Storage temperature	-65°C	+150°C
Ambient temperature (supplies applied)	-55°C	+125°C
Pb free package body temperature (soldering 10 seconds)		+260°C
Pb free package body temperature (soldering 2 minutes)		+183°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal resistance – junction to case	θ_{JC}			23.9		°C/W
Thermal resistance – junction to ambient	θ_{JA}			67.1		°C/W

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		3.15	3.3	3.6	V
Analogue supply range	AVDD		4.5	5	5.5	V
Ground	AGND, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Analogue operating current	I_{AVDD}	AVDD = 5V		55		mA
Digital operating current	I_{DVDD}	DVDD = 3.3V		40		mA
Analogue standby current	$I_{AVDD\ (Standby)}$	AVDD = 5V Clocks stopped		45		mA
Digital standby current	$I_{DVDD\ (Standby)}$	DVDD = 3.3V Clocks stopped		1.5		mA

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, 1kHz test signal, fs = 48kHz, MCLK = 512fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels						
Input LOW level	V_{IL}				0.3 x DVDD	V
Input HIGH level	V_{IH}		0.7 x DVDD			V
Output LOW level	V_{OL}	I_{OL} = 2mA			0.1 x DVDD	V
Output HIGH level	V_{OH}	I_{OH} = 2mA	0.9 x DVDD			V
DSD Input Characteristics						
DSD reference level		DSD Direct or DSD Plus Mode		0 50		dB_{DSD} %
DAC Performance						
Signal to Noise Ratio (Note 1)	SNR	A-weighted mono @ fs = 48kHz		126		dB
		A-weighted stereo @ fs = 48kHz	118	123		dB
		A-weighted stereo @ fs = 96kHz		121		dB
		A-weighted stereo @ fs = 192kHz		118		dB
		Non-weighted stereo @ fs = 48kHz		120		dB
Dynamic Range (Note 2)	DNR	A=weighted, -60dB full scale input		125		dB
Total Harmonic Distortion (Note 2)	THD	Mono 0dB @ fs = 48kHz		-100		dB
		Stereo 0dB @ fs = 48kHz		-100		dB
		Stereo 0dB @ fs = 96kHz		-100		dB
		Stereo 0dB @ fs = 192kHz		-100		dB
Channel Separation		1kHz		130		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.01		Degree
Power Supply Rejection Ratio	PSRR	100mVpp at 1kHz		-80		dB
		20Hz to 20kHz 100mVpp		-67		dB

TEST CONDITIONS

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25ºC, 1kHz test signal, fs = 48kHz, MCLK = 512fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Analogue Filter						
Bandwidth		-3dB		474		kHz
Passband edge response		20kHz		-0.0077		dB
Analogue Output Levels						
PCM full scale differential output level		Into 10kΩ load, 0dBFS input		2		V_{RMS}
DSD Direct differential output level		Into 10kΩ load, $0dB_{DSD}$ input		0.948		V_{RMS}
DSD Plus differential output level		Into 10kΩ load, $0dB_{DSD}$ input		0.991		V_{RMS}
Minimum resistance load		To midrail or AC coupled		2		kΩ
Maximum capacitance load				1		nF
Output DC level				AVDD/2		V
Reference Levels						
Potential divider resistance		AVDD to VMIDL/VMIDR and VMIDL/VMIDR to AGND		10		kΩ
Voltage at VMIDL/VMIDR				AVDD/2		V

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

MASTER CLOCK TIMING

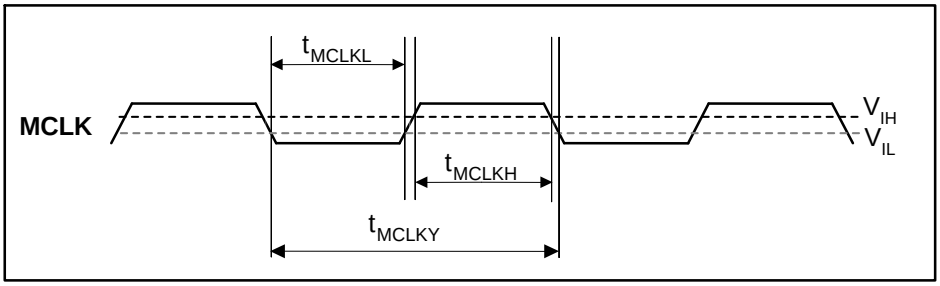


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing Information						
MCLK Master clock pulse width high	t_{MCLKH}		10			ns
MCLK Master clock pulse width low	t_{MCLKL}		10			ns
MCLK Master clock cycle time	t_{MCLKY}		27			ns
MCLK Duty cycle			40:60		60:40	

Table 1 MCLK Timing Requirements

PCM DIGITAL AUDIO INTERFACE TIMING

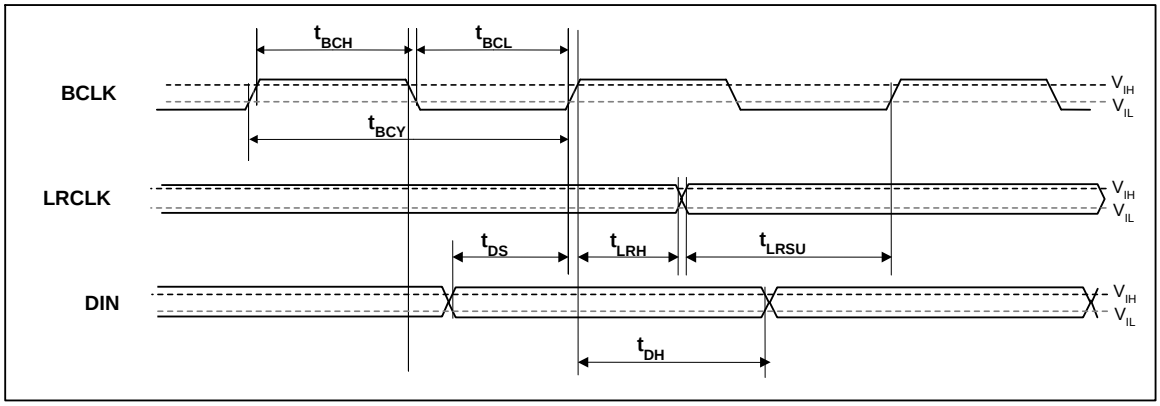


Figure 2 Digital Audio Data Timing

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		40			ns
BCLK pulse width high	t_{BCH}		16			ns
BCLK pulse width low	t_{BCL}		16			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}		8			ns
LRCLK hold time from BCLK rising edge	t_{LRH}		8			ns
DIN set-up time to BCLK rising edge	t_{DS}		8			ns
DIN hold time from BCLK rising edge	t_{DH}		8			ns

Table 2 Digital Audio Interface Timing Requirements

DSD AUDIO INTERFACE TIMING

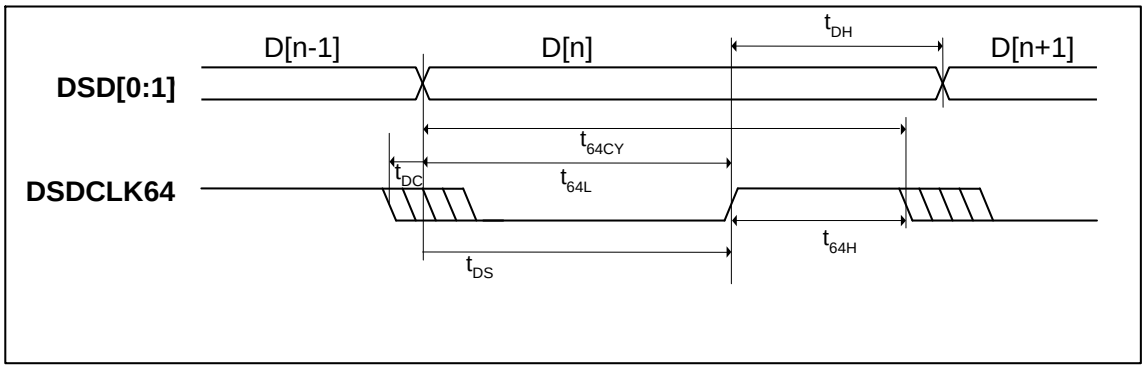


Figure 3 DSD Audio Timing - Normal Mode

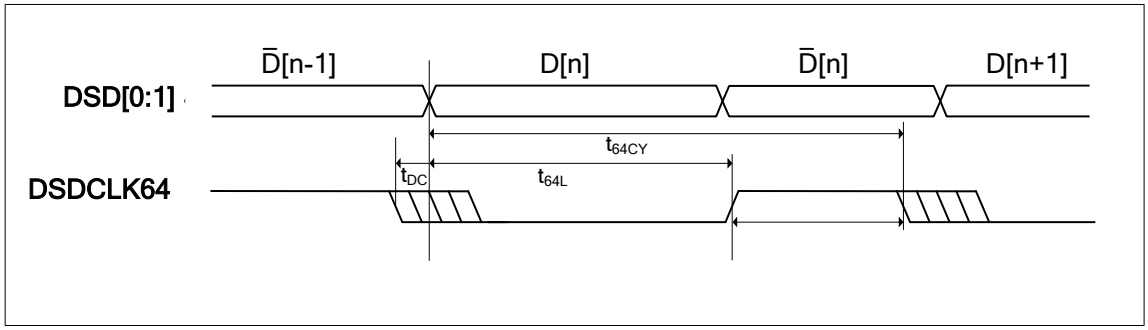


Figure 4 DSD Audio Timing - Phase Modulated Mode

Test Conditions

DVDD = 3.3V, GND = 0V, T_A = +25°C, fs = 44.1kHz, DSDCLK64 = 64fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
DSDCLK64 cycle time	t_{64CY}			354.3		ns
DSDCLK64 pulse width high	t_{64H}		140			ns
DSDCLK64 pulse width low	t_{64L}		140			ns
DSD[0:1] set-up time to DSDCLK64 rising edge	t_{DSN}		20			ns
DSD[0:1] hold time from DSDCLK64 rising edge	t_{DHN}		20			ns
Difference in edge timing of DSD[0:1] to DSDCLK64	t_{DC}		-10		10	ns

Table 3 DSD Audio Interface Timing Requirements

CONTROL INTERFACE TIMING – 3-WIRE MODE

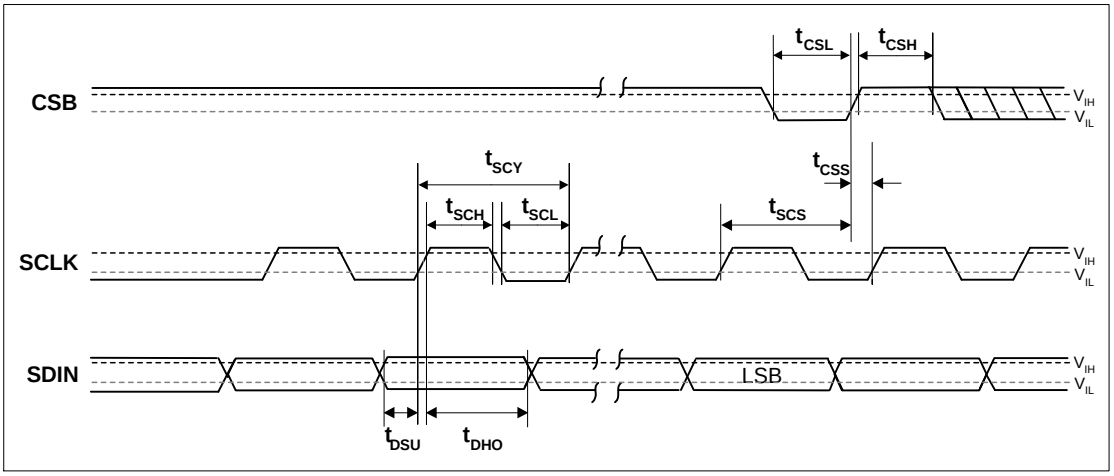


Figure 5 Control Interface Timing - 3-Wire Serial Control Mode

Test Conditions

DVDD = 3.3V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCLK rising edge to LATCH rising edge	t_{SCS}		40			ns
SCLK pulse cycle time	t_{SCY}		80			ns
SCLK pulse width low	t_{SCL}		32			ns
SCLK pulse width high	t_{SCH}		32			ns
SDIN to SCLK set-up time	t_{DSU}		20			ns
SCLK to SDIN hold time	t_{DHO}		20			ns
LATCH pulse width low	t_{CSL}		20			ns
LATCH pulse width high	t_{CSH}		20			ns
LATCH rising to SCLK rising	t_{CSS}		20			ns

Table 4 Control Interface Timing – 3-Wire Serial Control Mode

CONTROL INTERFACE TIMING – 2-WIRE MODE

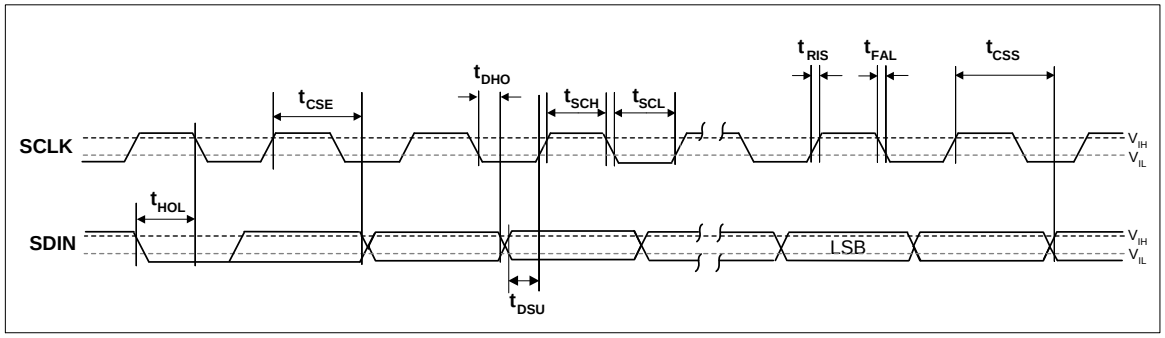


Figure 6 Control Interface Timing - 2-Wire Serial Control Mode

Test Conditions

DVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency		0		5	MHz
SCLK Low Pulse-Width	t_{SCL}	80			ns
SCLK High Pulse-Width	t_{SCH}	80			us
Hold Time (Start Condition)	t_{HOL}	600			ns
Setup Time (Start Condition)	t_{CSE}	600			ns
Data Setup Time	t_{DSU}	100			ns
SDIN, SCLK Rise Time	t_{RIS}			300	ns
SDIN, SCLK Fall Time	t_{FAL}			300	ns
Setup Time (Stop Condition)	t_{CSS}	600			ns
Data Hold Time	t_{DHO}			900	ns
Max Pulse width of spikes that will be suppressed	t_{PS}	4		6	ns

Table 5 Control Interface Timing – 2-wire Serial Control Mode

INTERNAL POWER ON RESET CIRCUIT

The WM8742 includes two internal Power On Reset (POR) circuits which are used to reset the digital logic into a default state after power up and to allow the analogue circuits to power-up silently.

The digital POR circuit is powered from DVDD. This circuit monitors DVDD and asserts the internal digital reset if DVDD are below the minimum DVDD threshold which will allow the digital logic to function.

The analogue POR circuit is powered from AVDD. The circuit monitors AVDD, tri-stating the DAC outputs and isolating the internal reference resistor strings from AVDDL and AVDDR until there is sufficient AVDD voltage to allow the analogue DAC stages to function correctly.

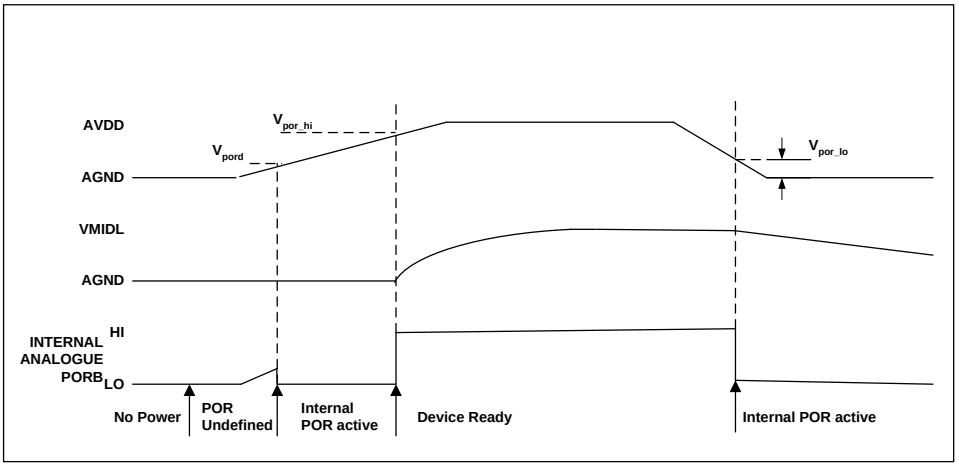


Figure 7 AVDD Power up Sequence

Test Conditions

AVDD = 5V, AGND = 0V, T_A = +25ºC, T_{A_max} = +125ºC, T_{A_min} = -25ºC, $AVDD_{max}$ = 5.5V, $AVDD_{min}$ = 4.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
AVDD level to POR rising edge (AVDD rising)	V_{por_hi}	Measured from AGND		2.00		V
AVDD level to POR falling edge (AVDD falling)	V_{por_lo}	Measured from AGND		1.84		V

Table 6 Analogue POR Timing

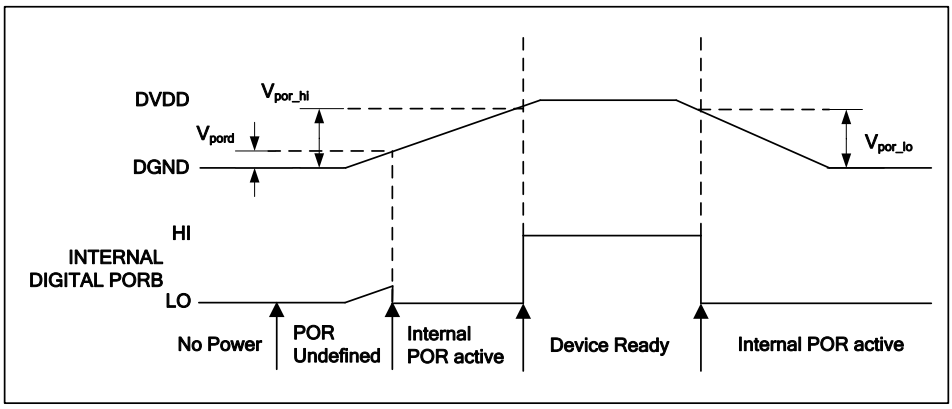


Figure 8 DVDD Power up Sequence

Test Conditions

DVDD = 3.3V, DGND = 0V, T_A = +25ºC, T_{A_max} = +125ºC, T_{A_min} = -25ºC, $DVDD_{max}$ = 3.6V, $DVDD_{min}$ = 3.0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
DVDD level to POR rising edge (DVDD rising)	V_{por_hi}	Measured from DGND		1.86		V
DVDD level to POR falling edge (DVDD falling)	V_{por_lo}	Measured from DGND		1.83		V

Table 7 Digital POR Timing

In a real application the designer is unlikely to have control of the relative power up sequence of AVDD and DVDD. The POR circuit ensures a reasonable delay between applying power to the device and Device Ready.

Figure 7 and Figure 8 show typical power up scenarios in a real system. DVDD must be established before the device can be written to. Any writes to the device before device ready will be ignored.

Note: DVDD must be established before the MCLK is started. This will ensure all synchronisation circuitry within the device is fully initialised and ready.

AVDD must be established before the device will output any signal. Whilst the device will output signal as soon as the Internal Analogue PORB indicates device ready, normal operation is not possible until the VMID pin has reached the midrail voltage.

DEVICE DESCRIPTION

INTRODUCTION

The WM8742 is an ultra high performance DAC designed for digital audio applications. Its range of features makes it ideally suited for use in professional recording environments, CD/DVD players, AV receivers and other high-end consumer audio equipment.

The WM8742 is a complete differential stereo audio digital-to-analogue converter. The system includes a dithered digital interpolation filter, fine resolution volume control and digital de-emphasis, followed by a multi-bit sigma delta modulator and switched capacitor multi-bit stage with differential voltage outputs. The device supports both PCM and DSD digital audio input formats.

The WM8742 includes a configurable digital audio interface support for a 3-wire and 2-wire serial control interface, and a hardware control interface. The software control interface may be asynchronous to the audio data interface; in which case control data will be re-synchronised to the audio processing internally. It is fully compatible with, and an ideal partner for, a range of industry standard microprocessors, controllers and DSPs.

Uniquely, the WM8742 has a large range of high performance low latency advanced digital filters. The full range of filters is selectable in software mode, and a limited range of filters are available under hardware control. The filters allow users the flexibility to choose characteristics to match their group delay, phase and latency requirements.

Operation using a master clock of 128fs, 192fs, 256fs, 384fs, 512fs or 768fs is supported. Sample rates (fs) from 32kHz to 192kHz are allowed, provided the appropriate master clock is input (see Table 11 for details).

In normal PCM mode, the audio data interface supports right justified, left justified and I^2S interface formats along with a highly flexible DSP serial port interface.

There are two DSD modes. In DSD Direct mode, the datastream is subjected to the minimum possible processing steps between input and output. In DSD Plus mode, the datastream is converted to PCM and filtered to allow reduction of out of band components. This step also provides additional benefits in allowing access to other PCM features such as volume control and advanced digital filtering.

The device is packaged in a small 28-lead SSOP.

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin with no software configuration necessary for sample rate selection.

MCLK is used to derive clocks for the DAC path in PCM mode. The DAC path consists of DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

CONTROL INTERFACE

The WM8742 supports 2-wire and 3-wire serial control, and hardware control. Selection of control mode is made by controlling the state of the MODE pin.

PIN	NAME	DESCRIPTION
24	MODE/ LRSEL	0 = Hardware control mode 1 = 3-wire serial control mode Z = 2-wire serial control mode

Table 8 Control Mode Configuration

SOFTWARE CONTROL INTERFACE

The software control interface may be operated using a 2-wire or 3-wire (SPI-compatible) serial interface. When operating under serial control, hardware configuration pins are ignored.

Note: DIFFHW will override all other pins, forcing the device into hardware control mode and differential mono mode.

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

Every rising edge of SCLK clocks in one bit of data on SDIN. A rising edge on CSB latches a complete control word consisting of 16 bits. The 3-wire interface protocol is shown in Figure 9.

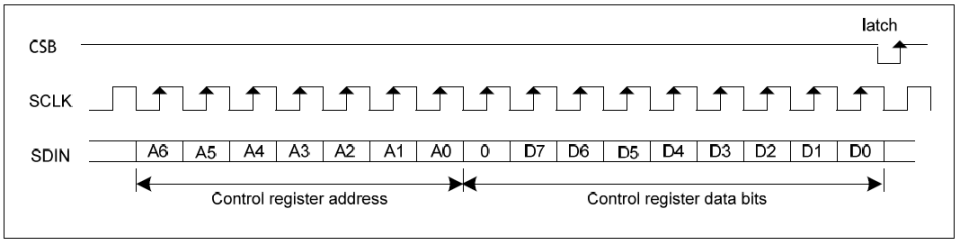


Figure 9 3-wire Serial Interface Protocol

Notes:

1. A[6:0] are Control Address Bits
2. D[7:0] are Control Data Bits
3. D[8] is always set to zero

3-WIRE CONTROL INTERFACE DAISY CHAINING

In daisy chaining mode, SDOUT (pin 25) outputs control data sampled on SDIN with a delay of 16 SCLK cycles. This data signal can be used to control another WM8742 in a daisy chain circuit as shown in Figure 10.

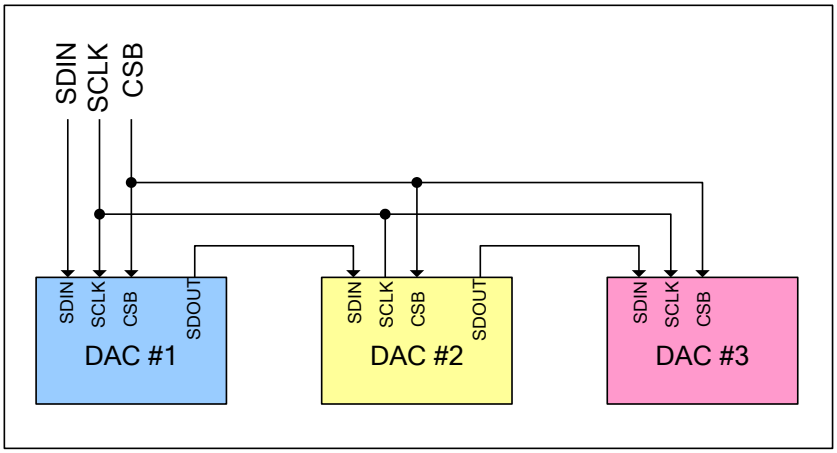


Figure 10 Control Interface Daisy Chaining Setup

To configure devices into daisy chain mode the CSB signal should be driven low while there is a register write to set register bit SDOUT=1. CSB should then be driven high, this sets the first device in daisy chain mode. CSB should then be driven low again while register bit SDOUT is set high. Setting CSB high again will cause the first register write to be output to the second device from the SDOUT pin, this sets the second device into daisy chain mode. This method must be repeated for the number

of devices in the chain until they are all set into daisy chain mode. Figure 11 shows the protocol for configuring the first two devices in the daisy chain.

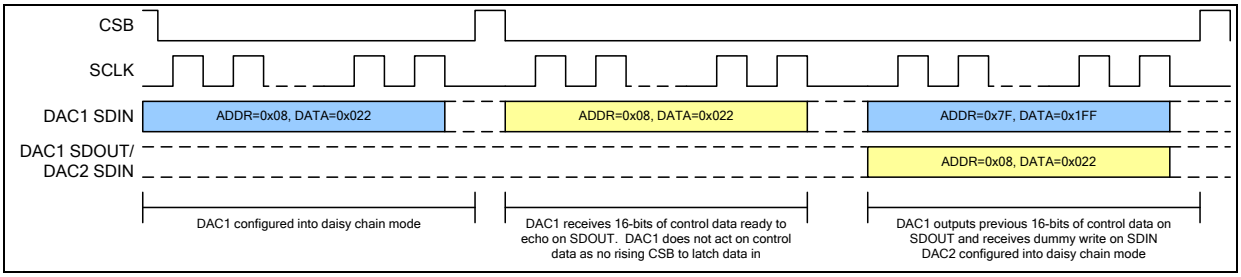


Figure 11 Initial Setup of Two WM8742 Devices into Control Interface Daisy Chain Mode

To write to a single device in the chain a complete sequence needs to be written to all the devices. Devices that do not require a register change must also be written to. The user can choose to write either the same data as the previous write, or write all 1s for the register address and data. All 1s will result in writing to a non-existent register, address 7Fh, preserving the current register settings. Figure 12 shows an example of how to access three WM8742 devices (the devices have all previously been configured in daisy chain mode):

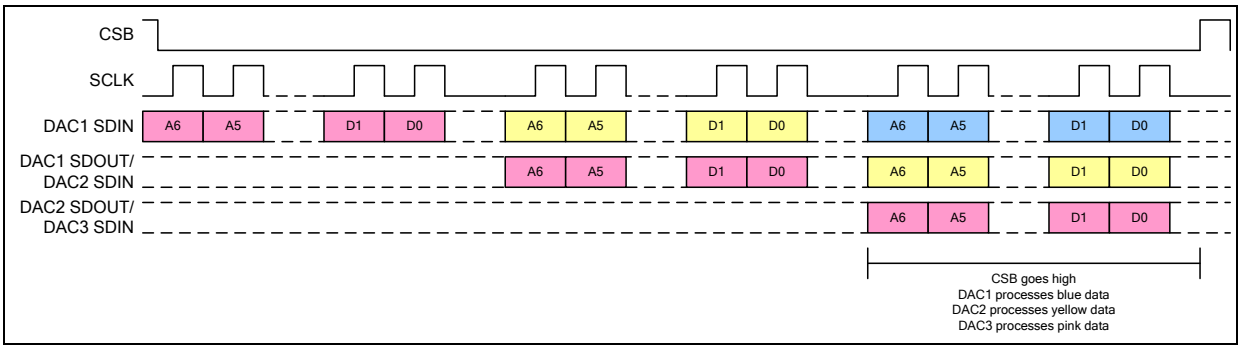


Figure 12 Daisy Chain Control Interface Example for Three WM8742 Devices

To ensure that only valid data is written to the devices in daisy chain mode, a pull up resistor is used in SDOUT. When connected to the SDIN pin of the next device in the chain, this results in all ones being written to the control interface of that device until the correct daisy chain data is written and latched.

Serial daisy chaining is available only when using 3-wire serial control mode. It is not available in 2-wire serial control mode or hardware control mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 Mode Control 2 08h	5	SDOUT	0	3 wire Serial Interface Daisy Chaining 0 = No Output 1 = Output on pin 25.

Table 9 Control Interface Daisy Chaining Selection

2-WIRE SERIAL CONTROL MODE

The WM8742 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8742).

The WM8742 operates as a slave device on the 2-wire control bus. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8742 and the R/W bit is '0', indicating a write, then the WM8742 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1', the WM8742 returns to the idle condition and wait for a new start condition and valid address.

Once the WM8742 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8742 register address plus the first bit of register data). The WM8742 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8742 acknowledges again by pulling SDIN low.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8742 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device reverts to the idle condition.

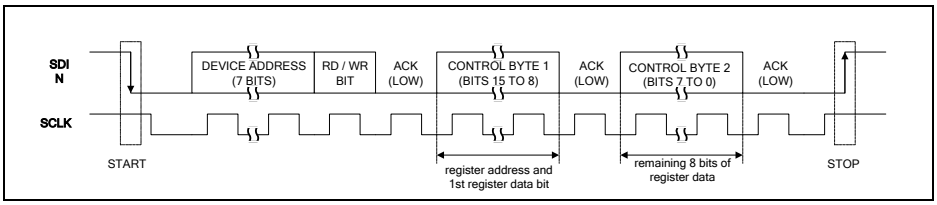


Figure 13 2-wire Serial Control Interface

The WM8742 device address can be configured between two options. This is selected by the SADDR pin.

PIN	NAME	DESCRIPTION
28	CSB/ SADDR/I²S	0 = 2-wire address 0011010 1 = 2-wire address 0011011

Table 10 2-wire Serial Control Mode Address Selection

DIGITAL AUDIO INTERFACE

PCM MODE

There are a number of valid PCM data input modes. Two channel and one channel differential mono modes can be selected by serial or hardware control. It is also possible to bypass the WM8742 digital filters and apply a signal at a rate 8fs (where fs is the sampling rate) directly to the switched capacitor stage.

PCM DIGITAL AUDIO INTERFACE

Audio data is applied to the DAC system via the Digital Audio Interface. Five popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I^2S mode
- DSP mode A
- DSP mode B

All five formats require the MSB to be transmitted first, and support word lengths of 16, 20, 24 and 32 bits, with the exception that 32 bit data is not supported in right justified mode. DIN and LRCLK may be configured to be sampled on the rising or falling edge of BCLK by adjusting register bits LRP and BCP.

In left justified, right justified and I^2S audio interface modes, the digital audio interface receives data on the DIN input pin. Stereo audio data is time multiplexed on DIN, with LRCLK indicating whether the left or right channel is present. LRCLK is also used as a timing reference to indicate the beginning or end of the data words.

The minimum number of BCLK periods per LRCLK period is two times the selected word length. LRCLK must be high for a period equal to the minimum number of BCLK periods, and low for a minimum of the same period. Any mark-to-space ratio on LRCLK is acceptable provided the above requirements are met.

The WM8742 will automatically detect when data with a LRCLK period of exactly 32 BCLKs is received, and select 16-bit mode. This overrides any previously programmed word length. The operating word length will revert to a programmed value only if a LRCLK period other than 32 BCLKs is detected.

In DSP mode A or DSP mode B, the data is time multiplexed onto DIN. LRCLK is used as a frame sync signal to identify the MSB of the first word. The minimum number of BCLKs per LRCLK period is two times the selected word length. Any mark to space ratio is acceptable on LRCLK provided the rising edge is correctly positioned.

LEFT JUSTIFIED MODE

In left justified mode, the MSB is sampled on the first rising edge of BCLK following a LRCLK transition. LRCLK is high during the left data word and low during the right data word.

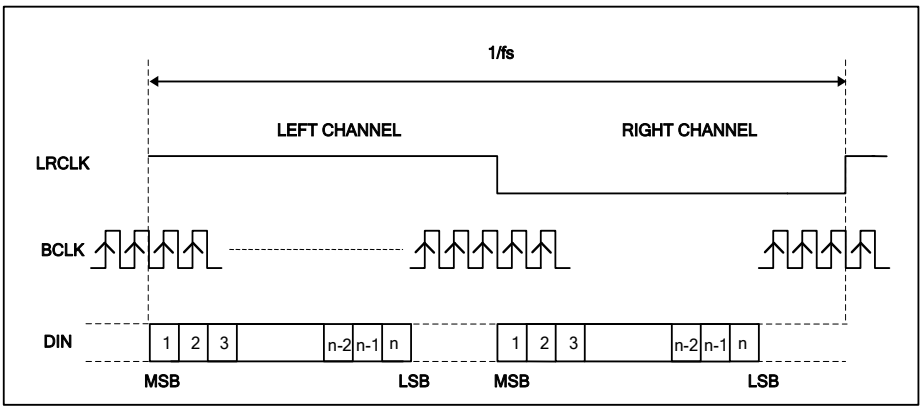


Figure 14 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB is sampled on the rising edge of BCLK preceding a LRCLK transition. LRCLK is high during the left data word and low during the right data word.

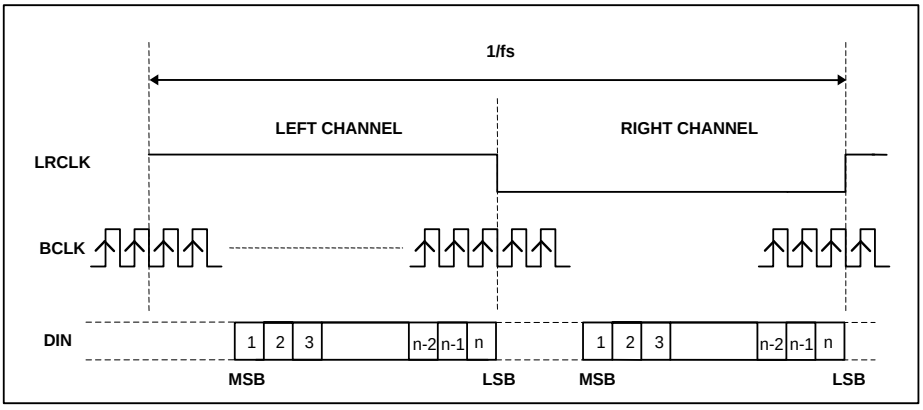


Figure 15 Right Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB is sampled on the second rising edge of BCLK following a LRCLK transition. LRCLK is low during the left data word and high during the right data word.

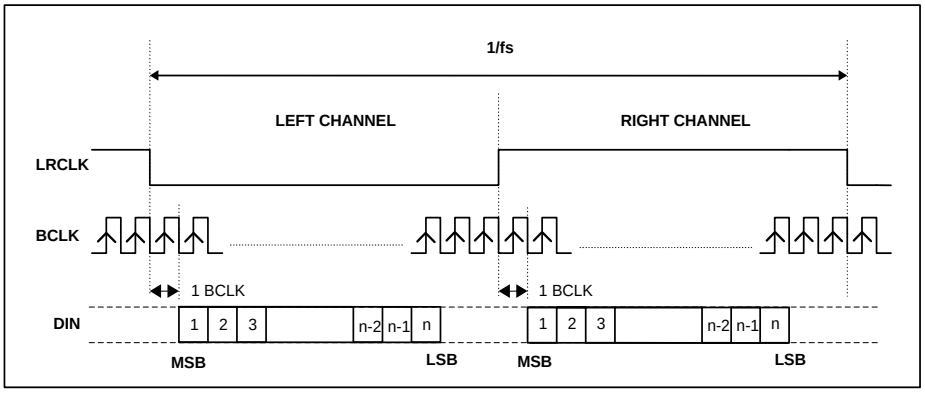


Figure 16 I²S Mode Timing Diagram

DSP MODE A

In DSP mode A, the first bit is sampled on the BCLK rising edge following the one that detects a low to high transition on LRCLK. No BCLK edges are allowed between the data words. The word order is DIN left, DIN right.

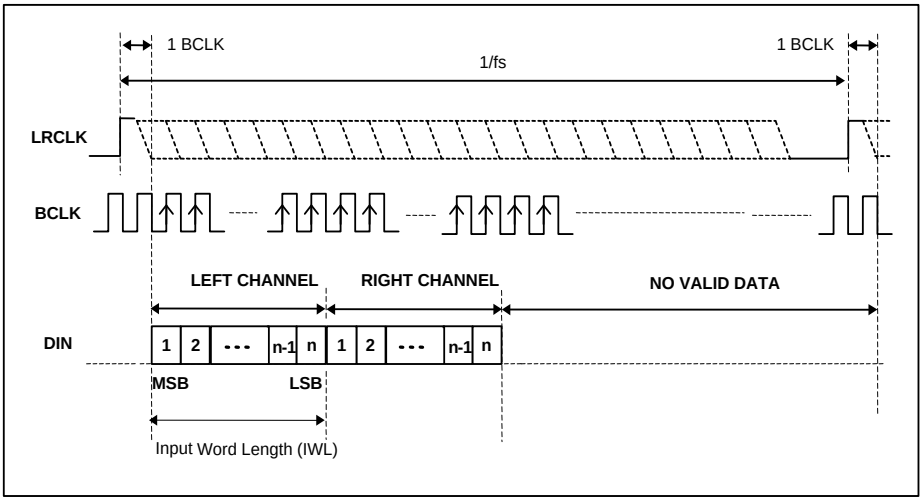


Figure 17 DSP Mode A Timing Diagram

DSP MODE B

In DSP mode B, the first bit is sampled on the BCLK rising edge, which detects a low to high transition on LRCLK. No BCLK edges are allowed between the data words. The word order is DIN left, DIN right.

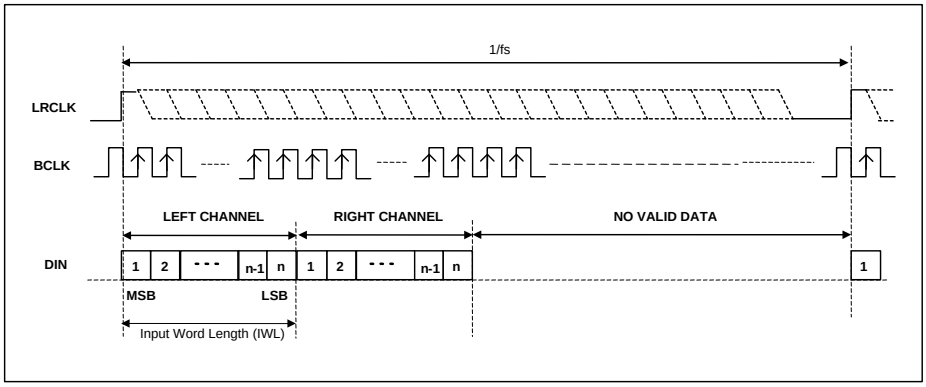


Figure 18 DSP Mode B Timing Diagram

PCM MODE SAMPLING RATES

The WM8742 supports master clock rates of 128fs to 768fs, where fs is the audio sampling frequency (LRCLK), typically 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz or 192kHz.

The WM8742 has a master clock detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate. The master clock should be synchronised with LRCLK, although the WM8742 is tolerant of phase differences or jitter on this clock.

SAMPLING RATE (LRCLK)	MASTER CLOCK (MCLK) FREQUENCY (MHZ)					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	Unavailable	Unavailable	8.192	12.288	16.384	24.576
44.1kHz	Unavailable	Unavailable	11.2896	16.9344	22.5792	33.8688
48kHz	Unavailable	Unavailable	12.288	18.432	24.576	36.864
88.2kHz	11.2896	16.9344	22.5792	33.8688	Unavailable	Unavailable
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
176.4kHz	22.5792	33.8688	Unavailable	Unavailable	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 11 Typical Relationships Between Master Clock Frequency and Sampling Rate in normal PCM mode

8FS MODE

Operation in 8FS mode requires that audio data for left and right channels is input separately on two pins. DINR (pin 4) is the input for right channel data and DINL (pin 2) is the input for left channel data. Hardware control of the device is not available.

The data can be input in two formats (left or right justified), selectable by register FMT[1:0], and two word lengths (20 or 24 bit), selectable by register IWL[1:0]. In both modes the data is clocked into the WM8742 MSB first.

For left justified data the word start is identified by the falling edge of LRCLK. The data is clocked in on the next 20/24 BCLK rising edges. This format is compatible with industry-standard DSPs and decoders such as the PMD100.

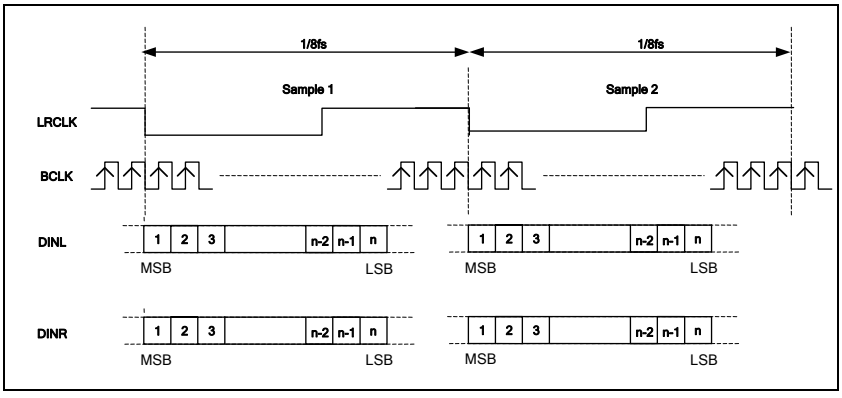


Figure 19 8FS Mode Left Justified Timing Requirements

For right justified mode, the data is justified to the rising edge of LRCLK and the data is clocked in on the preceding 20/24 BCLK rising edges before the LRCLK rising edge. This format is compatible with industry standard DSPs and decoders such as the DF1704 or SM5842.

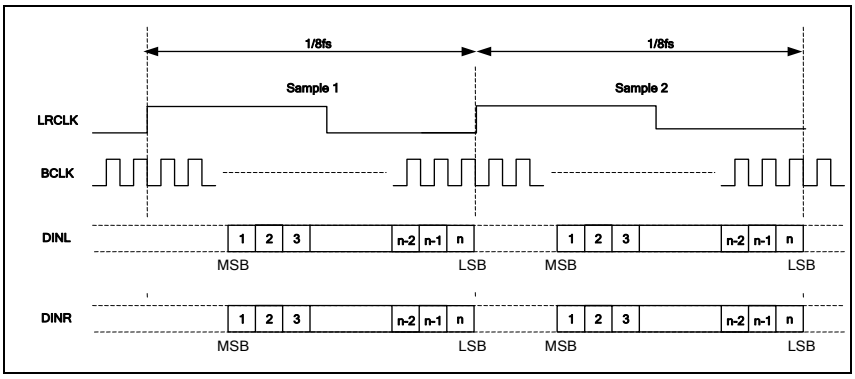


Figure 20 8FS Mode Right Justified Timing Requirements

In both modes the polarity of LRCLK can be switched using register bit LRP.

8FS MODE SAMPLING RATES

Since the data rate in 8FS mode is much faster than in standard PCM mode, there are restrictions on the MCLK rate that can be used. Specifically, only 512fs and 768fs modes are permitted restricting the sample rate to a maximum of 8x48kHz. The master clock should be synchronised with LRCLK, although the WM8742 is tolerant of phase differences or jitter on this clock.

Unlike in normal PCM mode, the master clock detection circuit does not operate in 8FS mode. The rate must be manually programmed using the control interface.

SAMPLING RATE	LRCLK FREQUENCY (kHz)	MASTER CLOCK (MCLK) FREQUENCY (MHz)	
fs	**8fs**	**512fs**	**768fs**
32kHz	256	16.384	24.576
44.1kHz	352.8	22.5792	33.8688
48kHz	384	24.576	36.864

Table 12 Typical Relationships Between Master Clock Frequency and Sampling Rate in 8FS Mode

AUDIO INTERFACE DAISY CHAINING

In daisy chain mode the DOUT pin outputs the audio data received on the DIN pin but delayed by two times the input word length. When this output is connected to the DIN pin of the next device in the chain, each WM8742 device will simultaneously sample different channel data in the same LRCLK period. Daisy chaining is only available in DSP audio interface mode and is limited by a maximum BCLK frequency of 24.576MHz.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 Mode Control 2 08h	4	DOUT	0	Daisy Chaining Multiple devices – multichannel off one PCM feed. 0 = No Output 1 = Output on pin 23.

Table 13 Daisy Chaining Audio Data Output Control

The following diagram illustrates timing for a daisy chain with 2 WM8742 devices.

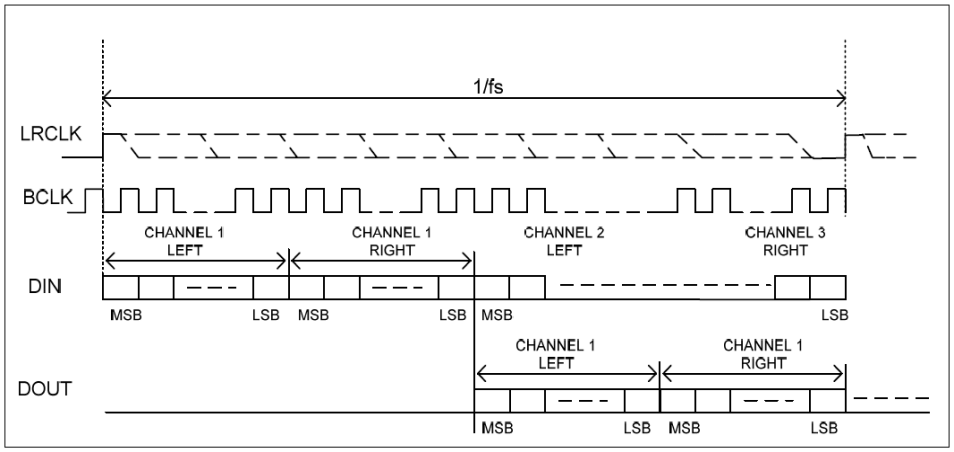


Figure 21 Audio Interface Daisy Chaining Timing

DSD MODE

The WM8742 supports DSD input bitstreams at 64x the oversampling rate. The data is supplied at a rate of 64 bits per normal word clock. In DSD, no word clock is provided.

The WM8742 supports two channels of bitstream or DSD audio. Data bitstreams and the 64fs clock are supplied to pins 1, 22 and 3 respectively. The MODESEL[1:0] register bits control whether the device operates in DSD direct, DSD plus or PCM modes.

DSD DIRECT

In DSD Direct mode the internal digital filters are bypassed, the input bitstream data is subjected to the minimal possible processing and is applied directly to the switched capacitor stage of the DAC system. Using this mode provides the purest possible representation of a DSD stream.

It is normally desirable to use an external analogue post-DAC analogue filter to combine the differential outputs of the DAC and remove high frequency energy from the output. This is particularly important in the case of DSD operation due to the presence of high frequency energy which is a result of the aggressive high order noise shaping used in the creation of the modulated DSD datastream.

DSD PLUS MODE

In DSD Plus mode the DSD data can be filtered in a similar manner to the data in the PCM path. The DSD Plus filters are selected using register bits DSDFILT[1:0]. DSD Plus mode is not available under hardware control.

Although DSD Plus mode requires that the bitstream is more heavily processed than DSD Direct, the advantage is that DSD Plus mode reduces the high frequency energy which is a result of the aggressive high order noise shaping used in the creation of the modulated DSD datastream. This means that a less aggressive, lower order, analogue filter can be used at the output. Furthermore the slew-rate requirements of the op-amps can be relaxed compared to DSD direct mode, due to the reduction in high frequency energy.

DSD DIGITAL AUDIO INTERFACE

DSD audio data is input to the WM8742 via the DSD digital audio interface. Two interface formats are supported:

- Uni-phase
- Bi-phase

To use this interface apply left data on input pin 1 (LRCLK/DSDL) and pin 22 (OSR/DSDR). A DSD clock is also required, running at 64FS, and should be applied to pin 3 (BCLK/DSD64CLK).

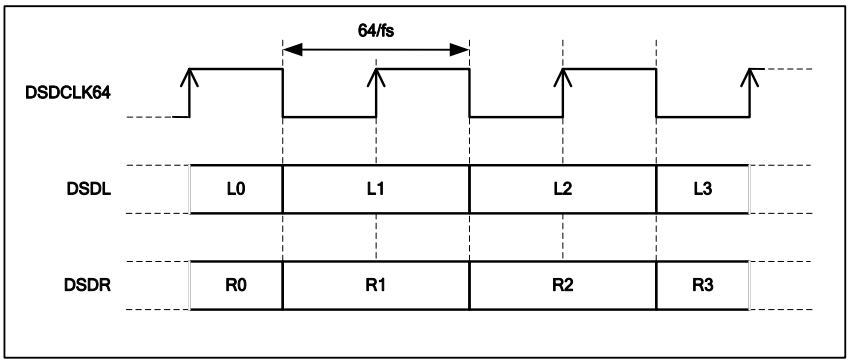


Figure 22 Uni-phase DSD Mode Timing Diagram

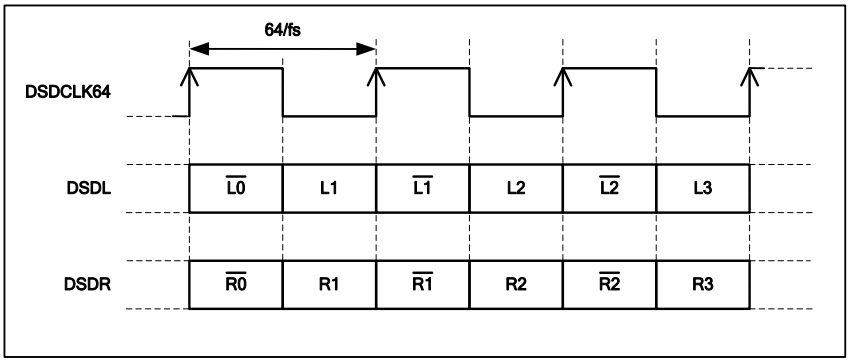


Figure 23 Bi-phase DSD Mode Timing Diagram

SOFTWARE CONTROL MODE

Software control allows access to all features of the WM8742. Selection of control mode is achieved by configuring the state of MODE/LRSEL (pin 24):

PIN	NAME	DESCRIPTION
24	MODE/ LRSEL	0 = Hardware control mode 1 = 3-wire serial control mode Z = 2-wire serial control mode

Table 14 Control Mode Configuration

DSD AND PCM MODE SWITCHING

The audio interface mode can be switched between DSD and PCM by writing MODESEL[1:0] in R7. It is recommended that the chip is forced into a MUTE state before dynamically switching modes.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Mode Control 1 07h	[1:0]	MODESEL	00	DSD/PCM mode select : 00 = PCM mode 01 = Direct DSD Operation 10 = DSD plus mode 11 = Unused

Table 15 PCM/DSD Software Mode Selection

PCM DIGITAL AUDIO INTERFACE CONTROL REGISTERS

The PCM digital audio input format is configured by register bits FMT [1:0] and IWL[1:0]:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 Format Control 05h	1:0	IWL[1:0]	10	Audio interface input word length select 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit
	3:2	FMT[1:0]	10	Audio interface input format select 00 = Right justified 01 = Left justified 10 = I^2S 11 = DSP

Table 16 Interface Format Controls

Note:

1. In all modes, the data is signed 2's complement. The WM8742 digital filters always input 24-bit data. If the interface is programmed into 32 bits, dither is applied according to Table 37 before truncation to the internal wordlength.

LRCLK POLARITY

In left justified, right justified or I²S modes, the LRP register bit controls the polarity of LRCLK. If this bit is set high, the expected polarity of LRCLK will be the opposite of that shown in Figure 14, Figure 15 and Figure 16. If this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 Format Control 05h	4	LRP	0	LRCLK polarity select: 0 = normal LRCLK polarity 1 = inverted LRCLK polarity

Table 17 LRCLK Polarity Control

In DSP modes, the LRP register bit is used to select between DSP mode A and B (see Figure 17 and Figure 18).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 Format Control 05h	4	LRP	0	DSP format select: 0 = DSP mode A 1 = DSP mode B

Table 18 DSP Format Control

BCLK / DSDCLK64 POLARITY

In PCM mode, LRCLK and DIN are sampled on the rising edge of BCLK by default, and should ideally change on the falling edge. Data sources which change LRCLK and DIN on the rising edge of BCLK can be supported by setting the BCP register bit. Setting BCP to 1 inverts the polarity of BCLK to the inverse of that shown in Figure 14, Figure 15, Figure 16, Figure 17 and Figure 18.

In DSD mode, DSDL and DSDR inputs are sampled a fixed delay after a falling 64fs clock edge. When BCP is set in DSD mode, DSDL and DSDR are sampled a fixed delay after a rising 64fs clock edge.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 Format Control 05h	5	BCP	0	BCLK / DSD64CLK polarity select: 0 = normal polarity 1 = inverted polarity

Table 19 BCLK Polarity Control

OVERSAMPLING RATE CONTROL

The user has control of the oversampling ratio of the WM8742, and can set to the device to operate in low, medium or high rate modes. For correct operation of the digital filtering and other processing on the WM8742, the user must ensure the correct value of OSR[1:0] is set at all times.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Mode Control 1 07h	[6:5]	OSR[1:0]	00	Oversampling Rate Selection 00 = Low rate (32/44.1/48kHz) 01 = Medium rate (96kHz) 10 = High rate (192kHz) 11 = Unused

Table 20 Oversampling Rate Control

MCLK/LRCLK RATIO CONTROL (NORMAL PCM MODE)

The ratio of MCLK/LRCLK can be programmed directly or auto-detected.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Mode Control 1 07h	[4:2]	SR[3:0]	000	MCLK to LRCLK sampling rate ratio control (Normal PCM Mode): 000 = auto detect sample rate 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = reserved

Table 21 MCLK/LRCLK Ratio Control (Normal PCM Mode)

8FS MODE

8FS Mode allows the use of custom digital filters by bypassing the WM8742 internal digital filters. When MODE8X is set, the PCM data input to the WM8742 is applied only to the digital volume control and then the analogue section of the DAC system, bypassing the digital filters.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Format Control 07h	7	MODE8X	0	8FS mode select: 0 = Normal operation 1 = 8FS mode (digital filters bypassed)

Table 22 8FS Mode Control

MCLK/LRCLK RATIO CONTROL (8FS MODE)

In 8FS mode the choice of clock ratios and sampling rates is limited – see Table 12 for details. Autodetect of MCLK/LRCLK ratio is not available in 8FS mode and must be set manually by the user for correct operation.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Mode Control 1 07h	[4:2]	SR[2:0]	000	MCLK to LRCLK sampling rate ratio control (8FS Mode): 000 = reserved 001 = 512fs 010 = 768fs 011 to 111 = reserved

Table 23 MCLK/LRCLK Ratio Control (8FS Mode)

ATTENUATION CONTROL

Each DAC channel can be attenuated digitally before being applied to the digital filter. Attenuation is set to 0dB by default but can be set between 0dB and -127.5dB in 0.125dB steps using the ten attenuation control bits LAT[4:0], LAT[9:5], RAT[4:0] and RAT[9:5].

All attenuation registers are double latched allowing new values to be pre-latched to both channels before being updated synchronously. Setting the UPDATE bit on any attenuation write will cause all pre-latched values to be immediately applied to the DAC channels.

REGISTER ADDRESS	BITS	LABEL	DEFAULT	DESCRIPTION
R0 DACLLSB Attenuation 00h	[4:0]	LAT[4:0]	00 (0dB)	LSBs of attenuation data for left channel in 0.125dB steps. See Table 25 for details.
	5	UPDATE	0	Attenuation data load control for left channel. 0 = Store LAT[4:0] value but don't update 1 = Store LAT[4:0] and update attenuation on registers 0-3
R1 DACLMSB Attenuation 01h	[4:0]	LAT[9:5]	00 (0dB)	MSBs of attenuation data for left channel in 4dB steps. See Table 25 for details.
	5	UPDATE	0	Attenuation data load control for left channel. 0 = Store LAT[9:5] value but don't update 1 = Store LAT[9:5] and update attenuation on registers 0-3
R2 DACRLSB Attenuation 02h	[4:0]	RAT[4:0]	00 (0dB)	LSBs of attenuation data for right channel in 0.125dB steps. See Table 25 for details.
	5	UPDATE	0	Attenuation data load control for right channel. 0 = Store RAT[4:0] value but don't update 1 = Store RAT[4:0] and update attenuation on registers 0-3
R3 DACRMSB Attenuation 03h	[4:0]	RAT[9:5]	00 (0dB)	MSBs of attenuation data for right channel in 4dB step. See Table 25 for details.
	5	UPDATE	0	Attenuation data load control for right channel. 0 = Store RAT[9:5] value but don't update 1 = Store RAT[9:5] and update attenuation on registers 0-3

Table 24 Attenuation Control

Note:

1. The UPDATE bit is not latched. If UPDATE=0, the attenuation value will be written to the pre-latch but not applied to the relevant DAC. If UPDATE=1, all pre-latched values and the current value being written will be applied on the next input sample.

DAC OUTPUT ATTENUATION

Registers LAT[9:0] and RAT[9:0] control the left and right channel attenuation. Table 25 shows how the attenuation levels are configured by the 10-bit words.

L/RAT[9:0]	ATTENUATION LEVEL
000(hex)	0dB
001(hex)	-0.125dB
:	:
:	:
:	:
3FE(hex)	-127.75dB
3FF(hex)	-∞dB (mute)

Table 25 Attenuation Control Levels

ATTENUATION CONTROL MODE

Setting the ATC register bit causes the left channel attenuation settings to be applied to both left and right channel DACs from the next audio input sample. No update to the attenuation registers is required for ATC to take effect. Right channels register settings are preserved regardless of the status of ATC.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 Volume Control 04h	2	ATC	0	Attenuator Control Mode: 0 = Right channels use Right attenuation 1 = Right Channels use Left Attenuation

Table 26 Attenuator Control Mode

VOLUME RAMP MODE

There are two ways to change the volume in the WM8742, controlled by VOL_RAMP. When VOL_RAMP=0, the volume changes in a single step from the current volume setting to the new volume when an update is applied to the gain control registers. When VOL_RAMP=1, the volume is automatically ramped from the current volume setting to the new volume setting when an update is applied to the volume control registers. The speed at which this happens is dependant on the sample rate as shown in Table 27 below:

SAMPLE RATE (kHz)	RAMP RATE (ms/dB)
32	1.000
44.1	0.726
48	0.667
88.2	0.726
96	0.667
176.4	0.726
196	0.667

Table 27 Volume Ramp Rates

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 Volume Control 04h	0	VOL_ RAMP	0	Volume ramp mode control: 0 = Apply volume change in a single step. 1 = Ramp between current volume setting and new volume setting.

Table 28 Volume Ramp Control

ANTI-CLIPPING DIGITAL ATTENUATION MODE

Audio material is regularly recorded up to 0dB level and heavily compressed. This may cause clipping and occasional distortion when the digital media is applied to a DAC. In order to prevent this in the WM8742, an anti-clipping mode is provided, which attenuates the digital signal by 2dB as it is processed through the digital filters.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 Volume Control 04h	1	ATT2DB	0	Anti-clipping mode control: 0 = Off, 0dB attenuation 1 = On, 2dB attenuation applied

Table 29 Anti-Clipping Digital Attenuation Control

DSD PLUS GAIN CONTROL

The gain in the DSD Plus data path can be adjusted. The default setting provides a 1.4Vrms differential output level.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 Mode Control 2 08h	6	DSD_ GAIN	0	DSD Plus gain control: 0 = Low gain, 1.4Vrms differential output level 1 = High gain, 2.0Vrms differential output level

Table 30 DSD Plus Gain Control

MUTE MODES

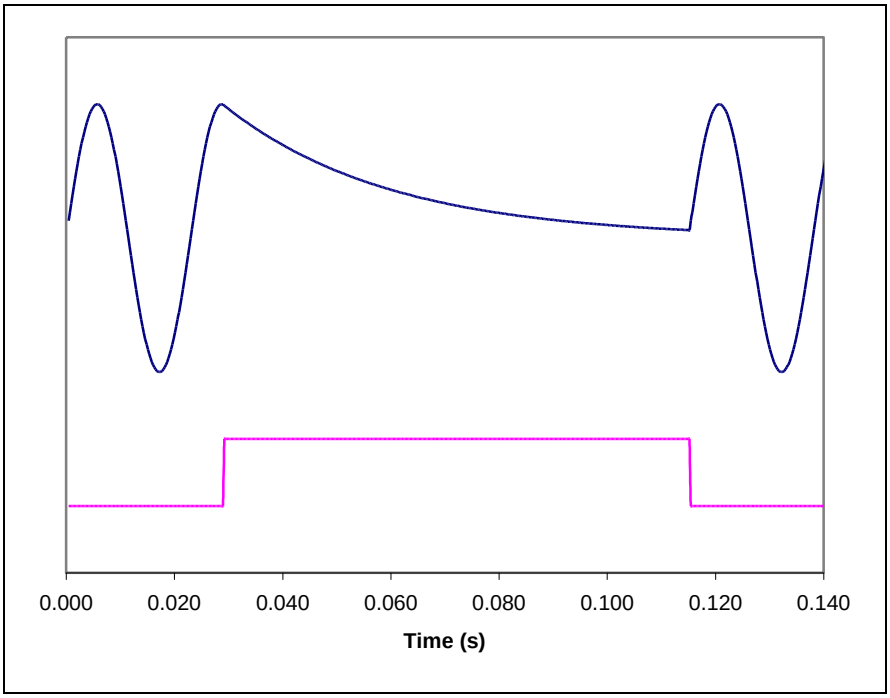


Figure 24 **Application and Release of Soft Mute**

Figure 24 shows the application and release of SOFTMUTE for a full amplitude sinusoid being played at 48kHz sampling rate. When SOFTMUTE (lower trace) is asserted, the WM8742 output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output decays towards V_{MID} in 1022x4/fs seconds. When SOFTMUTE is de-asserted, the signal gain will return to its previous value.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 PCM Control 04h	3	SOFTMUTE	0	Soft mute select 0 = Normal operation 1 = Soft mute both channels

Table 31 Soft Mute Control

ZERO FLAG OUTPUT

The WM8742 has one zero flag output pin, ZFLAG (pin 21). The zero flag feature is only valid for PCM data.

The WM8742 asserts Logic 1 on the ZFLAG pin when a sequence of more than 1024 zeros is input to the chip. The default value is a logical AND of both left and right channels. Under software control, the user can also set the zero flag pin to respond to either the left channel OR the right channel.

The zero flag pin can be used to control external muting circuits if required.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 Volume Control 04h	6:5	ZEROFLR [1:0]	00	Zero flag output: 00 = Pin assigned to logical AND of LEFT and RIGHT channels 01 = Pin assigned to LEFT channel 10 = Pin assigned to RIGHT channel 11 = ZFLAG disabled

Table 32 Zero Flag Output

ZFLAG FORCE HIGH CONTROL

It is possible to force the ZFLAG pin to Logic 1 by setting ZFLAG_HI=1 in R7. This is useful in situations where an application processor may require manual control of an external mute circuit. Setting ZFLAG_HI=0 will allow the ZFLAG pin to function as defined by ZFLAGLR[1:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 Mode Control 1 06h	7	ZFLAG_HI	0	ZFLAG Force High Control 0 = Normal operation 1 = Output Logic 1

Table 33 ZFLAG Force High Control

INFINITE ZERO DETECT

The IZD register configures the operation of the WM8742 analogue mute in conjunction with the zero flag feature. Table 20 shows the interdependency of the MUTEB pin, the IZD register and the zero flag.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 Volume Control 04h	4	IZD	0	IZD control of analogue mute: 0 = Never analogue mute 1 = Analogue mute when ZFLAG set

Table 20 Infinite Zero Detect Control

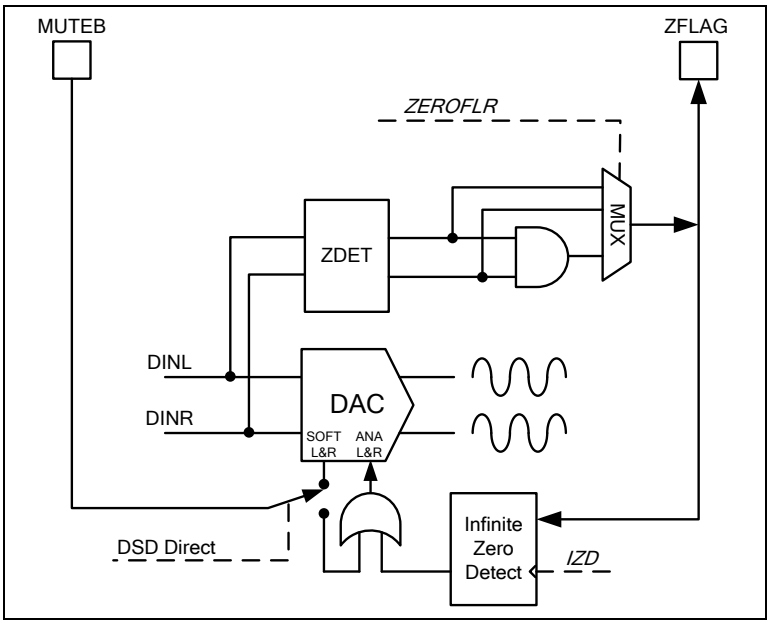


Figure 25 Software Control Mode MUTEB and ZFLAG Configuration

DE-EMPHASIS

Setting the DEEMPH[1:0] register bits enables de-emphasis support in the WM8742 digital filters. There are three de-emphasis filters, one each for sampling rates of 32kHz, 44.1kHz and 48kHz.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 Filter Control 06h	[6:5]	DEEMPH [1:0]	00	De-emphasis mode select: 00 = De-emphasis Off 01 = De-emphasis 32kHz 10 = De-emphasis 44.1kHz 11 = De-emphasis 48kHz

Table 34 De-emphasis Control

OUTPUT PHASE REVERSAL

The REV register bit controls the phase of the output signal. Setting the REV bit causes the phase of the output signal to be inverted.

Note: The REV bit can only be used in stereo mode. When in differential mono mode, the REV bit must remain set as 0.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 Format Control 05h	6	REV	0	Analogue output phase control: 0 = Normal 1 = Inverted

Table 35 Output Phase Control

DIFFERENTIAL MONO MODE

DIFF[1:0] sets the required differential output mode; normal stereo, reversed stereo, mono left or mono right, as shown in Table 36.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 Mode Control 2 08h	[3:2]	DIFF[1:0]	00	00 = Stereo
				10 = Stereo reverse (left and right channels swapped)
				01 = Mono left – differential outputs VOUTLP (17) is left channel. VOUTLN (16) is left channel inverted. VOUTRP (12) is left channel inverted. VOUTRN (13) is left channel.
				11 = Mono right – differential outputs. VOUTLP (17) is right channel inverted. VOUTLN (16) is right channel. VOUTRP (12) is right channel. VOUTRN (13) is right channel inverted.

Table 36 Differential Output Modes

Using these controls a pair of WM8742 devices may be used to build a dual differential stereo implementation with higher performance and differential output.

DITHER

Dither is applied whenever internal truncation occurs. It is also used when a 32 bit input word is applied to the DAC prior to truncation to the internal wordlength. Three types of dither can be selected to allow the sound quality if the device to be optimised.

TDF has a triangular probability density function and causes zero noise modulation i.e. the quantisation noise is invariant to the changes in the signal level. This mode is recommended and is selected by default.

RPDF has a rectangular probability density function and may cause noise modulation.

HPDF has a triangular probability density function with a high pass characteristic, which has a lower noise at low frequencies at the expense of raised noise levels at higher frequencies.

Alternatively the dither can be disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 Mode Control 2 08h	[1:0]	DITHER [1:0]	10	Digital filter dither mode select: 00 = dither off 01 = RPDF dither applied in Digital filter 10 = TPDF dither applied in Digital filter 11 = HPDF dither applied in Digital filter Note: DITHER[1:0] applies only to the dither mode in the Digital filter.

Table 37 Dither Control

NORMAL PCM MODE DIGITAL FILTER SELECTION

The WM8742 has a number of advanced digital filters that can be selected in all PCM operation modes (with the exception of 8FS mode).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 Filter Control 06h	[2:0]	FIRSEL	000	Selects FIR1 filter response 000 = Response 1 001 = Response 2 010 = Response 3 011 = Response 4 100 = Response 5

Table 38 PCM Advanced Digital Filter Selection

Five digital filters are available for selection in each of the three OSR modes (low, medium and high rate) as selected by the OSR bit described in Table 20. It is recommended that the device is muted before the filter response is changed to prevent noise as the filters are reset from appearing on the outputs. A summary of the filter characteristics is given in Table 39 below:

OSR	RESPONSE	NOTES
Low	1	Linear phase half-band filter for backward compatibility
	2	Minimum phase 'soft-knee' filter
	3	Minimum phase half-band filter
	4	Linear phase apodising filter
	5	Minimum phase apodising filter
Medium	1	Linear phase 'soft-knee' filter
	2	Minimum phase 'soft-knee' filter
	3	Linear phase 'brickwall' filter
	4	Minimum phase apodising filter
	5	Linear phase apodising filter
High	1	Linear phase 'soft-knee' filter
	2	Minimum phase 'soft-knee' filter
	3	Linear phase 'brickwall' filter
	4	Minimum phase apodising filter
	5	Linear phase apodising filter

Table 39 PCM Digital Filter Summary

For full details of the filter characteristics available in normal PCM mode, please see Table 64 to Table 66 and Figure 28 to Figure 57.

8FS MODE DIGITAL FILTER

In 8FS mode, the majority of the internal filters are bypassed. In this mode, the data is filtered using only the filter characteristic described by Table 67 and shown in Figure 58 and Figure 59.

DSD PLUS FILTER SELECTION

The WM8742 has a number of compensation filters that can be selected in DSD Plus mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 Filter Control 06h	[4:3]	DSDFILT [1:0]	00	Selects Compensation Filter response 00 = Response 1 01 = Response 2 10 = Response 3 11 = Response 4

Table 40 DSD Plus Digital Filter Selection

It is recommended that the device is muted before the filter response is changed to prevent noise as the filters are reset from appearing on the outputs.

Full details of these filters are described in Table 68 and Figure 60 to Figure 67.

DSD DIRECT DIGITAL FILTERS

The DSD Direct filters have been designed to provide the minimal of processing to the data with no decimation, re-quantisation or noise-shaping, in order to preserve the signal integrity as much as possible. As a result the filters have a wide bandwidth and a very gradual attenuation. It is recommended that whichever DSD Direct filter is chosen it is augmented by analogue post-DAC filtering in order to adhere to the Scarlet-Book SACD standard.

There are a total of four DSD Direct filter responses available, controlled by two register bits as described in Table 41 below:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 Additional Control 1 20h	0	DSD_NO_ NOTCH	0	DSD Direct 8fs Notch Filter 0: Enable 8fs notch filter 1: Disable 8fs notch filter
	1	DSD_ LEVEL	1	DSD Direct Filter Gain 0: High gain 1: Low gain

Table 41 DSD Direct Digital Filter Selection

DSD MUTE CONTROL

In DSD Direct mode, an analogue mute can be applied at the output of the DAC. This is controlled by register bit AMUTE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 Volume Control 04h	7	AMUTE	0	DSD Direct mute control: 0 = mute off 1 = mute on

Table 42 DSD Analogue Mute Control

POWER SAVING STANDBY CONTROL

Setting the PWDN register bit immediately connects all outputs to V_{MID} and resets the digital sections of the DAC system including the DLL, the audio interface and the DSP. Input data samples are not preserved, but all control register settings are maintained. When PWDN is cleared the WM8742 will repeat its power-on initialisation sequence.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 Format Control 05h	7	PWDN	0	Power Down Mode Select: 0 = Normal Mode 1 = Power Down Mode

Table 43 Powerdown Control

HARDWARE CONTROL MODE

When the MODE pin is held 'low' the WM8742 is set to hardware control mode and a limited feature set can be configured.

PIN	NAME	DESCRIPTION
24	MODE/ LRSEL	0 = Hardware control mode 1 = 3-wire serial control mode Z = 2-wire serial control mode

Table 44 MODE/LRSEL Hardware Control Pin Function

DSD AND PCM MODE SWITCHING

The audio interface mode can be switched between DSD Direct and PCM by controlling the state of pin DSD. It is recommended that the chip is forced into a MUTE state before dynamically switching modes.

PIN	NAME	DESCRIPTION
27	SCLK/DSD	0 = PCM Mode 1 = DSD Direct Mode

Table 45 SCLK/DSD Hardware Control Pin Function

AUDIO INPUT FORMAT

Under hardware control, it is possible to select between four different modes of operation for the PCM audio interface.

PIN NUMBER	28	23	
NAME	CSB/SADDR/I2S	IWO/DOUT	DESCRIPTION
STATUS	0	0	16-bit right justified
	0	1	24-bit right justified
	1	0	24-bit left justified
	1	1	24-bit I^2S

Table 46 CSB/SADDR/I2S and IWO/DOUT Hardware Control Pin Function

OVERSAMPLING RATE CONTROL

The user has control of the oversampling ratio of the WM8742, and can set to the device to operate in low, medium or high rate modes. For optimum operation of the digital filtering and other processing on the WM8742 in PCM hardware mode, the user must ensure the correct value of OSR is set at all times. Table 47 shows the correct settings:

PIN	NAME	DESCRIPTION
22	OSR/DSDR	Oversampling Rate Selection 0 = Low rate (32/44.1/48kHz) Z = Medium rate (88.2/96kHz) 1 = High rate (176.4/192kHz)

Table 47 OSR/DSDR Hardware Control Pin Function

MUTE PIN

A soft mute can be applied to the WM8742 in the digital domain in all PCM. A logic low on the MUTEB pin will cause the attenuation to ramp to infinite attenuation at a rate of 1022x(4/fs). Setting MUTEB high will return the signal gain to its previous value. Figure 26 shows the soft mute characteristic.

In DSD Direct mode the MUTEB pin controls the analogue mute in the DAC. This analogue mute is a 'hard' mute and is applied and released as soon as the MUTEB pin is toggled.

PIN	NAME	DESCRIPTION
25	MUTEB/ SDOUT	Mute control 0 = Mute on (no output) 1 = Mute off (normal operation

Table 48 MUTEB Hardware Control Pin Function

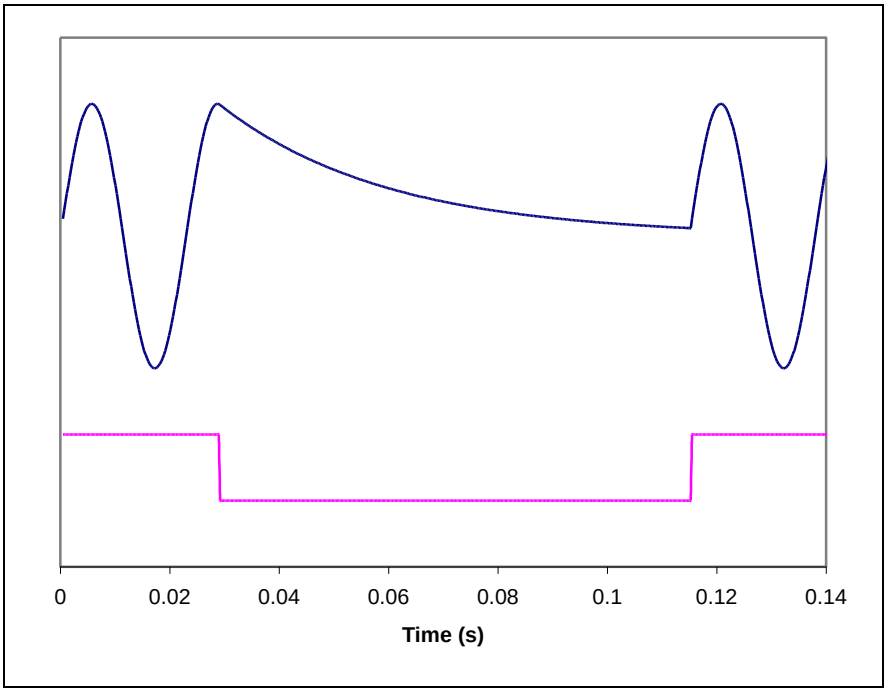


Figure 26 Hardware Control Mode Soft Mute Characteristic

ZERO FLAG

In hardware control mode the ZFLAG pin asserts when 1024 consecutive zero samples are applied to the left and right channels of the WM8742 when in PCM mode. In DSD mode, the ZFLAG has no function.

In hardware mode there is no access to the infinite zero detect and so there is no automute function. If this functionality is required, software mode must be used. Figure 27 shows the MUTEB and ZFLAG configuration.

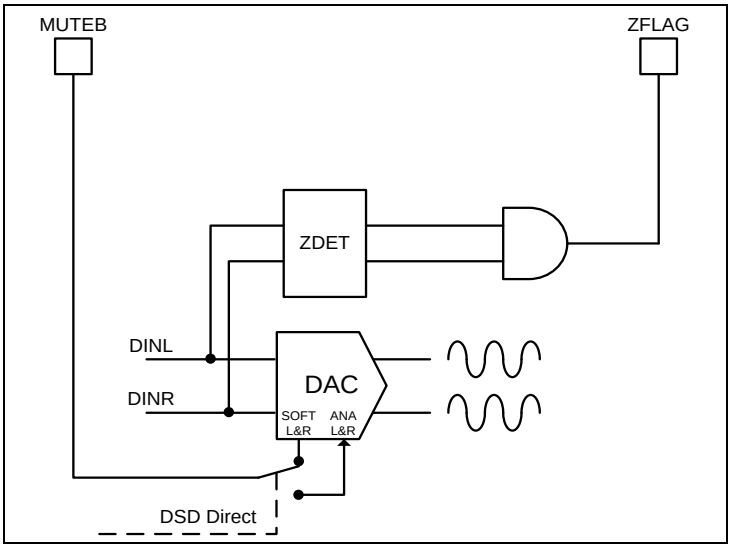


Figure 27 Hardware Control Mode MUTEB and ZFLAG Configuration

DE-EMPHASIS CONTROL AND ANTI-CLIPPING MODE

In hardware control mode, de-emphasis is supported with a maximum error of +1.5dB at a sampling rate of 44.1kHz.

Audio material is regularly recorded up to 0dB level and heavily compressed. This causes clipping and distortion when the digital media is applied to a DAC. In order to prevent this in the WM8742, an anti-clipping mode is provided, which attenuates the digital signal by 2dB as it is processed through the digital filters.

Under hardware control de-emphasis and the anti-clipping mode are only available when using PCM mode.

PIN	NAME	DESCRIPTION
26	SDIN/ DEEMPH	Deemphasis Control 0 = De-emphasis off 1 = De-emphasis on Z = Digital filter anti-clipping mode

Table 49 DEEMPH Hardware Control Pin Function

DIGITAL FILTER SELECTION

The WM8742 includes a wide range of digital filters. A limited set of these can be selected in hardware control mode as listed in Table 50. Full details of each digital filter response can be found in section PCM Digital Filter Selection, from page 38.

PIN	NAME	DESCRIPTION
4	FSEL/ DINR	Digital filter selection (32/44.1/48kHz): 0 = Response 1 1 = Response 5 Z = Response 4
		Digital filter selection (88.2/96kHz and 176.4/192kHz): 0 = Response 1 1 = Response 3 Z = Response 2

Table 50 FSEL/DINR Hardware Control Pin Function

There is no choice of digital filters in DSD Direct mode – only the very minimal filtering described in Figure 72 and Figure 73 is available.

DIFFERENTIAL MONO MODE

If DIFFHW (pin 6) is held to Logic 1, hardware controlled differential mono mode is selected. This overrides any other control pin or register bit. Differential mono mode allows the user to build a dual differential stereo DAC implementation with higher performance and differential output. DIFFHW is used in conjunction with MODE/LRSEL (pin 24) to define a 'left' or 'right' DAC as shown in Table 51.

PIN NUMBER	6	24	
NAME	DIFFHW	MODE/LRSEL	DESCRIPTION
	0	0	Hardware control (stereo)
	0	Z	2-wire Software Control
	0	1	3-wire software control)
	1	0	Mono Left – differential outputs VOUTLP = left channel VOUTLN = left channel inverted VOUTRP = left channel inverted VOUTRN = left channel
	1	1	Mono right – differential outputs VOUTLP = right channel inverted VOUTLN = right channel VOUTRP = right channel VOUTRN = right channel inverted

Table 51 DIFFHW and MODE/LRSEL Hardware Control Pin Functions

Differential mono mode is available for all PCM hardware controlled modes and DSD Direct hardware mode.

OVERVIEW OF FUNCTIONS

The WM8742 has many modes of operation, and certain restrictions on what functions are available in which modes. Table 52 gives an overview of the functions available in hardware and software control modes across all modes of operation:

	SOFTWARE MODE				HARDWARE MODE	
FUNCTION	**NORMAL PCM**	**8FS MODE**	**DSD PLUS**	**DSD DIRECT**	**NORMAL PCM**	**DSD DIRECT**
Selectable Digital Filters	5	✗	4	4	3	✗
Deemphasis Support	✓	✗	✗	✗	✓	✗
Adjustable DSP Dither	✓	✓	✓	✗	✗	✗
Differential Mono Mode	✓	✓	✓	✓	✓	✓
Digital Softmute	✓	✓	✓	✗	✓	✗
Analogue Mute	✓	✓	✓	✓	✓	✓
Zero Detect (ZFLAG)	✓	✓	✗	✗	✓	✗
Automute Function	✓	✗	✗	✗	✗	✗
Anti-Clipping Mode	✓	✓	✗	✗	✓	✗
Digital Attenuation	✓	✓	✓	✗	✗	✗
Powerdown Mode	✓	✓	✓	✓	✗	✗
Audio Interface Daisy Chain	✓	✗	✗	✗	✗	✗
3-wire Software Interface Daisy Chain	✓	✓	✓	✓	✗	✗

Table 52 Comparison of Functions Available across Operating Modes

✓ = function available

✗ = function not available

REGISTER MAP

Reg	Name	Addr	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0	DACLLSB Attenuation	00h	0	0	0	UPDATELL	LAT[4:0]					0x000
1	DACLMSB Attenuation	01h	0	0	0	UPDATELM	LAT[9:5]					0x000
2	DACRLSB Attenuation	02h	0	0	0	UPDATERL	RAT[4:0]					0x000
3	DACRMSB Attenuation	03h	0	0	0	UPDATERM	RAT[9:5]					0x000
4	Volume Control	04h	0	AMUTE	ZEROFLR[1:0]		IZD	SOFT MUTE	ATC	ATT2DB	VOL_RAMP	0x000
5	Format Control	05h	0	PWDN	REV	BCP	LRP	FMT[1:0]		IWL[1:0]		0x00A
6	Filter Control	06h	0	ZFLAG_HI	DEEMPH[1:0]		DSDFILT[1:0]		FIRSEL[2:0]			0x000
7	Mode Control 1	07h	0	MODE8X	OSR[1:0]		SR[2:0]			MODESEL[1:0]		0x000
8	Mode Control 2	08h	0	0	DSD_ GAIN	SDOUT	DOUT	DIFF[1:0]		DITHER[1:0]		0x002
9	Software Reset	09h	RESET									0x000
32	Additional Control 1	20h	0	0	0	0	0	0	0	DSD_ LEVEL	DSD_NO _NOTCH	0x000

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R0 DACLLSB Attenuation 00h	[4:0]	LAT[4:0]	00 (0dB)	LSBs of attenuation data for left channel in 0.125dB steps. See Table 25 for details.
	5	UPDATE	0	Attenuation data load control for left channel. 0 = Store LAT[4:0] value but don't update 1 = Store LAT[4:0] and update attenuation on registers 0-3

Table 53 R0 DACL LSB Attenuation Control Register

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R1 DACLMSB Attenuation 01h	[4:0]	LAT[9:5]	00 (0dB)	MSBs of attenuation data for left channel in 4dB steps. See Table 25 for details.
	5	UPDATE	0	Attenuation data load control for left channel. 0 = Store LAT[9:5] value but don't update 1 = Store LAT[9:5] and update attenuation on registers 0-3

Table 54 R1 DACL MSB Attenuation Control Register

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R2 DACRLSB Attenuation 02h	[4:0]	RAT[4:0]	00 (0dB)	LSBs of attenuation data for right channel in 0.125dB steps. See Table 25 for details.
	5	UPDATE	0	Attenuation data load control for right channel. 0 = Store RAT[4:0] value but don't update 1 = Store RAT[4:0] and update attenuation on registers 0-3

Table 55 R2 DACR LSB Attenuation Control Register

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R3 DACRMSB Attenuation 03h	[4:0]	RAT[9:5]	00 (0dB)	MSBs of attenuation data for right channel in 4dB step. See Table 25 for details.
	5	UPDATE	0	Attenuation data load control for right channel. 0 = Store RAT[9:5] value but don't update 1 = Store RAT[9:5] and update attenuation on registers 0-3

Table 56 R3 DACR MSB Attenuation Control Register

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R4 Volume Control 04h	0	VOL_RAMP	0	Ramps volume from existing attenuation setting to new setting when UPDATE applied. 0: Step volume change 1: Ramp volume change
	1	ATT2DB	0	Anti-clipping mode control. Attenuates PCM gain path by 2 dB: 0: 0dB gain 1: -2dB gain
	2	ATC	0	Attenuator Control Mode: 0 = Right channels use Right attenuation 1 = Right Channels use Left Attenuation
	3	SOFTMUTE	0	Soft mute select 0: Normal Operation 1: Soft mute both channels
	4	IZD	0	Enables infinite zero detect (detects 1024 zeros on input): 0 = Disable infinite zero detect 1 = Enable infinite zero detect
	6:5	ZEROFLR [1:0]	00	Zero flag output: 00 = Pin assigned to logical AND of LEFT and RIGHT channels 01 = Pin assigned to LEFT channel 10 = Pin assigned to RIGHT channel 11 = ZFLAG disabled
	7	AMUTE	0	Applies analogue mute in DSD mode 0 = Normal operation 1 = Analogue mute applied

Table 57 R4 Volume Control Register

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R5 Format Control 05h	[1:0]	IWL[1:0]	10	Audio interface input word length. 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit
	[3:2]	FMT[1:0]	10	Audio data format select. 00 = right justified mode 01 = left justified mode 10 = I2S mode 11 = DSP mode
	4	LRP	0	Polarity select for LRCLK/DSP mode select. 0 = normal LRCLK polarity/DSP mode A 1 = inverted LRCLK polarity/DSP mode B
	5	BCP	0	BCLK / DSD64CLK polarity select: 0 = normal polarity 1 = inverted polarity
	6	REV	0	Analogue output phase control: 0 = Normal 1 = Inverted
	7	PWDN	0	Power Down Mode Select: 0 = Normal Mode 1 = Power Down Mode

Table 58 R5 Format Control Register

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R6 Filter Control 06h	[2:0]	FIRSEL	000	Select advanced digital filter response: 000 = Response 1 001 = Response 2 010 = Response 3 011 = Response 4 100 = Response 5
	[4:3]	DSDFILT	00	Select DSD compensation filter response: 00 = Response 1 01 = Response 2 10 = Response 3 11 = Response 4
	[6:5]	DEEMPH [1:0]	00	De-emphasis mode select: 00 = De-emphasis Off 01 = De-emphasis 32kHz 10 = De-emphasis 44.1kHz 11 = De-emphasis 48kHz
	7	ZFLAG_HI	0	ZFLAG Force High Control 0 = Normal operation 1 = Output Logic 1

Table 59 R6 Filter Control Register

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R7 Mode Control 1 07h	[1:0]	MODESEL [1:0]	00	DSD/PCM mode select. 00 = PCM mode 01 = DSD Direct mode 10 = DSD Plus mode 11 = Unused
	[4:2]	SR[3:0]	000	MCLK to LRCLK sampling rate ratio control: 000 = auto detect sample rate 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs
	[6:5]	OSR[1:0]	00	Selects low, medium or high sample rate mode for filter selection (equivalent to OSR pin functionality in Hardware Mode) 00 = Low rate (32/44.1/48kHz) 01 = Medium rate (96kHz) 10 = High rate (192kHz) 11 = Unused
	7	MODE8X	0	8FS mode select: 0 = Normal operation 1 = 8FS mode (digital filters bypassed)

Table 60 R7 Mode Control Register 1

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R8 Mode Control 2 08h	[1:0]	DITHER[1:0]	10	ALU dither mode select: 00 = dither off 01 = RPDF dither applied in ALU 10 = TPDF dither applied in ALU 11 = HPDF dither applied in ALU Note: DITHER[1:0] applies only to the dither mode in the ALU.
	[3:2]	DIFF[1:0]	00	00 = Stereo
				10 = Stereo reverse (left and right channels swapped)
				01 = Mono left – differential outputs VOUTLP is left channel. VOUTLN is left channel inverted. VOUTRP is left channel inverted. VOUTRN is left channel.
				11 = Mono right – differential outputs. VOUTLP is right channel inverted. VOUTLN is right channel. VOUTRP is right channel. VOUTRN is right channel inverted.
	4	DOUT	0	Daisychaining Mode. Audio data output control: 0 = No audio data daisychaining 1 = Audio data output on pin 23
	5	SDOUT	0	Daisychaining Mode. Control data output control: 0 = No control data daisychaining 1 = Control data output on pin 25
	6	DSD_GAIN	0	DSD Plus gain control: 0 = Low gain, 1.4Vrms differential output level 1 = High gain, 2.0Vrms differential output level

Table 61 R8 Mode Control Register 2

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R9 Software reset 09h	[7:0]	RESET	00000000	Software reset. Writing to the register resets the entire chip, including the register map.

Table 62 R9 Software Reset Control Register

REGISTER ADDRESS	BITS	NAME	DEFAULT	DESCRIPTION
R32 Additional Control 1 20h	0	DSD_NO_NOTCH	0	DSD Direct 8fs Notch Filter 0: Enable 8fs notch filter 1: Disable 8fs notch filter
	1	DSD_LEVEL	1	DSD Direct Filter Gain 0: High Gain 1: Low Gain

Table 63 R32 Additional Control 1

DIGITAL FILTER CHARACTERISTICS

PCM MODE FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low Rate (32/44.1/48kHz) PCM Filter Response 1					
Passband	± 0.000057dB			0.454fs	
Passband Ripple				0.000057	dB
Stopband		0.546fs			
Stopband Attenuation		-111.8			dB
Attenuation at fs/2			-6.02		dB
Group Delay			43		fs
Low Rate (32/44.1/48kHz) PCM Filter Response 2					
Passband	± 0.000036 dB			0.408fs	
Passband Ripple				0.000036	dB
Stopband		0.522fs			
Stopband Attenuation		-111.1			dB
Attenuation at fs/2	Fs/2		-28.07		dB
Group Delay			8		fs
Low Rate (32/44.1/48kHz) PCM Filter Response 3					
Passband	± 0.000058 dB			0.454fs	
Passband Ripple				0.000058	dB
Stopband		0.546fs			
Stopband Attenuation		-110.3			dB
Attenuation at fs/2	Fs/2		-6.43		dB
Group Delay			7		fs
Low Rate (32/44.1/48kHz) PCM Filter Response 4					
Passband	± 0.000066 dB			0.417fs	
Passband Ripple				0.000066	dB
Stopband		0.500fs			
Stopband Attenuation		-110.4			dB
Attenuation at fs/2	Fs/2		-116.19		dB
Group Delay			47		fs
Low Rate (32/44.1/48kHz) PCM Filter Response 5					
Passband	± 0.000041 dB			0.417fs	
Passband Ripple				0.000041	dB
Stopband		0.500fs			
Stopband Attenuation		-111.8			dB
Attenuation at fs/2	Fs/2		-112.45		dB
Group Delay			8		fs

Table 64 Low Rate PCM Filter Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Medium Rate (88.2/96kHz) PCM Filter Response 1					
Passband	± 0.000021 dB			0.208fs	
Passband Ripple				0.000021	dB
Stopband		0.500fs			
Stopband Attenuation		-120.3			dB
Attenuation at fs/2	Fs/2		-120.41		dB
Group Delay			17		fs
Medium Rate (88.2/96kHz) PCM Filter Response 2					
Passband	± 0.000014 dB			0.208fs	
Passband Ripple				0.000014	dB
Stopband		0.500fs			
Stopband Attenuation		-120.8			dB
Attenuation at fs/2	Fs/2		-127.96		dB
Group Delay			9		fs
Medium Rate (88.2/96kHz) PCM Filter Response 3					
Passband	± 0.000048 dB			0.417fs	
Passband Ripple				0.000048	dB
Stopband		0.500fs			
Stopband Attenuation		-115.5			dB
Attenuation at fs/2	Fs/2		-116.89		dB
Group Delay			48		fs
Medium Rate (88.2/96kHz) PCM Filter Response 4					
Passband	± 0.000021 dB			0.208fs	
Passband Ripple				0.000021	dB
Stopband		0.458fs			
Stopband Attenuation		-120.0			dB
Attenuation at fs/2	Fs/2		-126.82		dB
Group Delay			9		fs
Medium Rate (88.2/96kHz) PCM Filter Response 5					
Passband	± 0.000023 dB			0.208fs	
Passband Ripple				0.000023	dB
Stopband		0.458fs			
Stopband Attenuation		-122.5			dB
Attenuation at fs/2	Fs/2		-130.52		dB
Group Delay			8		fs

Table 65 Medium Rate PCM Filter Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High Rate (176.4/192kHz) PCM Filter Response 1					
Passband	± 0.000010 dB			0.104fs	
Passband Ripple				0.000010	dB
Stopband		0.500fs			
Stopband Attenuation		-120.0			dB
Attenuation at fs/2	Fs/2		-127.5		dB
Group Delay			10		fs
High Rate (176.4/192kHz) PCM Filter Response 2					
Passband	± 0.000031 dB			0.104fs	
Passband Ripple				0.000031	dB
Stopband		0.500fs			
Stopband Attenuation		-120.0			dB
Attenuation at fs/2	Fs/2		-124.93		dB
Group Delay			4		fs
High Rate (176.4/192kHz) PCM Filter Response 3					
Passband	± 0.000873 dB			0.400fs	
Passband Ripple				0.000873	dB
Stopband		0.500fs			
Stopband Attenuation		-110.1			dB
Attenuation at fs/2	Fs/2		-112.67		dB
Group Delay			31		fs
High Rate (176.4/192kHz) PCM Filter Response 4					
Passband	± 0.000015 dB			0.104fs	
Passband Ripple				0.000015	dB
Stopband		0.400fs			
Stopband Attenuation		-120.0			dB
Attenuation at fs/2	Fs/2		-120.58		dB
Group Delay			6		fs
High Rate (176.4/192kHz) PCM Filter Response 5					
Passband	± 0.000001 dB			0.104fs	
Passband Ripple				0.000001	dB
Stopband		0.400fs			
Stopband Attenuation		-122.8			dB
Attenuation at fs/2	Fs/2		-128.58		dB
Group Delay			18		fs

Table 66 High Rate PCM Filter Characteristics

8FS MODE FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
8FS Mode Filter					
Passband	± 0.000021 dB			0.455	fs
Passband Ripple				0.000021	dB
Filter Cut-off	-3dB point		121.13		kHz
Group Delay			5		fs

Table 67 8FS Mode Filter Characteristics

DSD PLUS MODE FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DSD Plus Filter Response 1					
Passband	± 0.020423 dB			22.48	kHz
Passband Ripple				0.020423	dB
Stopband		127.69			kHz
Stopband Attenuation		-38.51			dB
Filter Cut-off	-3dB point		58.91		kHz
Group Delay			71		fs
DSD Plus Filter Response 2					
Passband	± 0.011308dB			23.04	kHz
Passband Ripple				0.011308	dB
Stopband		120.41			kHz
Stopband Attenuation		-44.52			dB
Filter Cut-off	-3dB point		49.83		kHz
Group Delay			127		fs
DSD Plus Filter Response 3					
Passband	± 0.019762 dB			27.35	kHz
Passband Ripple				0.019762	dB
Stopband		70.14			kHz
Stopband Attenuation		-26.28			dB
Filter Cut-off	-3dB point		49.74		kHz
Group Delay			46		Fs
DSD Plus Filter Response 4					
Passband	± 0.004140 dB			20.24	kHz
Passband Ripple				0.004140	dB
Stopband		70.03			kHz
Stopband Attenuation		-48.05			dB
Filter Cut-off	-3dB point		49.78		kHz
Group Delay			127		fs

Table 68 DSD Plus Filter Characteristics

PCM MODE FILTER RESPONSE

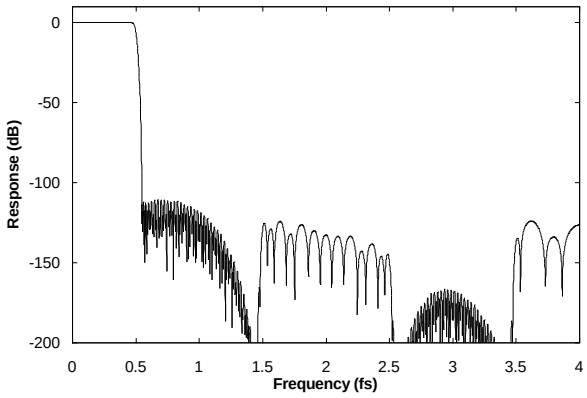


Figure 28 Low Rate PCM Filter 1 Frequency Response

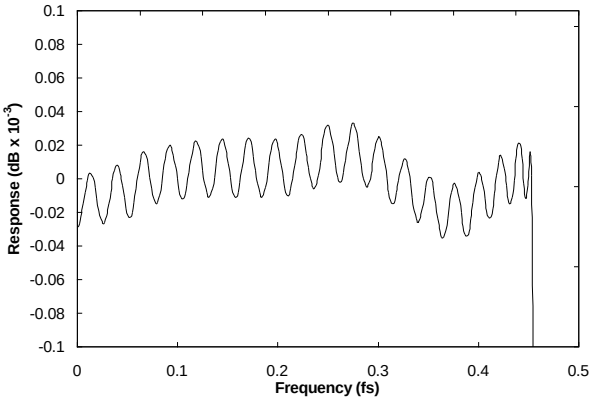


Figure 29 Low Rate PCM Filter 1 Ripple

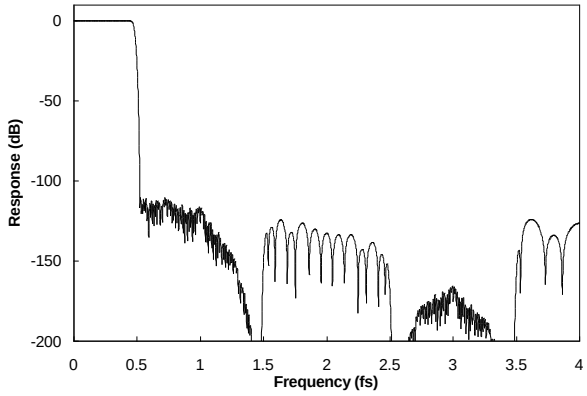


Figure 30 Low Rate PCM Filter 2 Frequency Response

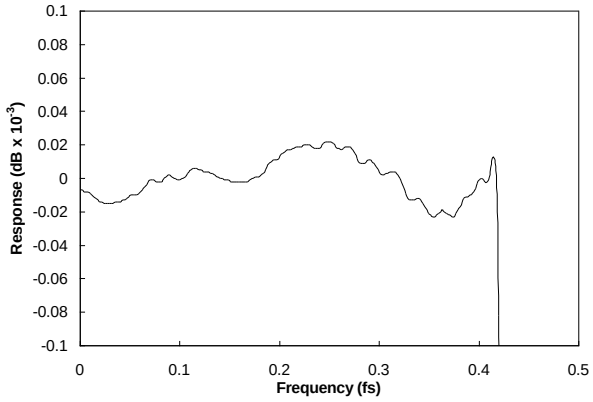


Figure 31 Low Rate PCM Filter 2 Ripple

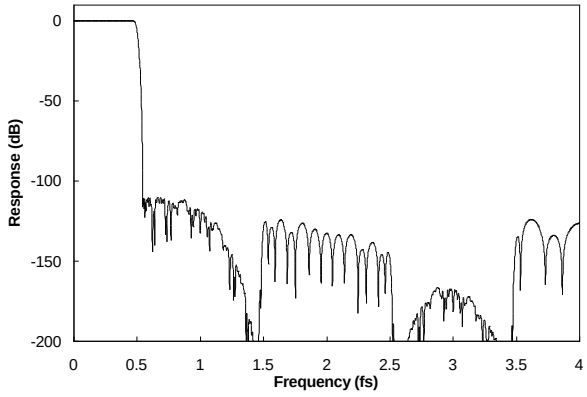


Figure 32 Low Rate PCM Filter 3 Frequency Response

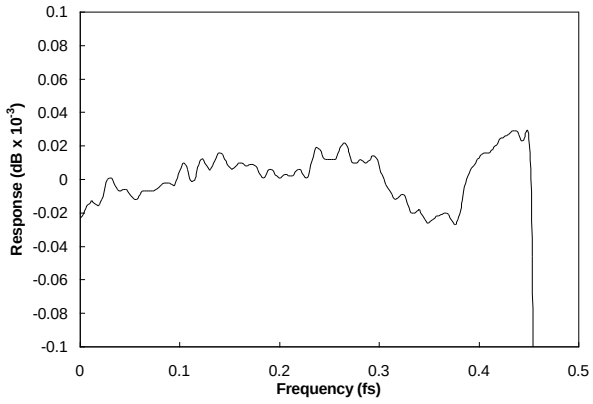


Figure 33 Low Rate PCM Filter 3 Ripple

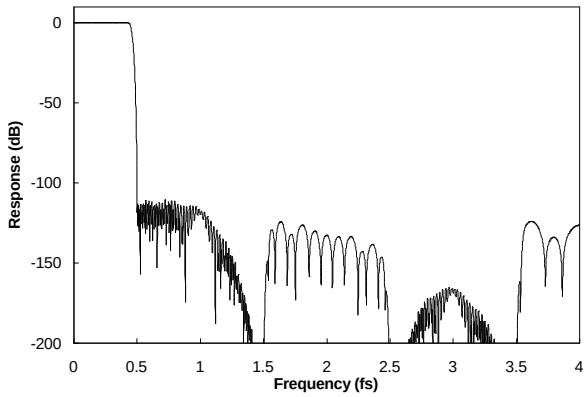


Figure 34 Low Rate PCM Filter 4 Frequency Response

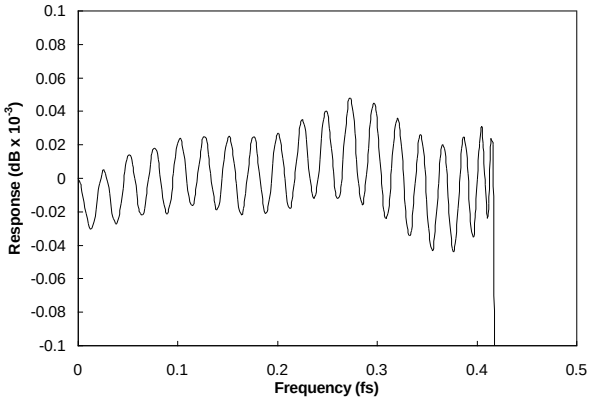


Figure 35 Low Rate PCM Filter 4 Ripple

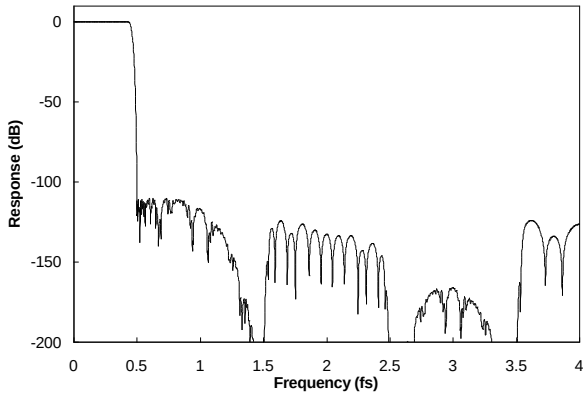


Figure 36 Low Rate PCM Filter 5 Frequency Response

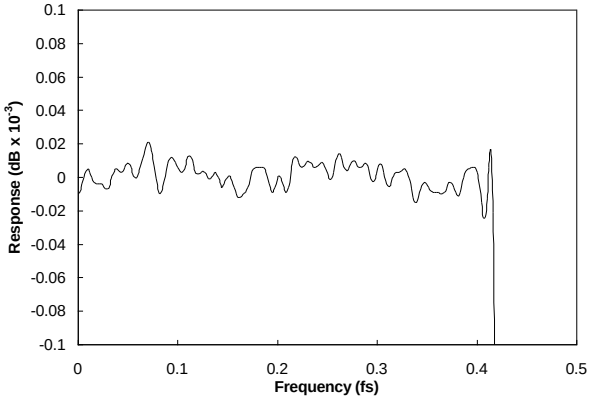


Figure 37 Low Rate PCM Filter 5 Ripple

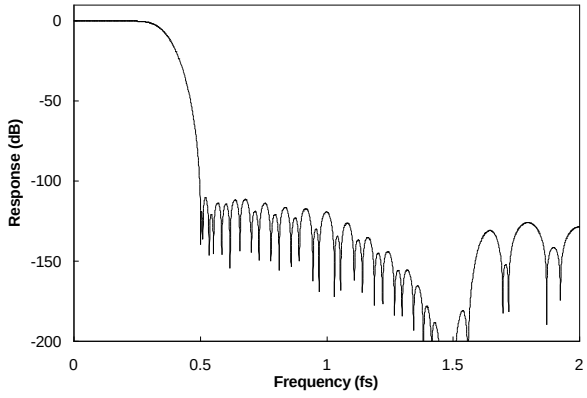


Figure 38 Medium Rate PCM Filter 1 Frequency Response

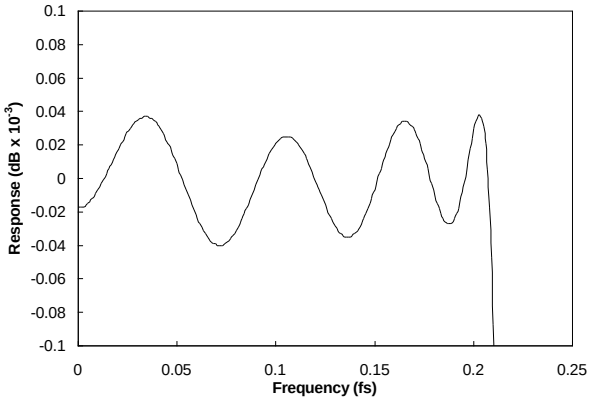


Figure 39 Medium Rate PCM Filter 1 Ripple

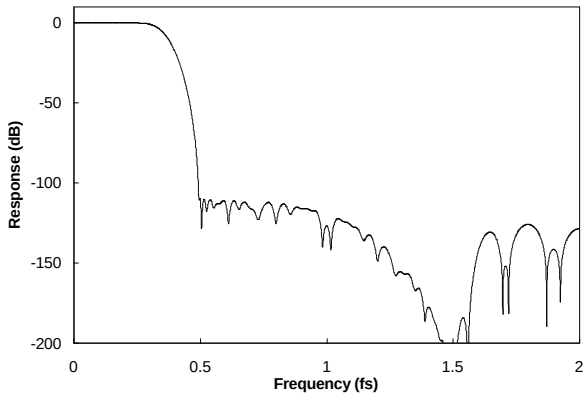


Figure 40 Medium Rate PCM Filter 2 Frequency Response

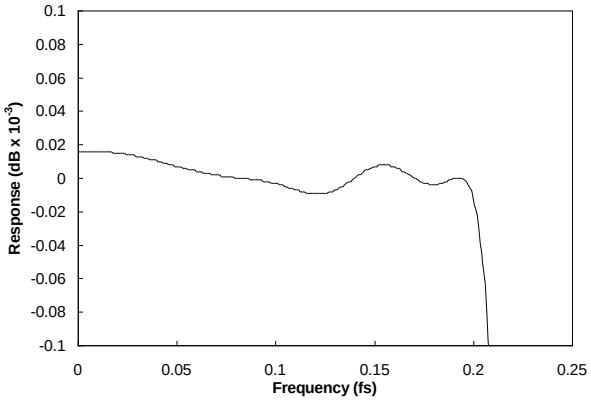


Figure 41 Medium Rate PCM Filter 2 Ripple

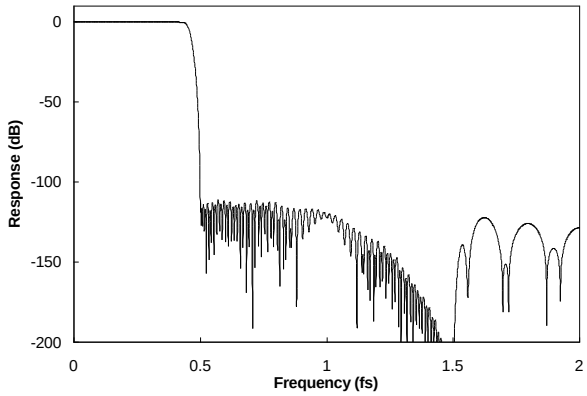


Figure 42 Medium Rate PCM Filter 3 Frequency Response

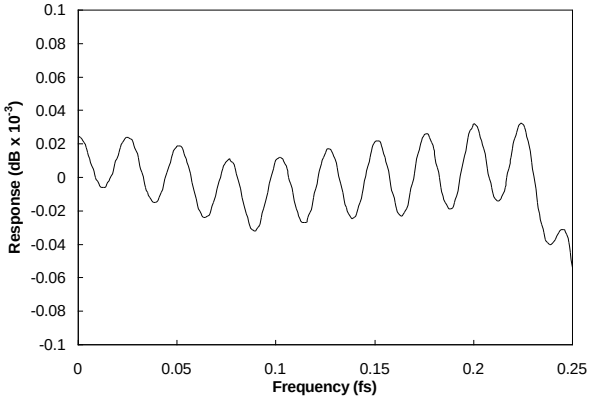


Figure 43 Medium Rate PCM Filter 3 Ripple

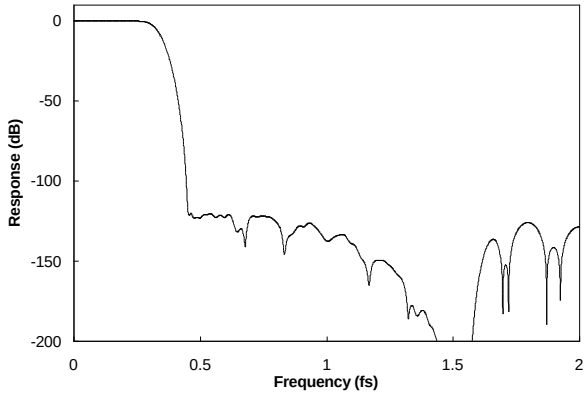


Figure 44 Medium Rate PCM Filter 4 Frequency Response

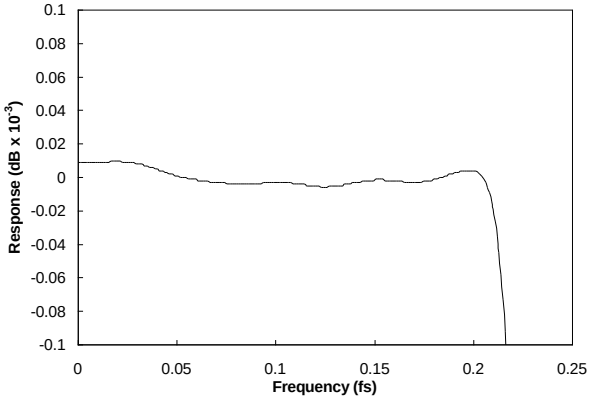


Figure 45 Medium Rate PCM Filter 4 Ripple

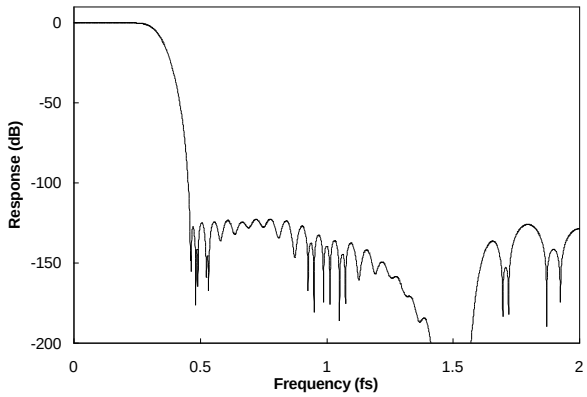


Figure 46 Medium Rate PCM Filter 5 Frequency Response

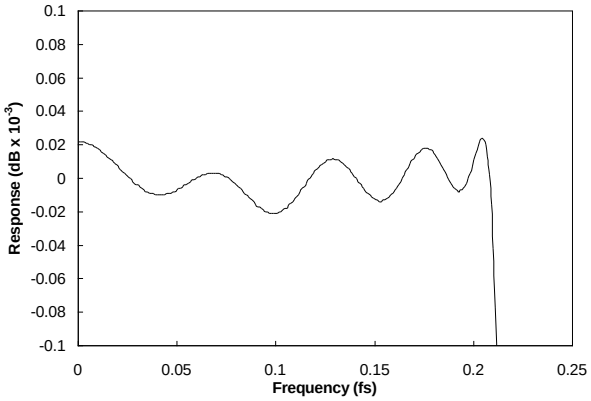


Figure 47 Medium Rate PCM Filter 5 Ripple

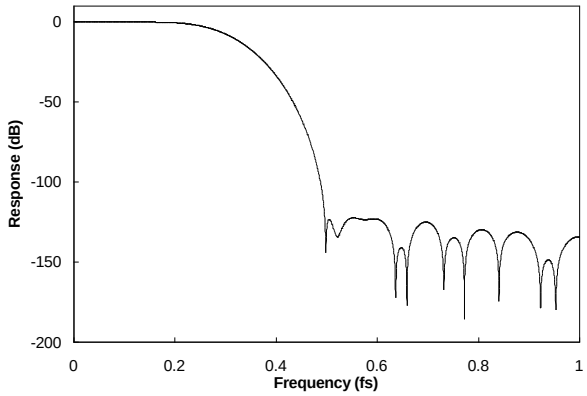


Figure 48 High Rate PCM Filter 1 Frequency Response

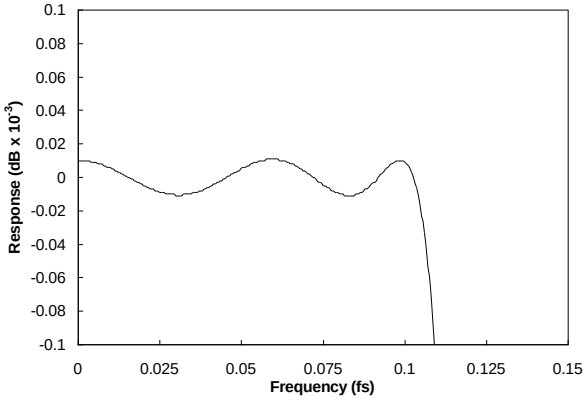


Figure 49 High Rate PCM Filter 1 Ripple

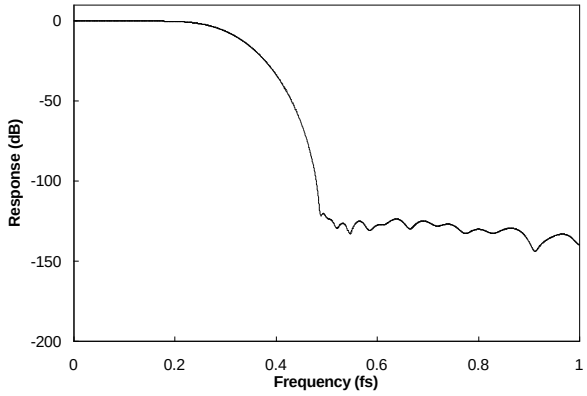


Figure 50 High Rate PCM Filter 2 Frequency Response

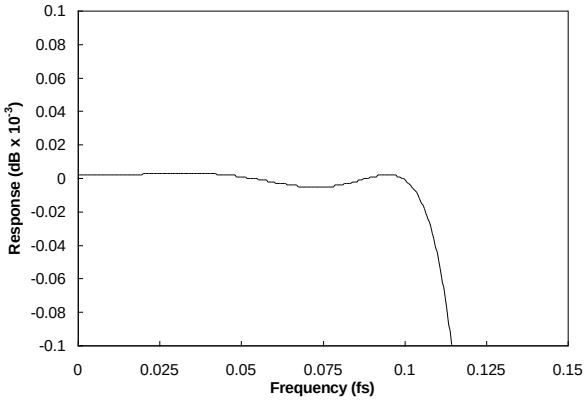


Figure 51 High Rate PCM Filter 2 Ripple

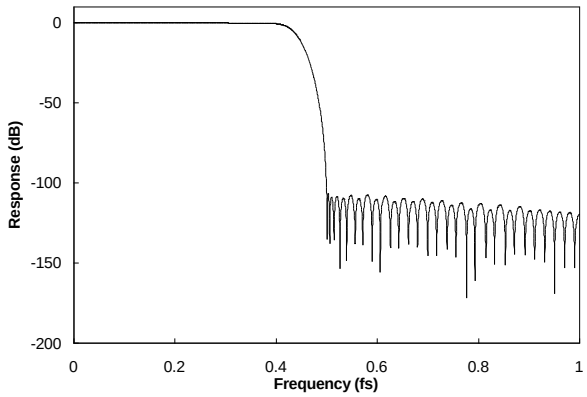


Figure 52 High Rate PCM Filter 3 Frequency Response

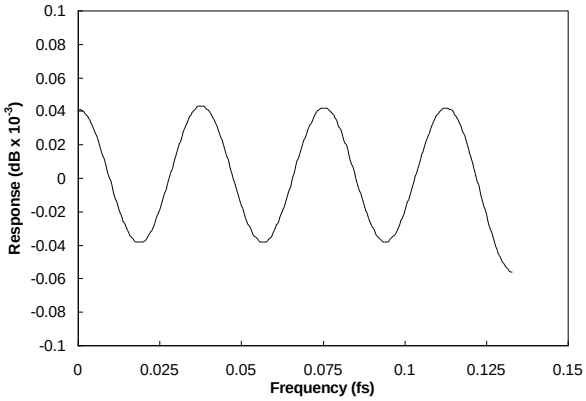


Figure 53 High Rate PCM Filter 3 Ripple

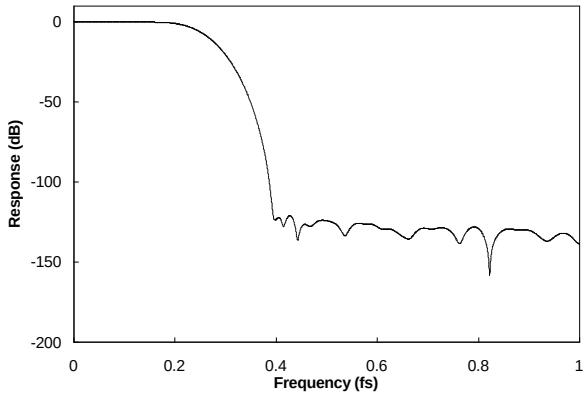


Figure 54 High Rate PCM Filter 4 Frequency Response

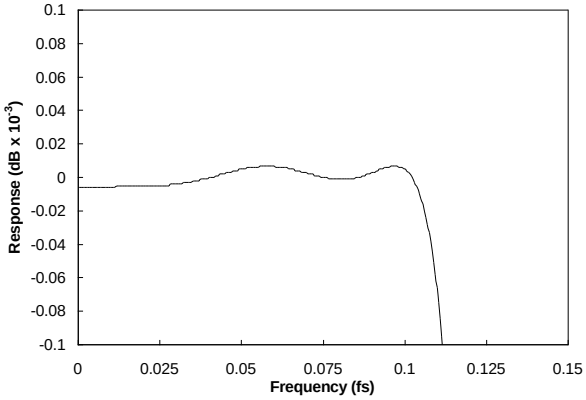


Figure 55 High Rate PCM Filter 4 Ripple

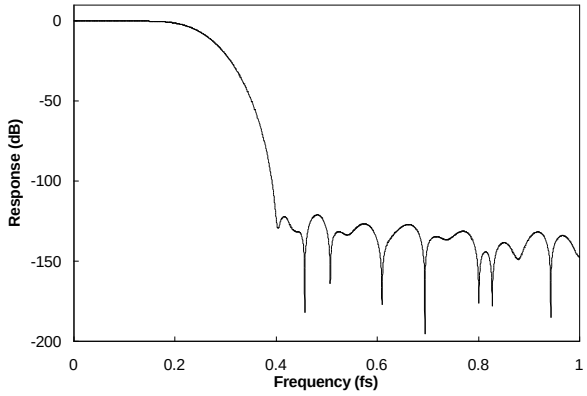


Figure 56 High Rate PCM Filter 5 Frequency Response

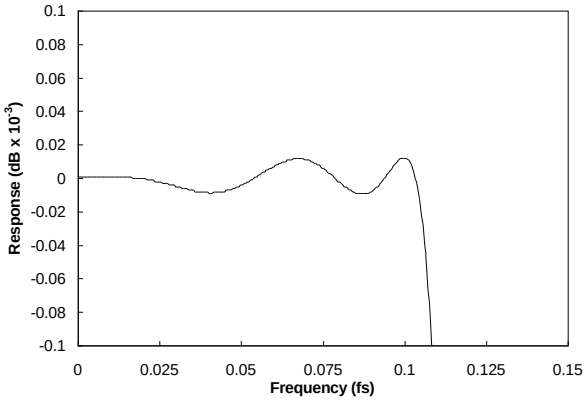


Figure 57 High Rate PCM Filter 5 Ripple

8FS MODE FILTER RESPONSE

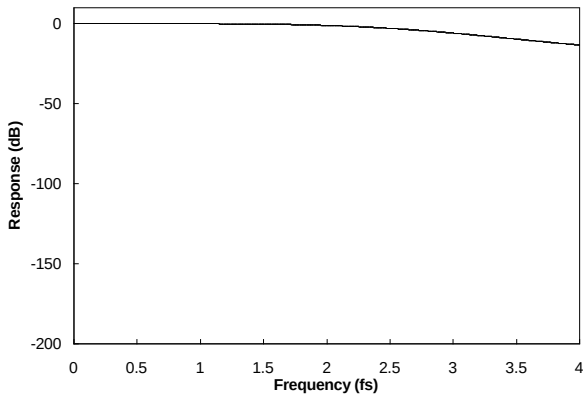


Figure 58 8FS Mode Filter Frequency Response

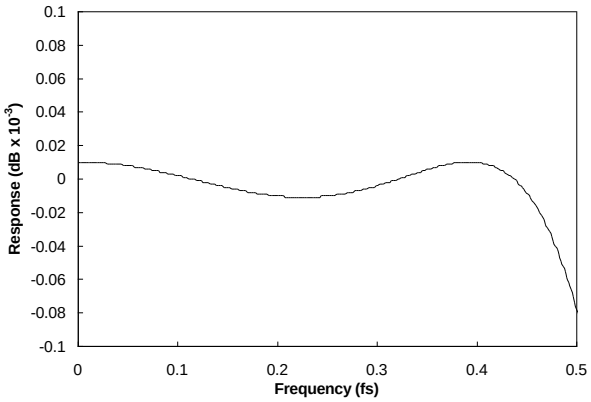


Figure 59 8FS Mode Filter Ripple

DSD PLUS MODE FILTER RESPONSE

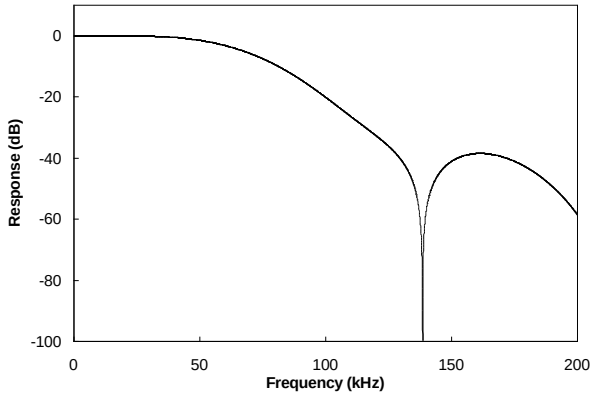


Figure 60 DSD Plus Mode Filter 1 Frequency Response

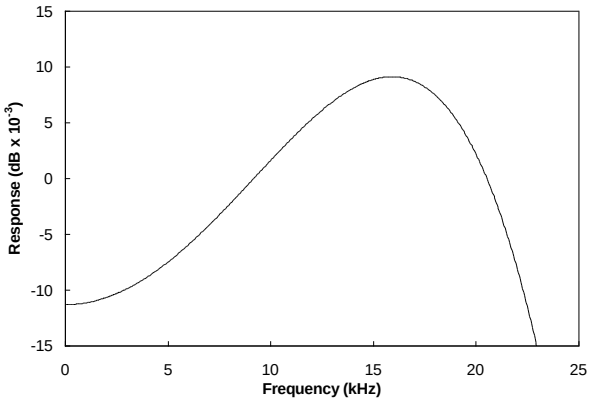


Figure 61 DSD Plus Mode Filter 1 Ripple

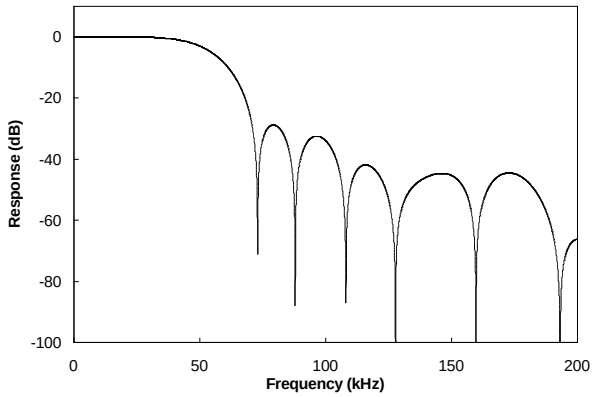


Figure 62 DSD Plus Mode Filter 2 Frequency Response

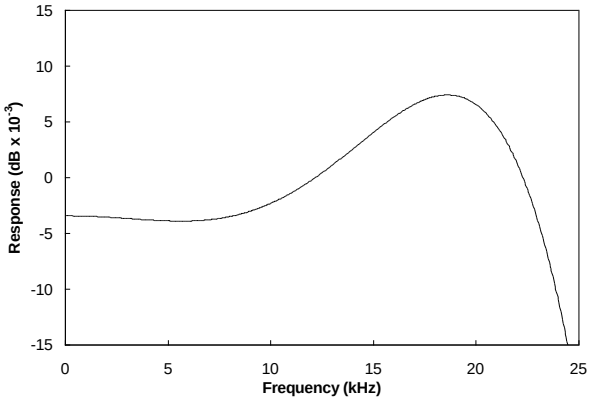


Figure 63 DSD Plus Mode Filter 2 Ripple

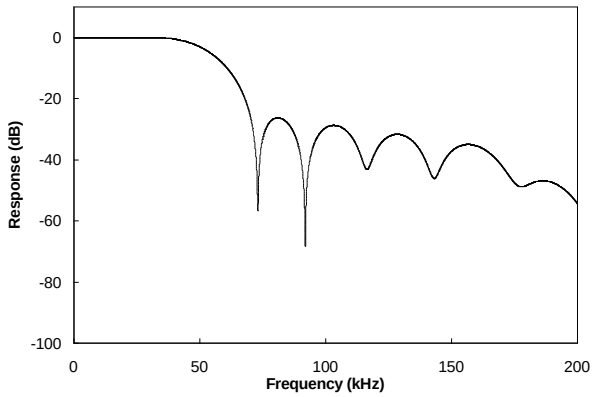


Figure 64 DSD Plus Mode Filter 3 Frequency Response

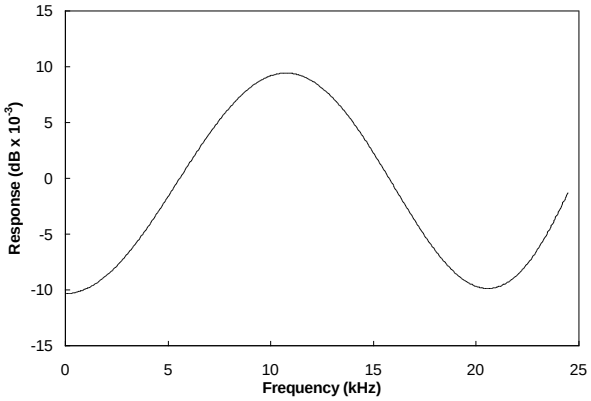


Figure 65 DSD Plus Mode Filter 3 Ripple

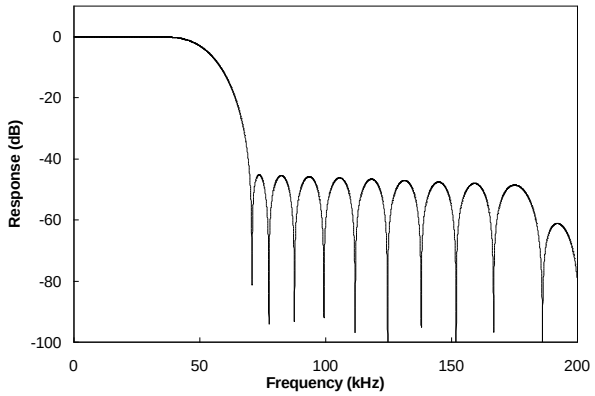


Figure 66 DSD Plus Mode Filter 4 Frequency Response

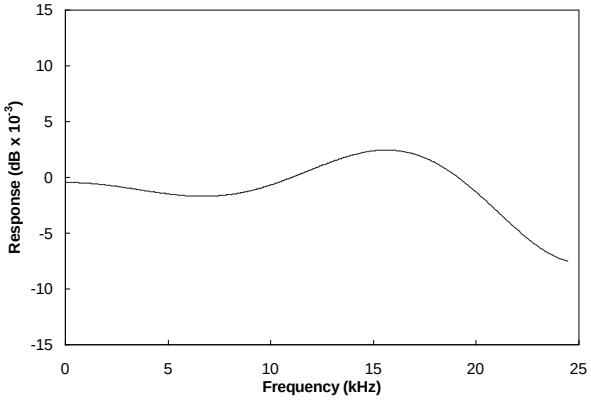


Figure 67 DSD Plus Mode Filter 4 Ripple

DSD DIRECT MODE FILTER RESPONSE

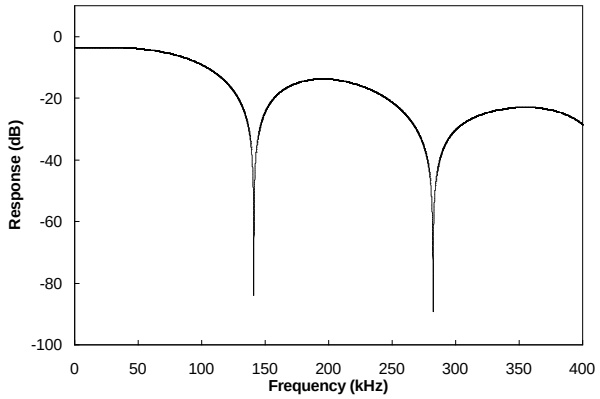


Figure 68 DSD Direct Mode Standard Low Gain Filter Frequency Response

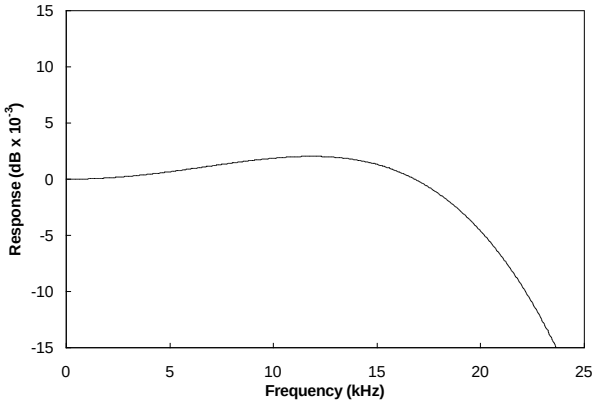


Figure 69 DSD Direct Mode Standard Low Gain Filter Ripple (Normalised)

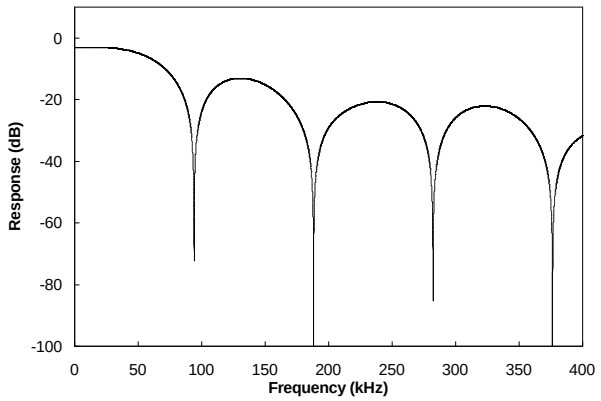


Figure 70 DSD Direct Mode Standard High Gain Filter Frequency Response

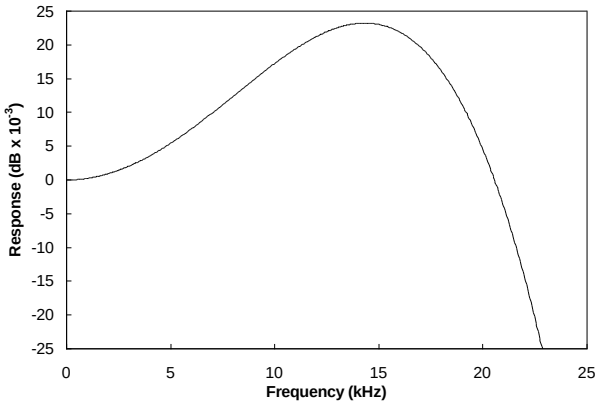


Figure 71 DSD Direct Mode Standard High Gain Filter Ripple (Normalised)

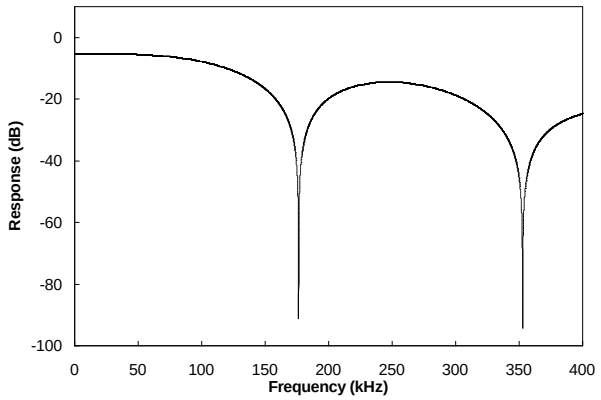


Figure 72 DSD Direct Mode 8fs Notch Low Gain Filter Frequency Response

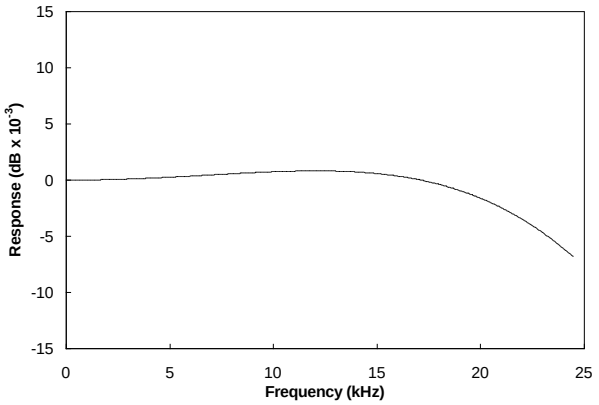


Figure 73 DSD Direct Mode 8fs Notch Low Gain Filter Ripple (Normalised)

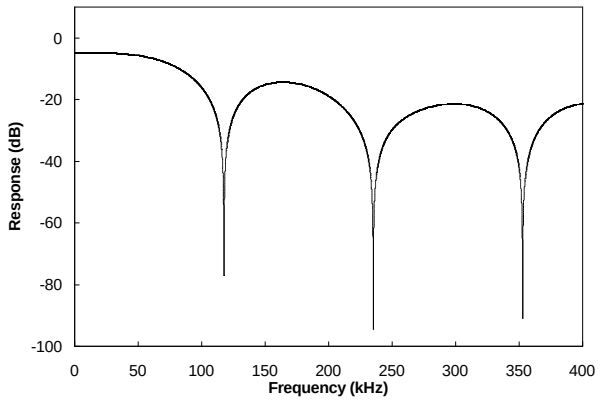


Figure 74 DSD Direct Mode 8fs Notch High Gain Filter Frequency Response

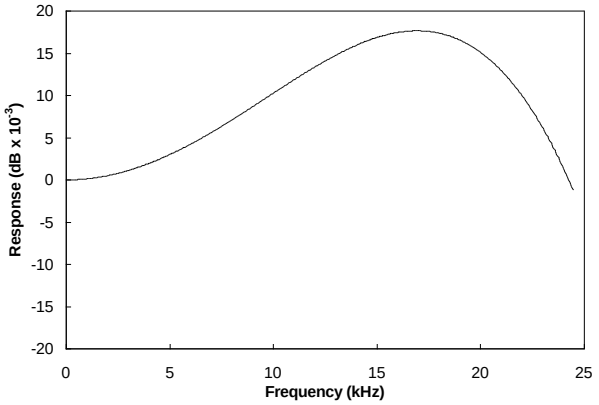


Figure 75 DSD Direct Mode 8fs Notch High Gain Filter Ripple (Normalised)

DE-EMPHASIS FILTER RESPONSE

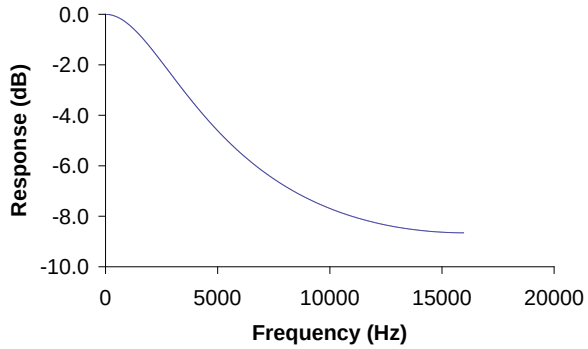


Figure 76 De-emphasis Frequency Response (32kHz)

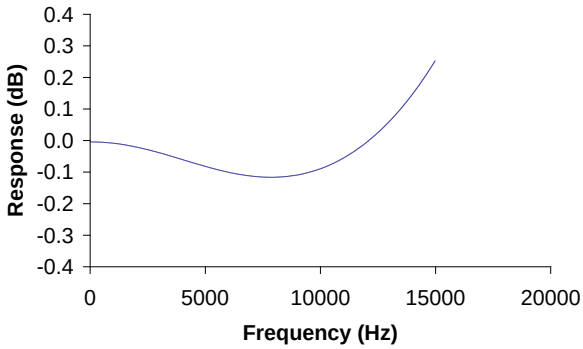


Figure 77 De-emphasis Error (32kHz)

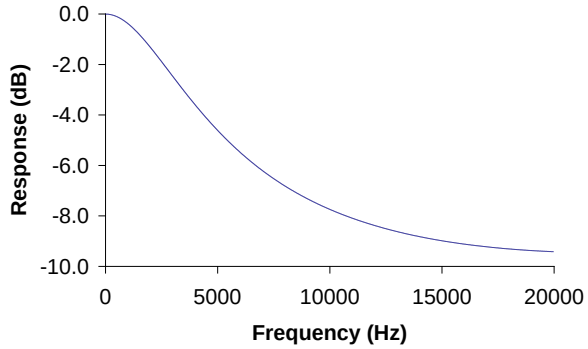


Figure 78 De-emphasis Fequency Response (44.1kHz)

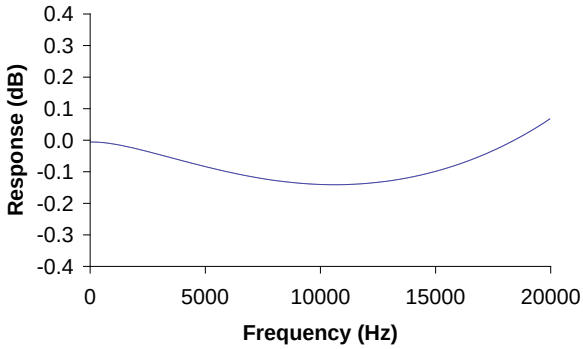


Figure 79 De-emphasis Error (44.1kHz)

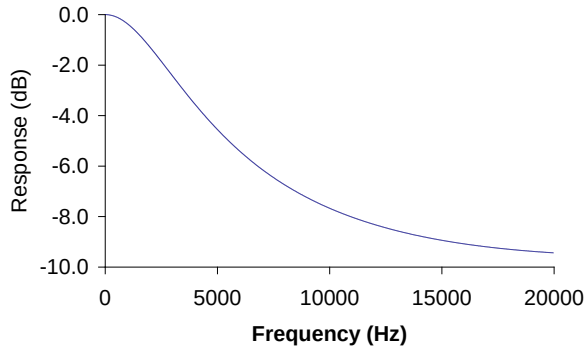


Figure 80 De-emphasis Frequency Response (48kHz)

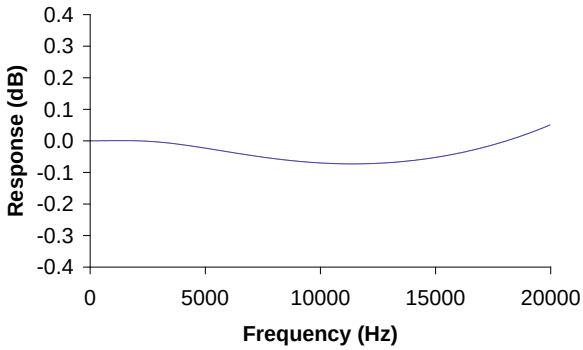
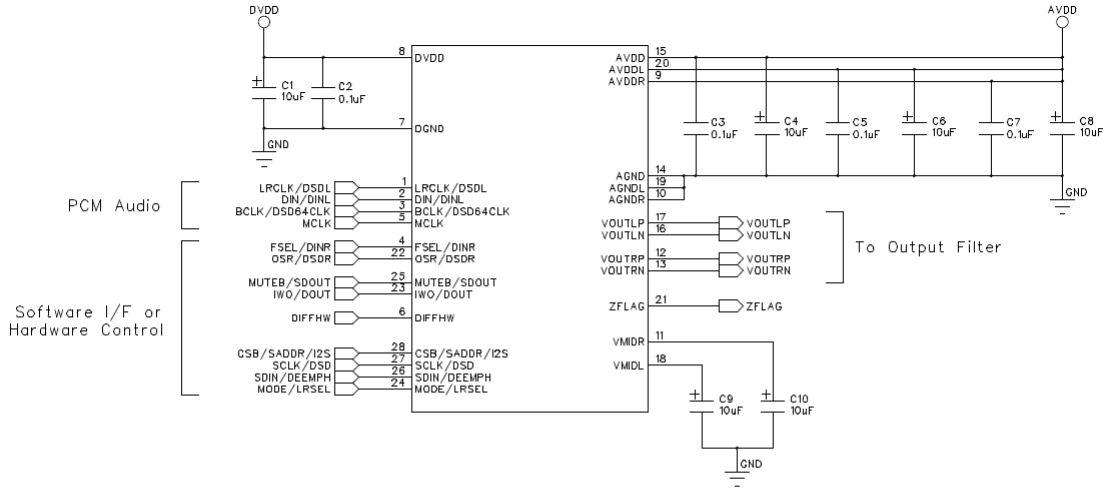


Figure 81 De-emphasis Error (48kHz)

APPLICATIONS INFORMATION



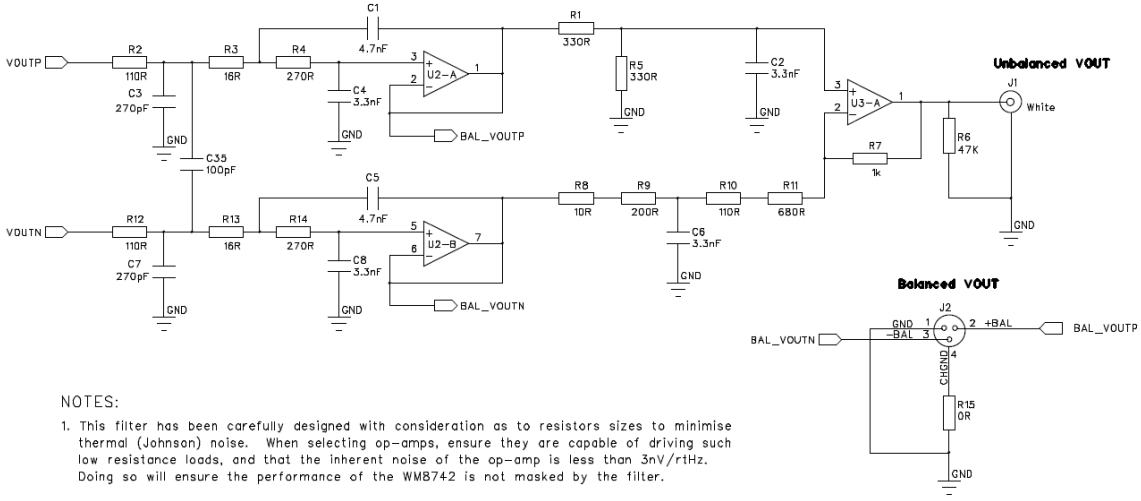
NOTES:

1. AGND and DGND should ideally be connected to a solid ground plane. If this is not possible, AGND and DGND should be connected as close to the WM8742 as possible.

2. C2, C3, C5, C7, C9 and C10 should be positioned as close to the WM8742 as possible.

3. For decoupling, capacitors with very low ESR are recommended for optimum device performance – see Application Note WAN0129 for more details.

Figure 82 External Components



NOTES:

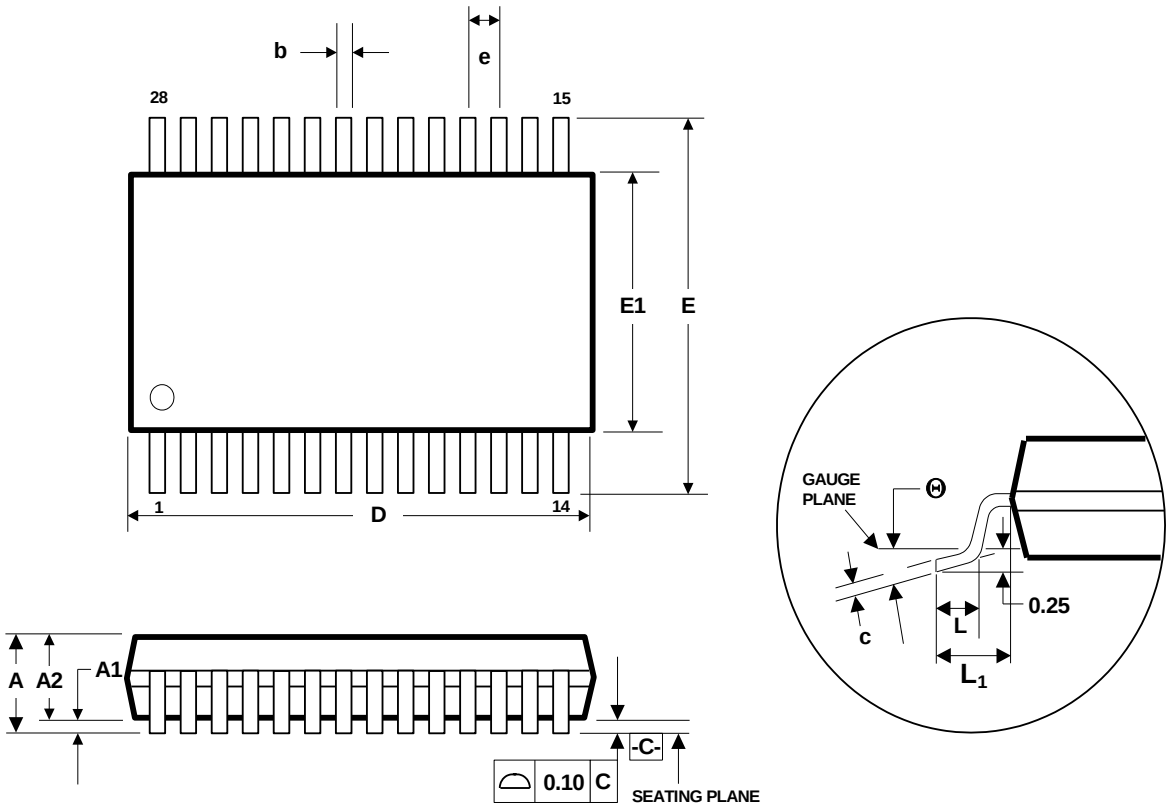
1. This filter has been carefully designed with consideration as to resistors sizes to minimise thermal (Johnson) noise. When selecting op-amps, ensure they are capable of driving such low resistance loads, and that the inherent noise of the op-amp is less than 3nV/rtHz. Doing so will ensure the performance of the WM8742 is not masked by the filter.

2. Capacitor dielectrics can cause distortion to the analog signal. Wolfson recommends that multilayer ceramic capacitors be used, with dielectric material C0G or NP0 for optimum performance.

Figure 83 External Filter Components

PACKAGE DIMENSIONS

DS: 28 PIN SSOP (10.2 x 5.3 x 1.75 mm) **DM007.E**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	0.25
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	9.90	10.20	10.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1		1.25 REF	
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

IMPORTANT NOTICE

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.

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REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	CHANGED BY
14/02/13	4.3	Digital supply operation changed from 3.0V to 3.6V to 3.15 to 3.6V	JMacD
14/02/13	4.3	Operating temp changed from -40°C to +85°C to 0°C to +70°C	JMacD
17/01/20	4.4	Ordering Information and Absolute Maximum Ratings updated – MSL information removed	PH