Standard Products

QCOTS™ UT9Q512K32 16Megabit SRAM MCM

Data Sheet

June, 2003

FEATURES

- 25ns maximum (5 volt supply) address access time
- Asynchronous operation for compatible with industry standard 512K x 8 SRAMs
- TTL compatible inputs and output levels, three-state bidirectional data bus
- Typical radiation performance
  - Total dose: 50krads
  - SEL Immune >80 MeV-cm^2/mg
  - LET$_{TH}$(0.25) = >10 MeV-cm^2/mg
  - Saturated Cross Section (cm^2) per bit, 5.0E-9
    - ≤1E-8 errors/bit-day, Adams 90% geosynchronous heavy ion
- Packaging options:
  - 68-lead dual cavity ceramic quad flatpack (CQFP) - (weight 7.37 grams)
- Standard Microcircuit Drawing 5962-01511
  - QML T and Q compliant part

INTRODUCTION

The QCOTS™ UT9Q512K32 Quantified Commercial Off-the-Shelf product is a high-performance 2M byte (16Mbit) CMOS static RAM multi-chip module (MCM), organized as four individual 524,288 x 8 bit SRAMs with a common output enable. Memory expansion is provided by an active LOW chip enable ($\overline{E}n$), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to each memory is accomplished by taking chip enable ($\overline{E}n$) input LOW and write enable ($\overline{W}n$) inputs LOW. Data on the eight I/O pins (DQ_0 through DQ_7) is then written into the location specified on the address pins (A_0 through A_{18}). Reading from the device is accomplished by taking chip enable ($\overline{E}n$) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}n$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The input/output pins are placed in a high impedance state when the device is deselected ($\overline{E}n$ HIGH), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E}n$ LOW and $\overline{W}n$ LOW). Perform 8, 16, 24 or 32 bit accesses by making $\overline{W}n$ along with $\overline{E}n$ a common input to any combination of the discrete memory die.

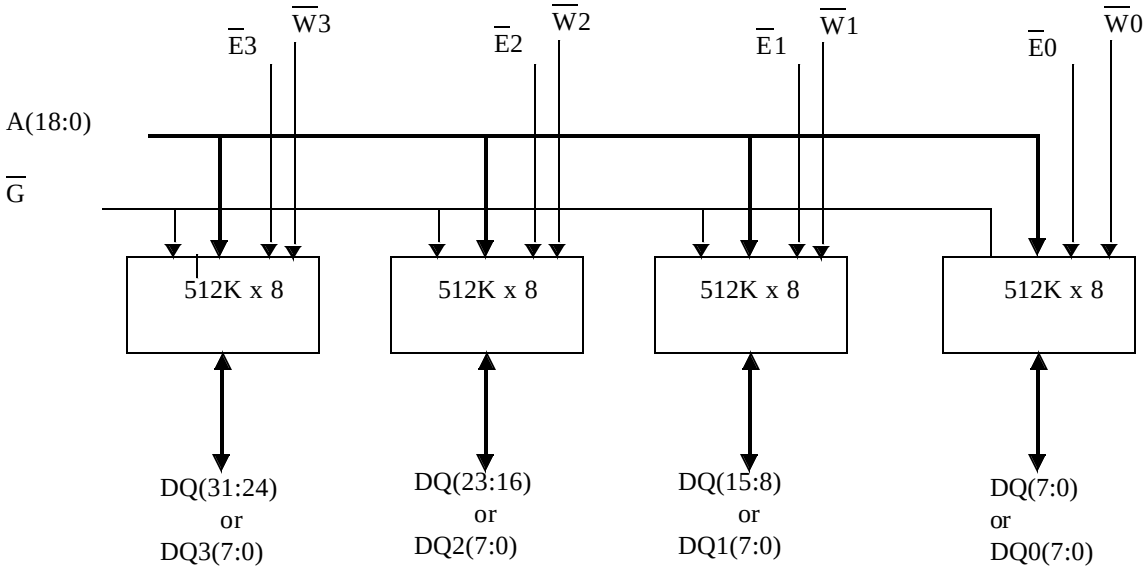


Figure 1. UT9Q512K32 SRAM Block Diagram

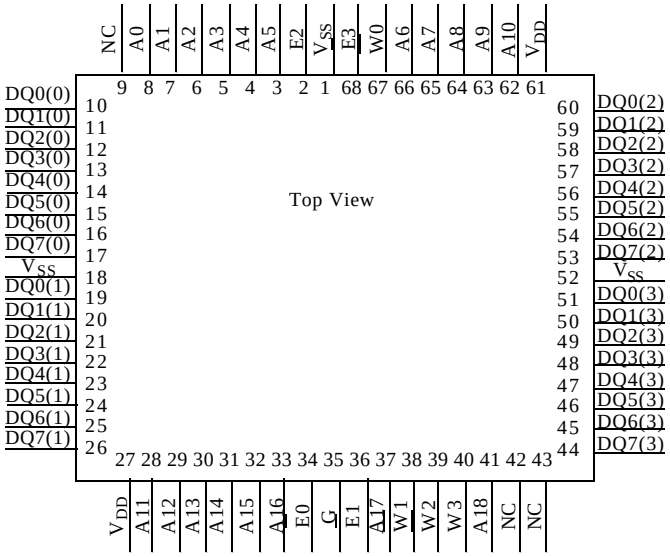


Figure 2. 25ns SRAM Pinout (68)

PIN NAMES

A(18:0)	Address	$\overline{Wn}$	Write Enable
DQn(7:0)	Data Input/Output	$\overline{G}$	Output Enable
$\overline{En}$	Enable	V_{DD}	Power
		V_{SS}	Ground

DEVICE OPERATION

The UT9Q512 has three control inputs called Enable 1 ($\overline{En}$), Write Enable ($\overline{Wn}$), and Output Enable ($\overline{G}$); 19 address inputs, A(18:0); and eight bidirectional data lines, DQ(7:0). $\overline{En}$ Device Enable controls device selection, active, and standby modes. Asserting $\overline{En}$ enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory. $\overline{Wn}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{Wn}$	$\overline{En}$	I/O Mode	Mode
X[1]	X	1	3-state	Standby
X	0	0	Data in	Write
1	1	0	3-state	Read[2]
0	1	0	Data out	Read

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

READ CYCLE

A combination of $\overline{Wn}$ greater than V_{IH} (min) and $\overline{En}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of Device Enable, Output Enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{Wn}$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as Device Enable and Output Enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM read Cycle 2, the Chip Enable - Controlled Access in figure 3b, is initiated by $\overline{En}$ going active while $\overline{G}$ remains asserted, $\overline{Wn}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).

SRAM read Cycle 3, the Output Enable - Controlled Access in figure 3c, is initiated by $\overline{G}$ going active while $\overline{En}$ is asserted, $\overline{Wn}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

WRITE CYCLE

A combination of $\overline{W}n$ less than V_{IL}(max) and $\overline{E}n$ less than V_{IL}(max) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}n$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access is defined by a write terminated by $\overline{W}n$ going high, with $\overline{E}n$ still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}n$, and by t_{ETWH} when the write is initiated by $\overline{E}n$. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the nine bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access is defined by a write terminated by the latter of $\overline{E}n$ going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}n$, and by t_{ETEF} when the write is initiated by the $\overline{E}n$ going active. For the $\overline{W}n$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

TYPICAL RADIATION HARDNESS

The UT9Q512K32 SRAM incorporates features which allows operation in a limited radiation environment.

Table 2. Radiation Hardness Design Specifications [1]

Total Dose	50	krad(Si)
Heavy Ion Error Rate [2]	<1E-8	Errors/Bit-Day

Notes:
1. The SRAM will not latchup during radiation exposure under recommended operating conditions.
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.5 to 7.0V
$V_{I/O}$	Voltage on any pin	-0.5 to 7.0V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.0W (per byte)
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	10°C/W
I_I	DC input current	±10 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
3. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	4.5 to 5.5V
T_C	Case temperature range	-40 to +125°C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

(-40°C to +125°C) (V_{DD} = 5.0V ± 10%)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2.0		V
V_{IL}	Low-level input voltage			0.8	V
V_{OL1}	Low-level output voltage	I_{OL} = 8mA, V_{DD} =4.5V		0.4	V
V_{OL2}	Low-level output voltage	I_{OL} = 200µA, V_{DD} =4.5V		0.08	V
V_{OH1}	High-level output voltage	I_{OH} = -4mA, V_{DD} =4.5V	2.4		V
V_{OH2}	High-level output voltage	I_{OH} = 200µA, V_{DD} =4.5V	3.0		V
C_{IN}[1]	Input capacitance	*f* = 1MHz @ 0V		32	pF
C_{IO}[1]	Bidirectional I/O capacitance	*f* = 1MHz @ 0V		16	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}, V_{DD} = V_{DD} (max)	-2	2	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS} V_{DD} = V_{DD} (max) $\overline{G}$ = V_{DD} (max)	-2	2	µA
I_{OS}[2, 3]	Short-circuit output current	V_{DD} = V_{DD} (max), V_O = V_{DD} V_{DD} = V_{DD} (max), V_O = 0V	-90	90	mA
I_{DD}(OP)	Supply current operating @ 1MHz (per byte)	Inputs: V_{IL} = 0.8V, V_{IH} = 2.0V I_{OUT} = 0mA V_{DD} = V_{DD} (max)		125	mA
I_{DD1}(OP)	Supply current operating @40MHz (per byte)	Inputs: V_{IL} = 0.8V, V_{IH} = 2.0V I_{OUT} = 0mA V_{DD} = V_{DD} (max)		180	mA
I_{DD2}(SB)	Supply current standby @0MHz (per byte)	Inputs: V_{IL} = V_{SS} I_{OUT} = 0mA $\overline{E1}$ = V_{DD} - 0.5, V_{DD} = V_{DD} (max) V_{IH} = V_{DD} - 0.5V	-40°C and 25°C	6	mA
			125°C	12	mA

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.

AC CHARACTERISTICS READ CYCLE (Pre/Post-Radiation)*

(-40°C to +125°C) (V_{DD} = 5.0V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}[1]	Read cycle time	25		ns
t_{AVQV}	Read access time		25	ns
t_{AXQX}[2]	Output hold time	3		ns
t_{GLQX}[2]	$\overline{G}$-controlled Output Enable time	3		ns
t_{GLQV}	$\overline{G}$-controlled Output Enable time (Read Cycle 3)		10	ns
t_{GHQZ}[2]	$\overline{G}$-controlled output three-state time		10	ns
t_{ETQX}[2,3]	$\overline{E}$n-controlled Output Enable time	3		ns
t_{ETQV}[3]	$\overline{E}$n-controlled access time		25	ns
t_{EFQZ}[1,2,4]	$\overline{E}$n-controlled output three-state time		10	ns

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Functional test.
2. Three-state is defined as a 500mV change from steady-state output voltage.
3. The ET (enable true) notation refers to the falling edge of $\overline{E}$n. SEU immunity does not affect the read parameters.
4. The EF (enable false) notation refers to the rising edge of $\overline{E}$n. SEU immunity does not affect the read parameters.

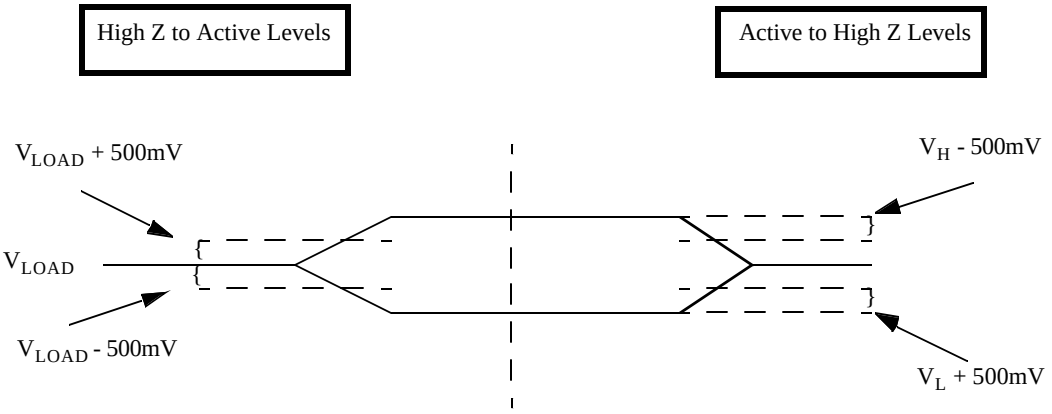
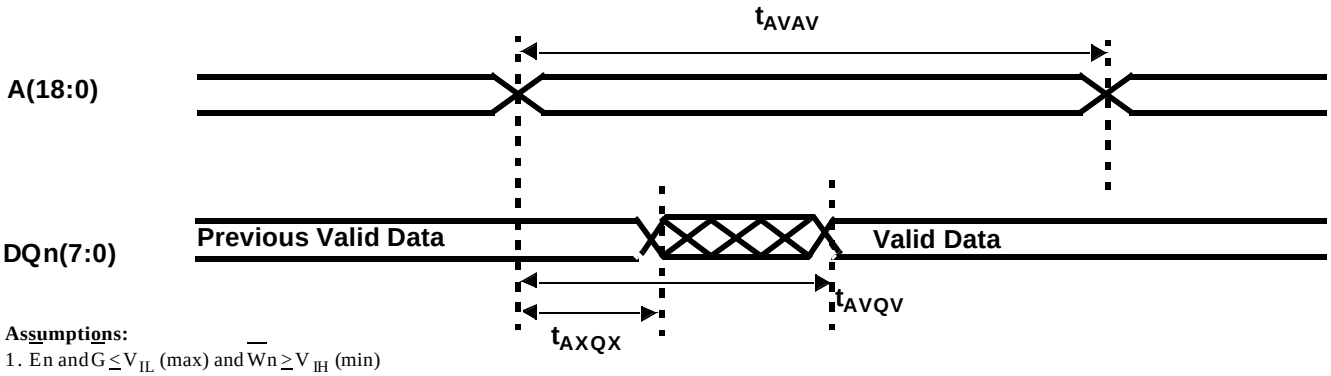
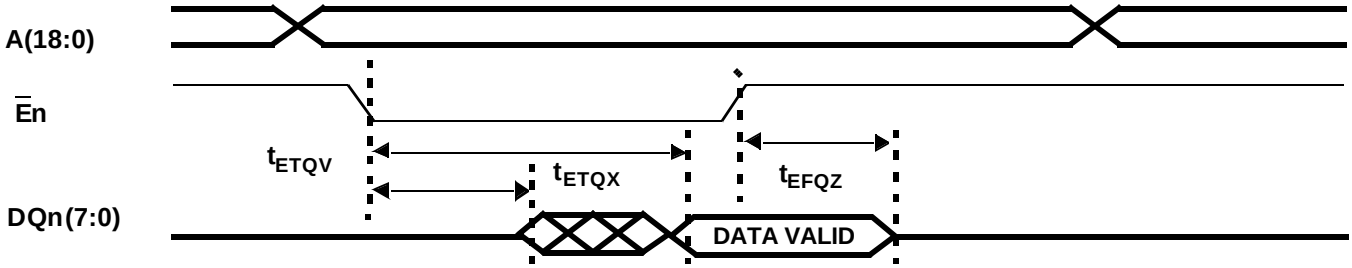


Figure 3. 5-Volt SRAM Loading



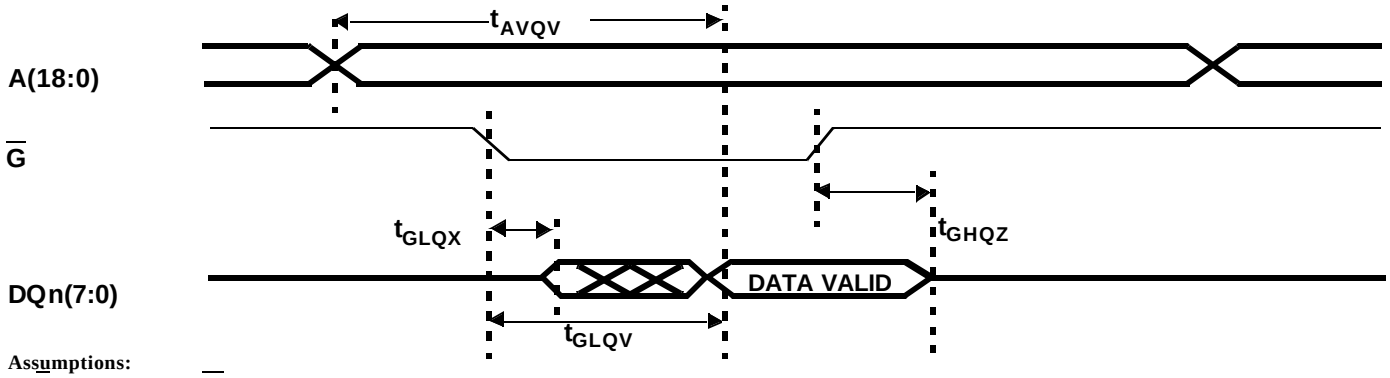
Assumptions:
1. $\overline{E}n$ and $G \leq V_{IL}$ (max) and $\overline{W}n \geq V_{IH}$ (min)

Figure 4a. SRAM Read Cycle 1: Address Access



Assumptions:
1. $G \leq V_{IL}$ (max) and $\overline{W}n \geq V_{IH}$ (min)

Figure 4b. SRAM Read Cycle 2: Chip Enable-Controlled Access



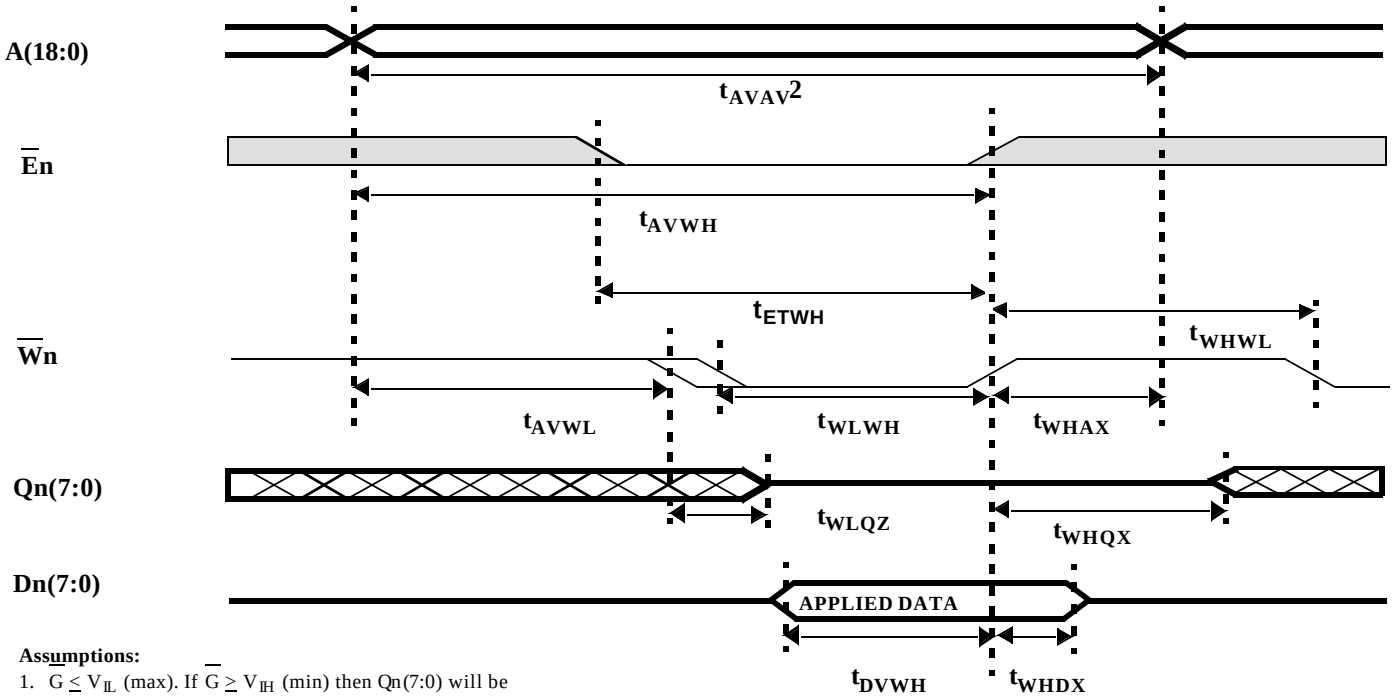
Assumptions:
1. $\overline{E}n \leq V_{IL}$ (max) and $\overline{W}n \geq V_{IH}$ (min)

Figure 4c. SRAM Read Cycle 3: Output Enable-Controlled Access

AC CHARACTERISTICS WRITE CYCLE (Pre/Post-Radiation)*
(-40°C to +125°C) (V_{DD} = 5.0V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}[1]	Write cycle time	25		ns
t_{ETWH}	Device Enable to end of write	20		ns
t_{AVET}	Address setup time for write ($\overline{E}$n - controlled)	1		ns
t_{AVWL}	Address setup time for write ($\overline{W}$n - controlled)	0		ns
t_{WLWH}	Write pulse width	20		ns
t_{WHAX}	Address hold time for write ($\overline{W}$n - controlled)	0		ns
t_{EFAX}	Address hold time for Device Enable ($\overline{E}$n - controlled)	0		ns
t_{WLQZ}[2]	$\overline{W}$n - controlled three-state time		10	ns
t_{WHQX}[2]	$\overline{W}$n - controlled Output Enable time	5		ns
t_{ETEF}	Device Enable pulse width ($\overline{E}$n - controlled)	20		ns
t_{DVWH}	Data setup time	15		ns
t_{WHDX}	Data hold time	0		ns
t_{WLEF}	Device Enable controlled write pulse width	20		ns
t_{DVEF}	Data setup time	15		ns
t_{EFDX}	Data hold time	0		ns
t_{AVWH}	Address valid to end of write	20		ns
t_{WHWL}[1]	Write disable time	5		ns

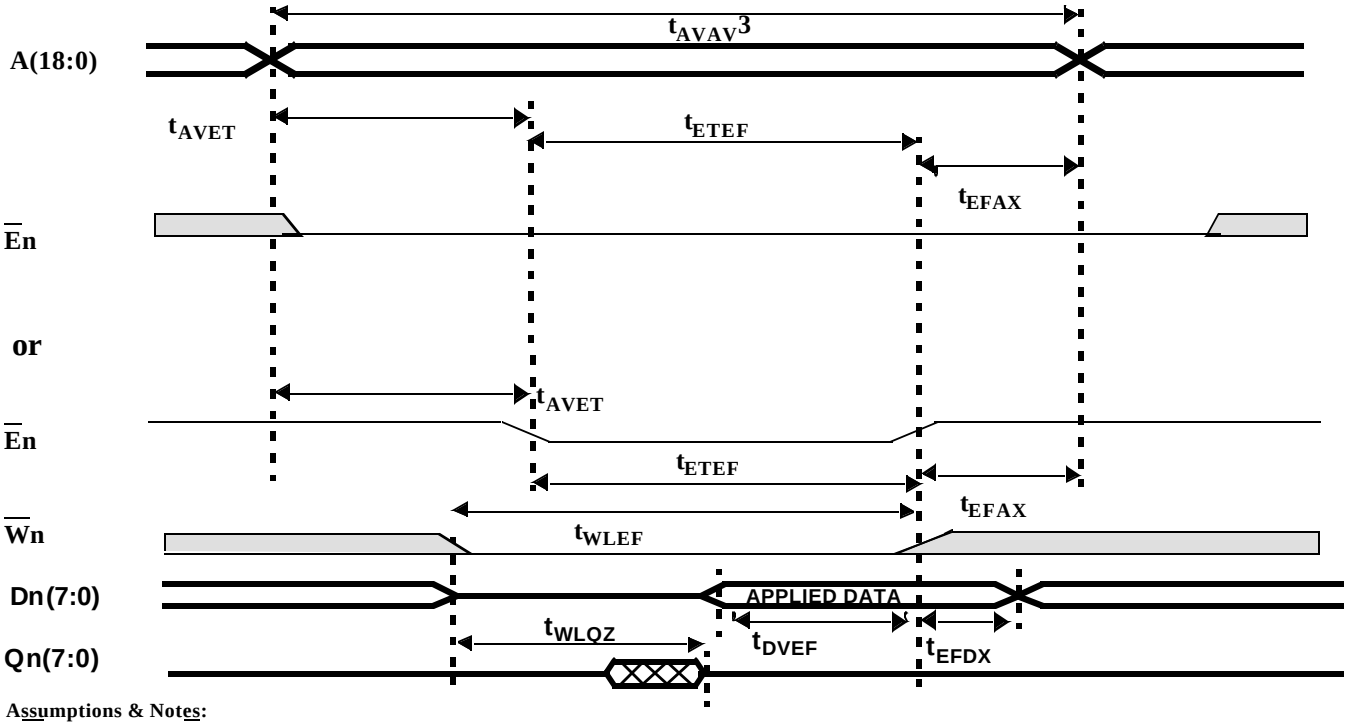
Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Functional test performed with outputs disabled (G high).
2. Three-state is defined as 500mV change from steady-state output voltage.



Assumptions:

1. $G \leq V_{IL}$ (max). If $G \geq V_{IH}$ (min) then Qn(7:0) will be in three-state for the entire cycle.
2. G high for t_{AVAV} cycle.

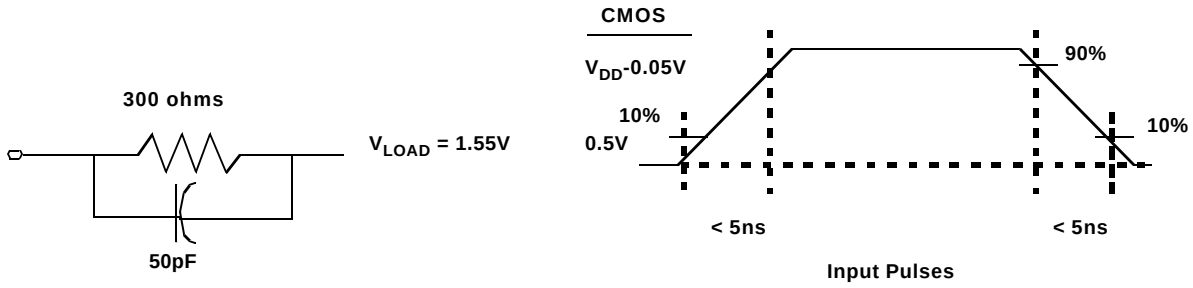
Figure 5a. SRAM Write Cycle 1: Write Enable - Controlled Access



Assumptions & Notes:

1. $G \leq V_{IL}$ (max). If $G \geq V_{IH}$ (min) then Qn(7:0) will be in three-state for the entire cycle.
2. Either En scenario above can occur.
3. G high for t_{AVAV} cycle.

Figure 5b. SRAM Write Cycle 2: Chip Enable - Controlled Access



Notes:

1. 50pF including scope probe and test socket capacitance.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD}/2$).

Figure 6. AC Test Loads and Input Waveforms

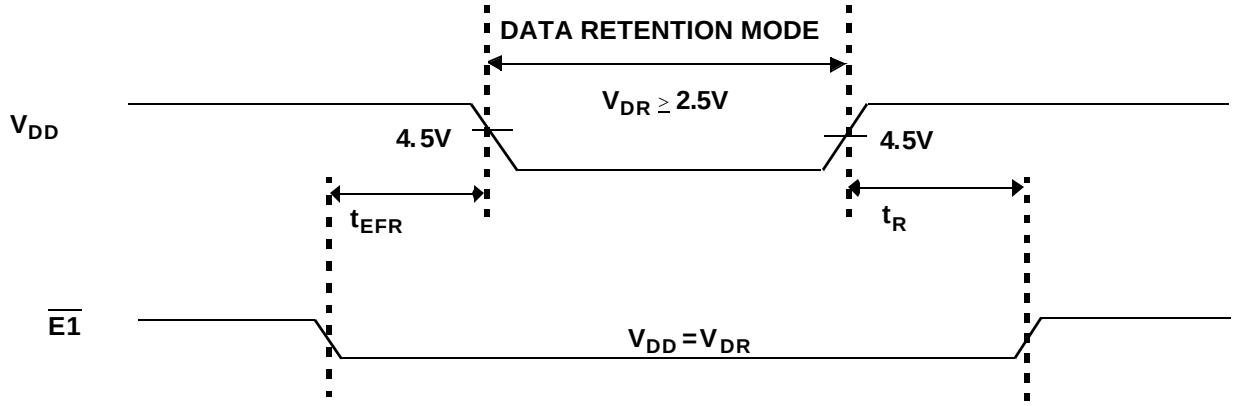


Figure 7. Low V_{DD} Data Retention Waveform

DATA RETENTION CHARACTERISTICS (Pre/Post-Irradiation)

(1 Second Data retention Test)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
V_{DR}	V_{DD} for data retention	2.5	--	V
I_{DDR} [1,2]	Data retention current (per byte)	--	5.0	mA
t_{EFR} [1,3]	Chip deselect to data retention time	0		ns
t_R [1,3]	Operation recovery time	t_{AVAV}		Ns

Notes:

1. En = V_{DD} - .2V, all other inputs = V_{DR} or V_{SS}.
2. Data retention current (I_{DDR}) Tc = 25°C.
3. Not guaranteed or tested.
4. V_{DR} = T=-40°C and 125°C.

DATA RETENTION CHARACTERISTICS (Pre/Post-Irradiation)

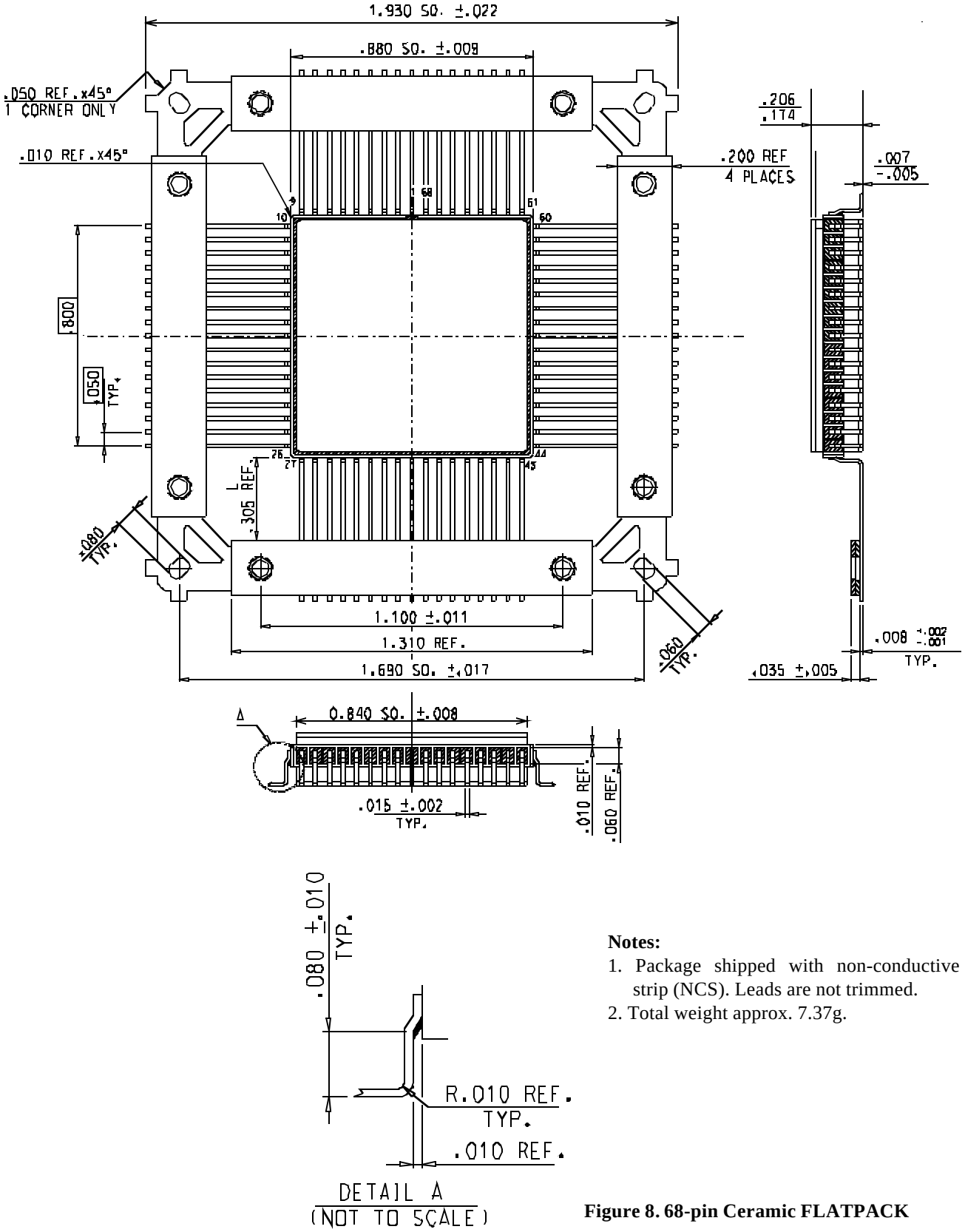
(10 Second Data Retention Test, T_C=-40°C and +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
V_{DD} [1]	V_{DD} for data retention	4.5	5.5	V
t_{EFR} [2, 3]	Chip select to data retention time	0		ns
t_R [2, 3]	Operation recovery time	t_{AVAV}		ns

Notes:

1. Performed at V_{DD} (min) and V_{DD} (max).
2. En = V_{SS}, all other inputs = V_{DR} or V_{SS}.
3. Not guaranteed or tested.

PACKAGING



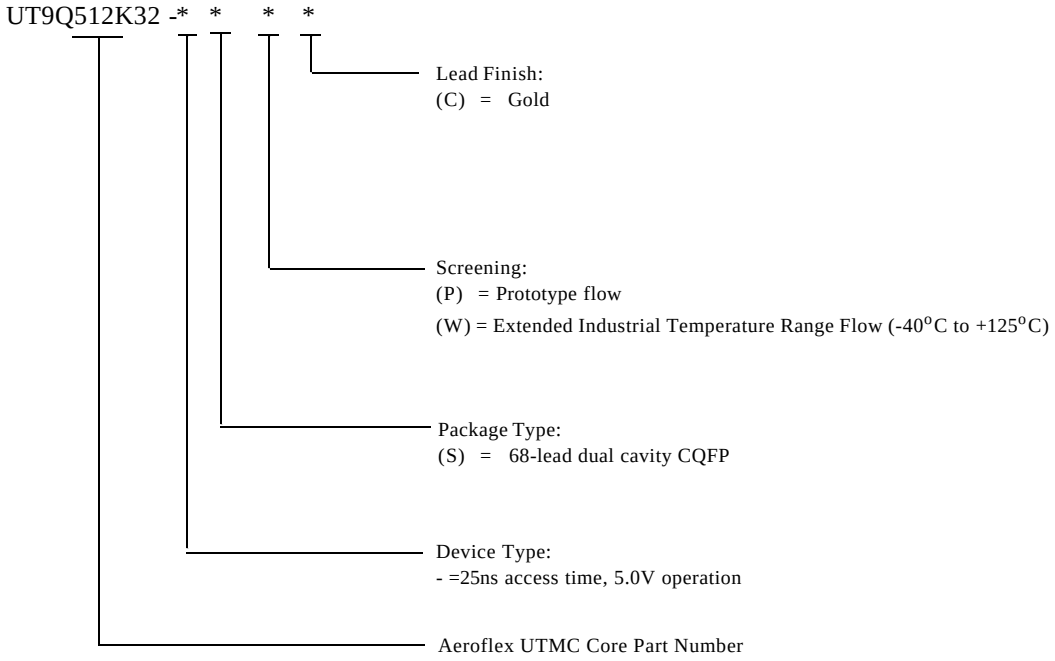
Notes:

1. Package shipped with non-conductive strip (NCS). Leads are not trimmed.
2. Total weight approx. 7.37g.

Figure 8. 68-pin Ceramic FLATPACK

ORDERING INFORMATION

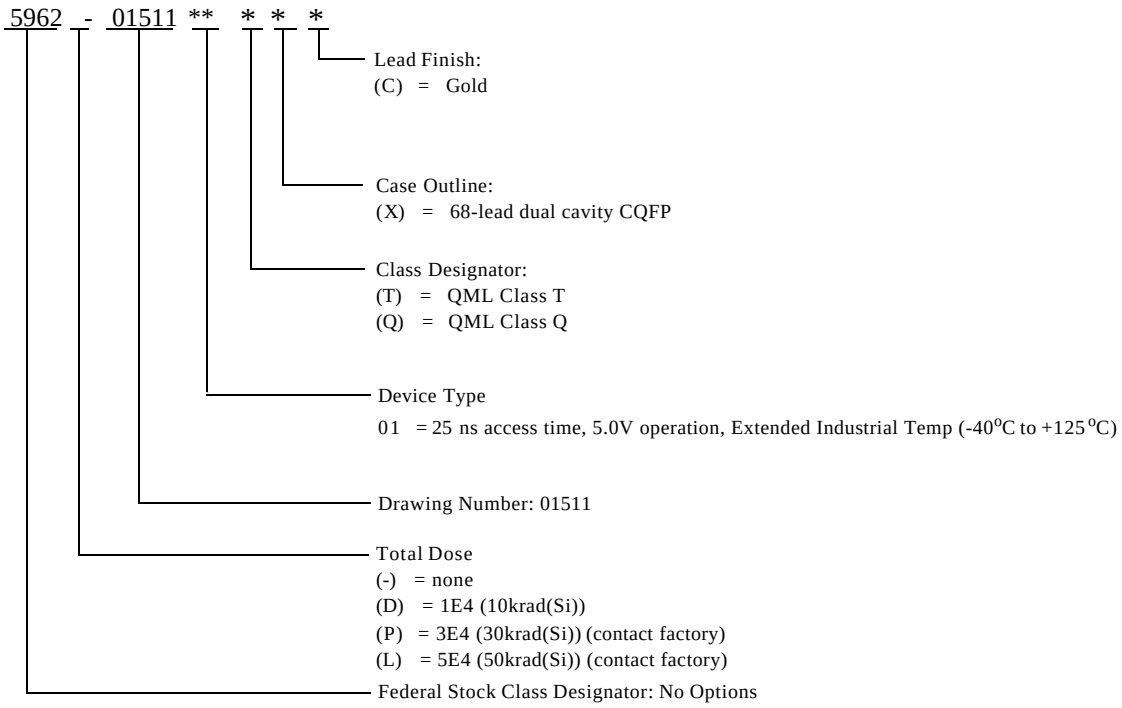
512K32 16Megabit SRAM MCM:



Notes:

1. Prototype flow per UTMC Manufacturing Flows Document. Devices are tested at 25°C. Gold lead finish only.
2. Extended Industrial Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -40°C to +125°C. Radiation neither tested nor guaranteed. Gold Lead Finish Only.

512K32 16Megabit SRAM MCM: SMD



Notes:
1. Total dose radiation must be specified when ordering. Gold finish only.
2. Only Extended Industrial temperature -40C to +125C. No military temp. test available.