

Features

- 8 configurable IOs supporting
 - CapSense buttons
 - LED Drive
 - Interrupt outputs
 - WAKE on interrupt input
 - User defined input or output
- 2.4V to 5.25V operating voltage
- Industrial temperature range: -40°C to +85°C
- I²C slave interface for configuration
 - Selectable to 50 kHz, 100 kHz and 400 kHz
- Reduce BOM cost
 - Internal oscillator - no external oscillators or crystal
 - Free development tool - no external tuning components
- Low operating current
 - Active current: continuous sensor scan: 1.5 mA
 - Sleep current: no scan, continuous sleep: 2.6 uA
- Available in 16-pin COL and 16-pin SOIC packages

Overview

The CapSense Express™ controller allows the control of 8 IOs configurable as capacitive sensing buttons or as GPIOs for driving LEDs or interrupt signals based on various button conditions. The GPIOs are also configurable for waking up the device from sleep based on an interrupt input.

The user has the ability to configure buttons, outputs, and parameters through specific commands sent to the I²C port. The IOs have the flexibility in mapping to capacitive buttons and as standard GPIO functions such as interrupt output or input, LED drive and digital mapping of input to output using simple logical operations. This enables easy PCB trace routing and reduces the PCB size and stack up. CapSense Express products are designed for easy integration into complex products.

Architecture

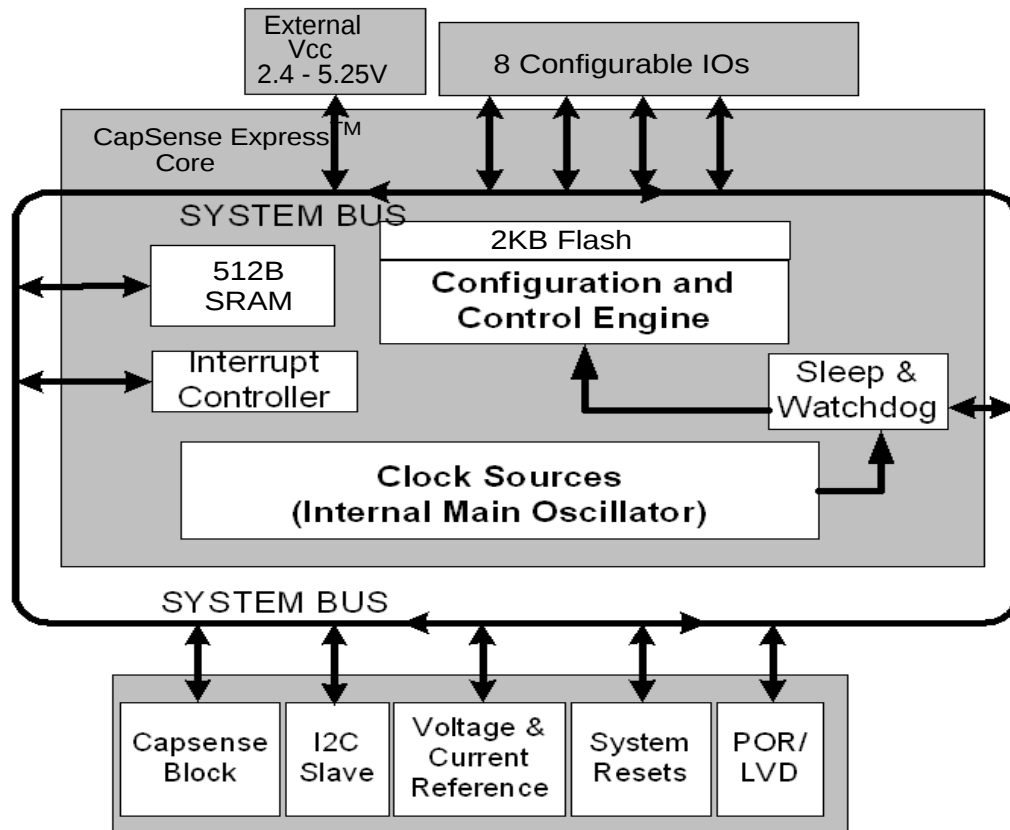
The logic block diagram illustrates the internal architecture of CY8C20180.

The user can configure registers with parameters needed to adjust the operation and sensitivity of the CapSense system. CY8C20180 supports a standard I²C serial communications interface that allows the host to configure the device and to read sensor information in real time through easy register access.

The CapSense Express Core

The CapSense Express Core has a powerful configuration and control block. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers. System resources provide additional capability, such as a configurable I²C slave communication interface and various system resets. The Analog System is composed of the CapSense PSoC block which supports capacitive sensing of up to eight inputs.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 16 Pin COL

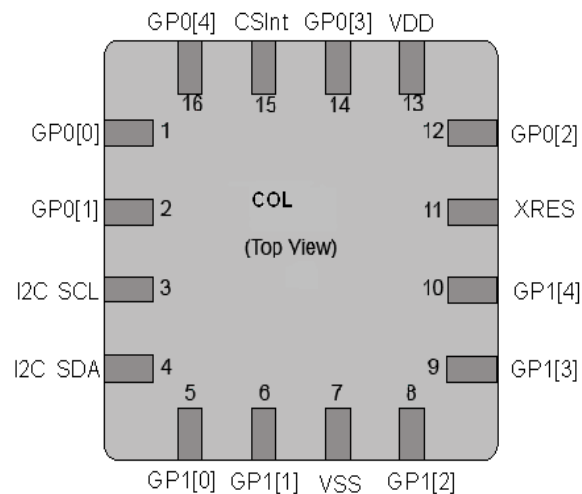
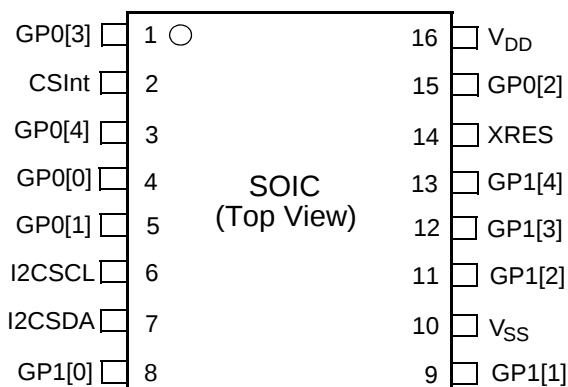


Table 1. Pin Definitions - 16 Pin COL

Pin Number	Name	Description
1	GP0[0]	Configurable as CapSense or GPIO
2	GP0[1]	Configurable as CapSense or GPIO
3	I ² C SCL	I ² C clock
4	I ² C SDA	I ² C data
5	GP1[0]	Configurable as CapSense or GPIO
6	GP1[1]	Configurable as CapSense or GPIO
7	VSS	Ground connection
8	GP1[2]	Configurable as CapSense or GPIO
9	GP1[3]	Configurable as CapSense or GPIO
10	GP1[4]	Configurable as CapSense or GPIO
11	XRES	Active HIGH external reset with internal pull down
12	GP0[2]	Configurable as CapSense or GPIO
13	V _{DD}	Supply voltage
14	GP0[3]	Configurable as CapSense or GPIO
15	CSInt	Integrating Input. The external capacitance is required only if 5:1 SNR cannot be achieved. Typical range is 10-100 nF.
16	GP0[4]	Configurable as CapSense or GPIO

Figure 2. Pin Diagram - 16 Pin SOIC

Table 2. Pin Definitions - 16 Pin SOIC

Pin Number	Name	Description
1	GP0[3]	Configurable as CapSense or GPIO
2	CSInt	Integrating Input. The external capacitance is required only if 5:1 SNR cannot be achieved. Typical range is 10-100 nF.
3	GP0[4]	Configurable as CapSense or GPIO
4	GP0[0]	Configurable as CapSense or GPIO
5	GP0[1]	Configurable as CapSense or GPIO
6	I ² C SCL	I ² C clock
7	I ² C SDA	I ² C data
8	GP1[0]	Configurable as CapSense or GPIO
9	GP1[1]	Configurable as CapSense or GPIO
10	V _{SS}	Ground connection
11	GP1[2]	Configurable as CapSense or GPIO
12	GP1[3]	Configurable as CapSense or GPIO
13	GP1[4]	Configurable as CapSense or GPIO
14	XRES	Active HIGH external reset with internal pull down.
15	GP0[2]	Configurable as CapSense or GPIO
16	V _{DD}	Supply voltage

The CapSense Analog System

The CapSense analog system contains the capacitive sensing hardware, which supports CapSense Successive Approximation (CSA) algorithm. This hardware performs capacitive sensing and scanning without external components. Capacitive sensing is configurable on each pin.

Additional System Resources

System resources provide additional capability useful to complete systems. Additional resources are low voltage detection and power on reset (POR).

- The I²C slave provides 50, 100, or 400 kHz communication over two wires.
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels and the advanced POR circuit eliminates the need for a system supervisor.

An internal 1.8V reference provides a stable internal reference so that capacitive sensing functionality is not affected by minor V_{DD} changes.

I²C Interface

The two modes of operation for the I²C interface are:

- Device register configuration and status read or write for controller.
- Command execution.

The I²C address is programmable during configuration. It can be locked to prevent accidental change by setting a flag in a configuration register.

CapSense Express Software Tool

An easy to use software tool integrated with PSoC Express is available for configuring and tuning CapSense Express devices. Refer to the Application Note [AN42137](#) for details of the software tool.

CapSense Express Register Map

CapSense Express supports user configurable registers through which the device functionality and parameters are configured. For details, refer to [CY8C201xx Register Reference](#) document.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T _{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C (0°C to 50°C). Extended duration storage temperatures above 65°C degrade reliability.
T _A	Ambient temperature with power applied	–40	–	+85	°C	
V _{DD}	Supply voltage on V _{DD} relative to V _{SS}	–0.5	–	+6.0	V	
V _{IO}	DC input voltage	V _{SS} – 0.5	–	V _{DD} + 0.5	V	
V _{IOZ}	DC voltage applied to tri-state	V _{SS} – 0.5	–	V _{DD} + 0.5	V	
I _{MIO}	Maximum current into any GPIO pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	

Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T _A	Ambient temperature	–40	–	+85	°C	
T _J	Junction temperature	–40	–	+100	°C	

DC Electrical Characteristics

DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	
I_{DD}	Supply current	–	1.5	2.5	mA	Conditions are $V_{DD} = 3.0V$, $T_A = 25^\circ C$
I_{SB}	Sleep mode current with POR and LVD active. Mid temperature range	–	2.6	4	μA	$V_{DD} = 2.55V$, $0^\circ C \leq T_A \leq 40^\circ C$
I_{SB}	Sleep mode current with POR and LVD active.	–	2.8	5	μA	$V_{DD} = 3.3V$, $-40^\circ C \leq T_A \leq 85^\circ C$
I_{SB}	Sleep mode current with POR and LVD active.	–	5.2	6.4	μA	$V_{DD} = 5.25V$, $-40^\circ C \leq T_A \leq 85^\circ C$

5 and 3.3V DC General Purpose IO Specifications

This Table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: $4.75V$ to $5.25V$ and $-40^\circ C \leq T_A \leq 85^\circ C$, $3.0V$ to $3.6V$ and $-40^\circ C \leq T_A \leq 85^\circ C$ respectively. Typical parameters apply to $5V$ and $3.3V$ at $25^\circ C$. These are for design guidance only.

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull up resistor	4	5.6	8	$k\Omega$	
V_{OH1}	High output voltage Port 0 pins	$V_{DD} - 0.2$	–	–	V	$I_{OH} = 10 \mu A$, $V_{DD} \geq 3.0V$, maximum of 20 mA source current in all IOs.
V_{OH2}	High output voltage Port 0 pins	$V_{DD} - 0.9$	–	–	V	$I_{OH} = 1 \text{ mA}$, $V_{DD} \geq 3.0V$, maximum of 20 mA source current in all IOs.
V_{OH3}	High output voltage Port 1 pins	$V_{DD} - 0.2$	–	–	V	$I_{OH} < 10 \mu A$, $V_{DD} \geq 3.0V$, maximum of 10 mA source current in all IOs.
V_{OH}	High output voltage Port 1 pins	$V_{DD} - 0.9$	–	–	V	$I_{OH} = 5 \text{ mA}$, $V_{DD} \geq 3.0V$, maximum of 20 mA source current in all IOs.
V_{OH5}	High output voltage. Port 1 pins with 3.0V LDO regulator enabled	2.75	3.0	3.2	V	$I_{OH} < 10 \mu A$, $V_{DD} \geq 3.1V$, maximum of 4 IOs all sourcing 5mA.
V_{OH6}	High Output Voltage Port 1 pins with 3.0V LDO regulator enabled	2.2	–	–	V	$I_{OH} = 5 \text{ mA}$, $V_{DD} \geq 3.1V$, maximum of 20 mA source current in all IOs.
V_{OH7}	High Output Voltage. Port 1 pins with 2.4V LDO regulator enabled	2.1	2.4	2.5	V	$I_{OH} < 10 \mu A$, $V_{DD} \geq 3.0V$, maximum of 20 mA source current in all IOs.
V_{OH8}	High Output Voltage. Port 1 pins with 2.4V LDO regulator enabled	2	–	–	V	$I_{OH} < 200 \mu A$, $V_{DD} \geq 3.0V$, maximum of 20 mA source current in all IOs.
V_{OL}	Low output voltage	–	–	0.75	V	$I_{OL} = 20 \text{ mA}$, $V_{DD} > 3V$, maximum of 60 mA sink current on even port pins and 60 mA sink current on odd port pins
V_{IL}	Input low voltage	–	–	0.75	V	$V_{DD} = 3$ to $3.6V$
V_{IH}	Input high voltage	1.6	–	–	V	$V_{DD} = 3$ to $3.6V$
V_{IL}	Input low voltage	–	–	0.8	V	$V_{DD} = 3.6$ to $5.25V$.
V_{IH}	Input high voltage	2.0	–	–	V	$V_{DD} = 3.6$ to $5.25V$.
V_H	Input hysteresis voltage	–	140	–	mV	

5 and 3.3V DC General Purpose IO Specifications (continued)

This Table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ respectively. Typical parameters apply to 5V and 3.3V at 25°C . These are for design guidance only.

Parameter	Description	Min	Typ	Max	Unit	Notes
I_L	Input leakage	–	1	–	nA	Gross tested to 1 μA .
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C

2.7 V DC General Purpose IO Specifications

This Table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4V to 3.0V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 2.7V at 25°C . These are for design guidance only.

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull up resistor	4	5.6	8	$k\Omega$	
V_{OH1}	High output voltage Port 0 pins	$V_{DD} - 0.2$	–	–	V	$I_{OH} \leq 10 \mu\text{A}$, maximum of 10 mA source current in all IOs.
V_{OH2}	High output voltage Port 0 pins	$V_{DD} - 0.5$	–	–	V	$I_{OH} = 0.2 \text{ mA}$, maximum of 10 mA source current in all IOs.
V_{OH3}	High output voltage Port 1 pins	$V_{DD} - 0.2$	–	–	V	$I_{OH} < 10 \mu\text{A}$, maximum of 10 mA source current in all IOs.
V_{OH4}	High output voltage Port 1 pins	$V_{DD} - 0.5$	–	–	V	$I_{OH} = 2 \text{ mA}$, maximum of 10 mA source current in all IOs.
V_{OL}	Low output voltage	–	–	0.75	V	$I_{OL} = 10 \text{ mA}$, maximum of 30 mA sink current on even port pins and 30 mA sink current on odd port pins
V_{OLP1}	Low output voltage port 1 pins	–	–	0.4	V	$I_{OL} = 5 \text{ mA}$ Maximum of 50mA sink current on even port pins and 50mA sink current on odd port pins $2.4 \leq V_{DD} \leq 3.6 \text{ V}$
V_{IL}	Input low voltage	–	–	0.75	V	$V_{DD} = 2.4 \text{ to } 3.6 \text{ V}$.
V_{IH1}	Input high voltage	1.4	–	–	V	$V_{DD} = 2.4 \text{ to } 2.7 \text{ V}$.
V_{IH2}	Input high voltage	1.6	–	–	V	$V_{DD} = 2.7 \text{ to } 3.6 \text{ V}$.
V_H	Input hysteresis voltage	–	60	–	mV	
I_{IL}	Input leakage	–	1	–	nA	Gross tested to 1 μA .
C_{IN}	Capacitive Load On Pins As Input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C .
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25°C .

DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V _{PPOR0}	V _{DD} Value PPOR Trip	–	2.36	2.40	V	V _{DD} must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V _{PPOR1}	V _{DD} = 2.7V V _{DD} = 3.3V, 5V	–	2.60	2.65	V	
VLVD0	V _{DD} Value for LVD trip	2.39	2.45	2.51	V	
VLVD2	V _{DD} = 2.7V	2.75	2.92	2.99	V	
VLVD6	V _{DD} = 3.3V V _{DD} = 5V	3.98	4.05	4.12	V	

AC Electrical Characteristics

5.0V and 3.3V AC General Purpose IO Specifications

Parameter	Description	Min	Max	Unit	Notes
TRise0	Rise time, strong mode, Cload = 50pF, Port 0	15	80	ns	V _{DD} = 3.0V to 3.6V and 4.75V to 5.25V, 10% - 90%
TRise1	Rise time, strong mode, Cload = 50pF, Port 1	10	50	ns	V _{DD} = 3.0V to 3.6V, 10% - 90%
TFall	Fall time, strong mode, Cload = 50pF, all ports	10	50	ns	V _{DD} = 3.0V to 3.6V and 4.75V to 5.25V, 10% - 90%

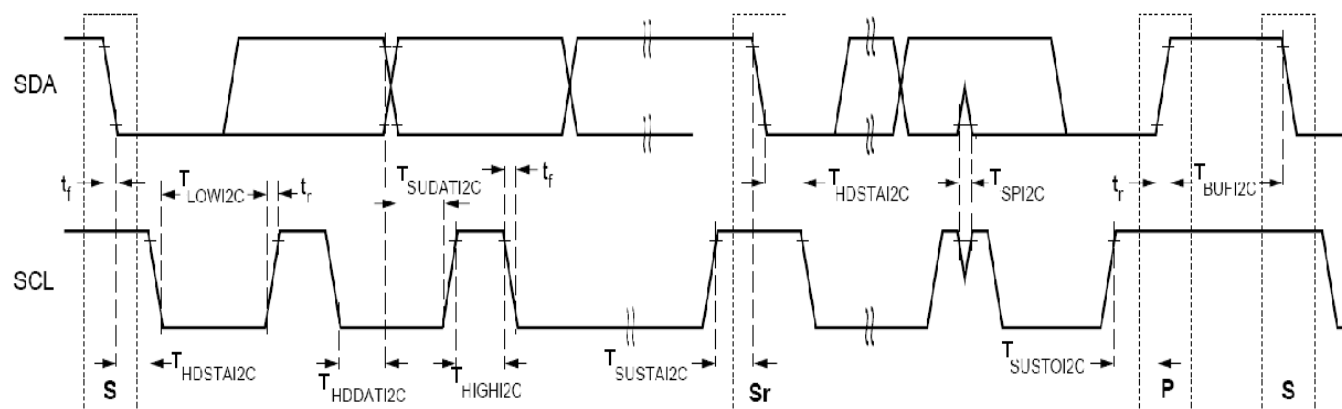
2.7V AC General Purpose IO Specifications

Parameter	Description	Min	Max	Unit	Notes
TRise0	Rise time, strong mode, Cload = 50pF, Port 0	15	100	ns	V _{DD} = 2.4V to 3.0V, 10% - 90%
TRise1	Rise time, strong mode, Cload = 50pF, Port 1	10	70	ns	V _{DD} = 2.4V to 3.0V, 10% - 90%
TFall	Fall time, strong mode, Cload = 50pF, all ports	10	70	ns	V _{DD} = 2.4V to 3.0V, 10% - 90%

AC I²C Specifications

Parameter	Description	Standard Mode		Fast Mode		Unit	Notes
		Min	Max	Min	Max		
F _{SCL12C}	SCL clock frequency	0	100	0	400	KHz	Fast mode not supported for V _{DD} < 3.0V
T _{HDSTA12C}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs	
T _{LOW12C}	LOW period of the SCL clock	4.7	–	1.3	–	μs	
T _{HIGH12C}	HIGH period of the SCL clock	4.0	–	0.6	–	μs	
T _{SUSTA12C}	Setup time for a repeated START condition	4.7	–	0.6	–	μs	
T _{HDDAT12C}	Data hold time	0	–	0	–	μs	
T _{SUDAT12C}	Data setup time	250	–	100	–	ns	
T _{SUSTOI2C}	Setup time for STOP condition	4.0	–	0.6	–	μs	
T _{BUFI2C}	BUS free time between a STOP and START condition	4.7	–	1.3	–	μs	
T _{SPI2C}	Pulse width of spikes suppressed by the input filter	–	–	0	50	ns	

Figure 3. Definition for Timing for Fast/Standard Mode on the I2C Bus



Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Temperature
CY8C20180-LDX2I	001-09116	16 COL ^[3]	Industrial
CY8C20180-SX2I	51-85068	16 SOIC	Industrial

Thermal Impedances by Package

Package	Typical θ_{JA} ^[1]
16 COL ^[3]	46 °C
16 SOIC	79.96 °C

Solder Reflow Peak Temperature

Package	Minimum Peak Temperature ^[2]	Maximum Peak Temperature
16 COL ^[3]	240 °C	260 °C
16 SOIC	240 °C	260 °C

Notes

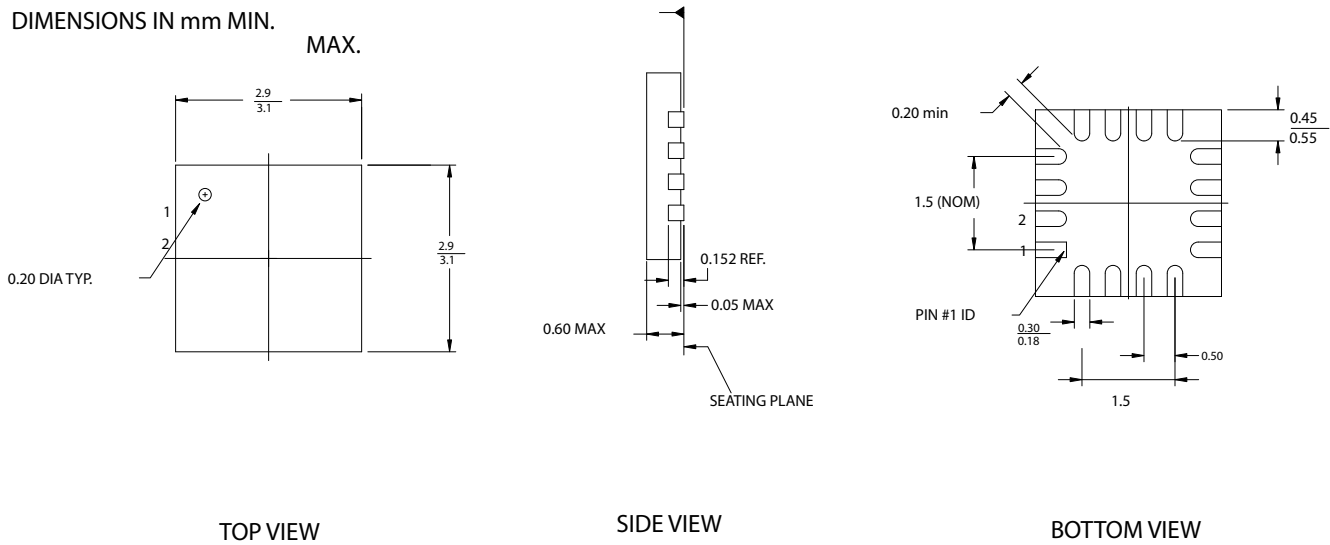
- $T_J = T_A + \text{Power} \times \theta_{JA}$.
- Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are $220 \pm 5^\circ\text{C}$ with Sn-Pb or $245 \pm 5^\circ\text{C}$ with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.
- Earlier termed as QFN package.

Package Diagram

Figure 4. 16L Chip On Lead 3 X 3 mm Package Outline (SAWN) - 001-09116 - (Pb-Free)

DIMENSIONS IN mm MIN.

MAX.



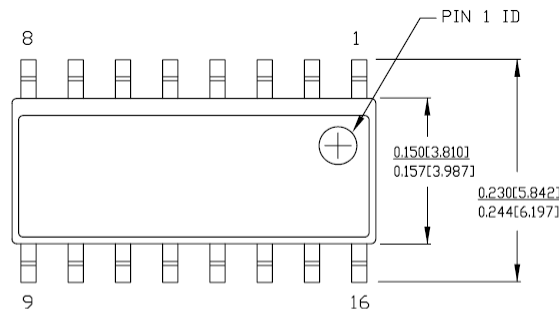
PART NO.	DESCRIPTION
LG16A	LEAD-FREE
LD16A	STANDARD

JEDEC # MO-220

Package Weight: 0.014g

001-09116-*C

Figure 5. 16 - Pin (150-Mil) SOIC (51-85068)

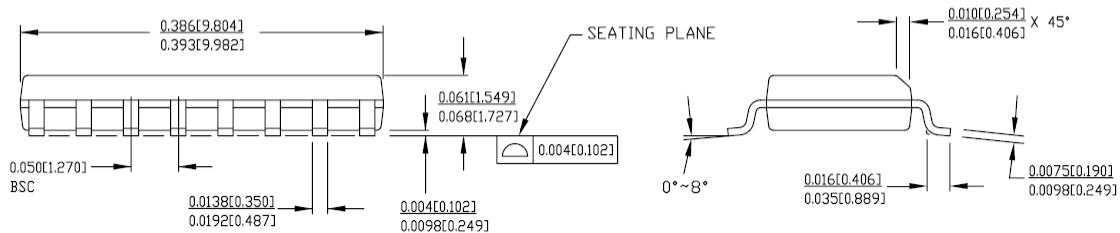


DIMENSIONS IN INCHES[MM] MIN.
MAX.

REFERENCE JEDEC MS-012

PACKAGE WEIGHT 0.15gms

PART #	
S16.15	STANDARD PKG.
SZ16.15	LEAD FREE PKG.



51-85068-*B

Document History Page

Document Title: CY8C20180 CapSense Express™ -8 Configurable IOs Document Number: 001-17346			
REV.	ECN.	Orig. of Change	Description of Change
**	1341766	TUP/FSU	New Data Sheet
*A	1494145	TUP/AESA	Changed to FINAL Datasheet Removed table - 2.7V DC General Purpose IO Specifications - Open Drain with a pull up to 1.8V Updated Logic Block Diagram
*B	1773608	TUP/AESA	Removed table - 3V DC General Purpose IO Specifications Updated Logic Block Diagram Updated table - DC POR and LVD Specifications Updated table - DC Chip Level Specifications Updated table - 5V and 3.3V DC General Purpose IO Specifications Updated table - 2.7V DC General Purpose IO Specifications Updated table - AC GPIO Specifications and split it into two tables for 5V/3.3V and 2.7V Added section on CapSense Express™ Software tool Updated 16-QFN Package Diagram
*C	2091026	DZU/MOHD /AESA	Updated table-DC Chip Level Specifications Updated table-Pin Definitions 16 pin COL Updated table-Pin Definitions 16 pin SOIC Updated table-5V and 3.3V DC General Purpose IO Specifications Updated table - 2.7V DC General Purpose IO Specifications Changed definition for Timing for Fast/Standard Mode on the I2C Bus diagram

© Cypress Semiconductor Corporation, 2007-2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.