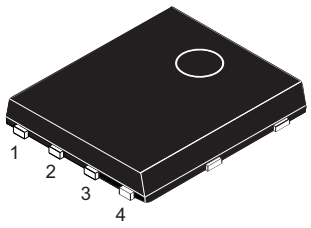
# STL13N65M2

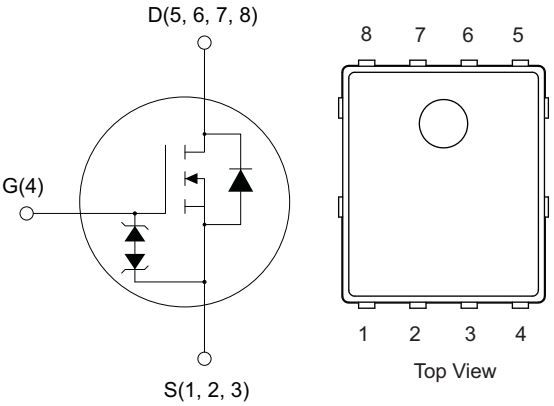
## N-channel 650 V, 0.365 Ω typ., 6.5 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 5x6 HV package

**Datasheet – production data**




**PowerFLAT™ 5x6 HV**

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STL13N65M2 | 650 V | 0.475 Ω | 6.5 A |

- Extremely low gate charge
- Excellent output capacitance ($C_{OSS}$) profile
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL13N65M2 | 13N65M2 | PowerFLAT™ 5x6 HV | Tape and reel |



This is information on a product in full production. www.st.com

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2 Electrical characteristics . . . . . 4

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3 Test circuits . . . . . 8

4 Package mechanical data . . . . . 9

5 Packaging mechanical data . . . . . 13

6 Revision history . . . . . 15

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ± 25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 6.5 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 4.1 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 26 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 52 | W |
| dv/dt (2) | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt(3) | MOSFET dv/dt ruggedness | 50 | V/ns |
| $T_{stg}$ | Storage temperature | - 55 to 150 | °C |
| $T_j$ | Max. operating junction temperature | 150 | |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 6.5$ A, di/dt $\leq 400$ A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, $V_{DD}$=400 V.
3. $V_{DS} \leq 520$ V

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 2.4 | °C/W |
| $R_{thj\text{-}pcb}$ | Thermal resistance junction-pcb max(1) | 59 | °C/W |

1. When mounted on 1 inch² FR-4, 2 Oz copper board

**Table 4. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$) | 1.5 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$; $V_{DD}$ = 50 V) | 110 | mJ |

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 5. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V, $T_C$=125 °C | | | 100 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ± 25 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 3 A | | 0.365 | 0.475 | Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz, | - | 590 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 27.5 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 1.1 | - | pF |
| $C_{oss\ eq.}$ (1) | Equivalent output capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 0 to 520 V | - | 168.5 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 6.5 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 520 V, $I_D$ = 10 A, $V_{GS}$ = 10 V (see *Figure 15*) | - | 17 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 3.3 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 7 | - | nC |

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 7. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 325 V, $I_D$ = 5 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 14* and *19*) | - | 11 | - | ns |
| $t_r$ | Rise time | | - | 7.8 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 38 | - | ns |
| $t_f$ | Fall time | | - | 12 | - | ns |

**Table 8. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 6.5 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 26 | A |
| $V_{SD}$ (2) | Forward on voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 6.5 A | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 10 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V (see *Figure 16*) | - | 312 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 2.7 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 17.5 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 10 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V, $T_j$ = 150 °C (see *Figure 16*) | - | 464 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 4 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 17.5 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

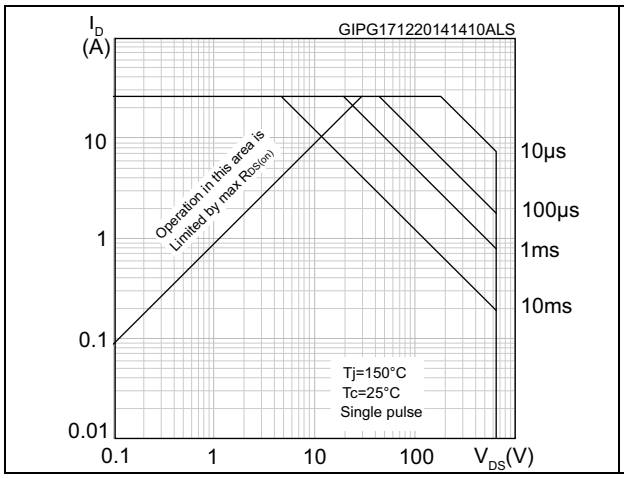



**Figure 3. Thermal impedance**

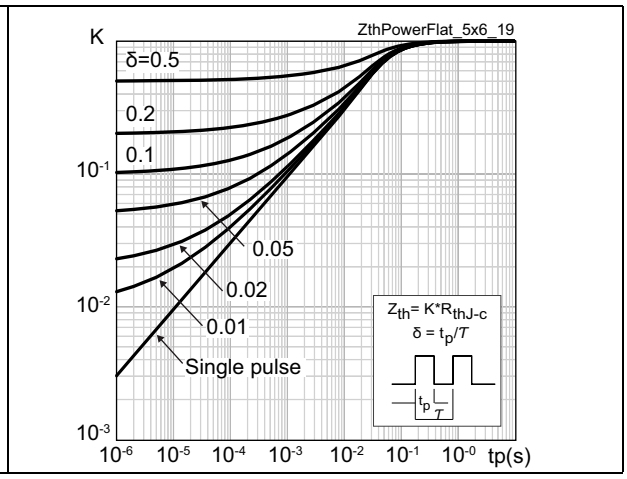



**Figure 4. Output characteristics**

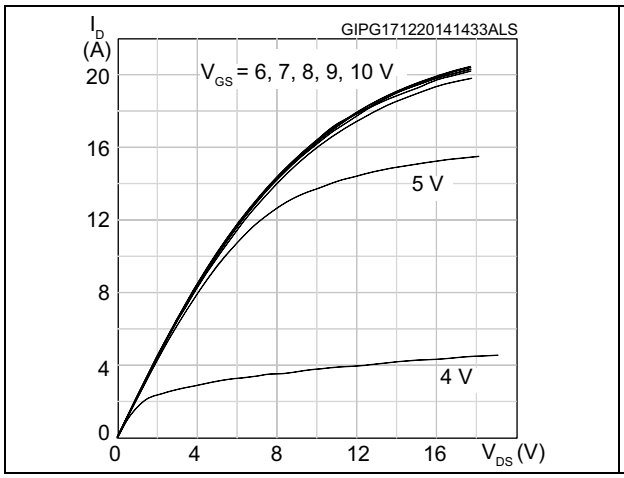



**Figure 5. Transfer characteristics**

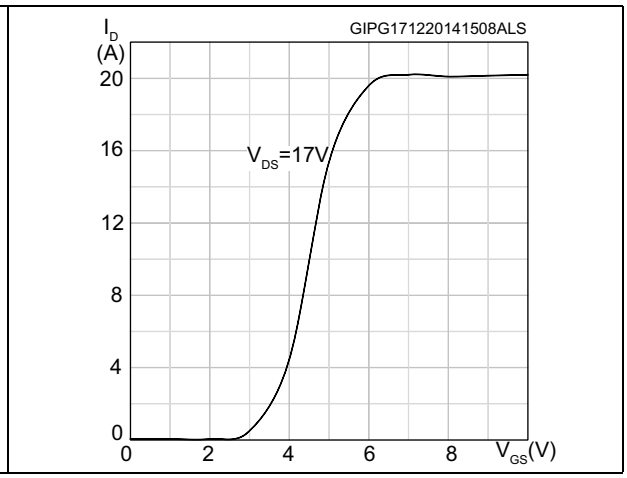



**Figure 6. Normalized $V_{BR(DSS)}$ vs temperature**

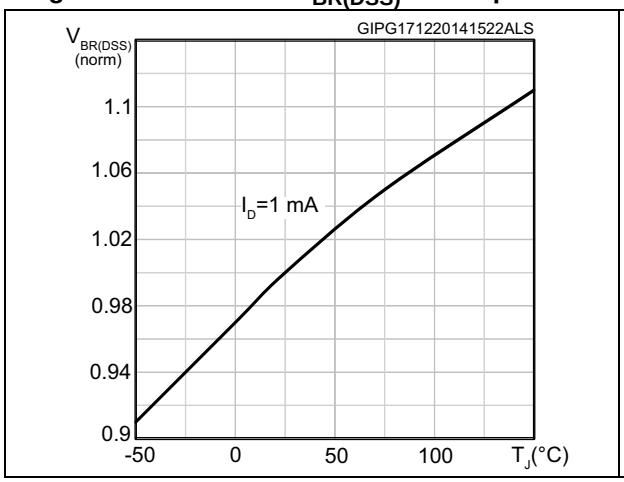



**Figure 7. Static drain-source on-resistance**

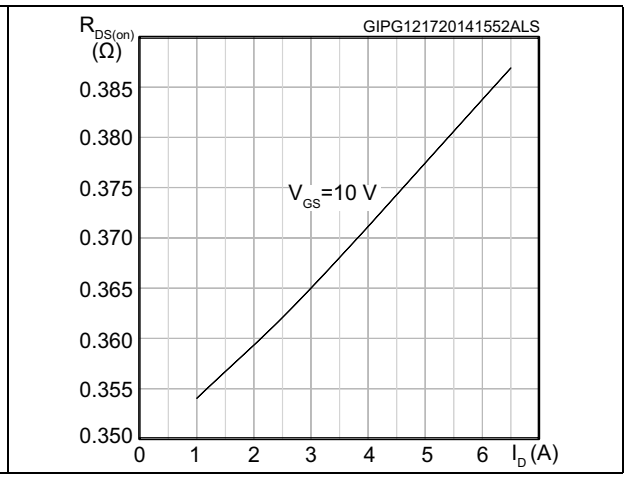


**Figure 8. Gate charge vs gate-source voltage**

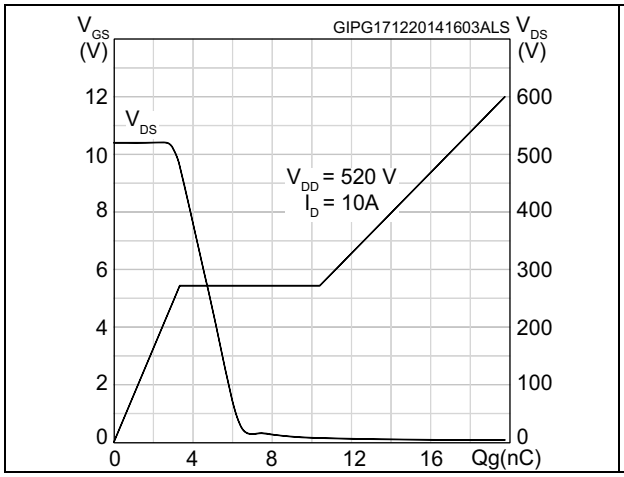



**Figure 9. Capacitance variations**

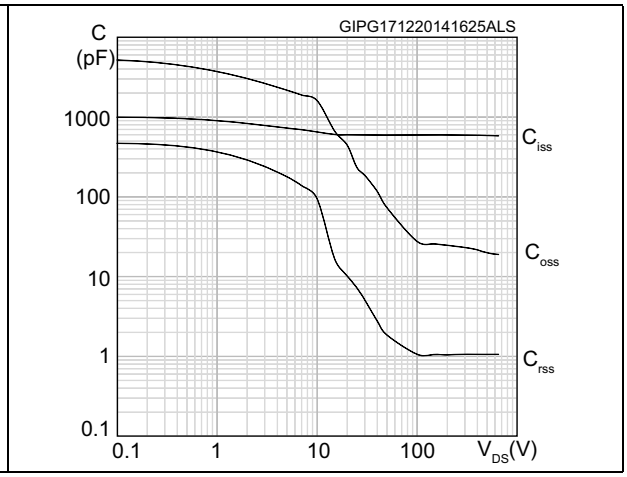



**Figure 10. Normalized gate threshold voltage vs temperature**

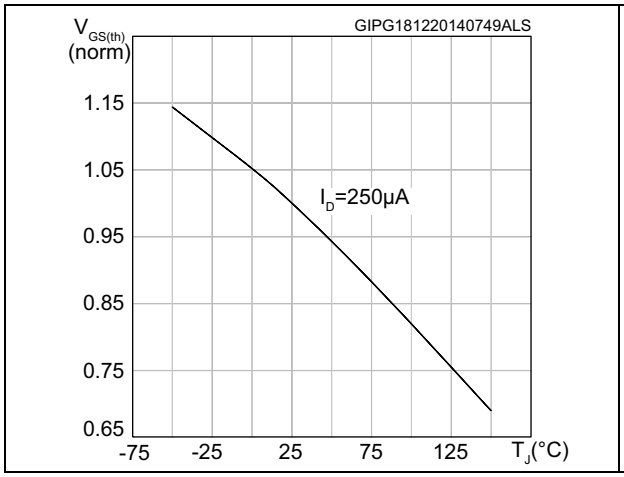



**Figure 11. Normalized on-resistance vs temperature**

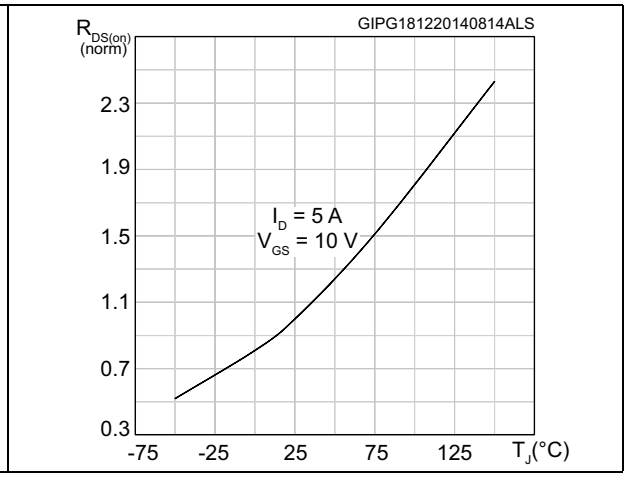



**Figure 12. Source-drain diode forward characteristics**

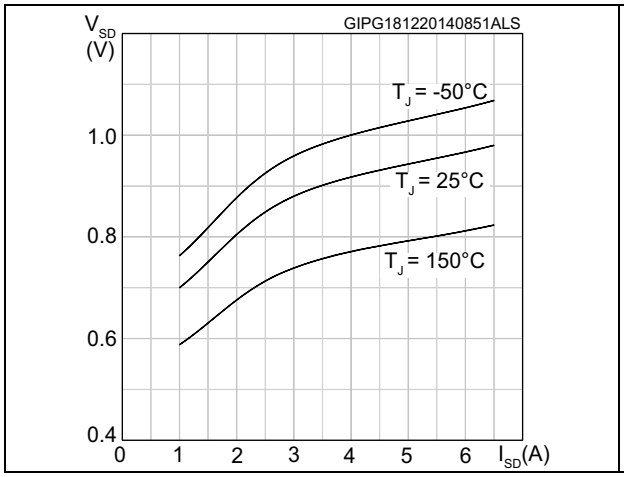
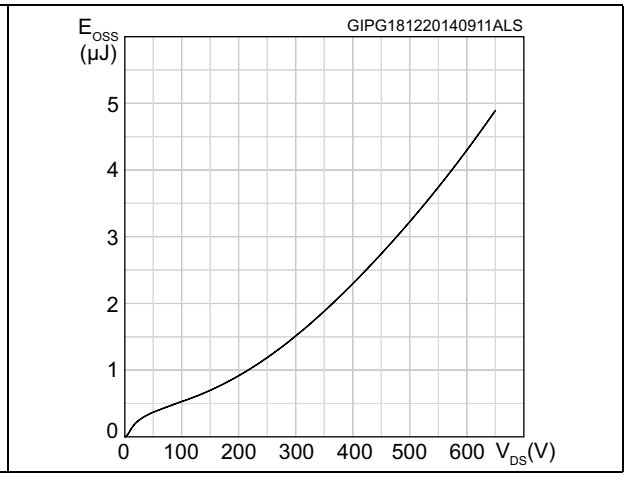



**Figure 13. Output capacitance stored energy**



# 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**

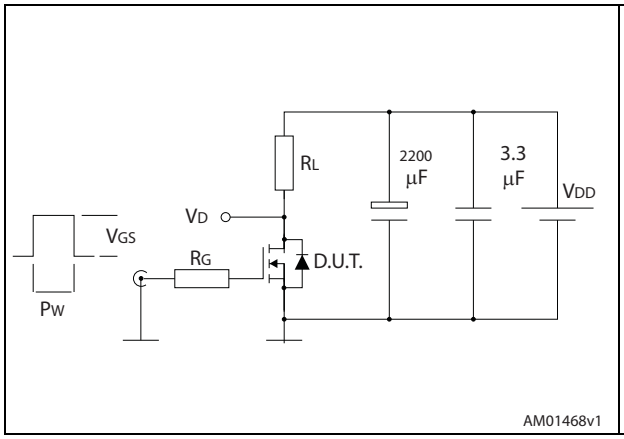



**Figure 15. Gate charge test circuit**

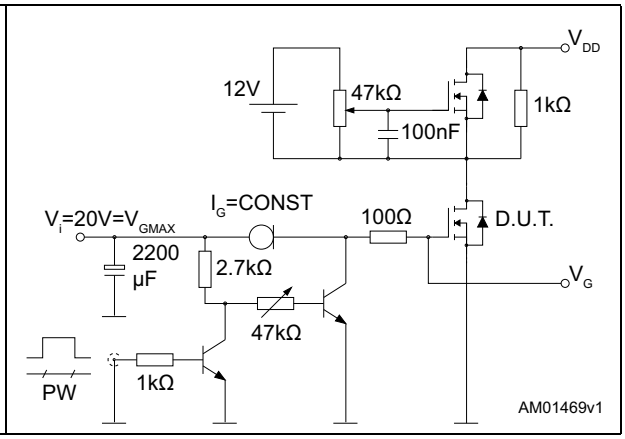



**Figure 16. Test circuit for inductive load switching and diode recovery times**

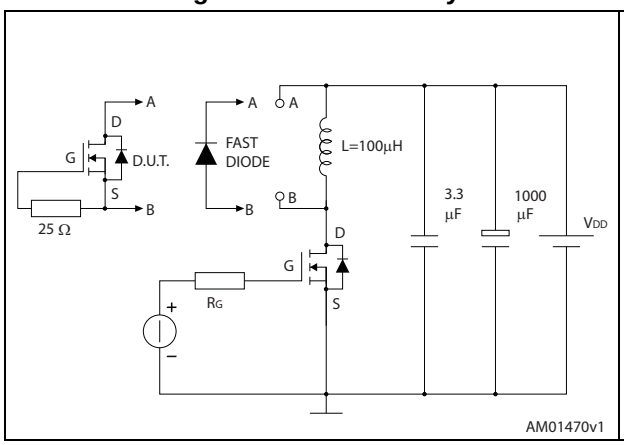



**Figure 17. Unclamped inductive load test circuit**

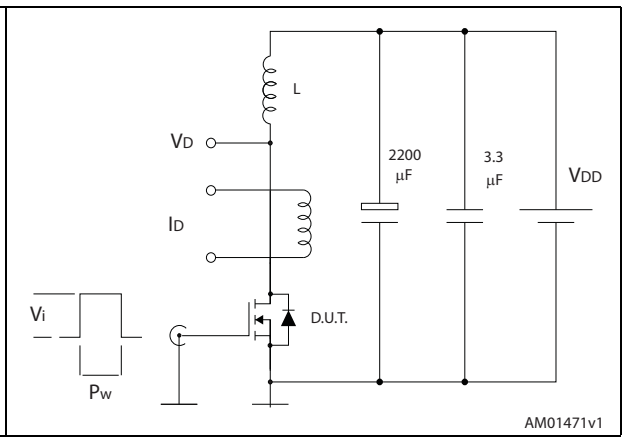



**Figure 18. Unclamped inductive waveform**

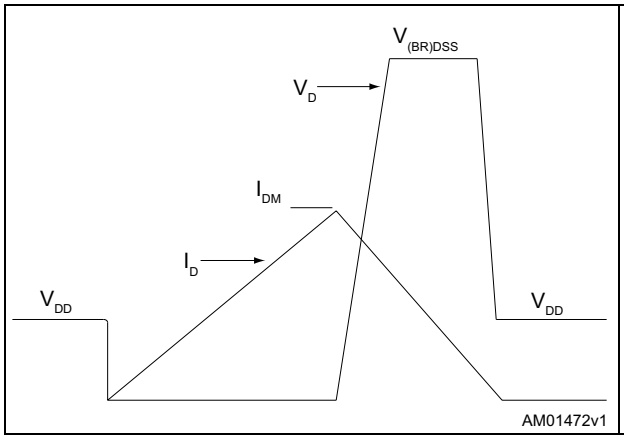
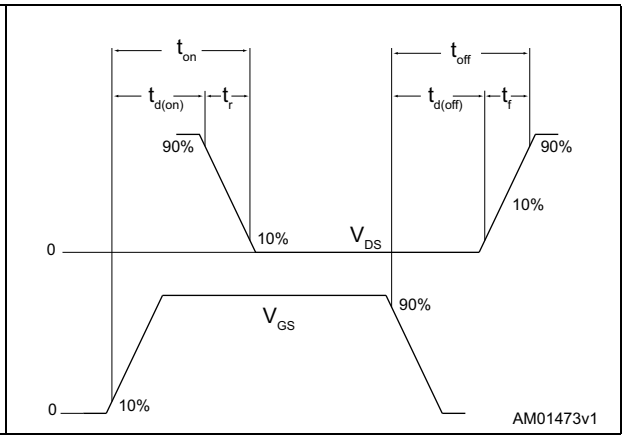



**Figure 19. Switching time waveform**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

**Figure 20. PowerFLAT™ 5x6 HV drawing**

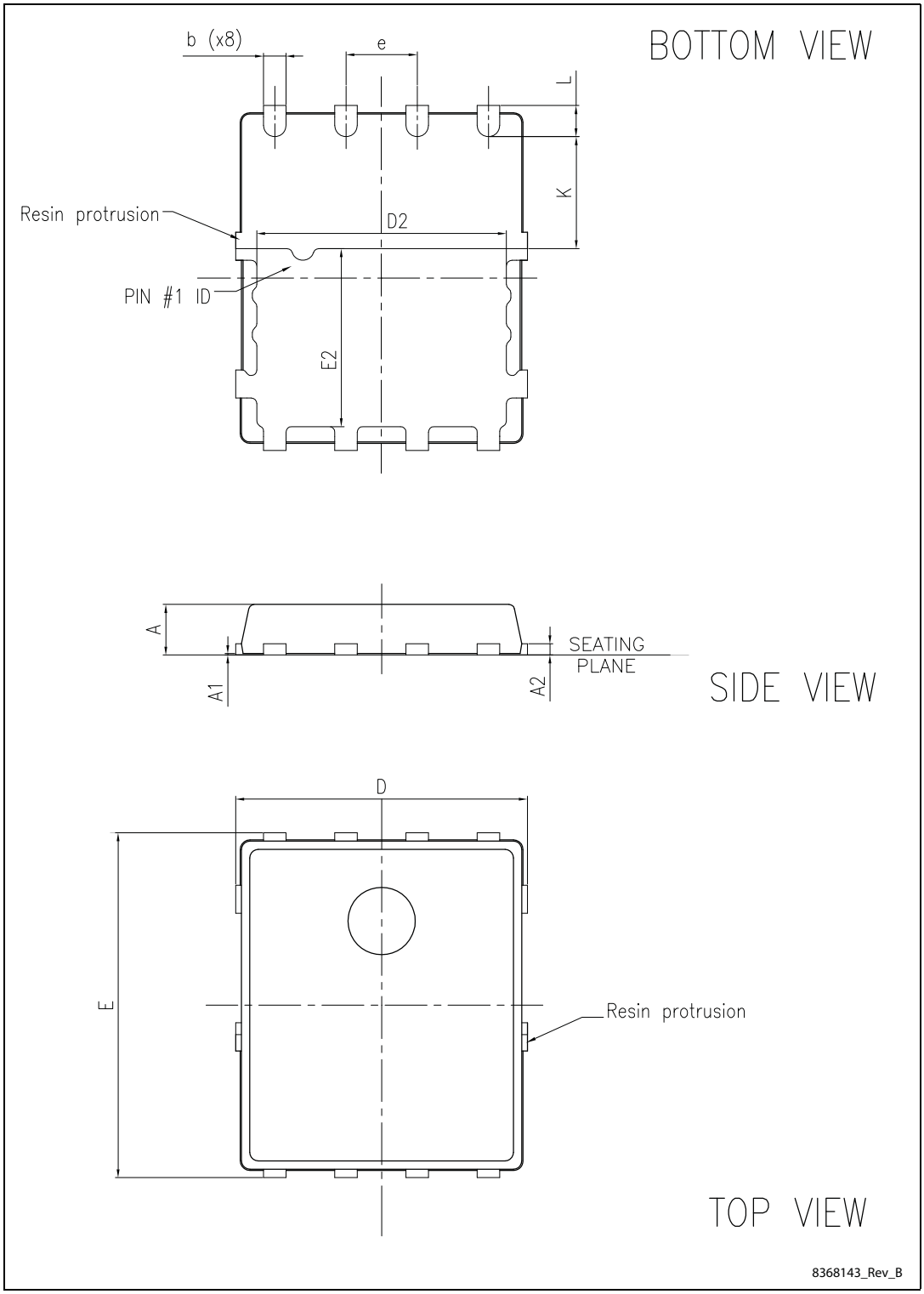


**Figure 21. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)**

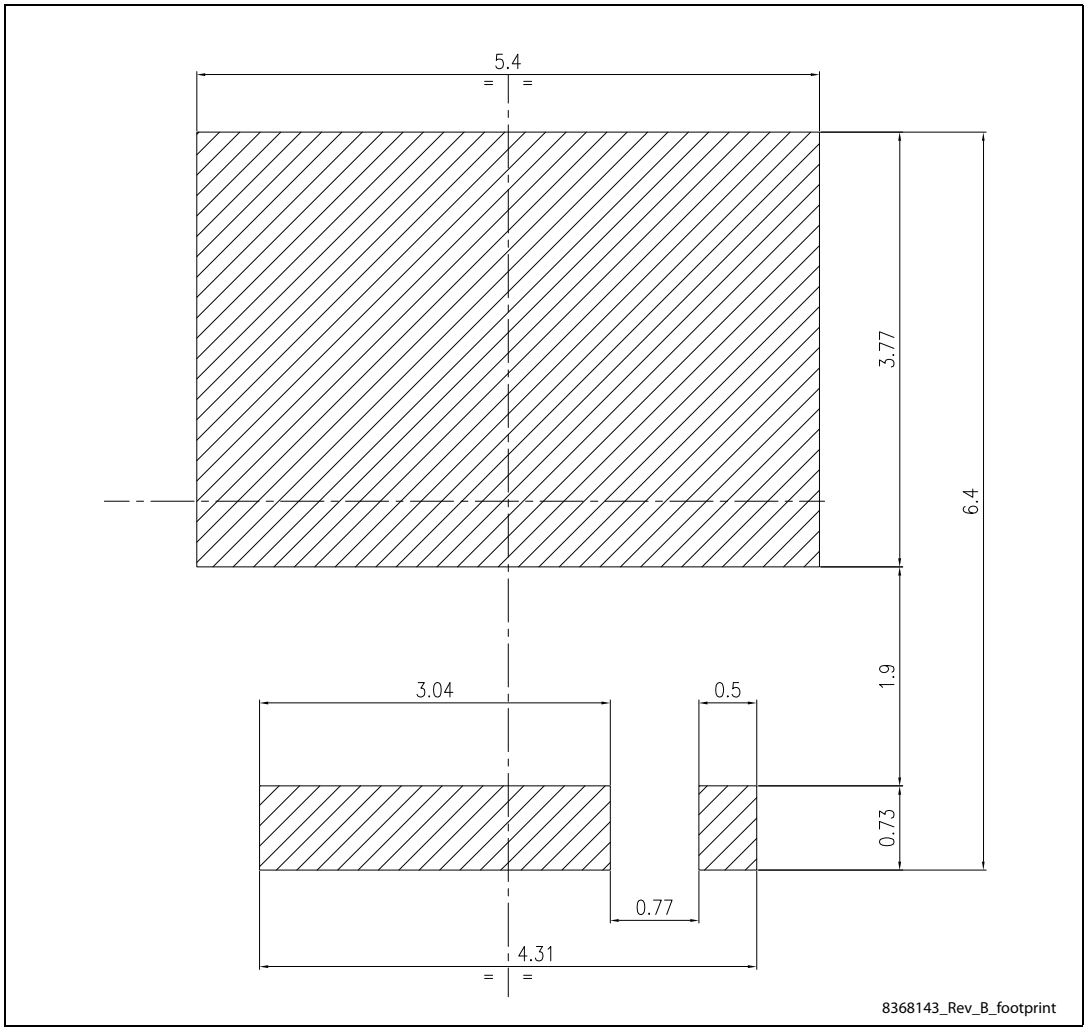


Table 9. PowerFLAT™ 5x6 HV mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | 5.00 | 5.20 | 5.40 |
| E | 5.95 | 6.15 | 6.35 |
| D2 | 4.30 | 4.40 | 4.50 |
| E2 | 3.10 | 3.20 | 3.30 |
| e | | 1.27 | |
| L | 0.50 | 0.55 | 0.60 |
| K | 1.90 | 2.00 | 2.10 |

# 5 Packaging mechanical data

**Figure 22. PowerFLAT™ 5x6 tape(a)**

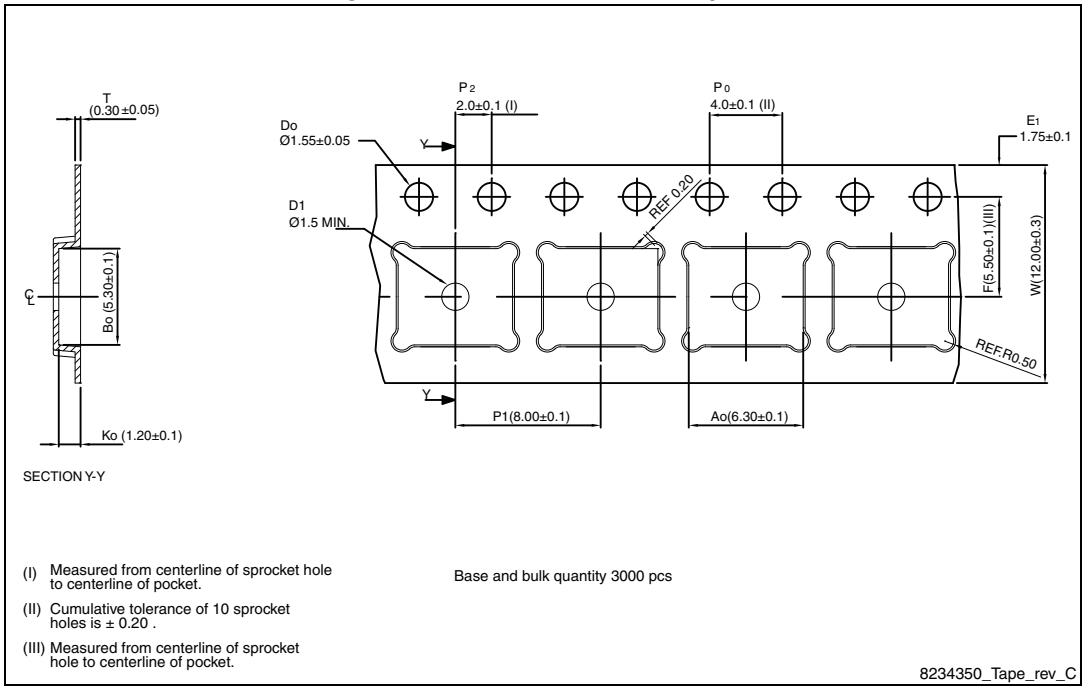
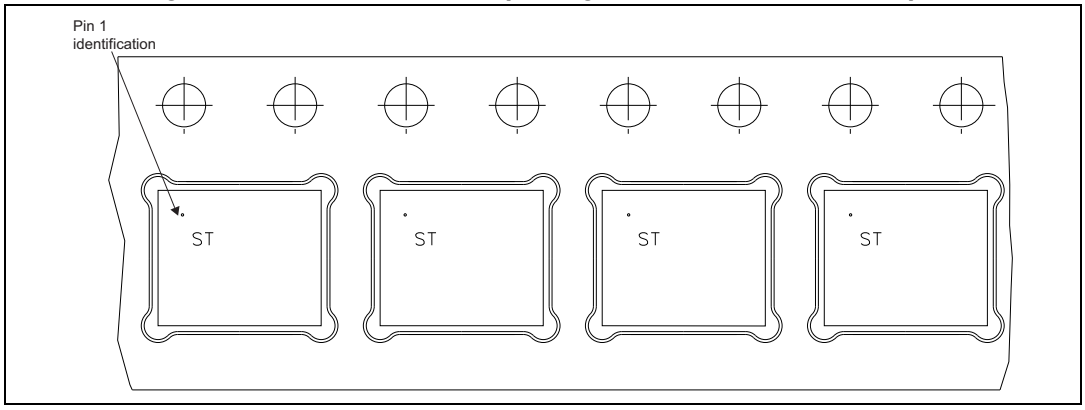
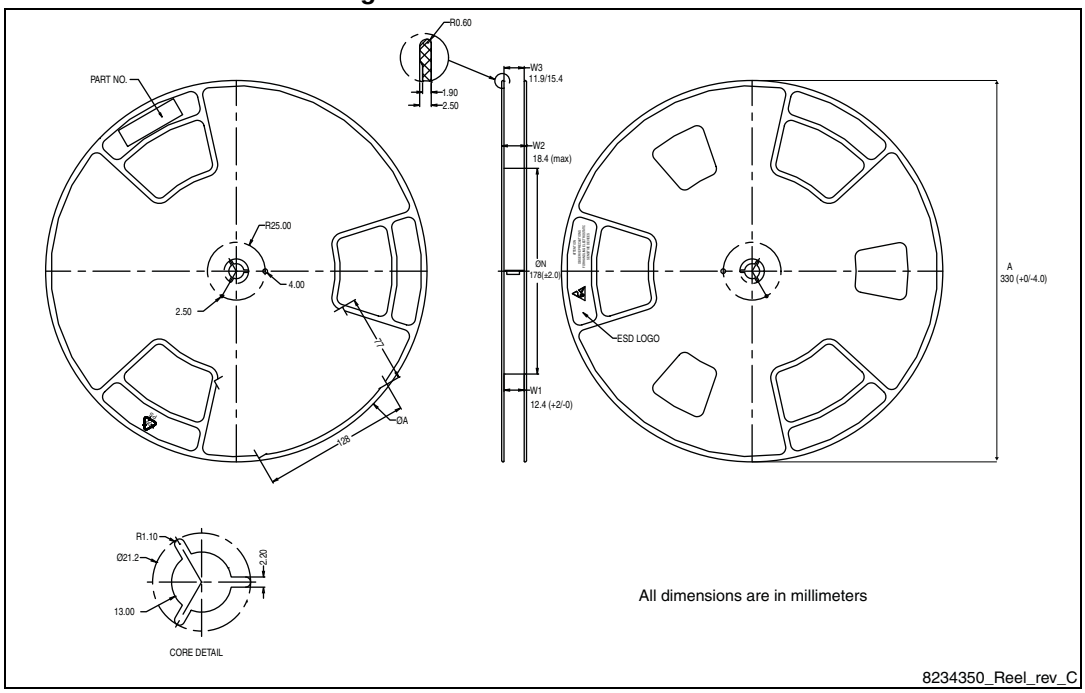



**Figure 23. PowerFLAT™ 5x6 package orientation in carrier tape.**




a. All dimensions are in millimeters.

**Figure 24. PowerFLAT™ 5x6 reel**



# 6 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 18-Dec-2014 | 1 | First release. |

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