Features

- Up to 128-voice Top-quality Wavetable Synthesis Chip
  - Two 64-voice RISC DSP Cores
  - Two High-speed CISC Control Processors
  - Versatile Programmable Digital Audio Routing Between the Two DSPs
- Voices Can Be Allocated for Synthesis and/or Effects and/or Audio Processing
- Maximum Single-shot PCM Wavesize of 4M Samples (93 Seconds @ 44.1 kHz)
- Samples Can Be Stored in 16-bit Floating Point Format (20-bit Dynamic), 16-bit Linear, 8-bit Linear
- Standard Audio Processing Firmware Includes Equalizer, Surround, MPEG Audio Decoder (Level 2)
- Sophisticated Built-in Cache Memories
  - Allows Use of Standard 90 ns 16-bit ROMs/RAMs
  - Guarantees Crisp Response Even Under Heavy Traffic Conditions
- GS Sound Set(1) under License from Roland® Corporation, Other Sound Sets Available
- 16-channel Audio-in, 16-channel Audio-out @ 22 Bits Audio/Channel
- 28-bit Internal Audio Path
- Two Serial MIDI-In, Two Serial MIDI-Out
- Firmware/Wavetable Data Can Reside in ROM, DRAM, SDRAM
- Up to 256M Bytes of External Memory with Support of SIMM (DRAM) and DIMM (SDRAM)
- High-speed 16-bit Burst Transfer for Firmware Download or Streaming Audio
- Compatible with ATSAM9707, Uses Proven Design and Development Tools
  - Sound Editor, Sound Bank Editor
  - Algorithm Compiler, Assembler, Source Debugger
  - Direct Development from PC Environment, No Special Emulator Required
- Top Dream® Technology
  - Single Low-frequency Crystal and Built-in PLL
  - 3.3V Supply, 5V-tolerant I/Os
  - Space-saving 144-lead TQFP Package
  - Power-down Mode
- Typical Applications: Karaokes, High-range Multimedia, Classical Organs, Digital Pianos, Professional Keyboards, Musical Samplers

Note: 1. The GS Sound Set is subject to special licensing conditions. Not to be used for musical instruments.

1. Description

The ATSAM9708 is a 128-voice integrated synthesizer, integrating two PDSP blocks and a memory management unit (MMU). One PDSP block is a combination of a specialized 64-slot RISC-based digital signal processor (DSP), a general-purpose 16-bit CISC-based control processor (P16), a cache memory and an “intelligent” peripheral I/O interface. Both PDSPs are fully independent and share the same external memory through the MMU.

Sound Synthesis

ATSAM9708 128-voice Integrated Sound Synthesizer

1772E–DRMSD–10-Apr-06

2. Block Diagrams

Figure 2-1. ATSAM9708 Block Diagram

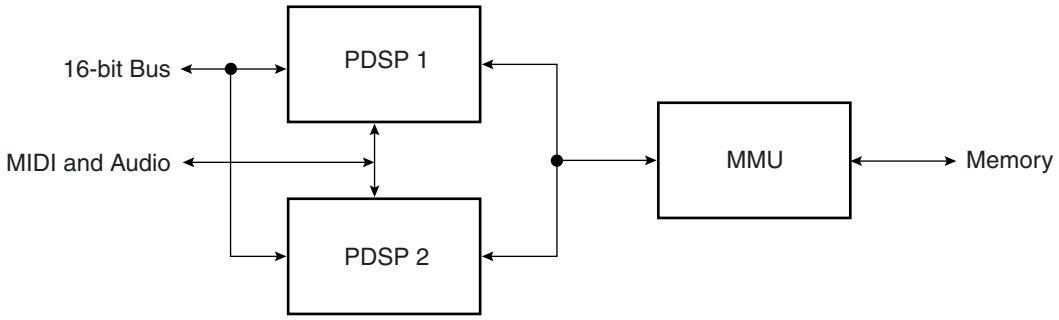
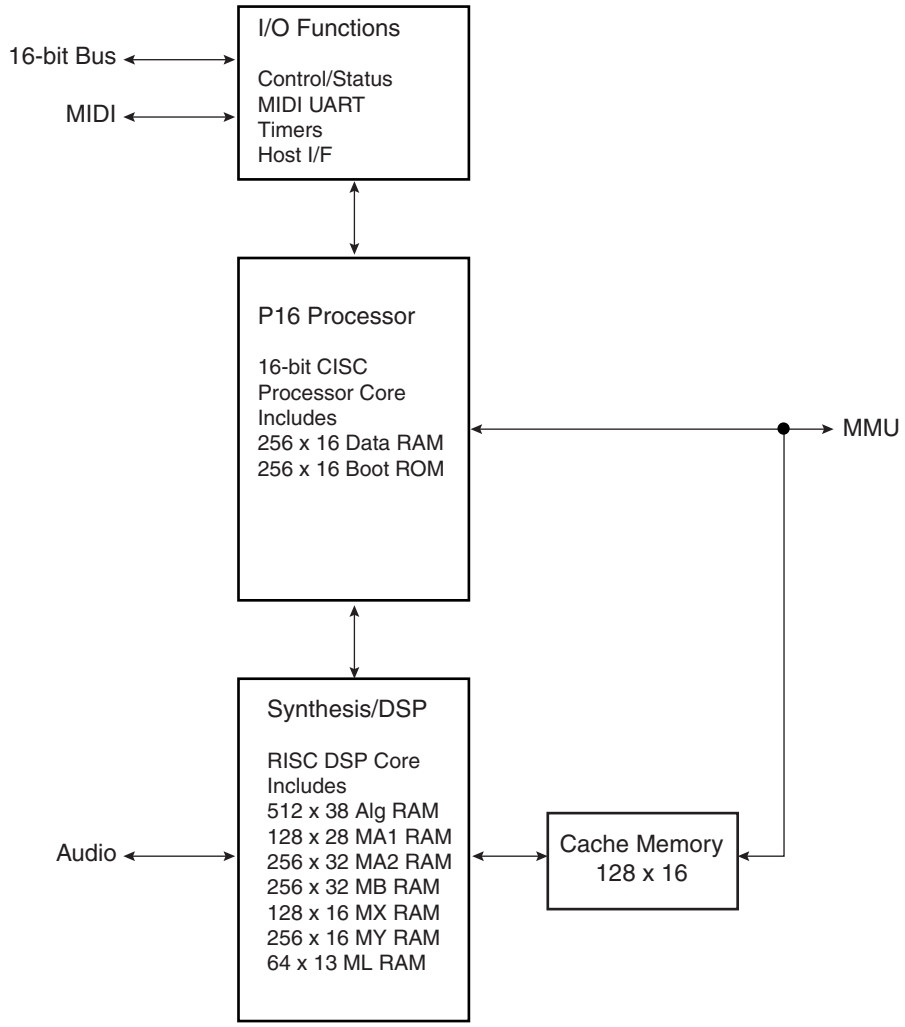


Figure 2-2. PDSP Block Diagram



3. Pin Description by Function

Table 3-1. Power Group

Name	Pin Count	Type	Function
GND	19	PWR	Power Ground. All GND pins should be returned to digital ground.
VC3	8	PWR	Core Power, +3.3V nominal (3V to 4.5V). All V_{C3} pins should be returned to +3.3V.
VCC1	5	PWR	Pad (except Memory Pad) Power, +3.0V to +5.5V. All V_{CC} pins should be returned to +5V (or 3.3V in case of single 3.3V supply).
VCC2	5	PWR	Memory Pad Power, +3.0V to +5.5V. All V_{CC} pins should be returned to +5V (for RAM or DRAM) or 3.3V (for SDRAM or 3.3V ROM).

Table 3-2. ISA Bus Group[1]

Name	Pin Count	Type	Function
PC_D[15:0][2, 3]	16	I/O	16-bit data bus to host processor. Information on these pins is: - 2 x parallel MIDI (MPU-401 type applications) - 2 x high-speed burst data transfers to/from external memory
PC_A[2:0]	3	IN	Selects one of 8 internal registers: 0, 1: MPU-401 register processor #1 2, 3: Burst data (16-bit) processor #1 4 - 5: MPU-401 register processor #2 6 - 7: Burst data (16-bit) processor #2
$\overline{\text{PC_CS}}$[4]	1	IN	Chip select from host, active low.
$\overline{\text{PC_WR}}$	1	IN	Write from host, active low.
$\overline{\text{PC_RD}}$	1	IN	Read from host, active low.
PC_READY	1	TSout	Open drain output buffer. Driven low during 16-bit burst mode transfers to synchronize host to the ATSAM9708 memory.
$\overline{\text{PC_IO16}}$	1	TSout	Open drain output buffer; driven low during 16-bit burst mode transfers. Indicates to host that a 16-bit I/O is in progress.
PC_IRQ	1	TSout	Tri-state output pin, active high. Can be connected directly to host PC_IRQ line.

Notes:
1. ISA bus group pins are powered by V_{CC1} power rail.
2. PC_D pads have 4 mA drive capabilities; other output pads have 16 mA drive capabilities.
3. To interface with PC ISA bus, V_{CC1} should be connected to 5V power and PC_D bus should be buffered. Direction is given by $\overline{\text{PC_RD}}$ signal.
4. Pin Names in this document exhibiting an overbar ($\overline{\text{PC_CS}}$ for example) indicates that the signal is active low.

Table 3-3. MIDI and Audio Group[1]

Name	Pin Count	Type	Function
MIDI1_IN	1	IN	Main MIDI input. Routed to PDSP#1, can also be routed to PDSP#2.
MIDI2_IN	1	I/O	Auxiliary MIDI input. Routed to PDSP#2[2]
MIDI1_OUT	1	OUT	Main MIDI output. Outputs from PDSP#1.
MIDI2_OUT	1	OUT	Auxiliary MIDI output. Outputs from PDSP#2[2]
OVCK_OUT	1	OUT	Buffered X2 output. Typically used to drive external sigma/delta DAC/ADC at f_S x 256.
BCK_OUT	1	OUT	Audio data bit clock. Provides timing to SD_OUT.
WS_OUT	1	OUT	Audio data word select. WS_OUT timing can be selected to be I2S- or Japanese-compatible.
SD_OUT[7:0]	8	OUT	8 stereo serial audio data output (16 audio channels). Each output holds 64 bits (2 x 32) of serial data per frame. Audio data has 22-bit precision[2].
SD_IN[7:0]	8	I/O	8 stereo serial audio data input (16 audio channels). Each input holds 64 bits (2 x 32) of serial data per frame. Audio data in is received with 20-bit precision[2].

Notes: 1. MIDI and Audio group pins are powered by V_{CC1} power rail.
2. These pins have alternate functions as GPIO pins (general-purpose input/output pins). See "General-purpose Input/Output Routing" on page 24 for more details.

Table 3-4. Memory Group[1]

Name	Pin Count	Type	Function
CK_OUT	1	OUT	Master clock for SDRAM operation. Frequency is 4 times the X1 frequency (typ 45.1584 MHz).
WA[26:0]	27	OUT	External memory address (ROM/SRAM/DRAM/SDRAM), up to 128M words (256M bytes). DRAM/SDRAM addresses are time-multiplexed on these pins as follows: WA0 - WA8: DRA0 - DRA8 WA18: DRA9 WA20: DRA10 WA22: DRA11
RBS	1	OUT	SRAM byte select. Should be connected to the lower RAM address when 8-bit wide SRAM is used. The type of RAM (16-bit/8-bit) can be selected by program.
WD[15:0]	16	I/O	PCM ROM/SRAM/DRAM/SDRAM data
$\overline{\text{WCS0}}$	1	OUT	PCM ROM chip select, active low
$\overline{\text{WCS1}}$	1	OUT	SRAM chip select, active low
$\overline{\text{WWE}}$	1	OUT	SRAM/DRAM/SDRAM write enable, active low. Timing compatible with SIMM DRAM early write feature.
$\overline{\text{WOE}}$	1	OUT	PCM ROM/SRAM output enable, active low

Table 3-4. Memory Group[1] (Continued)

Name	Pin Count	Type	Function
$\overline{RAS}$	1	I/O	DRAM/SDRAM row address strobe. At the end of reset $\overline{RAS}$ is tested to determine memory type configuration (pulled high to select SDRAM type). $\overline{RAS}$ should be pulled to V_{CC} or GND through an external 10K resistor.
$\overline{CAS}$	1	I/O	DRAM/SDRAM column address strobe. At the end of reset $\overline{CAS}$ is tested to determine memory type configuration (pulled high to select DRAM type). $\overline{CAS}$ should be pulled to V_{CC} or GND through an external 10K resistor.
$\overline{REFRESH}$	1	I/O	Indicates that a DRAM/SDRAM memory refresh cycle is in progress. To be used with multiple SIMM/DIMM modules to force refresh simultaneously on all modules. At the end of reset $\overline{REFRESH}$ is tested to select bootstrap state (pulled high to start built-in CPU bootstrap in case of ROMless applications).

Note: 1. Memory group pins are powered by V_{CC2} power rail.

Table 3-5. Miscellaneous Group

Name	Pin Count	Type	Function
LFT	1	ANA	PLL low pass filter. Should be connected to an external RC network.
TEST	1	IN	Test pin. Should be returned to GND.
LDTEST	1	IN	Test pin. Should be returned to GND.
$\overline{PDWN}$	1	IN	Power down, active low
$\overline{RESET}$	1	IN	Master reset input, active low. Schmidt trigger input.
X1, X2[1]	2	–	Crystal connection. Crystal frequency should be f_S x 256 (typ 11.2896 MHz). Crystal frequency is internally multiplied by 4 to provide the IC master clock. X1 can also be used as external clock input (3.3V input).

Note: 1. X2 cannot be used to drive external circuitry.

4. Pinout by Pin Number

Table 4-1. Pinout by Pin Number

Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
1	PC_D[10]	37	SD_IN[2]	73	WD[9]	109	VCC2
2	PC_D[9]	38	SD_IN[3]	74	WD[8]	110	GND
3	PC_D[8]	39	SD_OUT[0]	75	WD[7]	111	WA[9]
4	$\overline{\text{PC_IO16}}$	40	SD_OUT[1]	76	WD[6]	112	VC3
5	VCC1	41	VC3	77	WD[5]	113	GND
6	GND	42	GND	78	WD[4]	114	WA[10]
7	PC_READY	43	SD_OUT[2]	79	WD[3]	115	WA[11]
8	VC3	44	SD_OUT[3]	80	VC3	116	WA[12]
9	GND	45	WS_OUT	81	VCC2	117	WA[13]
10	$\overline{\text{PC_RD}}$	46	BCK_OUT	82	GND	118	WA[14]
11	$\overline{\text{PC_WR}}$	47	OVCK_OUT	83	GND	119	WA[15]
12	PC_A[0]	48	SD_IN[4]	84	WD[2]	120	WA[16]
13	PC_A[1]	49	SD_IN[5]	85	WD[1]	121	WA[17]
14	PC_IRQ	50	SD_IN[6]	86	WD[0]	122	WA[18]
15	PC_A[2]	51	GND	87	$\overline{\text{WWE}}$	123	WA[19]
16	$\overline{\text{PC_CS}}$	52	VCC1	88	$\overline{\text{WOE}}$	124	VCC2
17	VC3	53	SD_IN[7]	89	$\overline{\text{WCS0}}$	125	GND
18	GND	54	SD_OUT[4]	90	$\overline{\text{WCS1}}$	126	WA[20]
19	PC_D[0]	55	SD_OUT[5]	91	CK_OUT	127	WA[21]
20	VCC1	56	SD_OUT[6]	92	RBS	128	WA[22]
21	GND	57	SD_OUT[7]	93	WA[0]	129	WA[23]
22	PC_D[1]	58	VC3	94	WA[1]	130	WA[24]
23	PC_D[2]	59	GND	95	WA[2]	131	WA[25]
24	PC_D[3]	60	LFT	96	WA[3]	132	WA[26]
25	PC_D[4]	61	X1	97	VCC2	133	GND
26	PC_D[5]	62	X2	98	GND	134	$\overline{\text{RESET}}$
27	PC_D[6]	63	VC3	99	VC3	135	TEST
28	PC_D[7]	64	GND	100	GND	136	LDTEST
29	MIDI1_IN	65	WD[15]	101	WA[4]	137	$\overline{\text{PDWN}}$
30	MIDI2_IN	66	WD[14]	102	WA[5]	138	PC_D[15]
31	MIDI1_OUT	67	WD[13]	103	$\overline{\text{RAS}}$	139	PC_D[14]
32	MIDI2_OUT	68	WD[12]	104	$\overline{\text{CAS}}$	140	PC_D[13]
33	SD_IN[0]	69	VCC2	105	$\overline{\text{REFRESH}}$	141	PC_D[12]
34	SD_IN[1]	70	GND	106	WA[6]	142	VCC1
35	VCC1	71	WD[11]	107	WA[7]	143	GND
36	GND	72	WD[10]	108	WA[8]	144	PC_D[11]

5. Absolute Maximum Ratings

Table 5-1. Absolute Maximum Ratings

Ambient Temperature (Power Applied .....)-40°C to +85°C Storage Temperature ..... -65°C to +150°C Voltage on any pin (except X1) .....-0.5V to V_{CC} + 0.5V Voltage on X1 pin..... -0.5V to V_{C3} + 0.5V V_{CC} Supply Voltage .....-0.5V to +6.5V V_{C3} Supply Voltage .....-0.5V to +4.5V Maximum I_{OL} per I/O pin ..... 4.4mA (except PC_IRQ, PC_READY) Maximum I_{OL} PC_IRQ, PC_READY..... 16.16mA	*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect device reliability.

Note: All voltages with respect to 0V, GND = 0V

6. Recommended Operating Conditions

Table 6-1. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage(1)	3	3.3/5.0	5.5	V
V_{C3}	Supply voltage	3	3.3	4.5	V
t_A	Operating ambient temperature	0		70	°C

Note: 1. When using 3.3V supply, care must be taken that voltage applied on pin does not exceed V_{CC} + 0.5V.

7. DC Characteristics

Table 7-1. DC Characteristics (t_A = 25° C, V_{C3} = 3.3V ± 10%)

Symbol	Parameter	VCC	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	3.3 5.0	-0.5 -0.5		1.0 1.7	V
V_{IH}	High-level input voltage	3.3 5.0	2.3 3.3	3	3.8 5.5	V
V_{OL}	Low-level output voltage PC_D[15:0], PC_IRQ, PC_READY: I_{OL} = -24 mA Others except LFT: I_{OL} = -3.2 mA	3.3 5.0	0		0.45 0.45	V

Table 7-1. DC Characteristics (t_A = 25° C, V_{C3} = 3.3V ± 10%) (Continued)

Symbol	Parameter	VCC	Min	Typ	Max	Unit
V_{OL}	High-level output voltage PC_D[15:0], PC_IRQ, PC_READY: I_{OH} = 10 mA Others except LFT: I_{OH} = 0.8 mA	3.3 5.0	2.8 4.5			V
I_{CC}	Power supply current (crystal frequency = 12 MHz)	3.3 5.0		100 25	140 35	mA
	Power down supply current			TBD	TBD	µA

8. DSP RISC Signal Processor

Each of the two DSP engines operates on a frame-timing basis with the frame subdivided into 64 process slots. Each process is itself divided into 16 micro-instructions known as “algorithms”. Up to 32 different DSP algorithms can be stored on-chip in each DSP private Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications. Each DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24 dB resonant filtering for each voice, for a total polyphony of 128 voices. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

Each DSP also includes a 20 x 16 pipelined two’s complement multiplier, a 28-bit pipelined adder and eight 24-bit final accumulators.

A typical application uses around 75% of the capacity of the DSP engines for synthesis, thus providing a minimum of 96-voice wavetable polyphony. The remaining processing power is used for typical function like reverberation, chorus, direct sound, surround effect, equalizer, etc.

Frequently-accessed DSP parameter data are stored in 5 banks of on-chip RAM memory for each DSP. Sample data or delay lines, which are accessed relatively infrequently, are stored in external ROM, SRAM, DRAM or SDRAM memory. The combination of localized micro-program memory and localized parameter data allows micro-instructions to execute in 20 ns (50 MIPS) on each DSP. Separate buses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to 6 simultaneous operations (add, multiply, load, store, etc.), providing a total potential throughput of 600 million operations per second (MOPS).

9. P16 Control Processor and I/O Functions

Each of the two P16 control processors is a general-purpose 16-bit CISC processor core, that runs from external memory. A boot/macro ROM is included on-chip to accelerate commonly executed routines and to allow the use of RAM only devices for the external memory. Each P16 also includes 256 words of local RAM data memory.

Each P16 control processor writes to the parameter RAM blocks within its associated DSP in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the parallel 16-bit interface and then controls the DSP by writing into the parameter RAM banks of its associated DSP core. Slowly-changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

Each P16 control processor interfaces with other private peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the ISA PC 16-bit interface through specialized “intelligent” peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

The parallel interface is implemented using three address lines (A2, A1, A0), a chip select signal, read and write strobes from the host and a 16-bit data bus (PC_D0 - PC_D15).

This data bus cannot drive the PC bus directly. External buffers and an external decoder (PAL) or plug and play IC are required to map the 16-bit I/O addresses and AEN from the PC into the three address lines and chip select from the ATSAM9708.

The PDSP#1 responds on addresses 0 to 3 (A2A1A0 = 0XX), while PDSP#2 responds on addresses 4 to 7 (A2A1A0 = 1XX).

Each PDSP parallel interface supports a byte-wide I/O interface and a 16-bit port dedicated to burst transfers.

The byte-wide I/O interface is normally used to implement a MPU-401 UART-mode compatible interface. It is specified by address A1A0 = 0X, address 00 being the data register, address 01 being the status/control registers. Besides the standard two status bits of the MPU-401, two additional bits are provided to expand the MPU-401 protocol.

Address A1A0 = 10 specifies a 16-bit I/O port. It is mainly used for burst audio transfers to/from the PC using very efficient PC instructions like REP OUTSW or REP INSW which operate at maximum ISA bus bandwidth. This port may also be used for fast program or sound bank uploads.

10. DSP Cache RAM

The memory management unit (MMU) allows external ROM and/or RAM memory resources to be shared between the two DSPs and the two P16 control processors. This allows a single device (i.e., DRAM) to serve as sample memory storage/delay lines for the DSPs and as program storage/data memory for the P16 control processors.

The DSP cache RAM allows a dramatic reduction in the traffic with the external ROM/RAM, allowing use of standard 90 ns ROM parts with sampling frequencies up to 48 kHz. Average access request rate to external memory is only one for every two frames for each slot, which gives 64 accesses per synthesis frame. The MMU can provide up to 169 memory accesses per frame, which leaves over 100 accesses free per frame to be used by the P16 processors. This means that under full 128-voice polyphony traffic conditions, each P16 instruction average execution time is around 400 ns at 48 kHz sampling frequency.

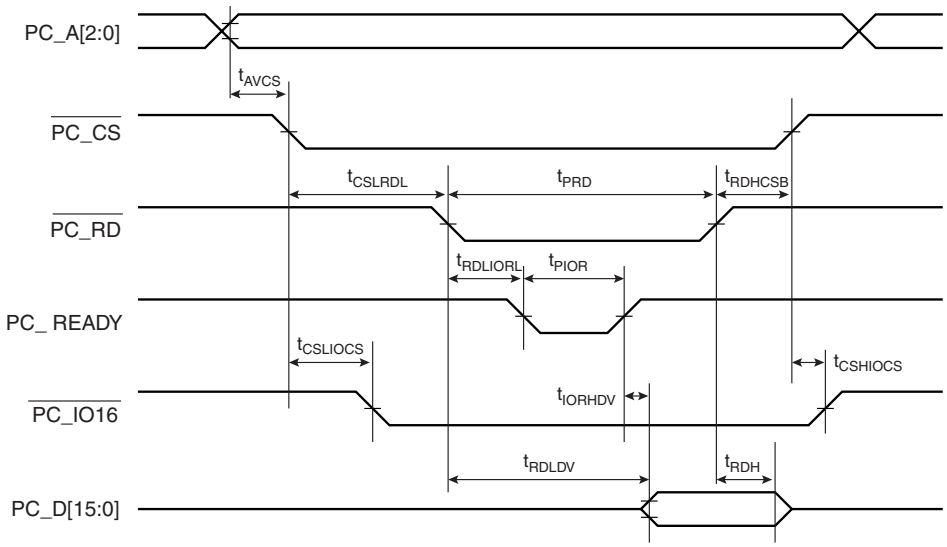
128-voice polyphony can be assured only when all samples are played at nominal frequency or down-transposed. Simultaneously playing a large number of up-transposed samples can adversely affect polyphony. For more details of possible polyphony for a given application, please refer to the application note “ATSAM9708 Memory Management Unit”.

11. Timing Diagrams

All timing conditions: V_{CC} = 5V, V_{C3} = 3.3V, t_A = 25°C; signals PC_READY, I/O $\overline{CS16}$, D0 - D15 with 220 ohms pull-up, 30 pF capacitance; signal PC_IRQ with 470 ohms pull-down, 30 pF capacitance; all other outputs except X2 and LFT load capacitance = 30 pF. All timings refer to t_{CK}, which is the internal master clock period. The internal master clock frequency is 4 times the frequency at pin X1; therefore, $t_{CK} = t_{XTAL}/4$. The sampling rate is given by $1/(t_{CK} * 1024)$. The maximum crystal frequency/clock frequency at X1 is 12.288 MHz (48 kHz sampling rate).

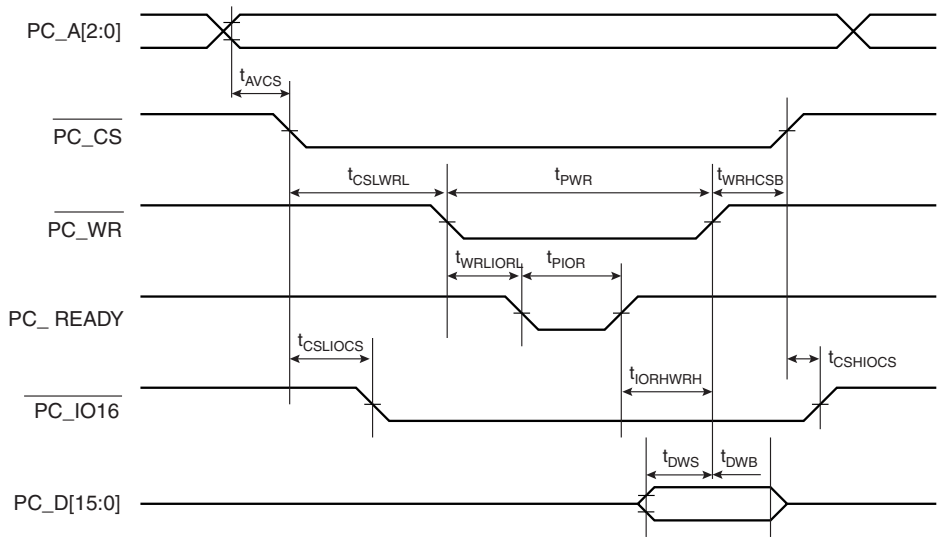
11.1 PC Host Interface

Figure 11-1. Host Interface Read Cycle



Note: PC_D[15:8] valid only if PC_A[2:1] = 10.

Figure 11-2. Host Interface Write Cycle



Note: PC_D[15:8] valid only if PC_A[2:1] = 10.

Table 11-1. PC Host Interface Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{AVCS}	Address valid to chip select low	0			ns
t_{CSLDRL}	Chip select low to $\overline{PC_RD}$ low	5			ns
t_{RDHCSH}	$\overline{PC_RD}$ high to $\overline{PC_CS}$ high	5			ns
t_{PRD}	$\overline{PC_RD}$ pulse width	50			ns
t_{RDLDV}	Data out valid from $\overline{PC_RD}$ (1)			20	ns
t_{DRH}	Data out hold from $\overline{PC_RD}$	5		10	ns
$t_{RDLIORL}$	PC_READY low from $\overline{PC_RD}$ (2)	0		10	ns
t_{PIRO}	PC_READY pulse width (2)			128	t_{ck}
t_{IORHDV}	PC_READY rising to data out valid (2)			0	ns
$t_{CSLIOCS}$	$\overline{PC_IO16}$ low from $\overline{PC_CS}$ low (3)	0		20	ns
$t_{CSHIOCS}$	$\overline{PC_IO16}$ high from $\overline{PC_CS}$ high (3)	0		20	ns
t_{CSLWRL}	$\overline{PC_CS}$ low to $\overline{PC_WR}$ low	5			ns
t_{WRHCSH}	$\overline{PC_WR}$ high to $\overline{PC_CS}$ high	5			ns
t_{PWR}	$\overline{PC_WR}$ pulse width	50			ns
$t_{WRLIORL}$	PC_READY low from $\overline{PC_WR}$ low (2)	0		10	ns
$t_{IORHWRH}$	PC_READY high to $\overline{PC_WR}$ high (2)	5			ns
t_{DWS}	Write data setup time	10			ns
t_{DWH}	Write data hold time	0			ns

Notes:
1. When data is already loaded into internal ATSAM9708 output register. In this case PC_READY stays high during the read cycle.
2. PC_READY goes into low only if the data is not ready to be loaded into/read from internal ATSAM9708 register. 128 t_{ck} corresponds to a single worst-case situation. At f_{CK} = 12.288 MHz, PC_READY is likely to never go low when using standard ISA bus timing.
3. $\overline{PC_IO16}$ is asserted low by ATSAM9708 if A2A1 = 10 to indicate fast 16-bit ISA bus transfer to the PC.

12. External Memory Timing

12.1 External Memory Overview

The following memories can be connected to the ATSAM9708:

- ROM or Flash memories, 16 bits wide
- Static RAMs, 8 bits or 16 bits wide
- DRAMs, 16 bits wide
- SDRAMs, 16 bits wide

DRAMs and SDRAMs cannot be connected at the same time. The type of dynamic RAM connection is determined at power-up by sensing the level of pins $\overline{RAS}$ and $\overline{CAS}$ (see Table 3-4 on page 4 and "Memory Type Configuration and Boot Configuration" on page 26).

Eight-bit wide static RAM can be connected using the additional Ram Byte Select (RBS) address signal. RBS allows access to two bytes of SRAM within one regular memory cycle, thereby providing 16 bits of data. Eight-bit wide SRAM can be connected only under control of $\overline{WCS1}$. The selection 8 bits/16 bits is done by firmware.

ROM and static RAMs use linear addressing (address lines WA0 to WA26). DRAM and SDRAMs use time-multiplexed addressing with a ROW/COL scheme (address lines DRA0 to DRA11). Additionally, SDRAMs use the DRA0/DRA11 lines for configuration and the DRA10 line for auto precharge.

ROM/SRAMs and DRAM/SDRAM address line share the same pins of the ATSAM9708. The timing is determined by the input signal DRAM. If DRAM is high at the beginning of a memory cycle, this indicates DRAM/SDRAM access.

If only one type of memory is connected (i.e., SDRAM), then the DRAM signal can be hardwired. Otherwise, it should be derived from an external decoding of high-order address lines.

12.2 External Memory Timing Overview

One memory cycle consists of six internal master clock cycles (6 x t_{CK}). The internal master clock period is one-fourth of the clock period at X1. The internal master clock is provided at pin CK_OUT when external SDRAM is connected ($\overline{RAS}$ sensed high during $\overline{RESET}$).

Figure 12-1. ROM and SRAM Basic Timing, DRAM = Low

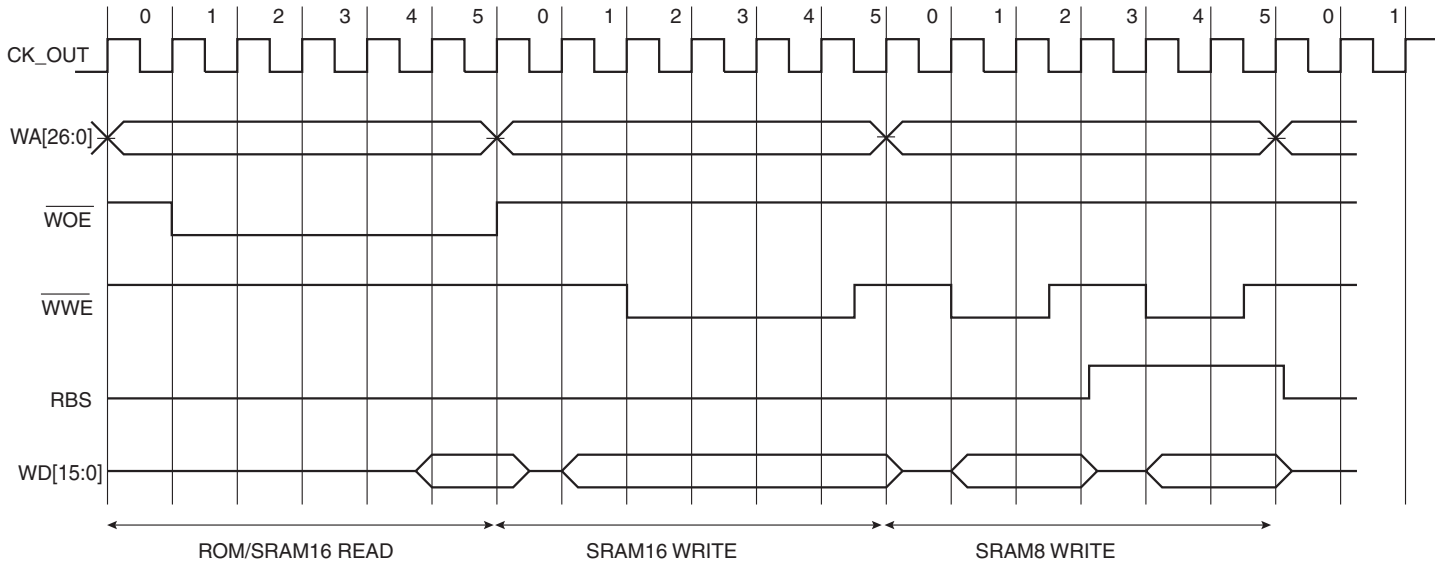
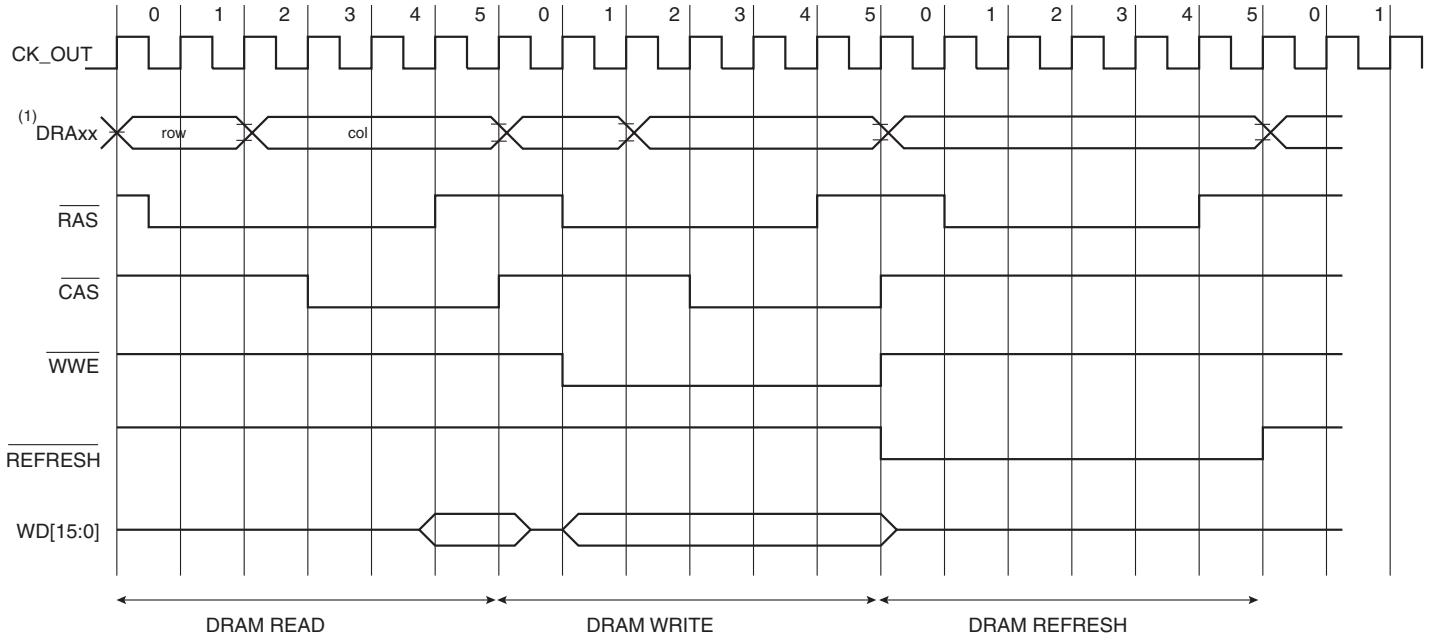
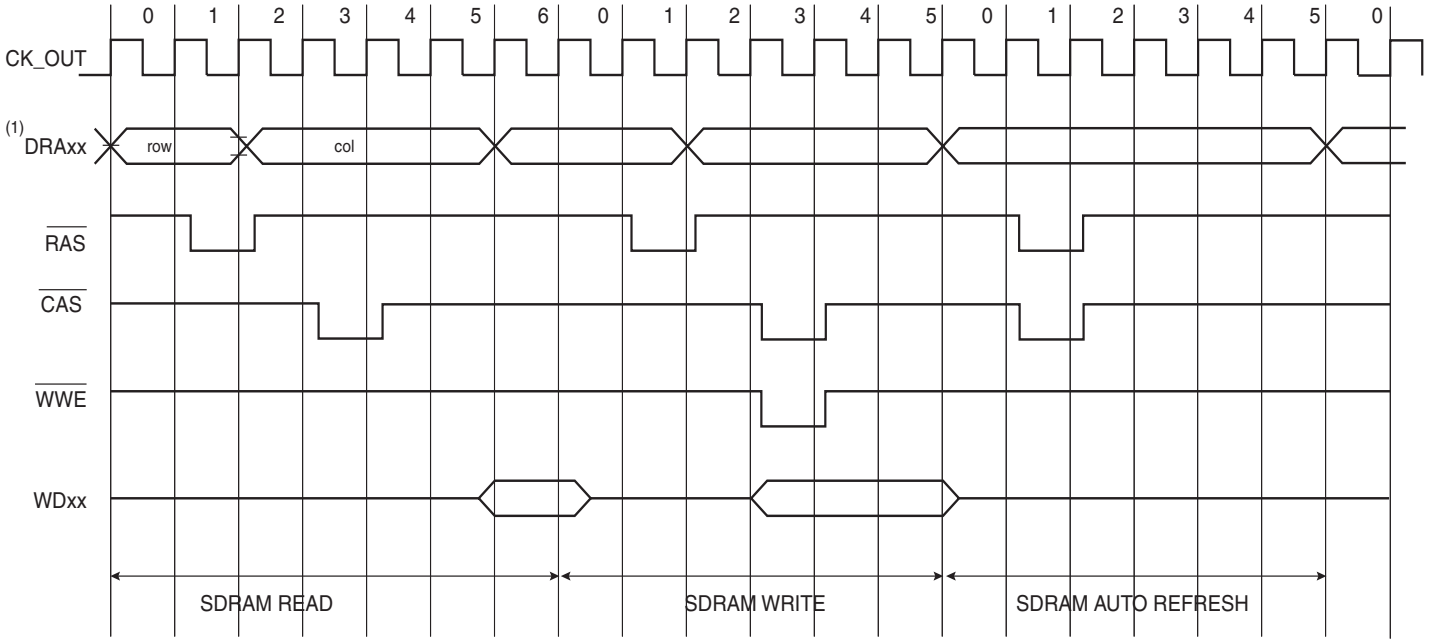


Figure 12-2. DRAM Basic Timing, DRAM = High



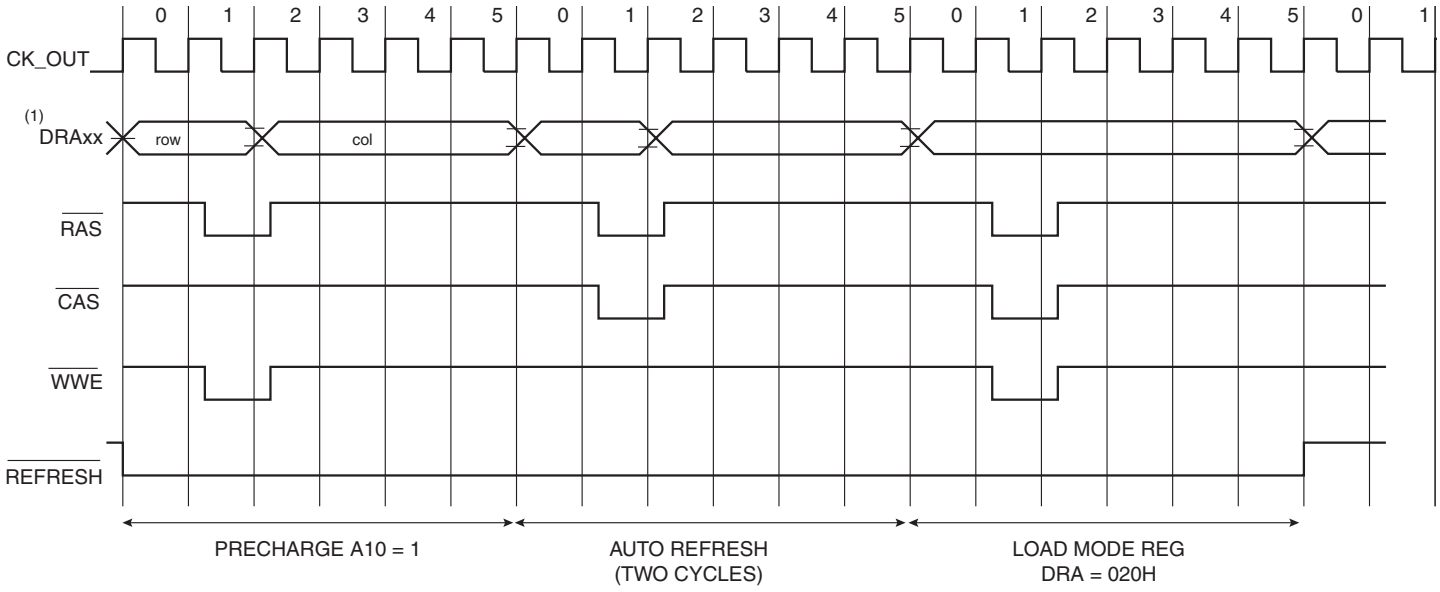
Note: 1. See Table 12-1 on page 16.

Figure 12-3. SDRAM Basic Timing, DRAM = High



Note: 1. See Table 12-1 on page 16.

Figure 12-4. SDRAM Init Sequence, DRAM = High



Note: 1. See Table 12-1 on page 16.

12.2.1 Basic Notes on SDRAM Timing

- $\overline{\text{RESET}}$ should be held low at least 100 µs (SDRAM timing requirement on idle cycles)
- SDRAM mode is fixed to sequential, burst length = 1, CAS latency 2, standard operation, programmed write burst length.
- SDRAM cycles for read: NOP - ACTIVE - NOP - READ AUTO PRECHARGE - NOP - NOP.
- SDRAM cycles for write: NOP - ACTIVE - NOP - WRITE AUTO PRECHARGE - NOP - NOP
- SDRAM cycles for refresh: NOP - AUTO REFRESH - NOP - NOP - NOP - NOP

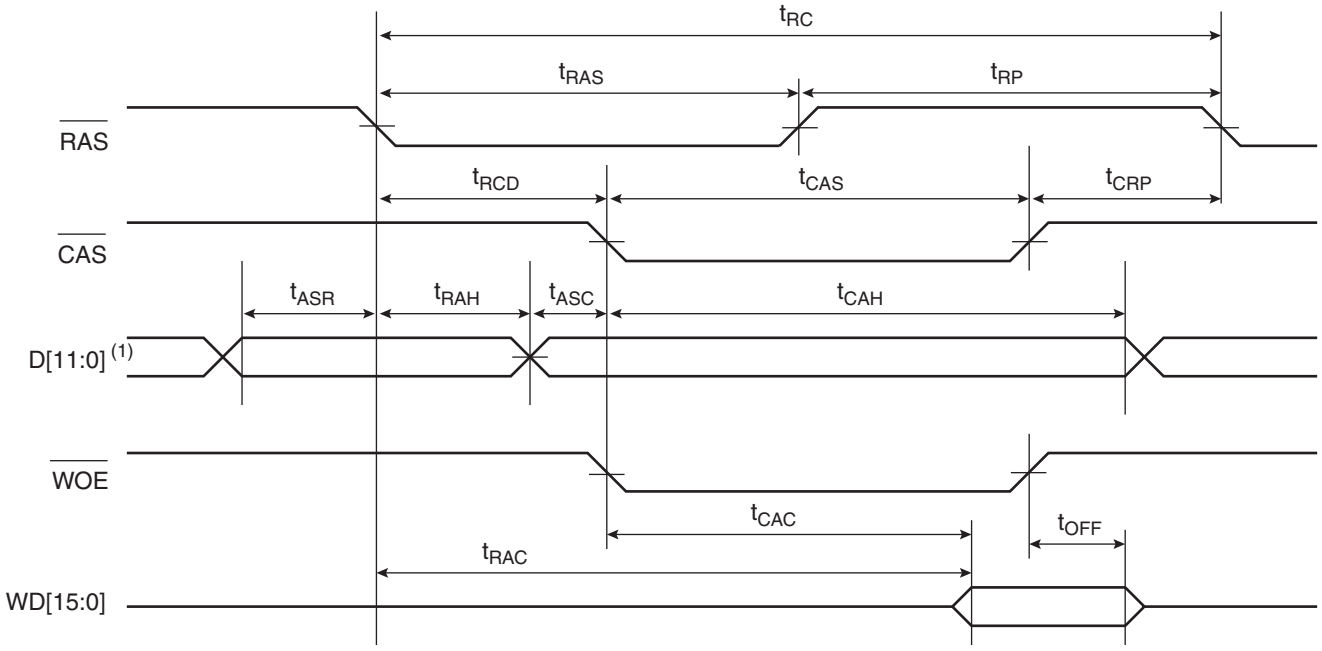
Table 12-1. RAS/CAS Correspondence to Physical Address[1]

Signal	Value at RAS Time	Value at CAS Time
WA0/DRA0	WA0	WA9
WA1/DRA1	WA1	WA10
WA2/DRA2	WA2	WA11
WA3/DRA3	WA3	WA12
WA4/DRA4	WA4	WA13
WA5/DRA5	WA5	WA14
WA6/DRA6	WA6	WA15
WA7/DRA7	WA7	WA16
WA8/DRA8	WA8	WA17
WA18/DRA9	WA18	WA19 (DRAM) Don’t care (SDRAM)
WA20/DRA10	WA20	WA21 (DRAM) High (SDRAM)
WA22/DRA11	WA22	WA23 (DRAM) Don’t care (SDRAM)

Note: Valid for DRAM and SDRAM unless otherwise stated.

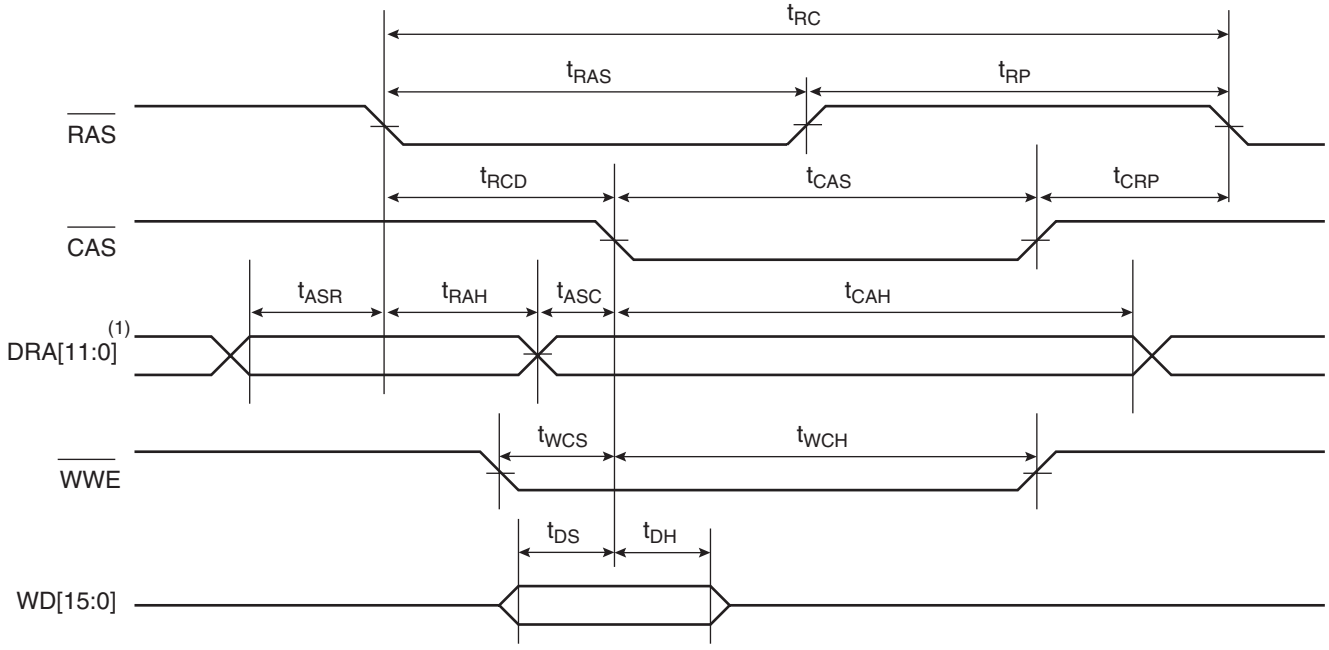
13. Detailed External DRAM Timing

Figure 13-1. Read Cycle



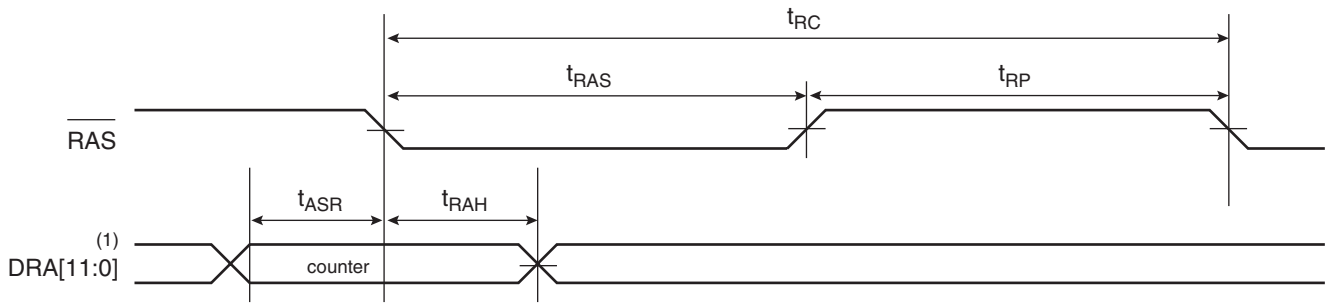
Note: 1. See Table 12-1 on page 16.

Figure 13-2. Write Cycle (Early Write)



Note: 1. See Table 12-1 on page 16.

Figure 13-3. Refresh Cycle ($\overline{RAS}$ Only)



Note: 1. See Table 12-1 on page 16.

Table 13-1. External DRAM Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Read/Write/Refresh cycle		6 x t_{CK}		ns
t_{RAC}	Access time from $\overline{RAS}$			5 x t_{CK} - 5	ns
t_{CAC}	Access time from $\overline{CAS}$			3 x t_{CK} - 5	ns
t_{OFF}	$\overline{CAS}$ high to output Hi-Z			2 x t_{CK} - 5	ns
t_{RP}	$\overline{RAS}$ precharge time	2 x t_{CK}			ns
t_{RAS}	$\overline{RAS}$ pulse width	4 x t_{CK} - 5			ns
t_{CAS}	$\overline{CAS}$ pulse width	3 x t_{CK} - 5			ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time		2 x t_{CK}		ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	2 x t_{CK} - 5			ns
t_{ASR}	Row address setup time	t_{CK} - 5			ns
t_{RAH}	Row address hold time	t_{CK} - 5			ns
t_{ASC}	Column address setup time	t_{CK} - 5			ns
t_{CAH}	Column address hold time	3 x t_{CK} - 5			ns
t_{WCS}	Write command set-up time		2 x t_{CK}		ns
t_{WCH}	Write command hold time		3 x t_{CK}		ns
t_{DS}	Write data set-up time		2 x t_{CK}		ns
t_{DH}	Write data hold time		3 x t_{CK}		ns
	Refresh counter average period (12-bit counter)		512 x t_{CK}		ns

The following points should be noted:

- The multiplexed $\overline{CAS}$, $\overline{RAS}$ addressing can support memory DRAM chips up to 16 Mbits x N as long as the number of row address lines and column address lines are identical. For example, device type 416C1200 is supported because it is a 1M x 16 organization with 10-bit row and 10-bit column. Device type 416C1000 is not supported because it is a 1M x 16 organization with 12-bit row and 8-bit column.
- The signal $\overline{WOE}$ is normally not used for DRAM connection. It is represented only for reference purposes.

- As $\overline{RAS}$ only counter refresh method is employed, several banks of DRAMs can be connected using simple external $\overline{CAS}$ decoding. Linear address lines (WAx) can be used to select between DRAM banks. For example, a 1M x 32 SIMM module may be connected as two 1M x 16 banks, with $\overline{CAS0}$ and $\overline{CAS1}$ selections issued from $\overline{CAS}$ and WA20.
- During a whole DRAM cycle (from $\overline{RAS}$ low to $\overline{CAS}$ rising), $\overline{WCS0}$ is asserted low.
- The equivalence between multiplexed DRAM address lines (DRA0 to DRA11) and the corresponding linear addressing (WA0 to WA23) is as follows:

	DRA11	DRA10	DRA9	DRA8	DRA7	DRA6	DRA5	DRA4	DRA3	DRA2	DRA1	DRA0
$\overline{RAS}$ time	WA22	WA20	WA18	WA8	WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA0
$\overline{CAS}$ time	WA23	WA21	WA19	WA17	WA16	WA15	WA14	WA13	WA12	WA11	WA10	WA9

- To save DRAM power consumption, $\overline{CAS}$ and $\overline{RAS}$ are cycled only when necessary. Therefore, depending on firmware loaded, total board power consumption may increase with synthesis processing traffic.

14. Detailed External ROM Timing

Figure 14-1. ROM Read Cycle

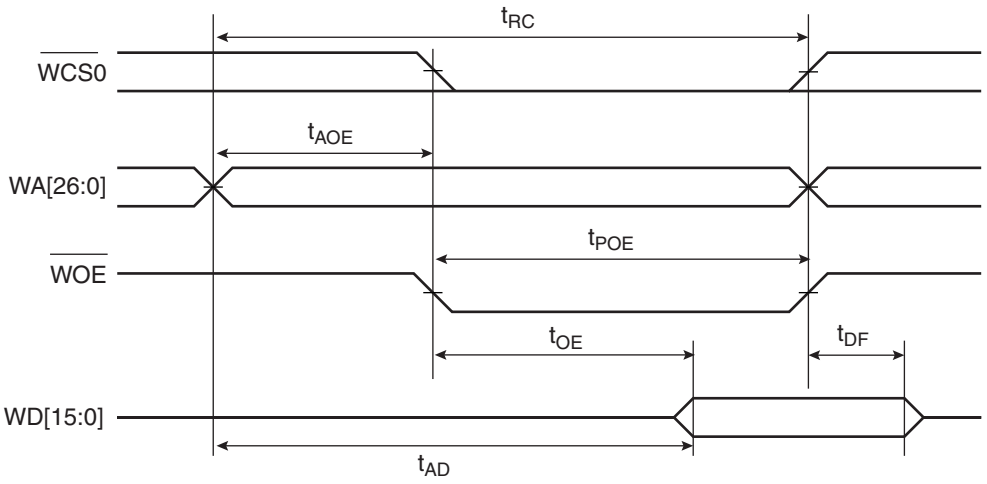


Table 14-1. External ROM Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Read cycle time		6 x t_{CK}		ns
t_{AOE}	Address valid to $\overline{WOE}$ low		t_{CK}		ns
t_{POE}	Output enable pulse width		5 x t_{ck}		ns
t_{AD}	Address access time	6 x t_{CK} - 5			ns
t_{OE}	Output enable access time	5 x t_{CK} - 5			ns
t_{DF}	Chip select or $\overline{WOE}$ high to input data High Z	0		t_{CK} - 5	ns

15. External RAM Timing

Figure 15-1. 16-bit SRAM Read Cycle

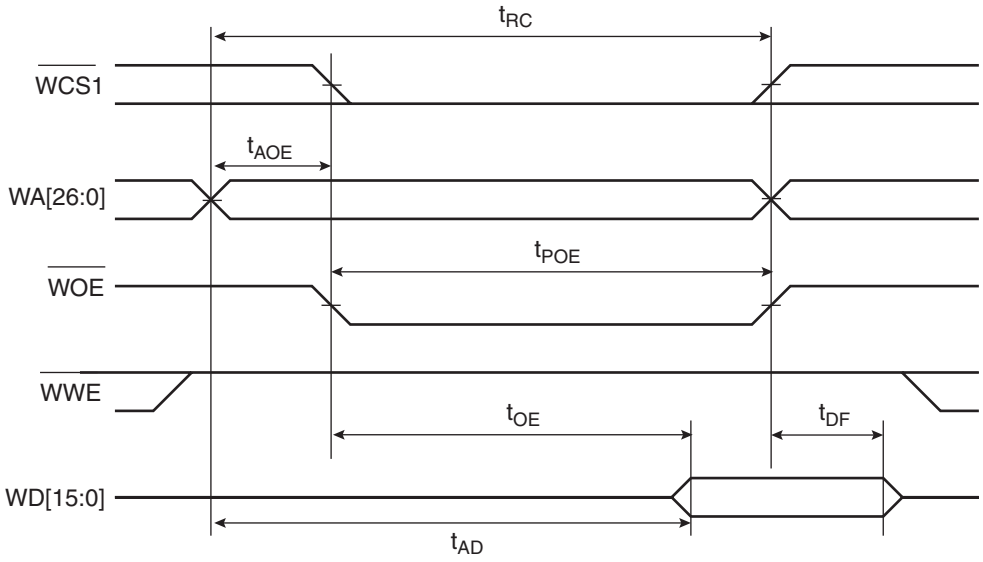


Figure 15-2. 16-bit SRAM Write Cycle

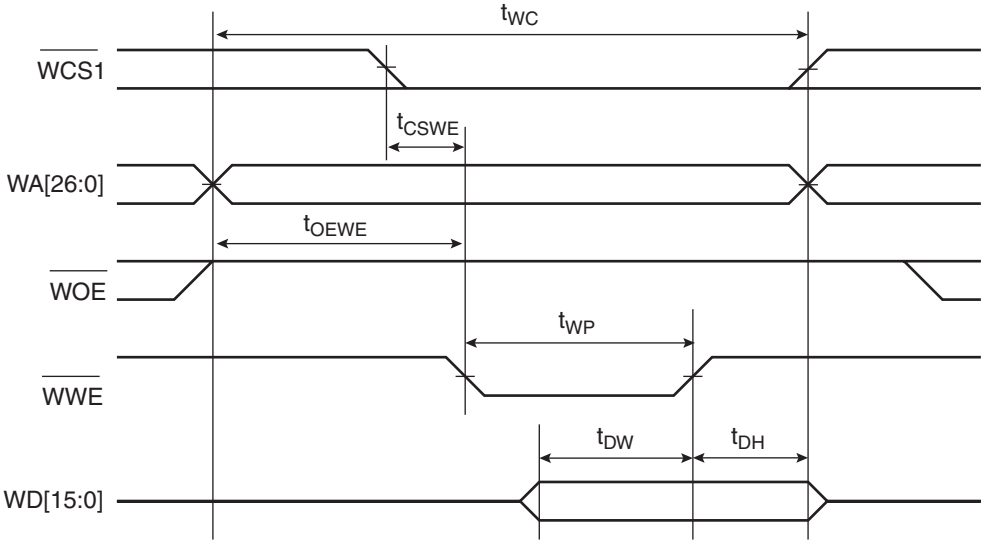


Table 15-1. External 16-bit SRAM Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Read cycle time		6 x t_{CK}		ns
t_{AOE}	Address valid to $\overline{WOE}$ low		t_{CK}		ns
t_{POE}	Output enable pulse width		5 x t_{CK}		ns
t_{AD}	Address access time	6 x t_{CK} - 5			ns
t_{OE}	Output enable access time	5 x t_{CK} - 5			ns
t_{DF}	Chip select or $\overline{WOE}$ high to input data High Z	0		t_{CK} - 5	ns

Table 15-1. External 16-bit SRAM Timing Parameters (Continued)

Symbol	Parameter	Min	Typ	Max	Unit
t_{WC}	Write cycle time		6 x t_{CK}		ns
t_{CSWE}	Write enable low from $\overline{CS}$	t_{CK} - 10			ns
t_{OEWE}	Write enable low from Address or $\overline{WOE}$	2t_{CK} - 10			ns
t_{WP}	Write pulse-width		3.5 x t_{CK}		ns
t_{DW}	Data out setup time	3.5 x t_{CK} - 10			ns
t_{DH}	Data out hold time	0.5 x t_{CK}			ns

Figure 15-3. 8-bit SRAM Read Cycle

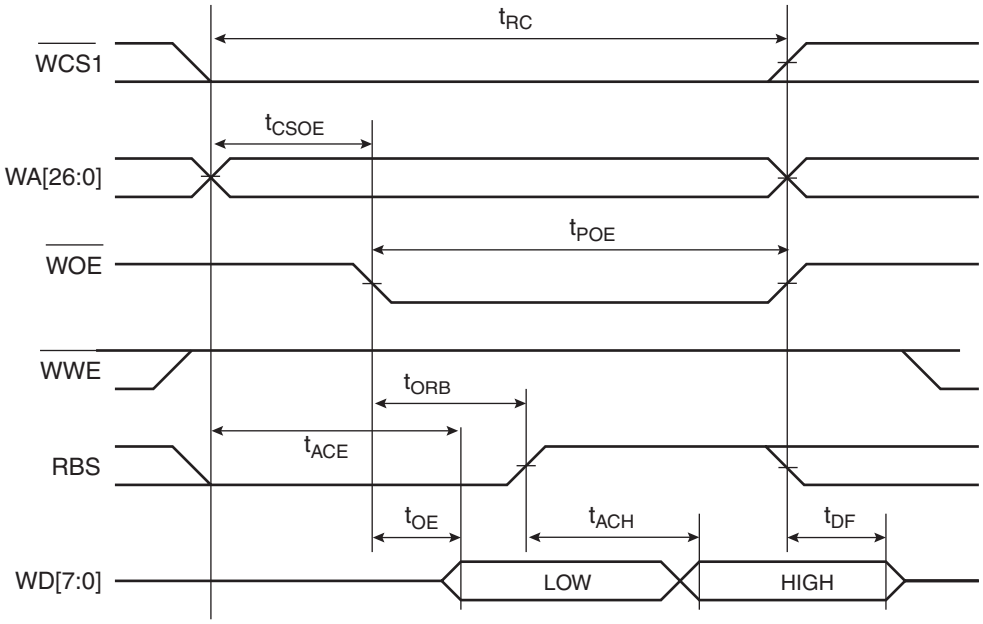


Figure 15-4. 8-bit SRAM Write Cycle

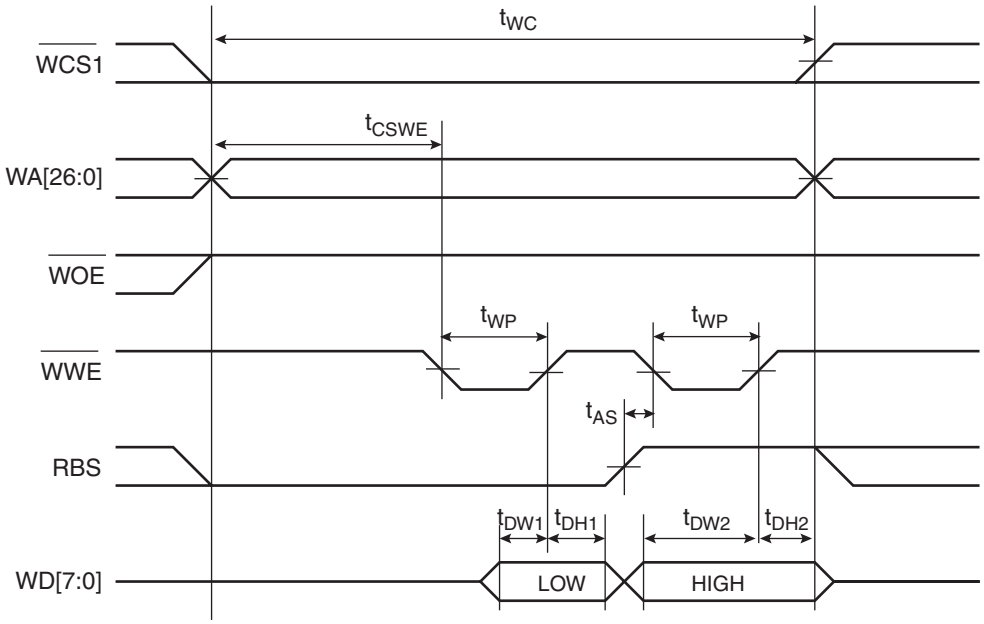


Table 15-2. External 8-bit SRAM Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Word (2 x bytes) read cycle time		6 x t_{CK}		ns
t_{CSOE}	Chip select low/address valid to $\overline{WOE}$ low		t_{CK}		ns
t_{POE}	Output enable pulse width		5 x t_{CK}		ns
t_{ACE}	Chip select/address low byte access time	3 x t_{CK} - 5			ns
t_{OE}	Output enable low byte access time	2 x t_{CK} - 5			ns
t_{ORB}	Output enable low to byte select high		2 x t_{CK}		ns
t_{ACH}	Byte select high byte access time	3 x t_{CK} - 5			ns
t_{DF}	Chip select or $\overline{WOE}$ high to input data High Z	0		t_{CK} - 5	ns
t_{WC}	Word (2 x bytes) write cycle time		6 x t_{CK}		ns
t_{CSWE}	1st $\overline{WWE}$ low from $\overline{CS}$ or Address or $\overline{WOE}$	t_{ck} - 10			ns
t_{WP}	Write (low and high byte) pulse width		1.5 x t_{CK}		ns
t_{DW1}	Data out low byte setup time	1.5 x t_{CK} - 10			ns
t_{DH1}	Data out low byte hold time	10			ns
t_{AS}	RBS high to second write pulse	t_{CK} - 5			ns
t_{DW2}	Data out high byte setup time	2.5 x t_{CK} - 10			ns
t_{DH2}	Data out high byte hold time	10			ns

16. Digital Audio Timing

Figure 16-1. Digital Audio Timing Diagram

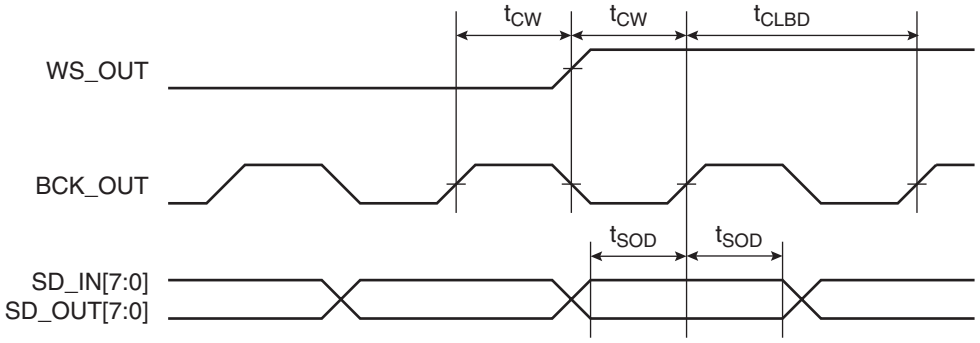
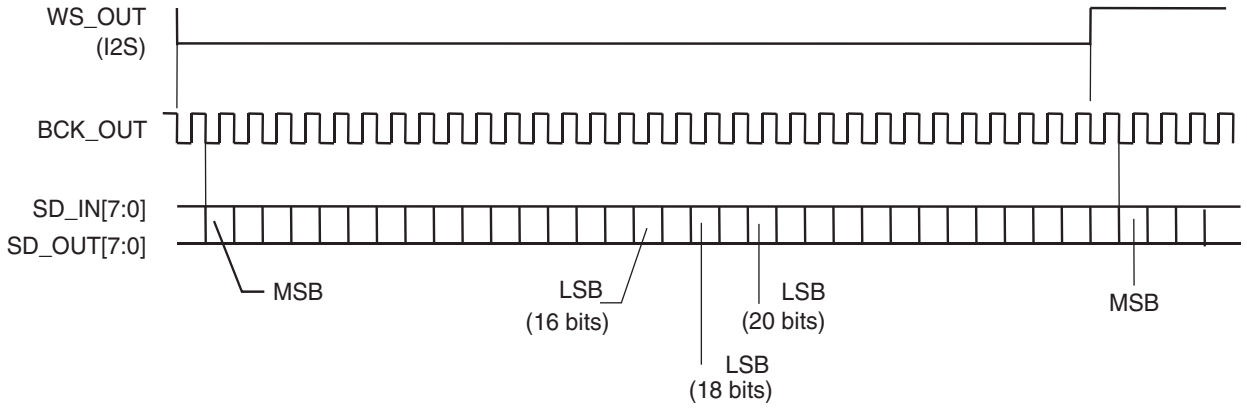


Table 16-1. Digital Audio Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	BCK_OUT rising to WS_OUT change	8 x t_{CK}- 10			ns
t_{SOD}	SD_IN[7:0]/SD_OUT[7:0] valid prior/after BCK_OUT rising	8 x t_{CK} - 10			ns
t_{CLBD}	BCK_OUT cycle time		16 x t_{CK}		ns

Figure 16-2. Digital Audio Frame Format



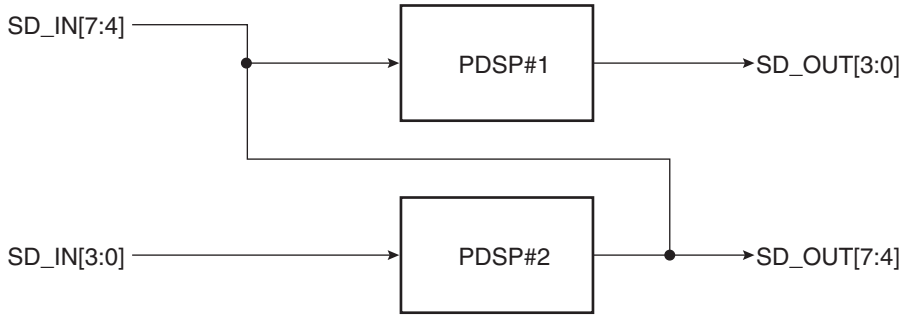
Note: SD_IN[7:0] is always 20 bits.

17. Audio Routing

Each PDSP can process eight digital audio inputs and generate eight digital audio outputs for a total of 16 digital audio-in and 16 digital audio-out.

The eight outputs from DSP#2 can be individually routed on DSP#1 inputs.

Figure 17-1. Audio Routing



18. MIDI Routing

The default configuration assigns MIDI1_IN/MIDI1_OUT to PDSP#1 and MIDI2_IN/MIDI2_OUT to PDSP#2.

Alternatively, MIDI1_IN can be routed as the same MIDI input to both PDSPs. In this case, the MIDI2_IN is available as a general-purpose input.

Also, if the MIDI2_OUT is not necessary, it can be defined as a general-purpose output.

19. General-purpose Input/Output Routing

MIDI2_IN, MIDI2_OUT, SD_IN[7, 6, 5, 3, 2, 1, 0] and SD_OUT[7:1] pins can be individually routed as general-purpose inputs or outputs as identified in Table 19-1.

Table 19-1. General-purpose Input/Output Routing

GPIO	Pin
GPIO_OUT[0] DSP#1	MIDI2_OUT
GPIO_OUT[1] DSP#1	SD_OUT[1]
GPIO_OUT[2] DSP#1	SD_OUT[2]
GPIO_OUT[3] DSP#1	SD_OUT[3]
GPIO_OUT[4] DSP#1	SD_IN[0]
GPIO_OUT[5] DSP#1	SD_IN[1]
GPIO_OUT[6] DSP#1	SD_IN[2]
GPIO_OUT[7] DSP#1	SD_IN[3]
GPIO_OUT[0] DSP#2	SD_OUT[4]
GPIO_OUT[1] DSP#2	SD_OUT[5]
GPIO_OUT[2] DSP#2	SD_OUT[6]
GPIO_OUT[3] DSP#2	SD_OUT[7]

Table 19-1. General-purpose Input/Output Routing (Continued)

GPIO	Pin
GPIO_OUT[4] DSP#2	MIDI2_IN
GPIO_OUT[5] DSP#2	SD_IN[5]
GPIO_OUT[6] DSP#2	SD_IN[6]
GPIO_OUT[7] DSP#2	SD_IN[7]
GPIO_IN[0] DSP#1	SD_IN[0]
GPIO_IN[1] DSP#1	SD_IN[1]
GPIO_IN[2] DSP#1	SD_IN[2]
GPIO_IN[3] DSP#1	SD_IN[3]
GPIO_IN[0] DSP#2	MIDI2_IN
GPIO_IN[1] DSP#2	SD_IN[5]
GPIO_IN[2] DSP#2	SD_IN[6]
GPIO_IN[3] DSP#2	SD_IN[7]

20. Bi-processor Operation

Each PDSP has access to the same memory space. Sample data, buffers and programs can therefore be shared between the two PDSPs, thus minimizing memory requirements.

Each P16 has the possibility to test a read-only bit that identifies the PDSP number it belongs to (PDSPID). This allows the firmware to make decisions according to the processor currently executing the code.

As an example, consider implementation of a 128-voice synthesizer. An easy way to share traffic between the two PDSPs would be to have PDSP#1 process even MIDI-numbered notes, while the PDSP#2 would process odd MIDI-numbered notes.

In this case, there would only be a single firmware processed by both P16s, with some coding as follows:

```
If (PDSPID == 0 && noteeven) then ProcessNote();
If (PDSPID == 1 && noteodd) then ProcessNote();
```

The two PDSPs may also execute completely different firmware. In this case, as both types of firmware start from address 100H, a test on PDSPID should be done at the beginning of the program to jump to the correct firmware.

21. Reset and Power-down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized. This may take about 20 ms. The $\overline{\text{RESET}}$ signal is normally derived from the PC master reset. However, a typical RC/diode power-up network can also be used for some applications.

After the low-to-high transition of $\overline{\text{RESET}}$, the following occurs:

- If $\overline{\text{REFRESH}}$ is sampled high at the low to high transition of $\overline{\text{RESET}}$ then the external SDRAM init cycles are executed (see ”Memory Type Configuration and Boot Configuration” on page 26).

- Both Synthesis/DSP enter an idle state.
- If $\overline{\text{REFRESH}}$ is low, then both P16 program execution starts from address 0100H in ROM space ($\overline{\text{WCS0}}$ low).
- If $\overline{\text{REFRESH}}$ is high, then both P16 program execution starts from address 0000H in internal bootstrap ROM space. Each internal bootstrap expects to receive 256 words from its respective 16-bit burst transfer port, which will be stored from 0100H to 01FFH into the external DRAM space. The bootstrap then resumes control at address 0100H.
- If $\overline{\text{PDWN}}$ is asserted low, then all I/Os and outputs will be floated and the crystal oscillator and PLL will be stopped. The chip enters a deep power-down sleep mode. To exit power down, $\overline{\text{PDWN}}$ has to be asserted high, then $\overline{\text{RESET}}$ applied.

22. Memory Type Configuration and Boot Configuration

At the end of power-up, when $\overline{\text{RESET}}$ input goes from low to high, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{REFRESH}}$ pins are sampled by the ATSAM9708 to determine memory type configuration and boot type. $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{REFRESH}}$ must be pulled to V_{CC} or GND through an external 10K resistor to select these different power-up configurations.

One memory type can be used for low pages (addresses [0-8000000h], AD[27] = 0) and a different type for high pages (addresses [8000000h-10000000h]).

Memory types allowed are Flash/ROM, SRAM, DRAM or SDRAM.

When using RAM (SRAM, DRAM or SDRAM) in low page, P16 must start in bootstrap state. When in bootstrap state, P16 program execution starts at address 0. If not in bootstrap, program execution starts at address 100h. Bootstrap is selected via the $\overline{\text{REFRESH}}$ pin.

Table 22-1. Memory Type and Boot Configuration

Pin Level Detected at Reset			Low Page		High Page	
REFRESH	**RAS**	**CAS**				
Stand-alone Mode			**Memory Type**	**Selected by**	**Memory Type**	**Selected by**
Low	Low	Low	Flash/ROM	$\overline{\text{WCS0}}$	SRAM	$\overline{\text{WCS1}}$
Low	Low	High	Flash/ROM	$\overline{\text{WCS0}}$	DRAM	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$
Low	High	Low	Flash/ROM	$\overline{\text{WCS0}}$	SDRAM	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$
Low	High	High	Flash/ROM	$\overline{\text{WCS0}}$	Selected by firmware	
Bootstrap Mode						
High	Low	Low	SRAM	$\overline{\text{WCS0}}$	Flash/ROM	$\overline{\text{WCS1}}$
High	Low	High	DRAM	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$	Flash/ROM	$\overline{\text{WCS1}}$
High	High	Low	SDRAM	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$	Flash/ROM	$\overline{\text{WCS1}}$

Note: 1. When accessing DRAM or SDRAM, DRAM/SDRAM is selected by signals $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ ($\overline{\text{WCS0}}$ and $\overline{\text{WCS1}}$ are inactive) and addresses are time-multiplexed on WA[..] pins as follows:
- WA0 - WA8: DRA0 - DRA8
- WA18: DRA9
- WA20: DRA10
- WA22: DRA11

When accessing SRAM, Flash or ROM, SRAM/Flash/ROM are selected by signals $\overline{\text{WCS0}}$, $\overline{\text{WCS1}}$ ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive) and WA[26:0] address pins:
- if low pages: $\overline{\text{WCS0}}$ = 0, $\overline{\text{WCS1}}$ = 1
- if high pages: $\overline{\text{WCS0}}$ = 1, $\overline{\text{WCS1}}$ = 0

23. Recommended Board Layout

Like all HCMOS high-integration ICs, some rules of board layout should be followed for reliable device operation:

23.1 GND, V_{CC}, V_{C3} Distribution, Decouplings

All GND, V_{CC}, V_{C3} pins should be connected. GND and V_{CC} planes are strongly recommended below the ATSAM9708. The board GND and V_{CC} distribution should be in grid form. If 3.3V is not available, then V_{C3} can be connected to V_{CC} by two 1N4148 diodes in series.

Recommended decoupling is 0.1 µF at each corner of the IC with an additional 10 µF decoupling close to the crystal. V_{C3} requires a single 0.1µF decoupling close to the IC.

23.2 Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the ATSAM9708 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from ATSAM9708.

23.3 Buses

Parallel layout from PC_D[15:0] and DRA[11:0]/WD[15:0] should be avoided. The PC_D[15:0] bus is an asynchronous high-transient current-type bus. Even on short distances, it can induce pulses on DRA[11:0]/WD[15:0] which can corrupt addresses and/or data on these buses.

A ground plane should be implemented below the PC_D[15:0] bus, which connects both to the PC-ISA connector and to the ATSAM9708 GND.

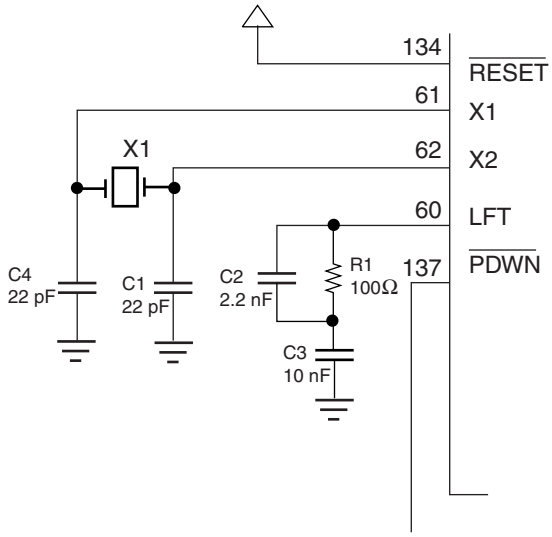
A ground plane should be implemented below the DRA[11:0]/WD[15:0] bus, which connects both to the DRAM SIMM grounds and to the ATSAM9708.

23.4 Analog Section

A specific AGND ground plane should be provided, which connects to the GND ground by a single trace. No digital signals should cross the AGND plane. Refer to the Codec vendor recommended layout for correct implementation of the analog section.

24. Recommended Crystal Compensation and LFT Filter

Figure 24-1. Recommended Crystal Compensation and LFT Filter



25. Mechanical Dimensions

Figure 25-1. 144-lead TQFP Package Drawing

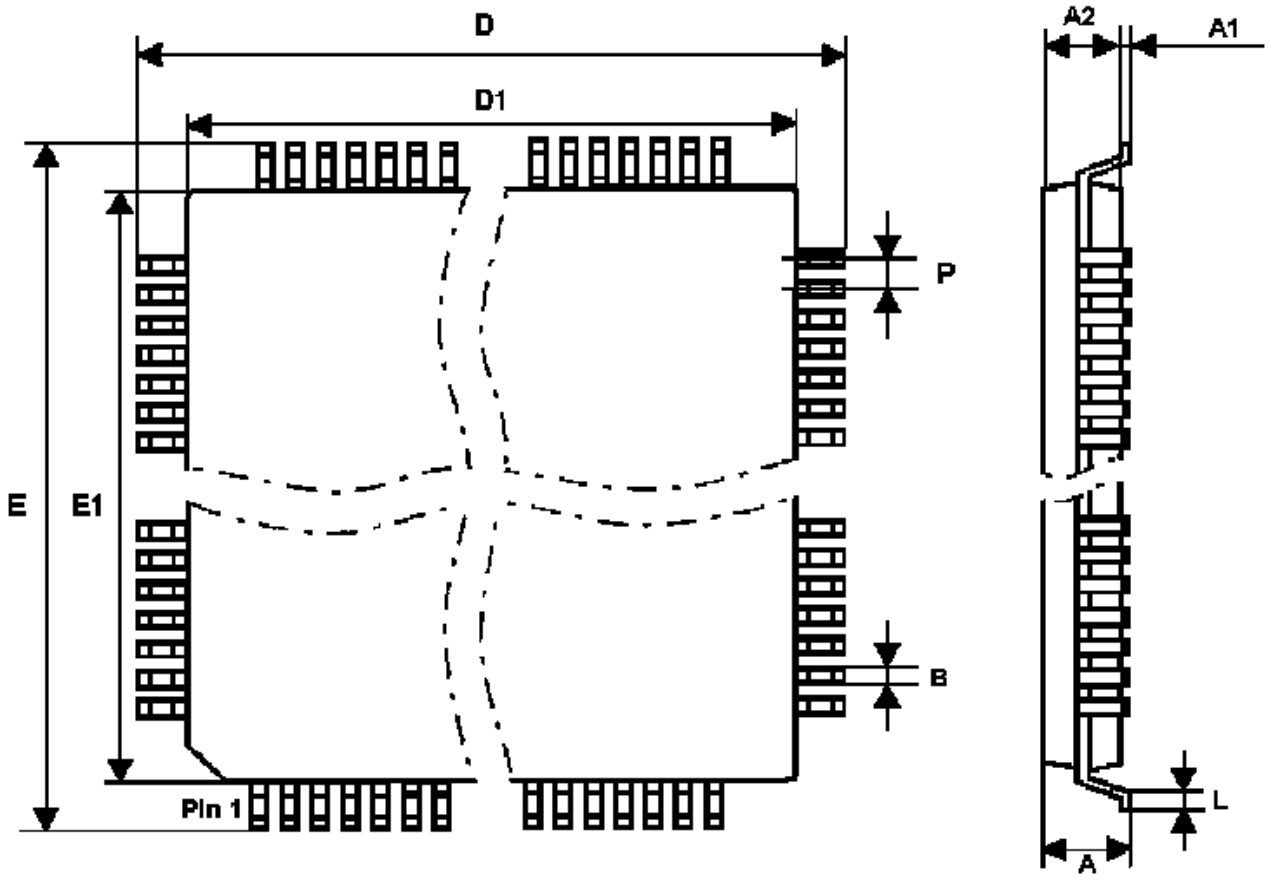


Table 25-1. 144-lead TQFP Package Dimensions (in millimeters)

	Min	Nom	Max
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	21.90	22.00	22.10
D1	19.90	20.00	20.10
E	21.90	22.00	22.10
E1	19.90	20.00	20.10
L	0.45	0.60	0.75
P		0.50	
B	0.17	0.22	0.27

26. Revision History

Table 26-1. Revision History

Document	Comments
1772A	Issue date: July-01
1772B	Issue date: 10-Jan-02
1772C	Issue date: 05-Nov-02
	Atmel product designation AT added to SAM product identification on all pages.
	Document format updated on all pages.
	All figures modified to conform to Table 2, ISA Bus Group and Table 6, Pinout.
	Table 6, page 6 Pinout. PC_READY, overline added.
	Table 7, Absolute Maximum Ratings, Table 8, Recommended Operating Conditions, Table 9, DC Characteristics; modified to conform to Table 2, ISA Bus Group and Table 6, Pinout, page 7.
	Change to table 10 on page 12.
	MIDI Routing, signal names modified on page 25.
	Buses, bus names modified to conform to Table 2, ISA Bus Group and Table 6, Pinout, on page 28.
	Trademark information modified.
1772D	Issue date: 15-Jan-04
	ROM/RAM memory speed corrected to read 90 ns on pages 1, 10.
	Updated Figures 5, 6, 7 and 8 in section External Memory Timing Overview on pages 14. 15 and 16.
	Updated Figure 12 and Table 13 with new timing information on page 19.
	Updated Figures 13, 14 and 15 and Tables 14 and 15 with new timing information on pages 20, 21 and 22.
1772E	Updated Figure 12-3 on page 15.
	Updated CAS state in Bootstrap Mode in Table 22-1, “Memory Type and Boot Configuration,” on page 26.

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