

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4510 BCD up/down counter

Product specification
File under Integrated Circuits, IC06

December 1990

BCD up/down counter

74HC/HCT4510

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4510 are high-speed Si-gate CMOS devices and are pin compatible with the “4510” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4510 are edge-triggered synchronous up/down BCD counters with a clock input (CP), an up/down count control input (UP/DN), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH

parallel load input (PL), four parallel inputs (D₀ to D₃), four parallel outputs (Q₀ to Q₃), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on D₀ to D₃ is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW-to-HIGH transition of CP if $\overline{CE}$ is LOW. UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when Q₀ and Q₃ are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when Q₀ to Q₃ and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (Q₀ to Q₃ = LOW) independent of all other input conditions.

Logic equation for terminal count: $\overline{TC} = \overline{CE} \cdot \{(\overline{UP/DN}) \cdot Q_0 \cdot Q_3 + (\overline{UP/DN}) \cdot \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3}\}$

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay CP to Q _n	C _L = 15 pF; V _{CC} = 5 V	21	23	ns
f _{max}	maximum clock frequency		57	58	MHz
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	50	53	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}. For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

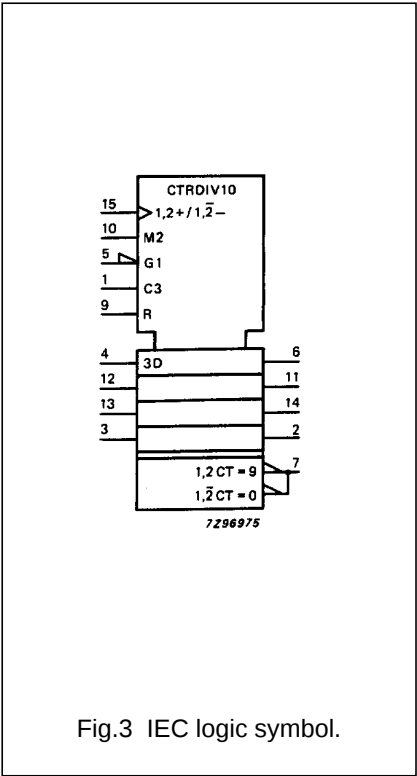
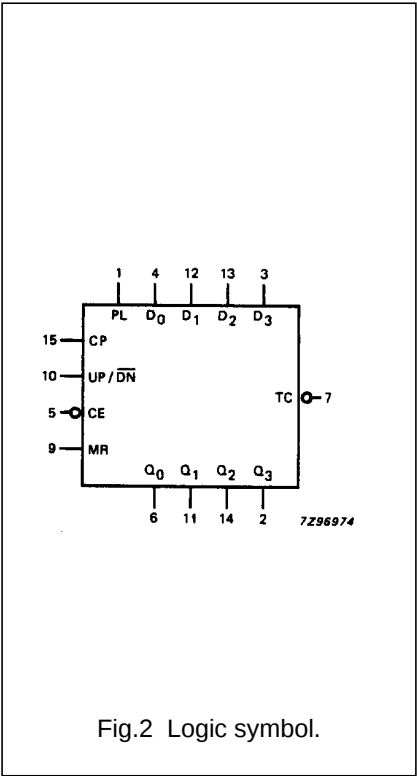
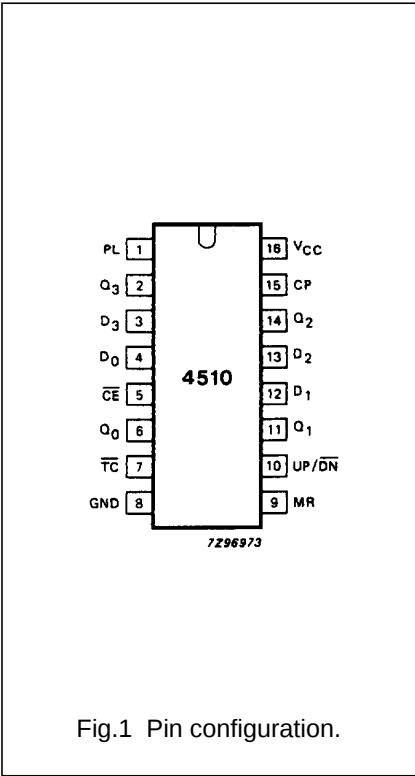
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	D ₀ to D ₃	parallel inputs
5	$\overline{\text{CE}}$	count enable input (active LOW)
6, 11, 14, 2	Q ₀ to Q ₃	parallel outputs
7	$\overline{\text{TC}}$	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/ $\overline{\text{DN}}$	up/down control input
15	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V _{CC}	positive supply voltage



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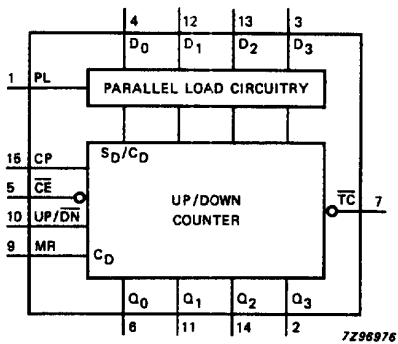


Fig.4 Functional diagram.

FUNCTION TABLE

MR	PL	UP/DN	CE	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↑	count down
L	L	H	L	↑	count up
H	X	X	X	X	reset

Notes

- 1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- ↑ = LOW-to-HIGH clock transition

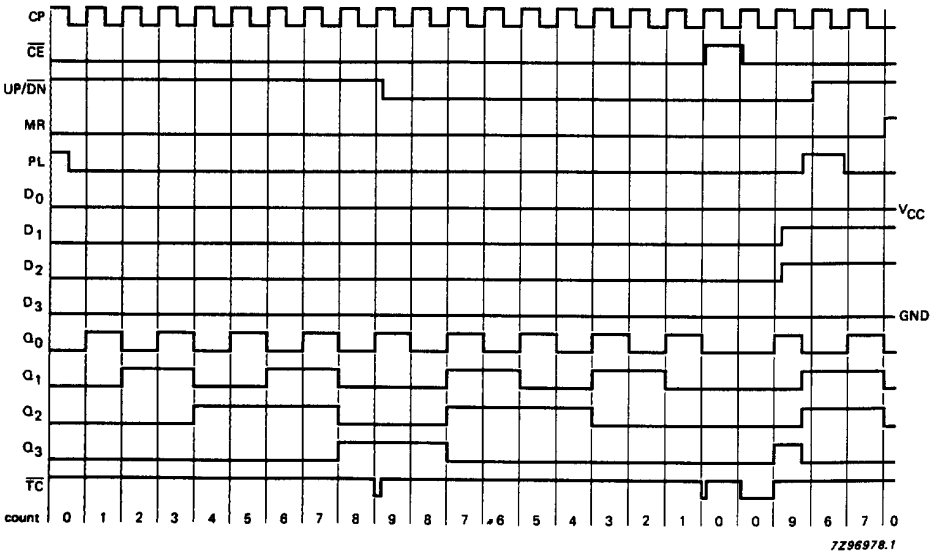


Fig.5 Timing diagram.

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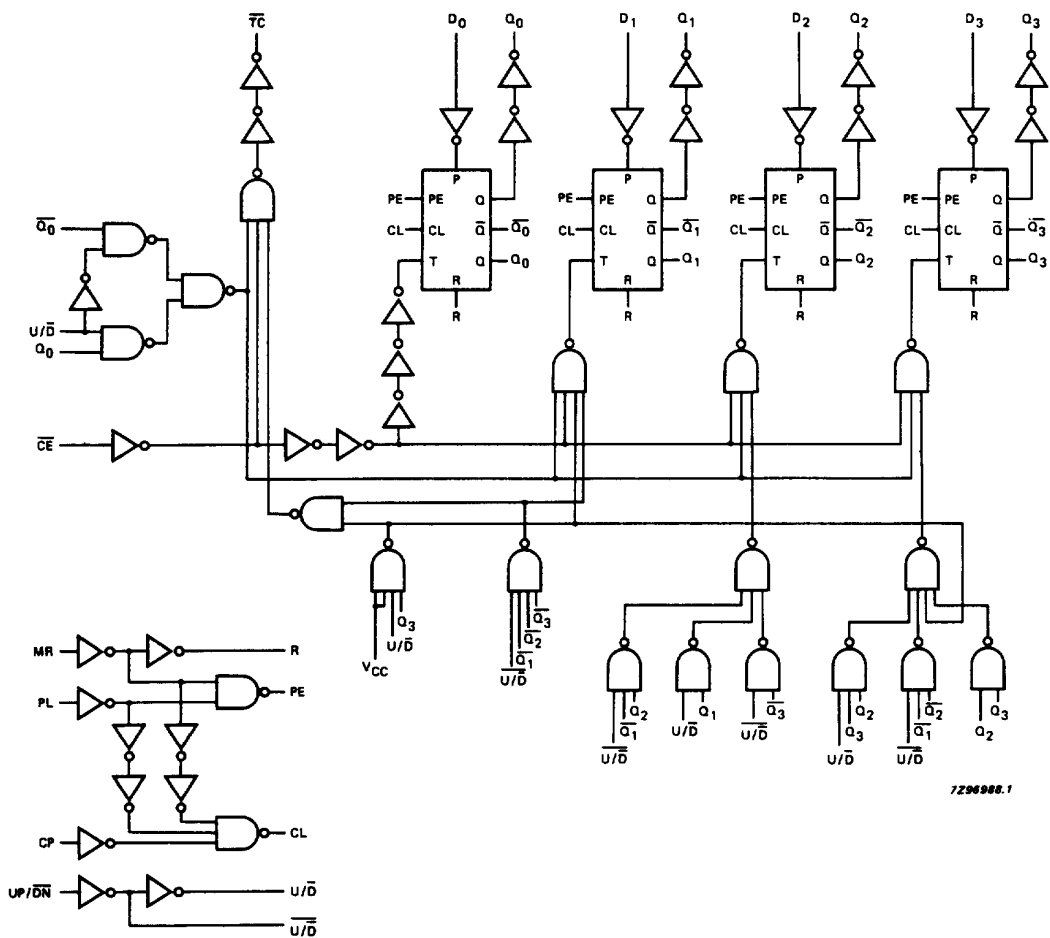


Fig.6 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		69 25 20	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.7
t _{PHL}	propagation delay MR to Q _n		63 23 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.10
t _{PLH} / t _{PHL}	propagation delay PL to Q _n		77 28 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.9
t _{PHL} / t _{PLH}	propagation delay CP to TC		74 27 22	260 52 44		325 65 55		395 78 66	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay CE to TC		36 13 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.8
t _{PLH}	propagation delay MR to TC		69 25 20	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	Fig.10
t _{PHL} / t _{PLH}	propagation delay PL to TC		91 33 26	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig.9
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.9
t _w	pulse width CP, CE HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t _w	parallel load pulse width HIGH	80 16 14	22 8 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.10
t _w	master reset pulse width HIGH	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.10

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SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{rem}	removal time MR to CP	80 16 14	28 10 8		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.10
t _{rem}	removal time PL to CP	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.10
t _{su}	set-up time UP/DN to CP	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.8
t _{su}	set-up time CE to CP	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.8
t _{su}	set-up time D _n to PL	100 20 17	17 6 5		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.11
t _h	hold time CE to CP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.8
t _h	hold time D _n to PL	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig.11
t _h	hold time UP/DN to CP	0 0 0	−19 −7 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.8
f _{max}	maximum clock pulse frequency	6.0 30 35	17 52 62		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below

INPUT	UNIT LOAD COEFFICIENT
D_n	0.75
$PL, \overline{CE}$	1.00
UP/DN	1.00
CP	1.25
MR	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

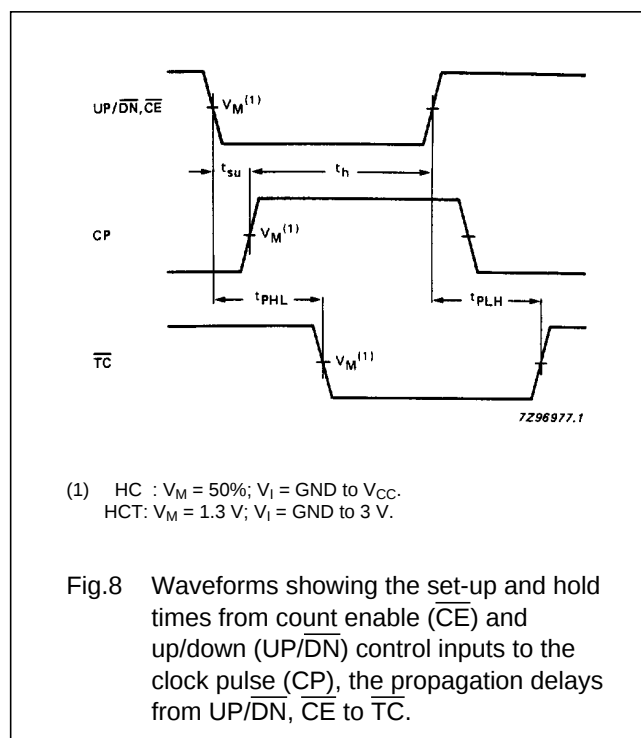
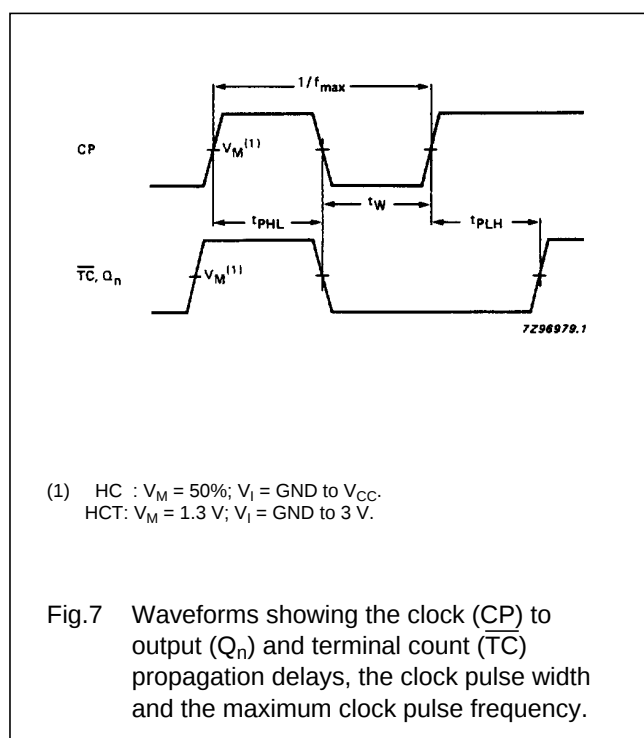
SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		27	50		63		75	ns	4.5	Fig.7
t _{PHL}	propagation delay MR to Q _n		25	42		53		63	ns	4.5	Fig.10
t _{PLH} / t _{PHL}	propagation delay PL to Q _n		28	53		66		80	ns	4.5	Fig.9
t _{PHL} / t _{PLH}	propagation delay CP to $\overline{TC}$		29	58		73		87	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay $\overline{CE}$ to $\overline{TC}$		17	31		39		47	ns	4.5	Fig.8
t _{PLH}	propagation delay MR to $\overline{TC}$		31	50		63		75	ns	4.5	Fig.10
t _{PHL} / t _{PLH}	propagation delay PL to $\overline{TC}$		35	68		85		102	ns	4.5	Fig.10
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.9
t _w	pulse width CP, $\overline{CE}$ HIGH or LOW	16	9		20		24		ns	4.5	Fig.7
t _w	parallel load pulse width HIGH	16	6		20		24		ns	4.5	Fig.10
t _w	master reset pulse width HIGH	20	4		25		30		ns	4.5	Fig.10

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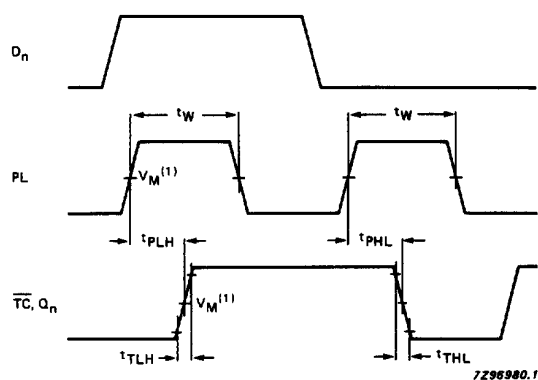
SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{rem}	removal time MR to CP	23	13		29		35		ns	4.5	Fig.10
t _{rem}	removal time PL to CP	17	10		21		26		ns	4.5	Fig.10
t _{su}	set-up time UP/DN to CP	20	12		25		30		ns	4.5	Fig.8
t _{su}	set-up time CE to CP	20	6		25		30		ns	4.5	Fig.8
t _{su}	set-up time D _n to PL	20	6		25		30		ns	4.5	Fig.11
t _h	hold time CE to CP	5	0		5		5		ns	4.5	Fig.8
t _h	hold time D _n to PL	5	0		5		5		ns	4.5	Fig.11
t _h	hold time UP/DN to CP	0	−5		0		0		ns	4.5	Fig.8
f _{max}	maximum clock pulse frequency	30	53		24		20		MHz	4.5	Fig.7

AC WAVEFORMS



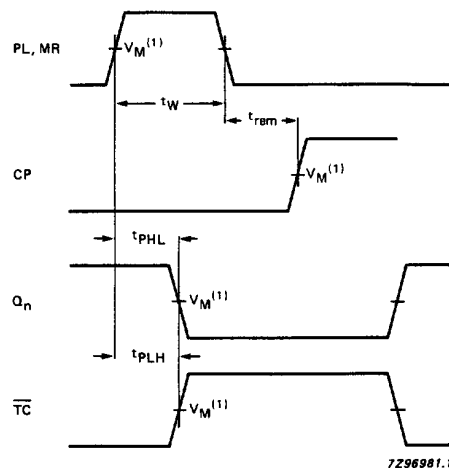
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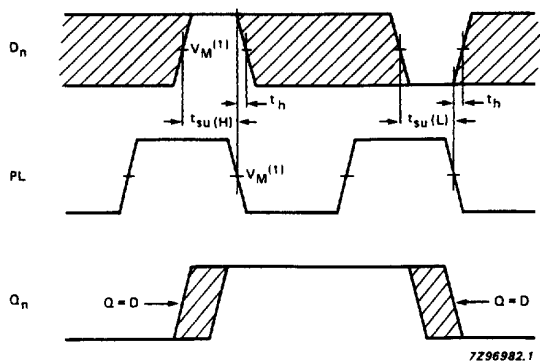
- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.9 Waveforms showing the preset enable pulse width, preset enable to output delays and output transition times.



- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.10 Waveforms showing the master reset pulse, master reset to terminal count and Q_n delay and master reset to clock removal time.



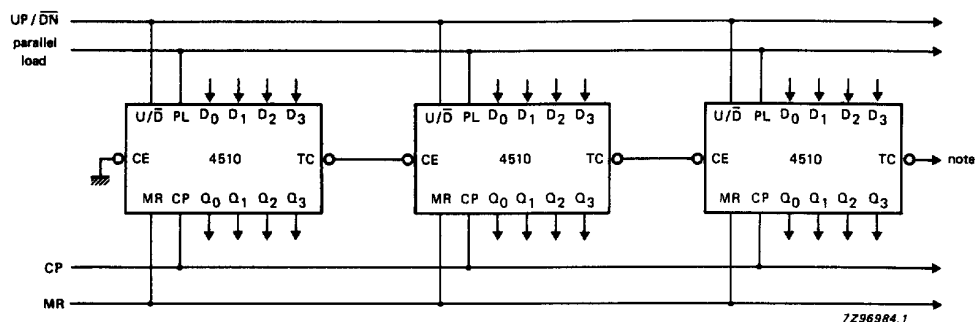
- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.11 Waveforms showing the data set-up and hold times to parallel load (PL).

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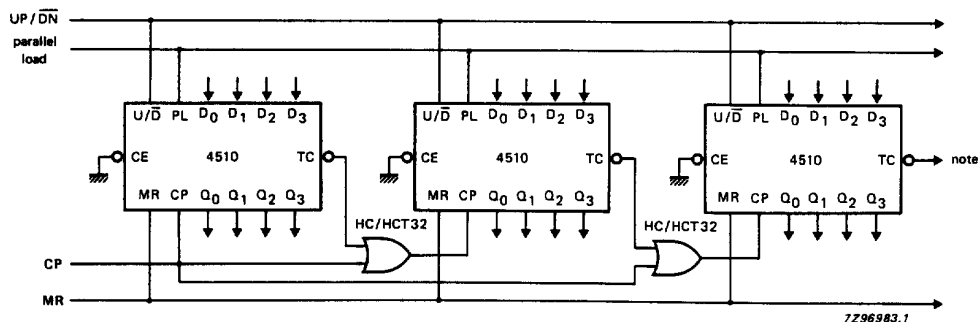
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APPLICATION INFORMATION



Terminal count ($\overline{TC}$) lines at the 2nd, 3rd, etc. stages may have a negative-going glitch pulse resulting from differential delays of different 4510s. These negative-going glitches do not affect proper 4510 operation. However, if the terminal count signals are used to trigger other edge sensitive logic devices, such as flip-flops or counters, the terminal count signals should be gated with the clock signal using a 2-input OR gate such as HC/HCT32.

Fig.12 Cascading counter packages (parallel clocking).

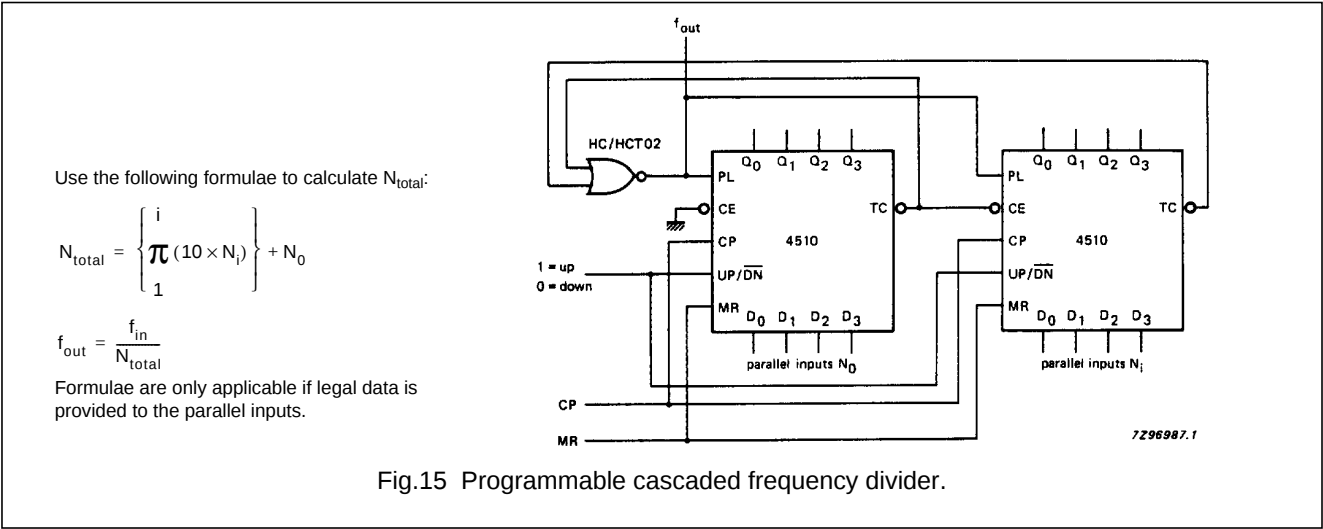
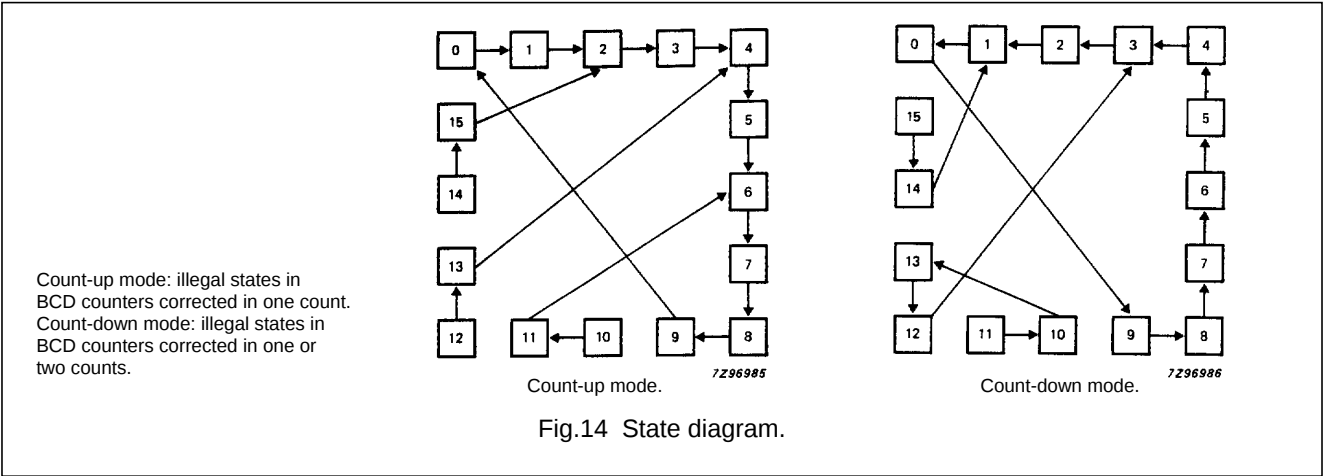


Ripple clocking mode: the $\overline{U/\overline{D}}$ control can be changed at any count. The only restriction on changing the $\overline{U/\overline{D}}$ control is that the clock input to the first counting stage must be "HIGH". For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages and $\overline{TC}$ is connected directly to the $\overline{CP}$ input of the next stage with $\overline{CE}$ grounded.

Fig.13 Cascading counter packages (ripple clocking).

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parallel inputs				count-up n	count-down n
D ₃	D ₂	D ₁	D ₀		
0	0	0	0	9	(1)
0	0	0	1	8	1
0	0	1	0	7	2
0	0	1	1	6	3
0	1	0	0	5	4
0	1	0	1	4	5
0	1	1	0	3	6
0	1	1	1	2	7
1	0	0	0	1	8
1	0	0	1	(1)	9

Note

1. no count; f_{out} is HIGH.

PACKAGE OUTLINES

See “74HC/HCT/HCU/HCMOS Logic Package Outlines”.