Built-in Low Consumption and High Accuracy Shunt Regulator

High Efficiency, Low Standby Power and CCM Corresponding Secondary Side Synchronous Rectification Controller IC

BM1R00178F

General Description

BM1R00178F is synchronous rectification controller to be used in the secondary side output. It has a built-in low consumption and high accuracy shunt regulator, which reduces standby power. Since the shunt regulator is made up of completely independent chips, it can operate as a GND reference even when it is used with High Side. At continuous conduction mode (CCM) operation, further space saving can be realized when operating without the input switching synchronizing signal of the primary side. BM1R00178F also feature a wide operating supply voltage of 2.7V to 32V for various output applications.
In addition, by adopting the high voltage 120V (Max) process, it is possible to monitor the drain voltage directly.

Features

- Built-in Low Consumption and High Accuracy Shunt Regulator, which Reduces Standby Power
- Synchronous Rectification FET Layout: High/Low Side
- 120V (Max) High Voltage Process DRAIN Monitor Pin
- Wide Supply Voltage Range of 2.7V to 32V
- Supports Drive Type: PWM, QR and LLC Controller etc.
- No Input Required on the Primary-Side at CCM
- Built-in Over Voltage Protection for SH_IN and SH_OUT Pin
- Built-in Thermal Shutdown Function

Key Specifications

- Supply Voltage 2.7V to 32V
- Circuit Current (No Switching): 800μA(Typ)
- DRAIN Monitor Pin Absolute Voltage: 120V(Max)
- Operating Temperature Range: -40°C to +105°C

Package	W(Typ) x D(Typ) x H(Max)
SOP8	5.00mm x 6.20mm x 1.71mm



Applications

- AC/DC Output Power Conversion Applications: Charger, Adapter, TV, Rice Cooker, Humidifier, Air Conditioning, Vacuum Cleaner, etc.

Typical Application Circuits

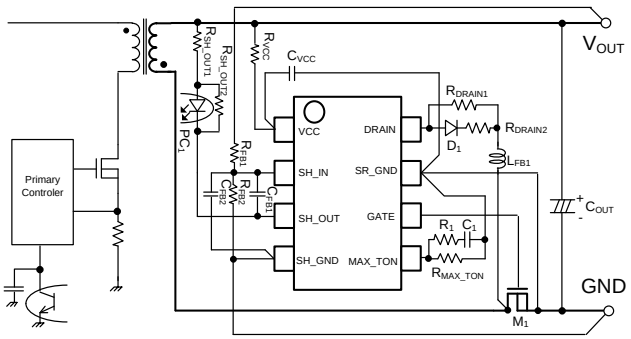


Figure 1. Flyback Application Circuit (Low side FET)

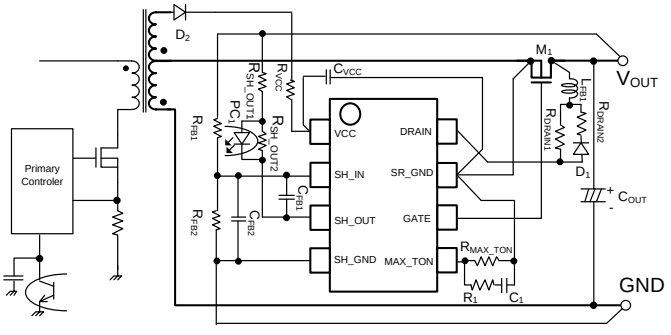
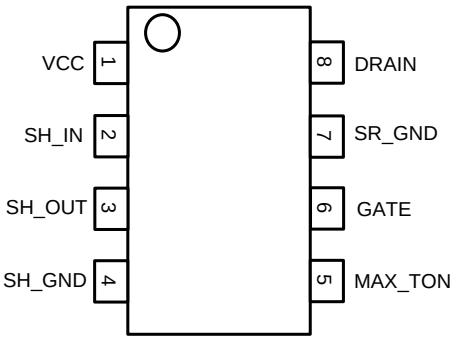


Figure 2. Flyback Application Circuit (High side FET)

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Pin Configuration

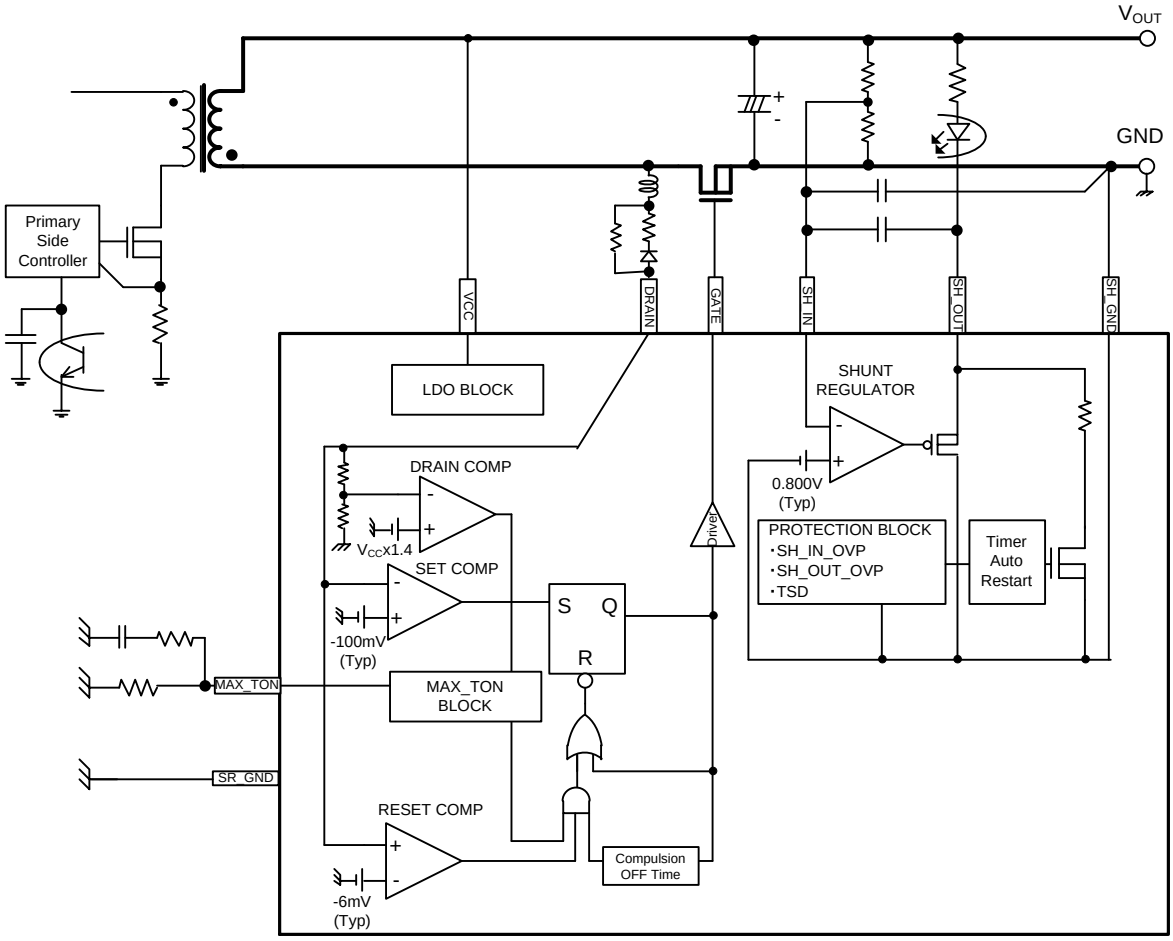
(TOP VIEW)



Pin Description

Pin No.	Pin Name	Function
1	VCC	Power supply input
2	SH_IN	Shunt regulator reference input
3	SH_OUT	Shunt regulator power supply / output
4	SH_GND	Shunt regulator GND
5	MAX_TON	Set maximum on time
6	GATE	Secondary side FET GATE drive
7	SR_GND	Synchronous rectification GND
8	DRAIN	Secondary side FET DRAIN monitor

Block Diagram



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Description of Block

1. **SET_COMP Block**
   Monitors the DRAIN pin voltage, and outputs a signal to turn on the FET if the DRAIN pin voltage is less than or equal to -100mV (Typ).

2. **RESET_COMP Block**
   Monitors the DRAIN pin voltage and outputs a signal to turn off the FET if the DRAIN pin voltage is more than or equal to -6mV (Typ).

3. **Compulsion OFF Time Block**
   When the FET is turned OFF due to RESET COMP detection, resonance waveforms appear on the DRAIN pin. To prevent the resonance waveforms from turning on the FET, an OFF state should be forced for a certain time.

   Operation sequence of each block is shown on the figure below.

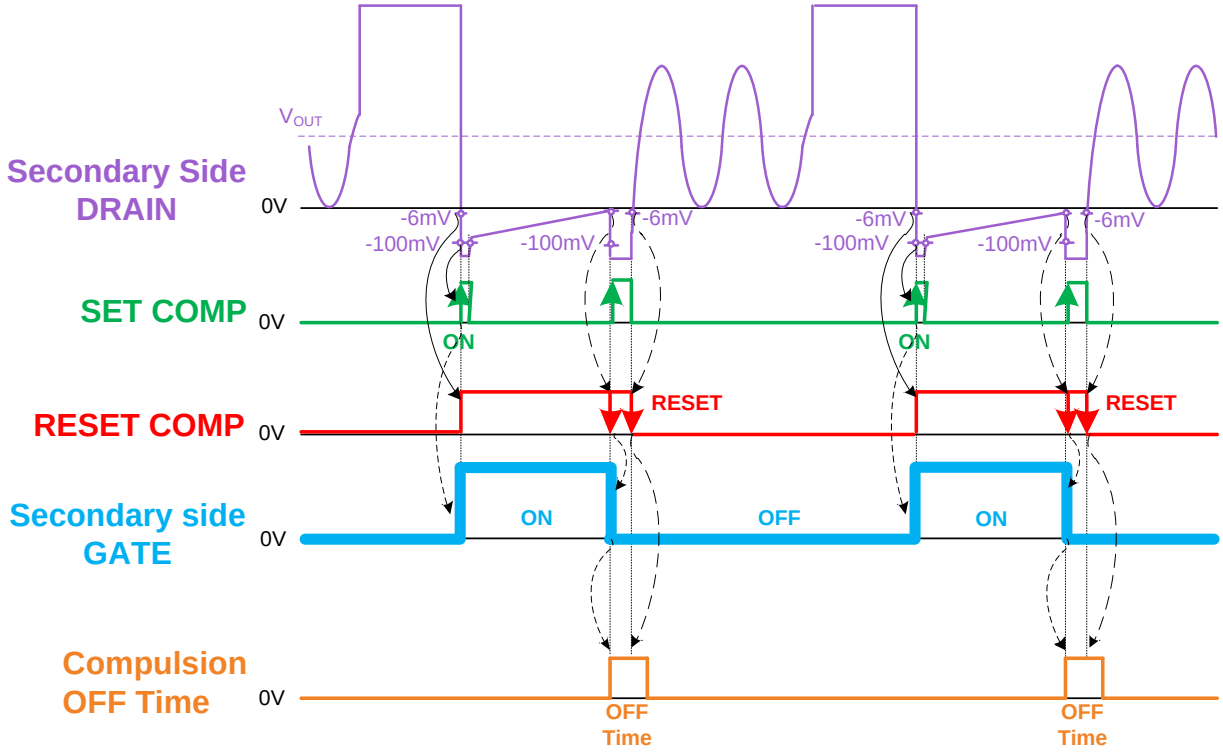


Figure 3. Operation sequence

About Maximum Input Frequency
The Maximum Operating Frequency of the IC depends on the Compulsion OFF Time. For example, BM1R00178F Compulsion OFF Time is equal to 3.000μs. Considering a variation of 9%, the maximum input frequency is given by the following:

$$f_{MAX} = \frac{1}{3.000(\mu s)\times 1.09} = 305 \quad [\text{kHz}]$$

However, because the frequency largely fluctuates depending on the input voltage, load conditions, etc., it will be different for each application.

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Description of Block – continued

4. MAX_TON Block

MAX_TON block sets the maximum ON time. The rising edge whose DRAIN pin voltage is equal to or more than the output voltage V_{CC} x 1.4 V (Typ) is detected and counting is started. In addition, the synchronous rectification FET will be forced OFF after the set time has elapsed.
The relationship between the resistance value (R_{MAX_TON}) and set time (t_{MAX_ON}) is described as follows:

$$t_{MAX_TON} \ [\mu s] \times 10 \ [k\Omega/\mu s] = R_{MAX_TON} \quad [k\Omega]$$

Calculation Example:
If you want to set the maximum ON time to 10μs, the value of R_{MAX_TON} is as follows:

$$10 \ [\mu s] \times 10 \ [k\Omega/\mu s] = 100 \quad [k\Omega]$$

However, the formula above is for an ideal approximation only. It is strongly advised that the operation of the actual application should be verified.
By setting this time, it becomes possible to prevent the simultaneous ON operation of the primary side and the secondary side in CCM.
The drive sequence in CCM operation is shown in the figure below:

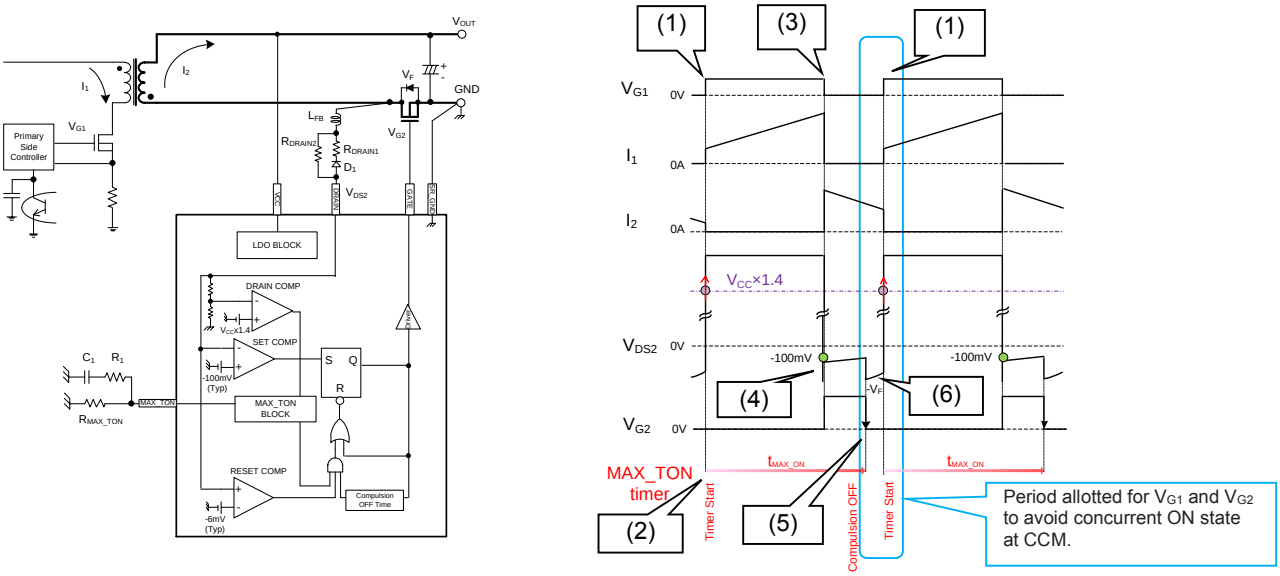


Figure 4. The drive sequence in CCM operation

(1) Primary side FET = ON. Current I_1 flows to the primary side FET. Secondary side drain voltage V_{DS2} rises.
(2) The V_{DS2} = V_{CC}×1.4 detects the rise edge of the threshold, MAX_TON timer start.
(3) Primary side FET=OFF. Current I_2 flows through the Body Diode of the secondary side FET (OFF state).
(4) Secondary side drain voltage V_{DS2}≦-100mV by current I_2, Secondary side FET=ON.
(5) Elapsed the set time in MAX_TON pin, the secondary side FET = compulsion OFF.
(6) Since the I_2 current flows through the Body Diode, V_F voltage occurs.

In order to reduce the influence of the switching noise as much as possible, capacitor C_1 and resistor R_1 in series should be connected to the MAX_TON pin. It is recommended that the capacitance be about 1000pF and the resistance value be about 1kΩ. This also serves as phase compensation of MAX_TON pin and therefore should be connected.
For quasi-resonance(QR), LLC application, this function is unnecessary because it basically does not operate in CCM. The setting method of the MAX_TON pin is invalidated by pulling up to the VCC pin.

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Description of Block – continued

5. SHUNT REGULATOR Block

It is a low consumption, high accuracy shunt regulator that controls the AC/DC output voltage. Since it is a built-in completely separate chip from the synchronous rectification chip, GND insulation is possible. Therefore, if the FET is placed on the high side, the synchronous rectification application can also make the shunt regulator the secondary side GND reference. It can also be used as a protection comparator.

6. PROTECTION Block

When protection is detected, the timer starts counting. After completion, drive the photo coupler from the SH_OUT pin to stop the primary side drive operation.

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Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
VCC Input Voltage	V_{MAX_VCC}	-0.3 to +40 *(Note 1)*	V
MAX_TON Output Voltage	$V_{MAX_MAX_TON}$	-0.3 to +V_{MAX_VCC} *(Note 1)*	V
SH_IN Input Voltage	$V_{MAX_SH_IN}$	-0.3 to +40 *(Note 2)*	V
SH_OUT Input/Output Voltage	$V_{MAX_SH_OUT}$	-0.3 to +40 *(Note 2)*	V
Gate Output Voltage	V_{MAX_GATE}	-0.3 to +15.5 *(Note 1)*	V
Drain Input Voltage	V_{MAX_DRAIN}	120 *(Note 1) (Note 3)*	V
Maximum Junction Temperature	Tjmax	+150	°C
Storage Temperature	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Reference SR_GND.

(Note 2) Reference SH_GND.

(Note 3) When a negative voltage is applied, current flows through the ESD protection device. This current value is about 6mA or less and will require a current limiting resistor to the DRAIN pin.

Thermal Resistance *(Note 4)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 6)*	2s2p *(Note 7)*	
SOP8				
Junction to Ambient	θ_{JA}	197.4	109.8	°C/W
Junction to Top Characterization Parameter *(Note 5)*	Ψ_{JT}	21	19	°C/W

(Note 4) Based on JESD51-2A(Still-Air)

(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 6) Using a PCB board based on JESD51-3.

(Note 7) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	20	32	V
Operating Temperature	Topr	-40	+25	+105	°C
MAX_TON R_{MAX_TON} Resistor Range	R_{MAX_TON}	56	-	300	kΩ
MAX_TON R_1	R_1	0.5	1	2	kΩ
MAX_TON C_1	C_1	680	1000	2200	pF

Electrical Characteristics (Unless otherwise specified V_{CC}=20V V_{SH_OUT}=20V Ta=25°C)

Parameter	Symbol	Spec			Unit	Conditions
		Min	Typ	Max		
Circuit Current						
Circuit Current1	I_{ON}	0.5	1	2	mA	f_{SW}=50kHz at Switching Mode (GATE=OPEN)
Circuit Current2	I_{ACT}	350	800	1400	µA	Switching Stop Mode
Circuit Current3	I_{OFF}	18	35	60	µA	V_{CC}=1.9V, UVLO Mode
VCC Item						
VCC UVLO Threshold Voltage1	V_{UVLO1}	2.00	2.30	2.65	V	V_{CC} Sweep Up
VCC UVLO Threshold Voltage2	V_{UVLO2}	1.95	2.25	2.60	V	V_{CC} Sweep Down
SR Controller BLOCK						
GATE Turn ON Threshold	V_{GON}	-150	-100	-50	mV	V_{DRAIN}=+300mV to -300mV
GATE Turn OFF Threshold	V_{GOFF}	-10	-6	-1	mV	V_{DRAIN}=-300mV to +300mV
Compulsion OFF Time	t_{COFF}	2.730	3.000	3.270	µs	
MAX_TON BLOCK						
MAX_TON Timer Start Threshold Voltage	$V_{MAX_ON_START}$	24	28	32	V	V_{CC}=20V Pulse Input to DRAIN Pin
MAX_TON Timer	t_{MAX_ON}	9.4	10	10.6	µs	R_{MAX_TON}=100kΩ V_{CC}=3V, V_{DRAIN}=-0.3V↔+7V
MAX_TON Output Voltage	V_{MAX_ON}	0.24	0.40	0.56	V	
Drain Monitor BLOCK						
Drain Pin Sink Current	I_{D_SINK}	130	250	550	µA	V_{DRAIN}=120V
Drain Pin Source Current1	I_{DRAIN_SO1}	-23	-11	-5	µA	V_{DRAIN}=0.1V
Drain Pin Source Current2	I_{DRAIN_SO2}	-3.0	-1	-0.3	µA	V_{DRAIN}=-0.2V
Driver BLOCK						
GATE Pin High Voltage	V_{GATE_H1}	11	12	14	V	V_{CC}=20V
High Side FET ON-Resistance1	R_{HIONR1}	12.0	23.0	50.0	Ω	V_{CC}=2.7V, I_{OUT}= -10mA
High Side FET ON-Resistance2	R_{HIONR2}	6.0	12.0	24.0	Ω	V_{CC}=5.0V, I_{OUT}= -10mA
High Side FET ON-Resistance3	R_{HIONR3}	4.0	9.0	18.0	Ω	V_{CC}=10V, I_{OUT}= -10mA
Low Side FET ON-Resistance1	$R_{LOWONR1}$	1.1	2.2	4.4	Ω	V_{CC}=2.7V, I_{OUT}= +10mA
Low Side FET ON-Resistance2	$R_{LOWONR2}$	0.9	1.8	3.6	Ω	V_{CC}=5.0V, I_{OUT}= +10mA
Delay Time GATE Pin Turn ON	t_{DELAY_ON}	-	50	-	ns	V_{DRAIN}=+300mV to -300mV
Delay Time GATE Pin Turn OFF	t_{DELAY_OFF}	-	100	-	ns	V_{DRAIN} =-300mV to +300mV

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Electrical Characteristics - continued

Parameter	Symbol	Spec			Unit	Conditions
		Min	Typ	Max		
Shunt Regulator BLOCK						
Reference Voltage	V_{SHREF}	0.796	0.800	0.804	V	V_{SH_OUT}=5V SH_OUT Sink Current=100µA
Reference Voltage Changing Ratio by Temperature	ΔV_{SHEMP}	-	-4	-	mV	V_{SH_OUT}=5V SH_OUT Sink Current=100µA Ta=+25°C to +105°C
SH_OUT Coefficient of the Reference Voltage1	ΔV_{SHREF1}	-	1	-	mV	V_{SH_OUT}=2.7V to 5V SH_OUT Sink Current=100µA
SH_OUT Coefficient of the Reference Voltage2	ΔV_{SHREF2}	-	2	-	mV	V_{SH_OUT}=5V to 20V SH_OUT Sink Current=100µA
Reference Input Current	I_{SH_IN}	-0.2	0.0	+0.2	µA	V_{SH_IN}=2V
Dynamic Impedance1	R_{SH_OUT1}	-	0.3	-	Ω	SH_OUT Sink Current =100µA to 300µA (V_{SH_OUT}=2.7V)
Dynamic Impedance2	R_{SH_OUT2}	-	0.2	-	Ω	SH_OUT Sink Current =100µA to 300µA (V_{SH_OUT}=20V)
SH_OUT Current at SH_IN=Low	I_{SH_OUT}	20	40	75	µA	V_{SH_IN}=0V, V_{SH_OUT}=5V
SH_OUT Regulation Current	$I_{SH_OUT_REG}$	1	-	-	mA	V_{SH_IN}=0.85V, V_{SH_OUT}=5V
SH_IN OVP Detection Voltage1	V_{SHI_OVP1}	0.90	1.00	1.10	V	V_{SH_IN} Sweep Up
SH_IN OVP Detection Voltage2	V_{SHI_OVP2}	0.85	0.95	1.05	V	V_{SH_IN} Sweep Down
SH_OUT OVP Detection Voltage1	V_{SHO_OVP1}	32.5	35	37.5	V	V_{SH_OUT} Sweep Up
SH_OUT OVP Detection Voltage2	V_{SHO_OVP2}	31.5	34	36.5	V	V_{SH_OUT} Sweep Down
Protection Detect Timer	$t_{PROTECTION}$	100	200	300	µs	
SH_OUT Pull Down Current at Protection Detect Mode	$I_{PROTECTION}$	1.3	2.5	5.0	mA	V_{SH_IN}=0V, V_{SH_OUT}=5V

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Typical Performance Curves

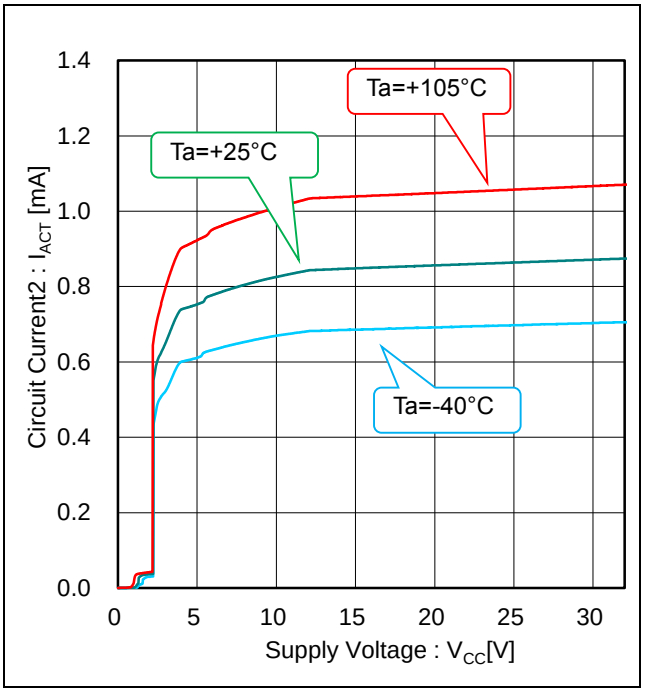


Figure 5. Circuit Current2 vs Supply Voltage
(Switching Stop Mode)

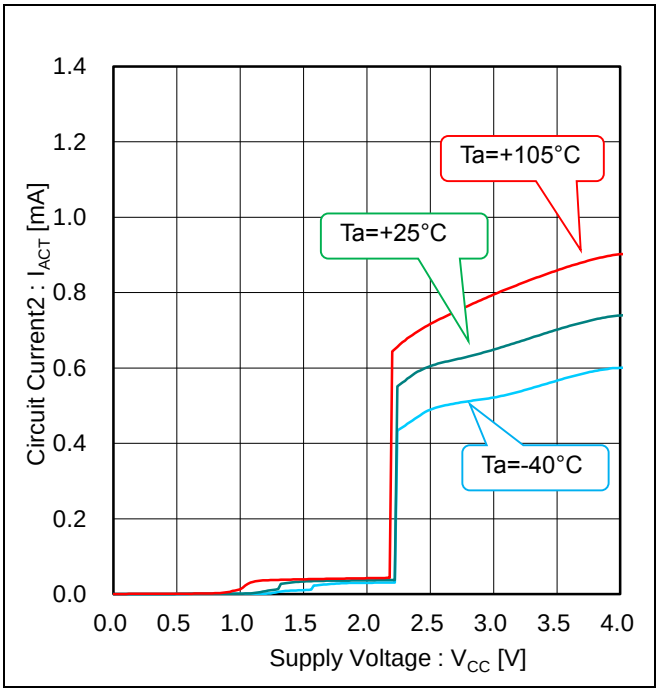


Figure 6. Circuit Current2 vs Supply Voltage
(Switching Stop Mode V_{CC} Zoom)

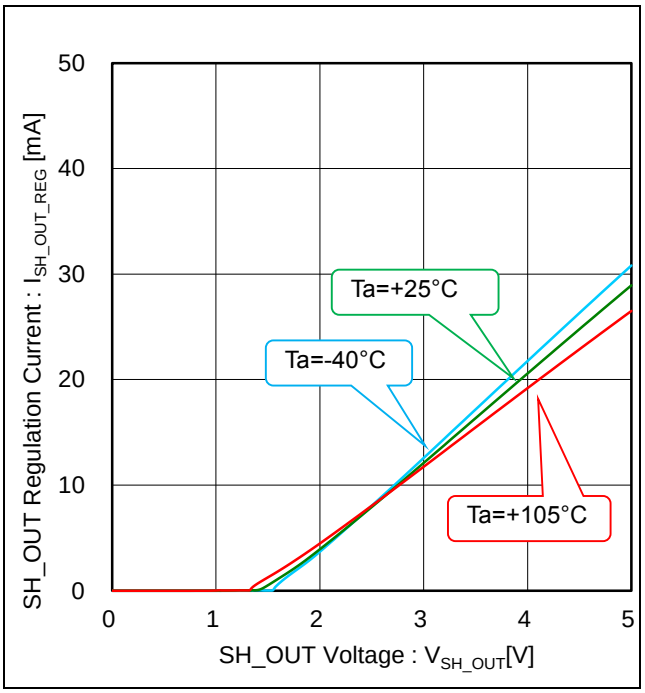


Figure 7. SH_OUT Regulation Current vs SH_OUT Voltage
(V_{SH_IN}=0.85V)

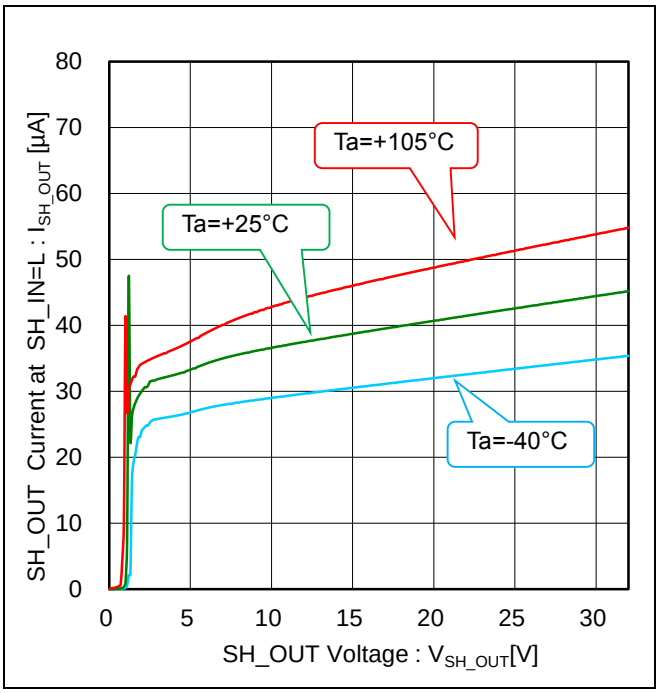


Figure 8. SH_OUT Current at SH_IN=L vs SH_OUT Voltage
(V_{SH_IN}=0V)

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Typical Performance Curves - continued

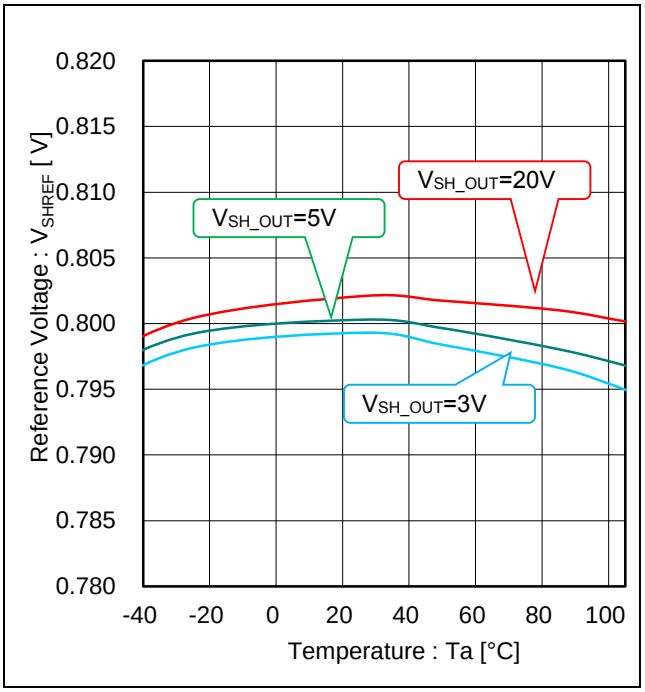


Figure 9. Reference Voltage vs Temperature
(SH_OUT Sink Current=100μA)

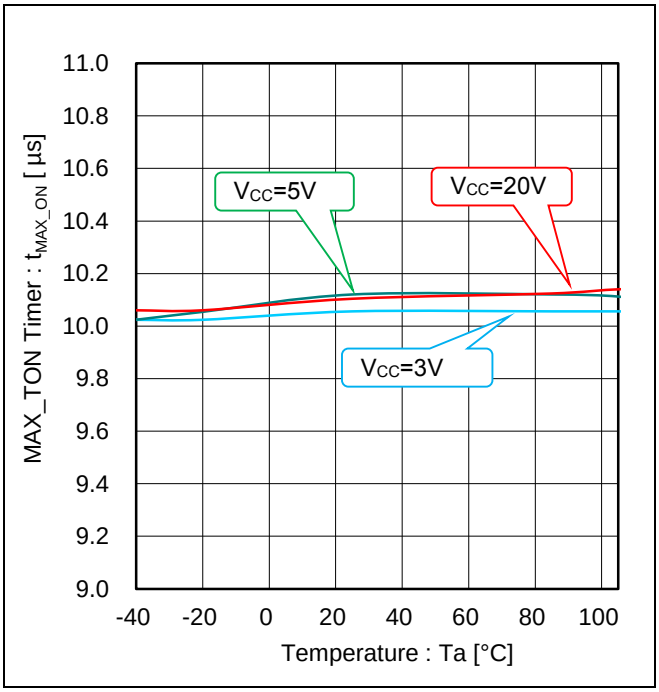


Figure 10. MAX_TON Timer vs Temperature
(R_{MAX_TON}=100kΩ, V_{DRAIN}=-0.3V↔+7V)

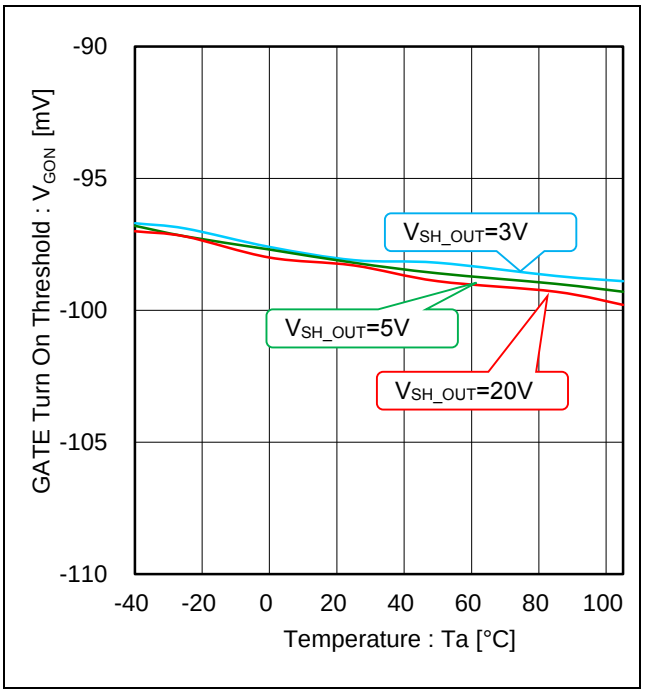


Figure 11. GATE Turn On Threshold vs Temperature
(DRAIN Sweep Down)

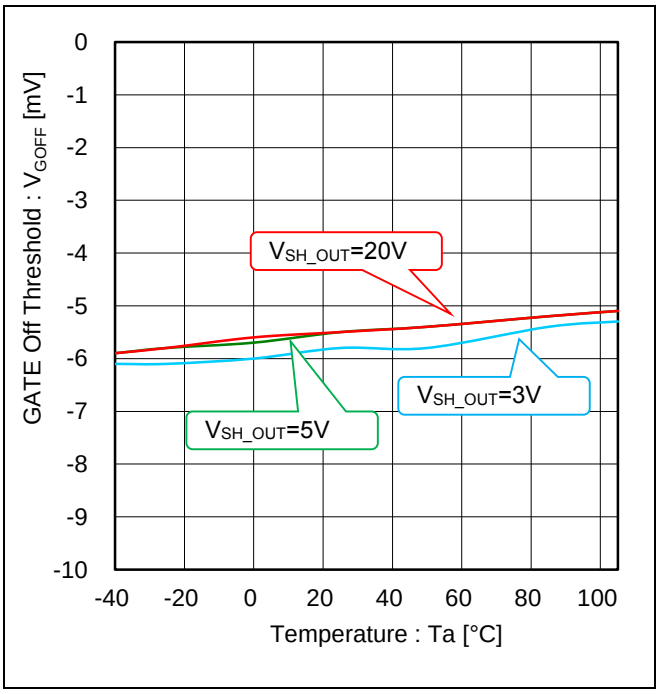


Figure 12. GATE Turn Off Threshold vs Temperature
(DRAIN Sweep Up)

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Typical Performance Curves - continued

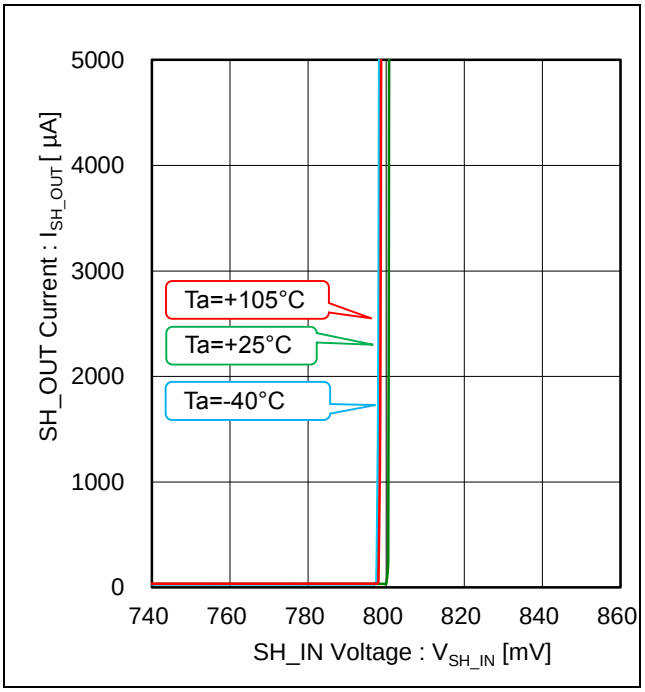


Figure 13. SH_OUT Current vs SH_IN Voltage
(V_{SH_OUT}=5V)

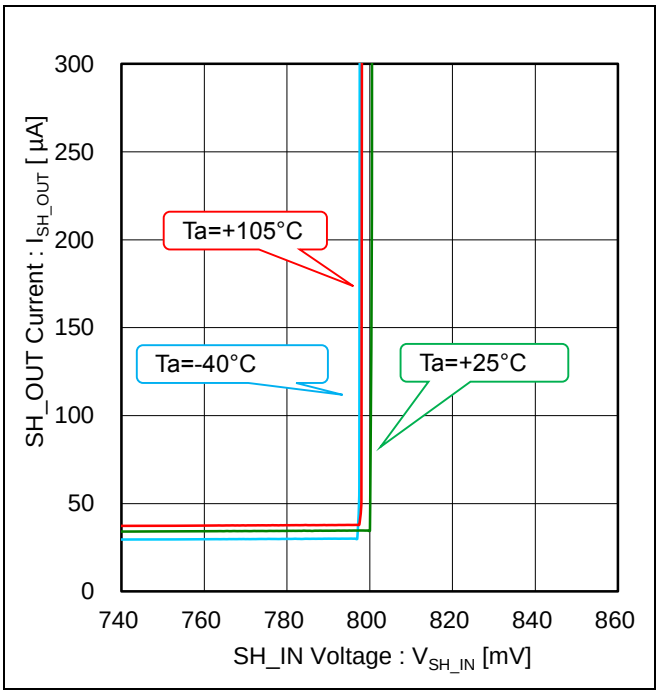


Figure 14. SH_OUT Current vs SH_IN Voltage
(V_{SH_OUT}=5V, I_{SH_OUT} ZOOM UP)

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Timing Chart

The startup sequence is shown below.

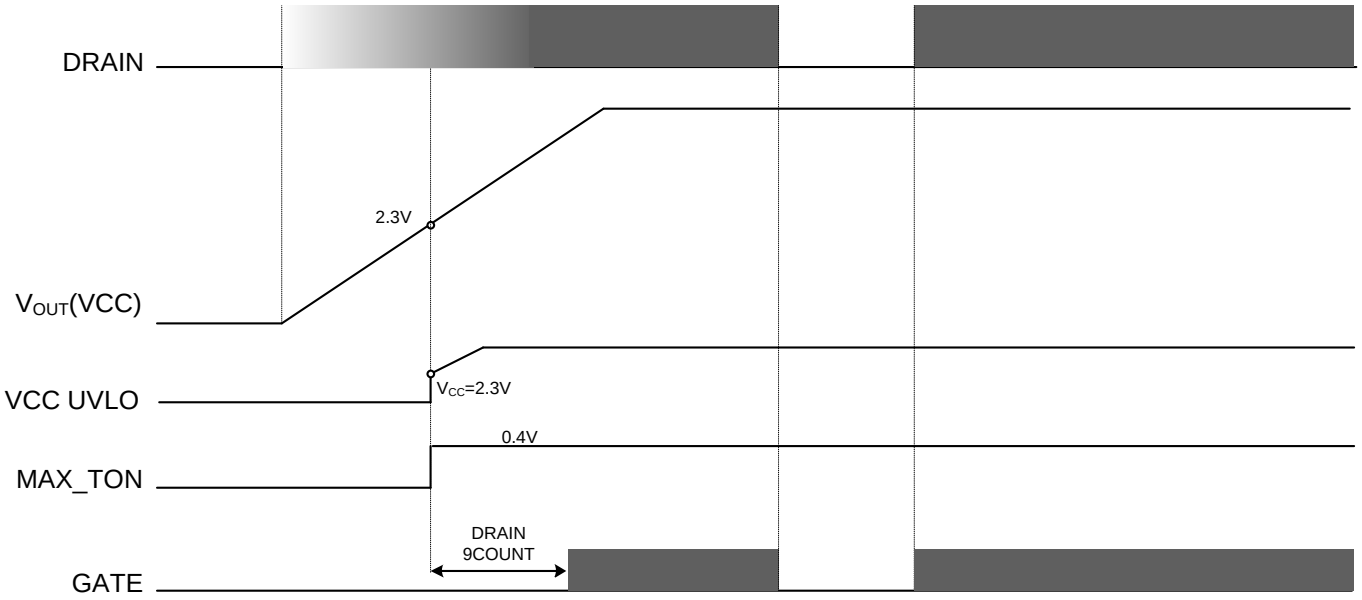


Figure 15. Startup Sequence

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Application Examples

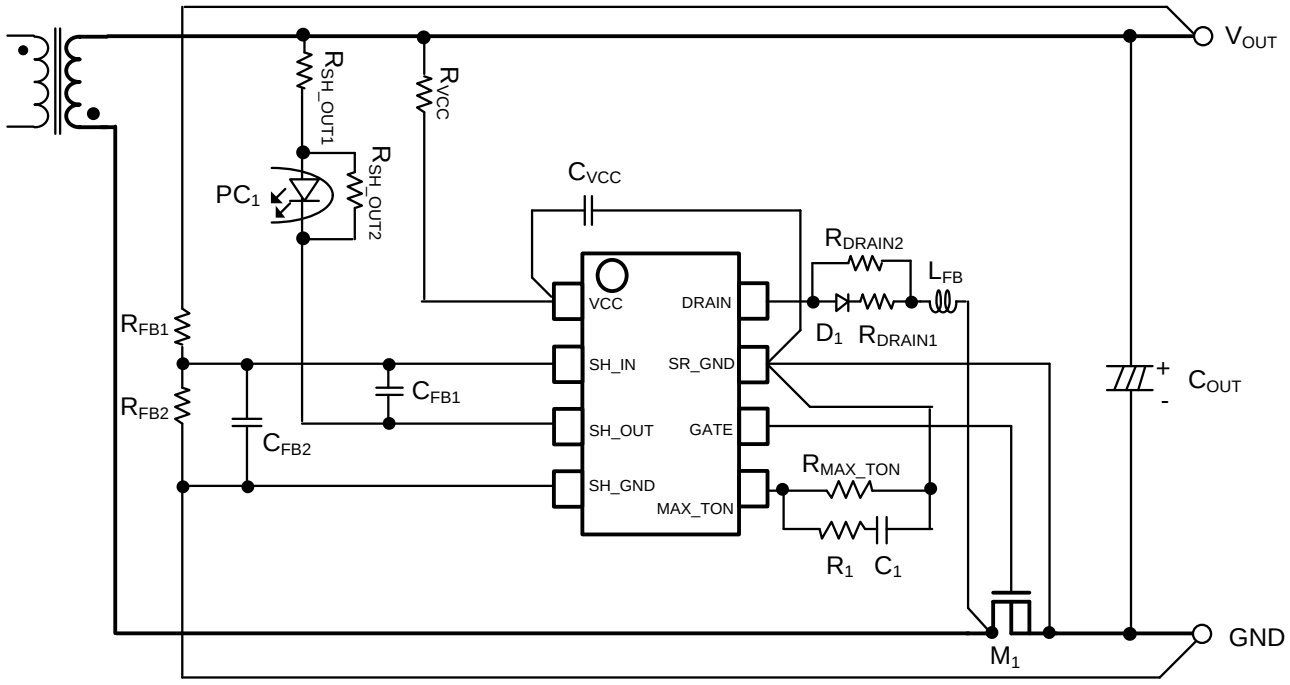


Figure 16. Flyback Application Circuit
(Low Side FET)

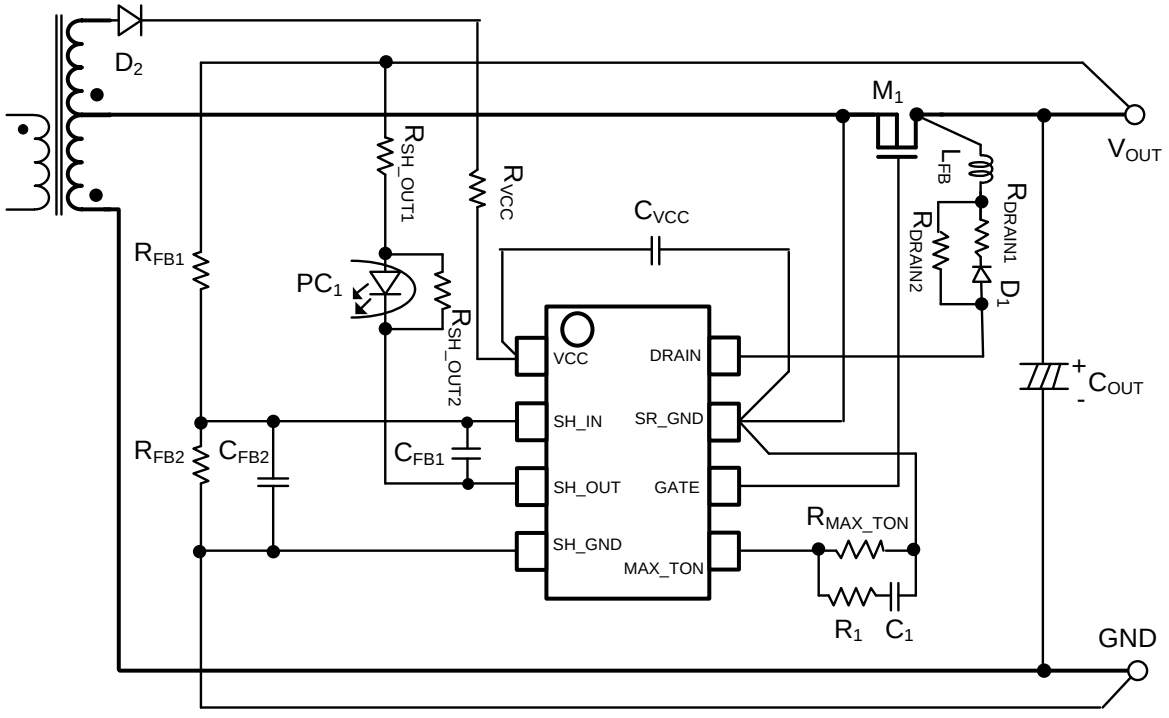


Figure 17. Flyback Application Circuit
(High Side FET)

The built-in shunt regulator block is separated in the IC from the synchronous rectification controller. Therefore, if the FET is placed on the high side, the synchronous rectification application can also make the shunt regulator the secondary side GND reference.

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Application Examples - continued

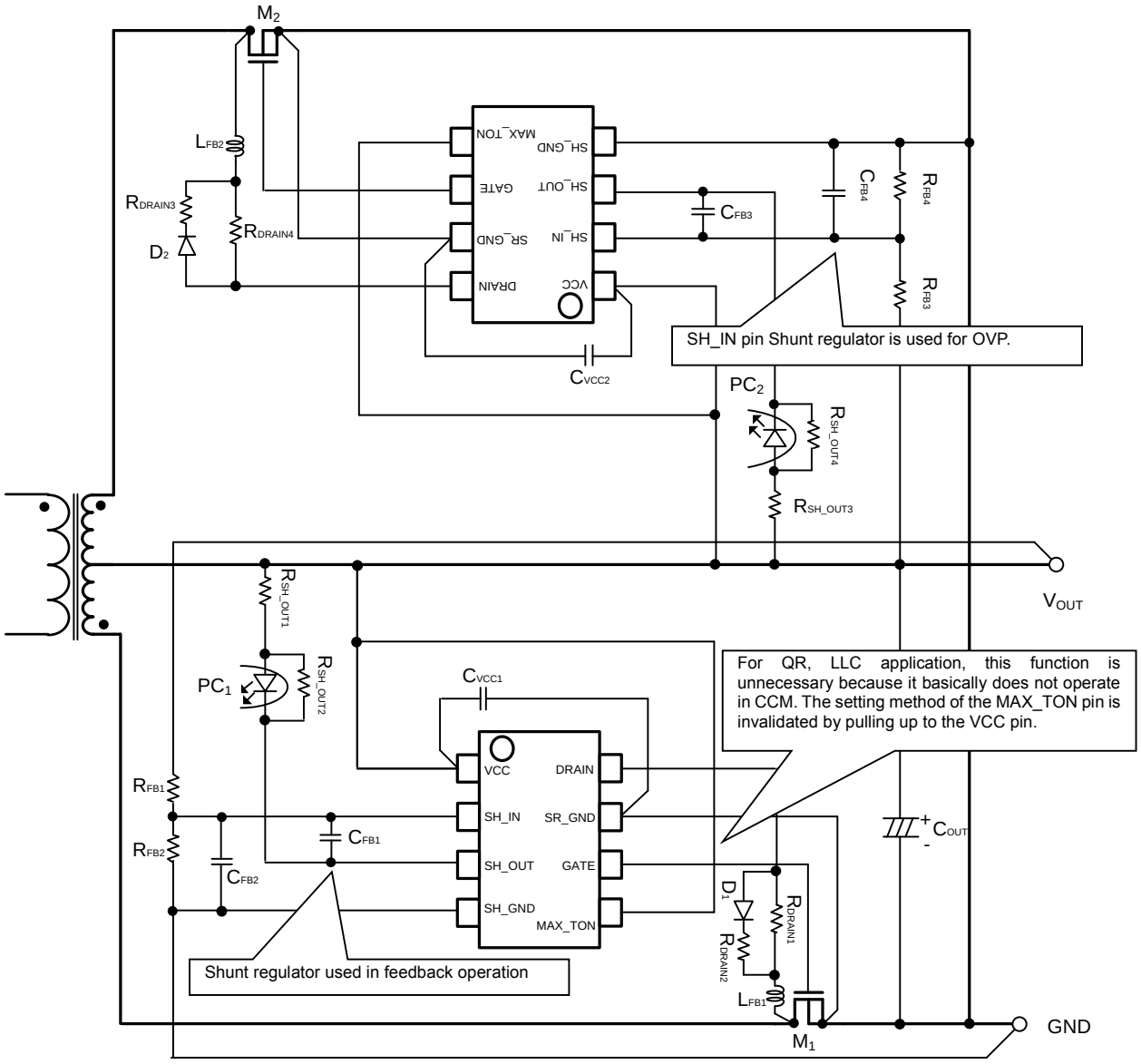


Figure 18. Resonant half-bridge application circuit

Regarding Protection Applications
The built-in shunt regulator is high voltage, low current consumption and high accuracy, and also suitable as a comparator for protection application. On the above LLC application, the shunt regulator is used as an overvoltage protection circuit.

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Selection of Components Externally Connected

1. MAX_TON Pin Setting
A resistance value which is connected to the MAX_TON pin is used to set the timer to force the GATE output OFF. (For detailed operation, please see "Description of Block Operation / MAX_TON Block")
Set timer is proportional to the resistance value which can be set in the range of 56kΩ to 300kΩ. This IC is capable of an accuracy of 10μs ± 6% at 100kΩ. However, accuracy deteriorates as the resistance value gets further away from 100kΩ. For example, 5.6μs ±0.9μs at 56kΩ, 30μs ±4.5μs at 300kΩ. (See graph below)

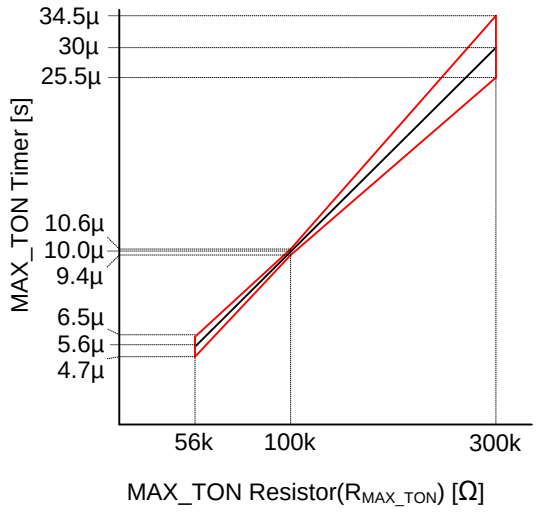


Figure 19. MAX_TON Timer vs MAX_TON Resistor

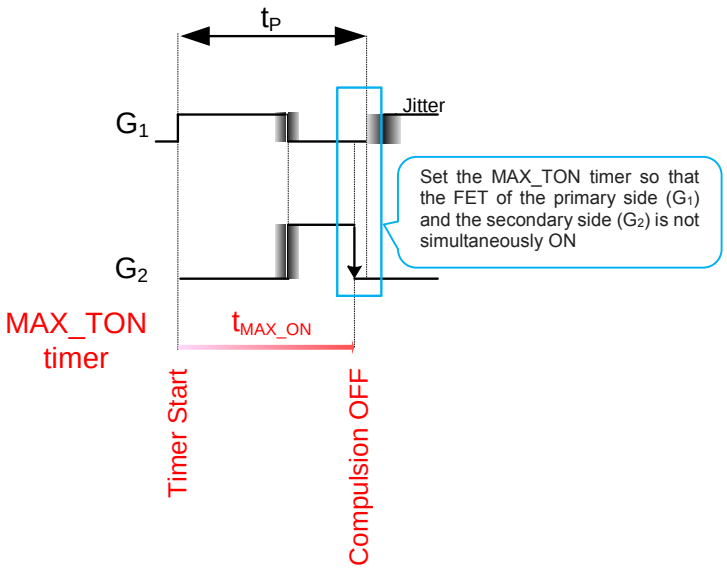


Figure 20. Primary FET and secondary FET Sequence at CCM

To prevent destruction due to surge current in CCM, set the MAX_TON timer before turning on the primary side FET (G_1) to forcibly OFF the secondary side FET (G_2). Including such variations, select a resistance value of MAX_TON Pin (R_{MAX_TON}) so that the MAX_ON timer setting time is less than one cycle in the primary side ($t_P > t_{MAX_ON}$).

$$R_{MAX_TON} < \frac{10\times10^3}{(1+\Delta t_{MAX_ON}+\Delta R+\Delta f_{MAX})\times(f_{MAX}+f_{JITTER})} \quad [k\Omega]$$

Frequency Variation Ratio

Maximum Frequency Value

where:
f_{MAX} is the primary side of the maximum frequency [kHz]
Δf_{MAX} is the primary side of the maximum frequency accuracy [%]
f_{JITTER} is the primary side of the jitter frequency [kHz]
Δt_{MAX_ON} is Secondary side MAX_TON timer time accuracy [%]
ΔR is Secondary side MAX_TON When the connection resistance accuracy [%]

2. Calculation Example

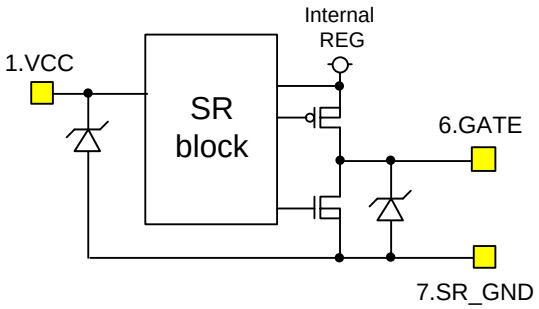
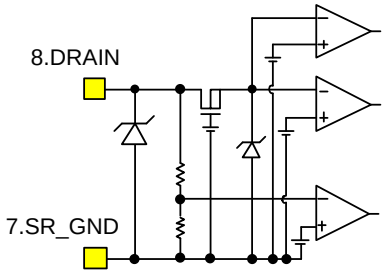
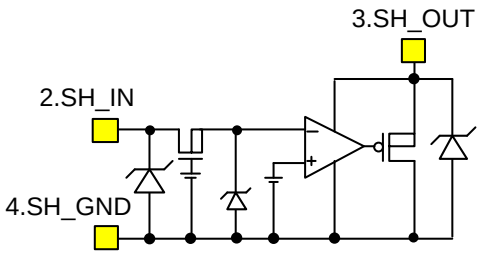
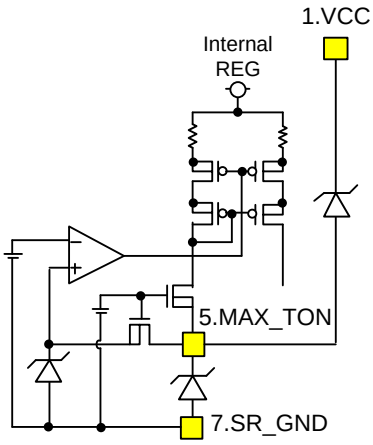
$$R_{MAX_TON} < \frac{10\times10^3}{(1+0.06+0.01+0.05)\times(100+8)} = 82.67 \quad [k\Omega]$$

f_{MAX} is the primary side of the maximum frequency 100[kHz]
Δf_{MAX} is the primary side of the maximum frequency accuracy 5[%]
f_{JITTER} is the primary side of the jitter frequency 8[kHz]
Δt_{MAX_ON} is Secondary side MAX_TON timer time accuracy 6[%]
ΔR is Secondary side MAX_TON When the connection resistance accuracy 1[%]

With these conditions, MAX_TON Resistor(R_{MAX_TON}) should be set to 82kΩ or less. In addition, it is recommended that the temperature characteristics of each component should also be taken into account.

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I/O Equivalence Circuits

Pin 1: VCC / Pin 6: GATE / Pin 7: SR_GND	Pin 8: DRAIN
	
Pin 2: SH_IN / Pin 3: SH_OUT / Pin 4: SH_GND	**Pin 5: MAX_TON**
	

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Notes on the Layout

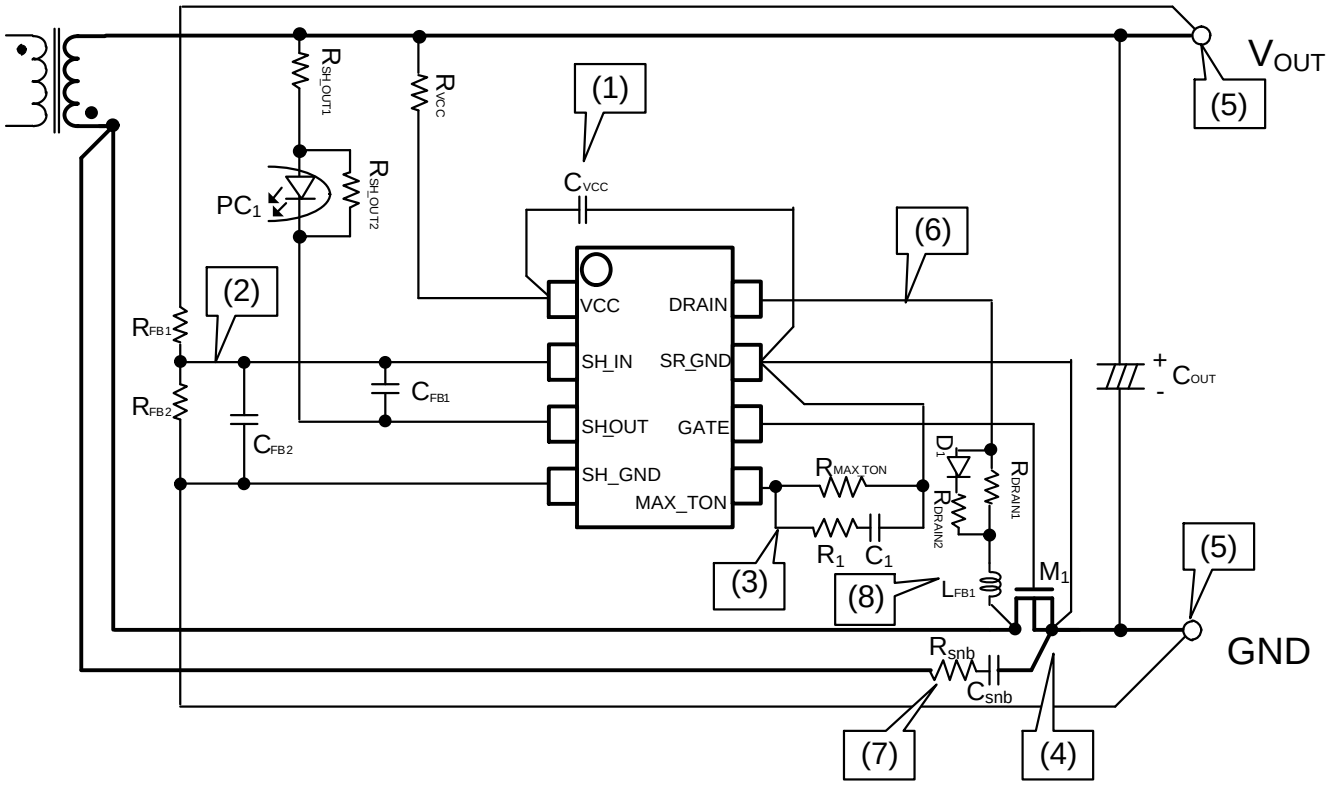


Figure 21. Flyback Application Circuit
(Low Side FET)

(1) VCC line may malfunction under the influence of switching noise.
Therefore, it is recommended to insert a capacitor C_{VCC} between the VCC and SR_GND pin.
(2) SH_IN pin is a high impedance line. To avoid crosstalk, electrical wiring should be as short as possible and not in parallel with the switching line.
(3) MAX_TON pin has a 0.4V output. Therefore, there is a possibility that compulsion OFF time may be affected by the switching operation, we recommend connecting R_{MAX_TON}, R_1, C_1 just before MAX_TON pin output as much as possible and connecting to SR_GND pin with independent wiring as much as possible. It is also recommended to use an independent electrical wiring in connection with SR_GND pin.
(4) The synchronous rectification controller IC must accurately monitor the V_{DS} generated in the FET. Accordingly, the electrical wiring between the DRAIN to DRAIN and SR_GND to SOURCE of the IC and FET respectively **should be connected independently.**
(5) The feedback resistors of V_{OUT} are recommended to be connected to the GND of the output with an independent electrical wiring.
(6) The DRAIN pin is a switching line. Use a narrow wiring and connect as short as possible.
(7) Use an independent wiring if connecting a snubber circuit between the DS of the FET. The connection of the transformer output and the SOURCE of the FET should be thick and short as possible.
(8) Due to the DRAIN pin detects the small voltage, a malfunction which the switch turns ON/OFF caused by the surge voltage may occur. So that, the filters such as the ferrite bead are recommended for alleviating the surge voltage.

Configuration example*(Note 8)*:
L_{FB1} (a ferrite bead for suppressing the surge voltage): MMZ1608S202ATA00(TDK)
D_1 (a schottky barrier diode): RB751G-40(ROHM)
R_{DRAIN1} (a filter resistor for the FET turn off): 0.3kΩ to 2kΩ
R_{DRAIN2} (a current limiting resistor to the DRAIN pin): 150Ω

(Note 8) The value is not a guaranteed value, but for reference. Please choose the optimum values of the components after sufficient evaluations based on the actual application.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

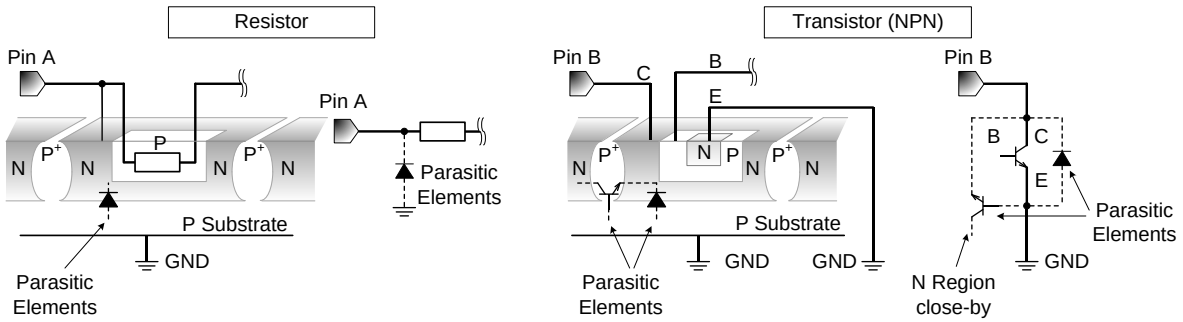


Figure 22. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

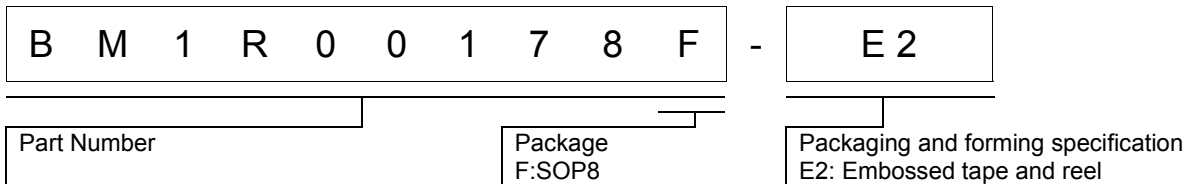
Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit (TSD)

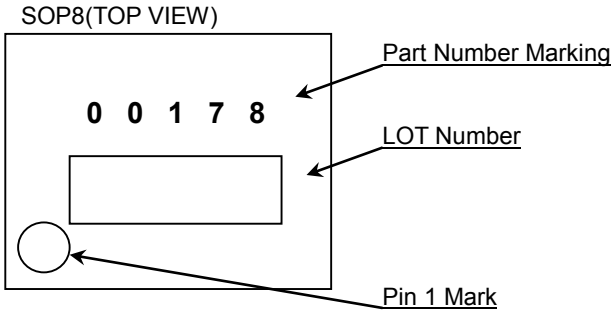
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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Ordering Information



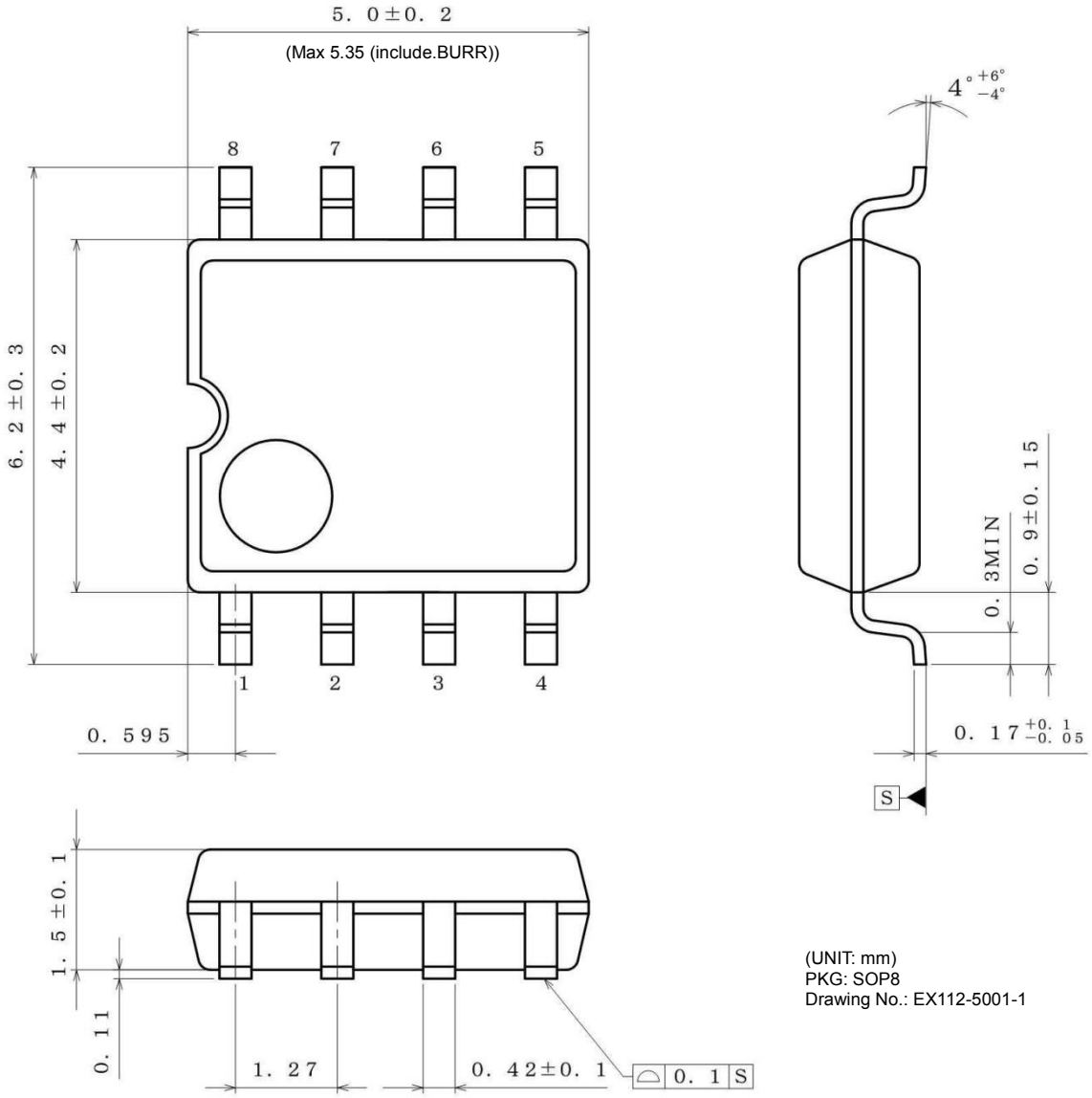
Marking Diagram



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Physical Dimension and Packing Information

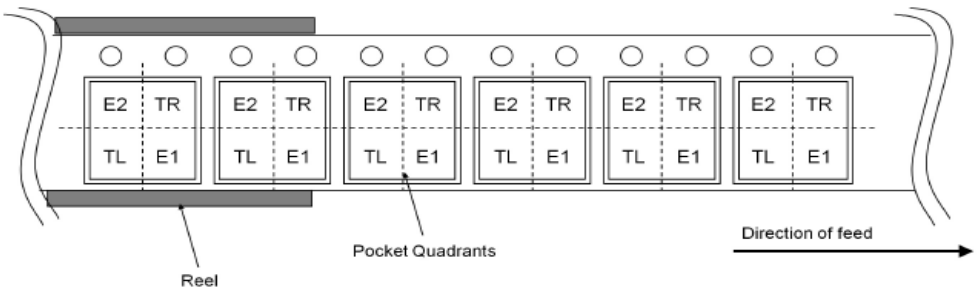
Package Name	SOP8



(UNIT: mm)
PKG: SOP8
Drawing No.: EX112-5001-1

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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Revision History

Date	Revision	Changes
06.Feb.2018	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BM1R00178F - Web Page

Part Number	BM1R00178F
Package	SOP8
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes