FAIRCHILD SEMICONDUCTOR TM

September 1996

# NDT014

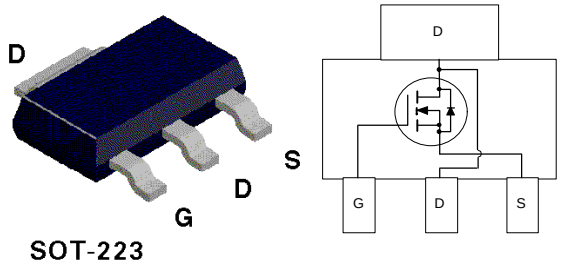
## N-Channel Enhancement Mode Field Effect Transistor

### General Description

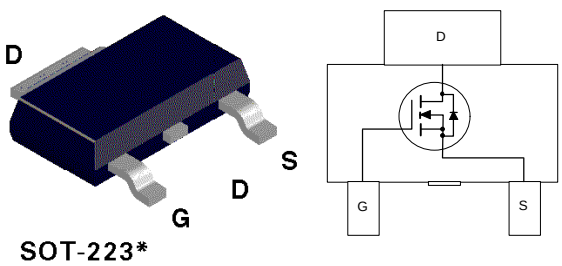
Power SOT N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

### Features

- 2.7A, 60V. $R_{DS(ON)}$ = 0.2Ω @ $V_{GS}$ = 10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.




SOT-223




SOT-223*
(J23Z)

## Absolute Maximum Ratings

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | NDT014 | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 60 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | ±2.7 | A |
| | - Pulsed | | ±10 | |
| $P_D$ | Maximum Power Dissipation | (Note 1a) | 3 | W |
| | | (Note 1b) | 1.3 | |
| | | (Note 1c) | 1.1 | |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | | -65 to 150 | °C |
| **THERMAL CHARACTERISTICS** | | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 42 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 12 | °C/W |

* Order option J23Z for cropped center drain lead.

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## Electrical Characteristics ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 60 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | | 25 | µA |
| | | $V_{DS}$ = 48 V, $V_{GS}$ = 0 V, $T_J$=125°C | | | 250 | µA |
| $I_{GSSF}$ | Gate - Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate - Body Leakage, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 1.6 A | | 0.18 | 0.2 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 25 V, $I_D$ = 1.6 A | | 2 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 155 | | pF |
| $C_{oss}$ | Output Capacitance | | | 60 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 15 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{D(on)}$ | Turn - On Delay Time | $V_{DD}$ =30 V, $I_D$ = 10 A, $V_{GEN}$ = 10 V, $R_{GEN}$ = 24 Ω | | 10 | 20 | ns |
| $t_r$ | Turn - On Rise Time | | | 64 | 100 | ns |
| $t_{D(off)}$ | Turn - Off Delay Time | | | 10 | 20 | ns |
| $t_f$ | Turn - Off Fall Time | | | 10 | 20 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 48 V, $I_D$ = 10 A, $V_{GS}$ = 10 V | | 5 | 11 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 1.2 | 3.1 | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 2 | 5.8 | nC |

## Electrical Characteristics ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 2.7 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | | | 22 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.7A (Note 2) | | 0.95 | 1.6 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_F$ = 10 A, $dI_F/dt$ = 100 A/µs | | | 140 | ns |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

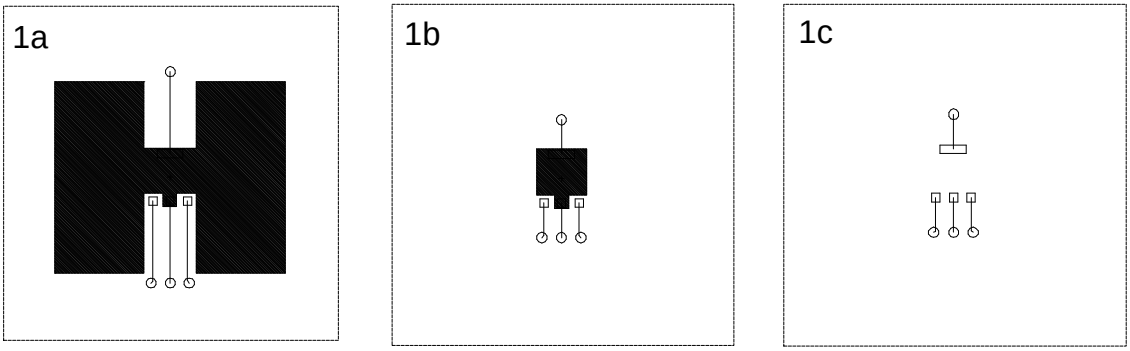
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 42°C/W when mounted on a 1 $in^2$ pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 $in^2$ pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 $in^2$ pad of 2oz copper.




Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

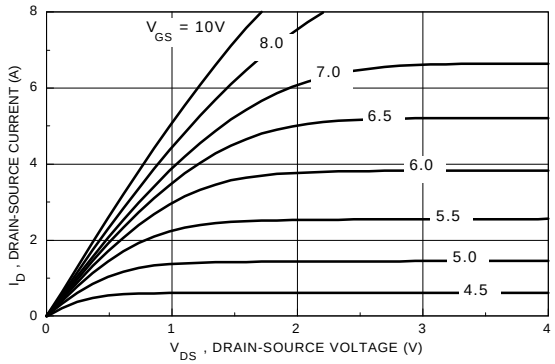



**Figure 1. On-Region Characteristics.**

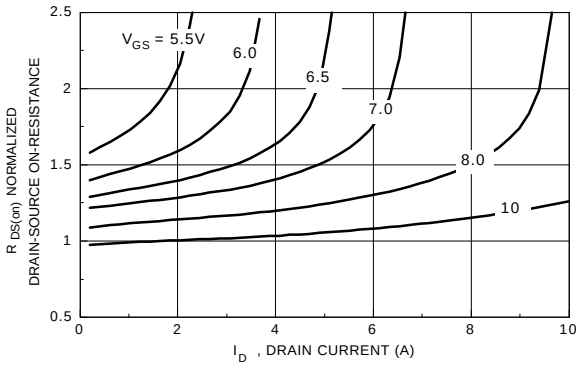



**Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.**

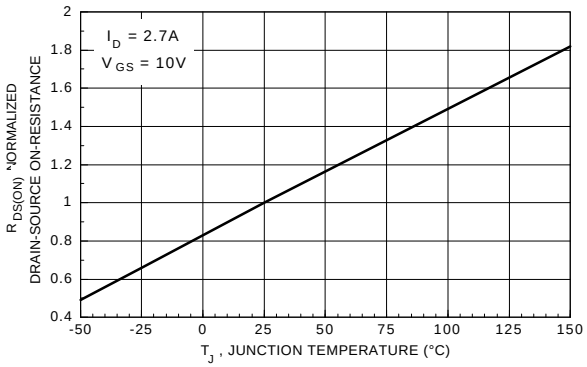



**Figure 3. On-Resistance Variation with Temperature.**

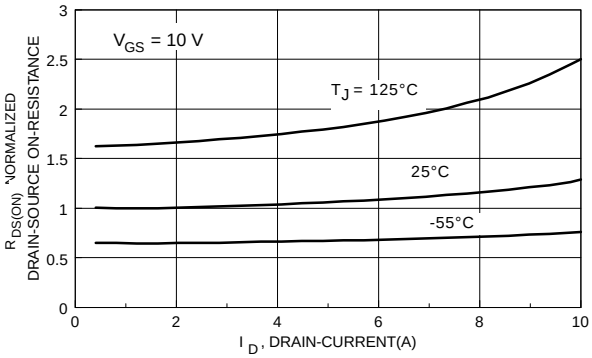



**Figure 4. On-Resistance Variation with Drain Current and Temperature.**

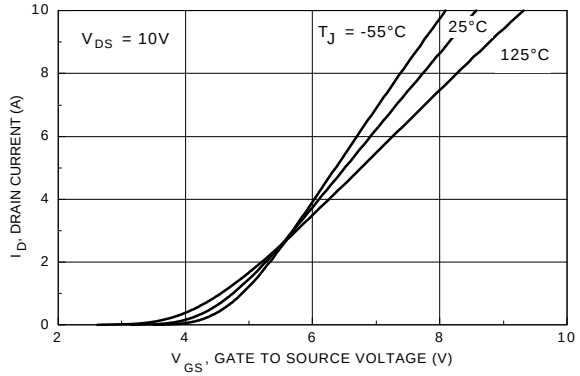



**Figure 5. Transfer Characteristics.**

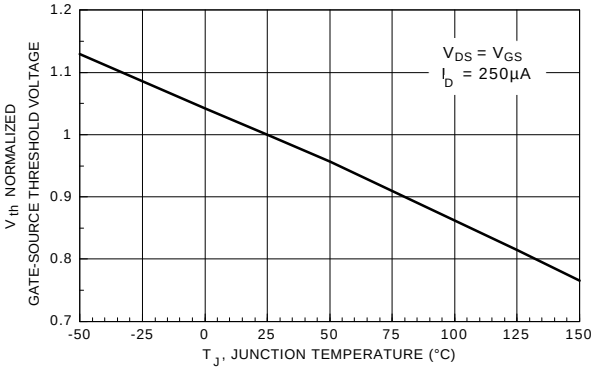



**Figure 6. Gate Threshold Variation with Temperature.**

## Typical Electrical Characteristics (continued)

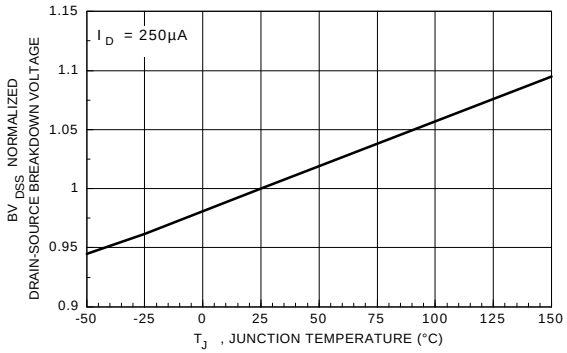



**Figure 7. Breakdown Voltage Variation with Temperature.**

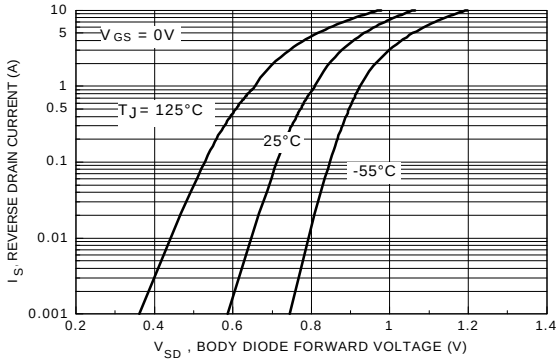



**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.**

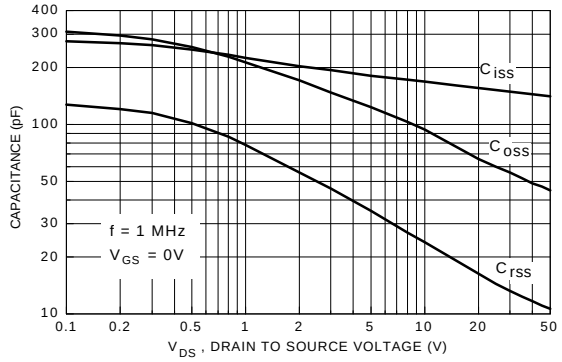



**Figure 9. Capacitance Characteristics.**

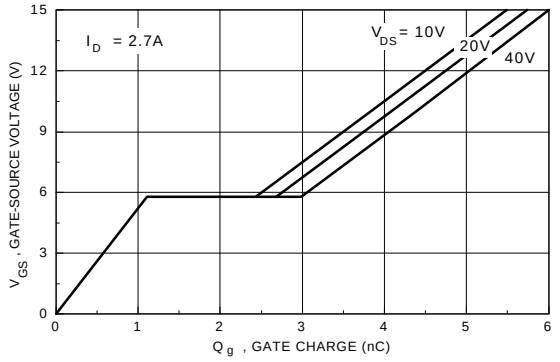



**Figure 10. Gate Charge Characteristics.**

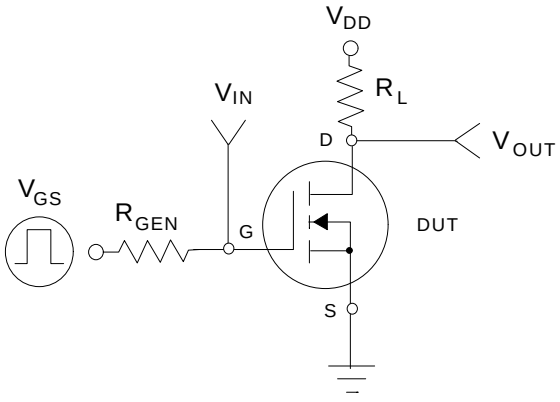



**Figure 11. Switching Test Circuit.**

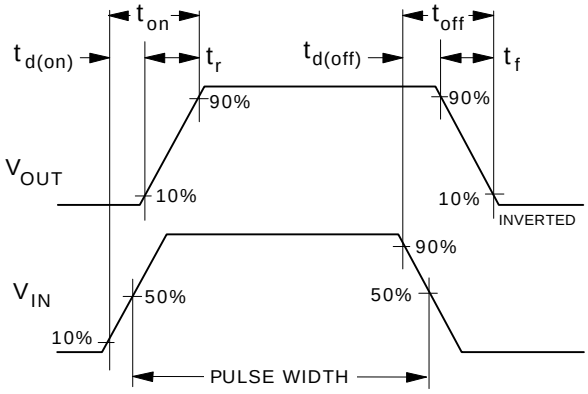



**Figure 12. Switching Waveforms.**

## Typical Electrical Characteristics (continued)

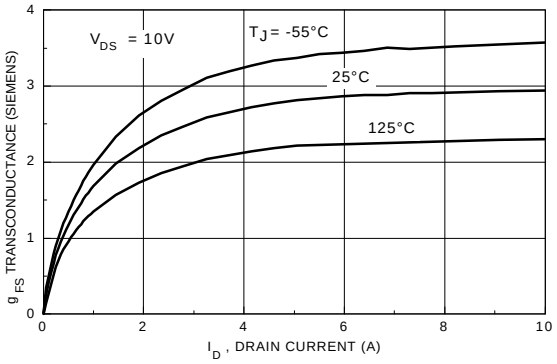



**Figure 13. Transconductance Variation with Drain Current and Temperature.**

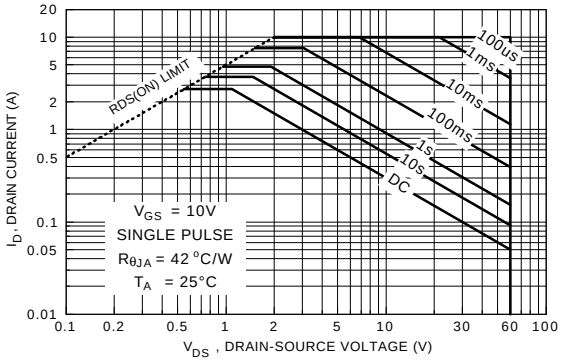



**Figure 14. Maximum Safe Operating Area.**

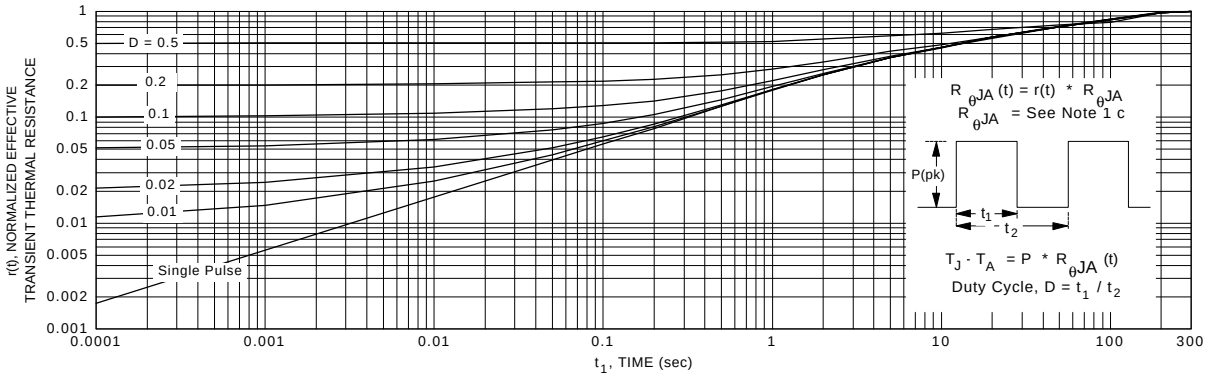


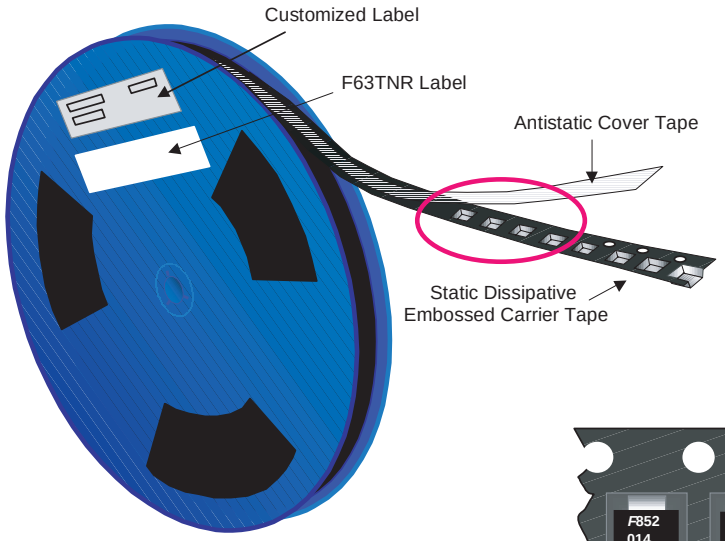

**Figure 15. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

# SOT-223 Tape and Reel Data and Package Dimensions

FAIRCHILD SEMICONDUCTOR™

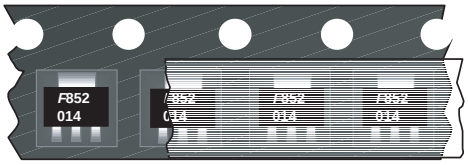
## SOT-223 Packaging Configuration: Figure 1.0




**Packaging Description:**

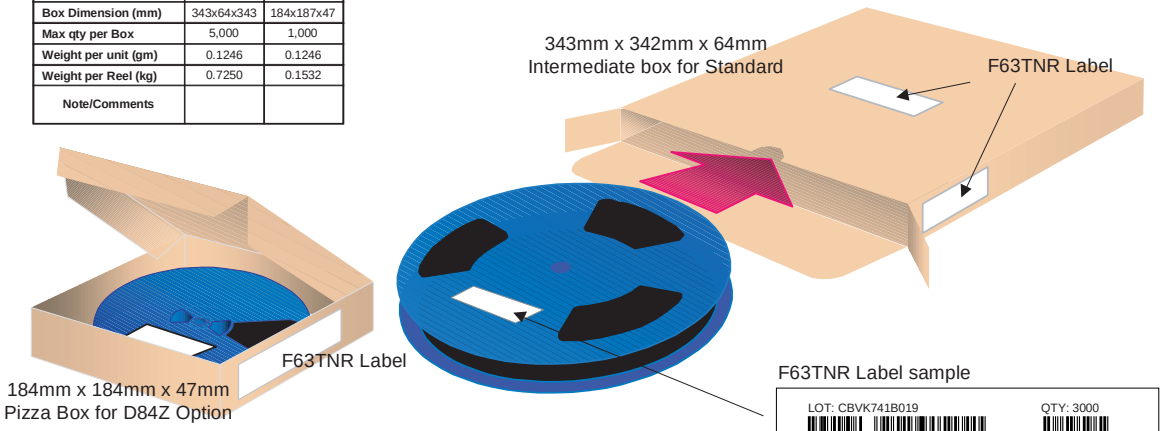
SOT-223 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

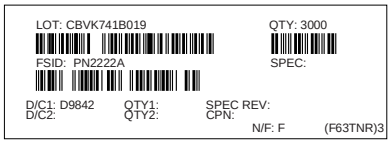



**SOT-223 Unit Orientation**

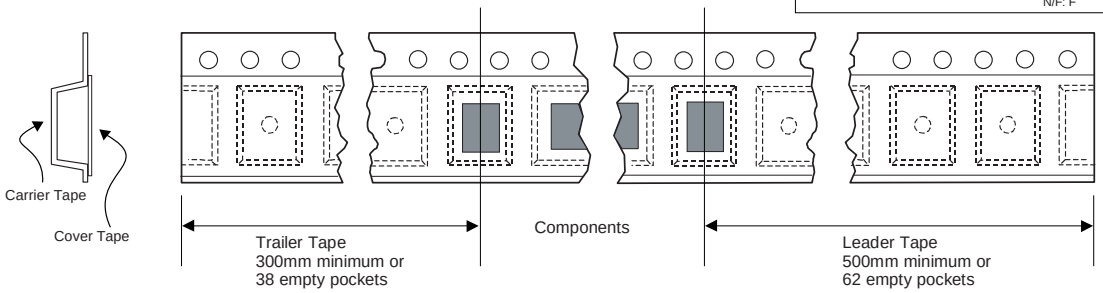
| SOT-223 Packaging Information | | |
|---|---|---|
| **Packaging Option** | Standard (no flow code) | D84Z |
| **Packaging type** | TNR | TNR |
| **Qty per Reel/Tube/Bag** | 2,500 | 500 |
| **Reel Size** | 13" Dia | 7" Dia |
| **Box Dimension (mm)** | 343x64x343 | 184x187x47 |
| **Max qty per Box** | 5,000 | 1,000 |
| **Weight per unit (gm)** | 0.1246 | 0.1246 |
| **Weight per Reel (kg)** | 0.7250 | 0.1532 |
| **Note/Comments** | | |




F63TNR Label sample

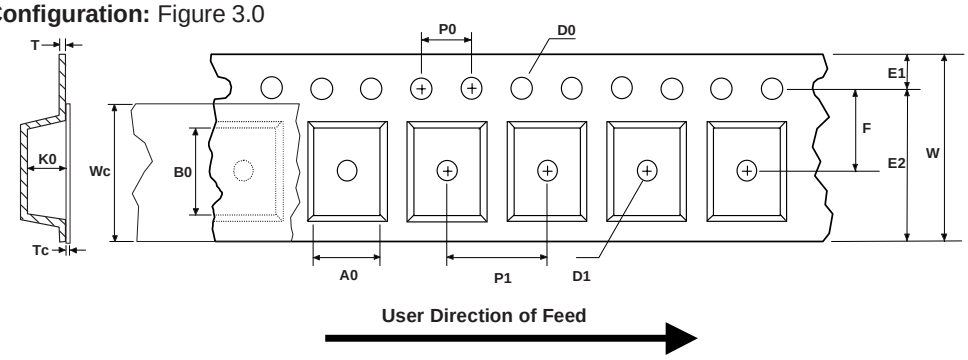



## SOT-223 Tape Leader and Trailer Configuration: Figure 2.0



# SOT-223 Tape and Reel Data and Package Dimensions, continued

**SOT-223 Embossed Carrier Tape**
**Configuration:** Figure 3.0

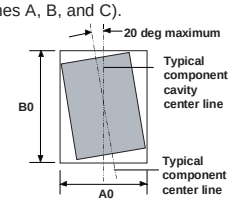



| Dimensions are in millimeter | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pkg type** | **A0** | **B0** | **W** | **D0** | **D1** | **E1** | **E2** | **F** | **P1** | **P0** | **K0** | **T** | **Wc** | **Tc** |
| **SOT-223** (12mm) | 6.83 +/-0.10 | 7.42 +/-0.10 | 12.0 +/-0.3 | 1.55 +/-0.05 | 1.50 +/-0.10 | 1.75 +/-0.10 | 10.25 min | 5.50 +/-0.05 | 8.0 +/-0.1 | 4.0 +/-0.1 | 1.88 +/-0.10 | 0.292 +/- 0.0130 | 9.5 +/-0.025 | 0.06 +/-0.02 |

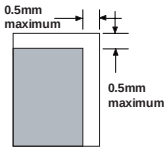
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).




Sketch A (Side or Front Sectional View)
**Component Rotation**

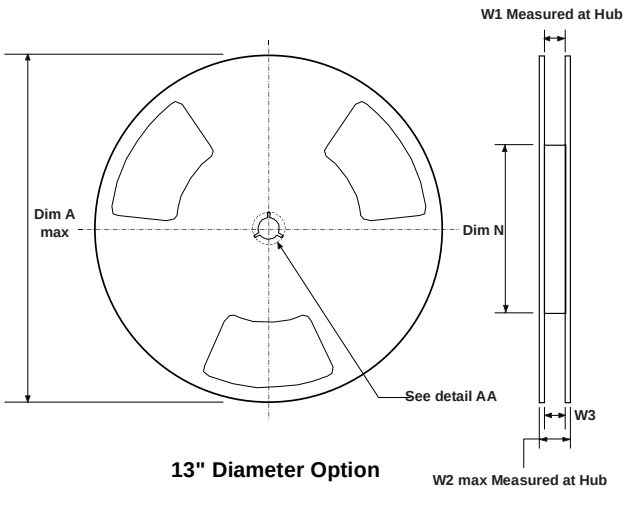



Sketch B (Top View)
**Component Rotation**

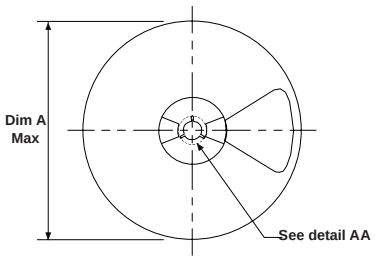



Sketch C (Top View)
**Component lateral movement**

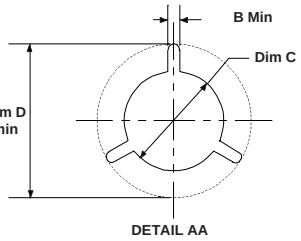
**SOT-223 Reel Configuration:** Figure 4.0




**13" Diameter Option**




**7" Diameter Option**

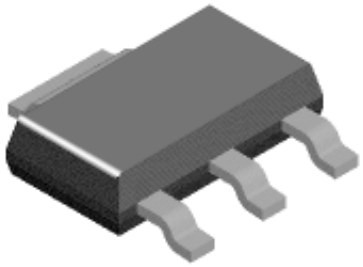


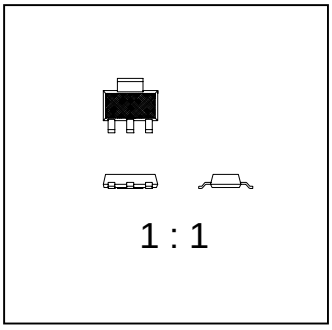

**DETAIL AA**

| Dimensions are in inches and millimeters | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Tape Size** | **Reel Option** | **Dim A** | **Dim B** | **Dim C** | **Dim D** | **Dim N** | **Dim W1** | **Dim W2** | **Dim W3 (LSL-USL)** |
| 12mm | 7" Dia | 7.00 177.8 | 0.059 1.5 | 512 +0.020/-0.008 13 +0.5/-0.2 | 0.795 20.2 | 5.906 150 | 0.488 +0.078/-0.000 12.4 +2/0 | 0.724 18.4 | 0.469 – 0.606 11.9 – 15.4 |
| 12mm | 13" Dia | 13.00 330 | 0.059 1.5 | 512 +0.020/-0.008 13 +0.5/-0.2 | 0.795 20.2 | 7.00 178 | 0.488 +0.078/-0.000 12.4 +2/0 | 0.724 18.4 | 0.469 – 0.606 11.9 – 15.4 |

## SOT-223 Tape and Reel Data and Package Dimensions, continued

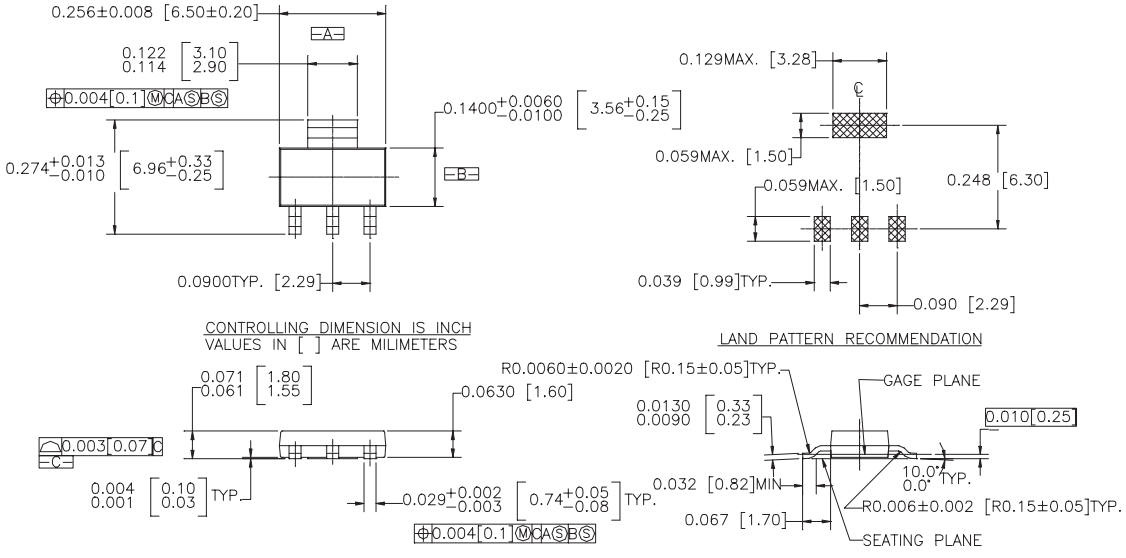
# SOT-223 (FS PKG Code 47)






Scale 1:1 on letter size paper

Part Weight per unit (gram): 0.1246




NOTES : UNLESS OTHERWISE SPECIFIED
1. STANDARD LEAD FINISH TO BE 150 MICROINCHES/ 3.81 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.
2. REFERENCE JEDEC REGISTRATION TO−261, VARIATION AA, ISSUE A, DATED JAN 1990

SOT223, 4 LEADS

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FACT Quiet Series™
FAST®
FASTr™
GTO™
HiSeC™
ISOPLANAR™
MICROWIRE™
POP™
PowerTrench™
QFET™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
TinyLogic™
UHC™
VCX™

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |