Data Sheet of RL508
FM Tuner

Revision History

Version	Content	Effective Date
0.1	Initial version	2014/03/11

General Description

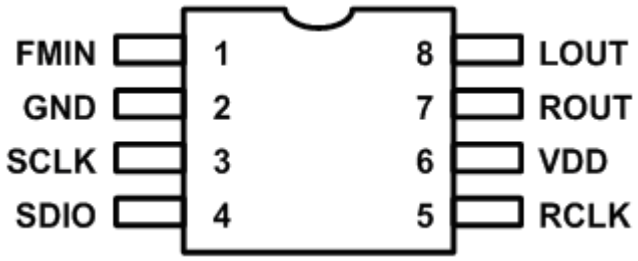
The RL508 is a single-chip broadcast FM stereo radio tuner with fully integrated building blocks as LNA, VCO with digital synthesizer, digital channel selection filter, digital FM demodulator and MPX decoder. The RL508 integrates the tuner function from antenna input to stereo audio output for worldwide European, US, Japanese and China FM bands. The FM tuner only requires a minimum amount of small and low cost external components to be a very attractive solution for portable devices. With a powerful audio engine, the RL508 is able to deliver optimum sound quality under hostile channel conditions.

Features

- Worldwide FM band support (64–108 MHz)
- Digital frequency synthesizer
- On-chip VCO
- On-chip loop filter
- Autonomous search tuning
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- Signal strength measurement
- Programmable de-emphasis (50/75 μs)
- Digital adaptive noise suppression
- Volume control
- 32.768 kHz, 12M, 24M, 13M, 26M, 19.2M, 38.4MHz reference clock
- 2-wire control interface
- 2.0 V to 3.6 V supply voltage
- Integrated LDO regulator
- SOP-8 package
- Pb-free / RoHS compliant
- Integrated crystal oscillator
- Built in audio amp for 32ohm load

Applications

- Headphones
- MP3, MP4 players
- Portable radios
- PDA
- Notebook PC
- Gift



Reference

- RL508 EVB Quick Start Guide
- RL508 Programming Guide
- RL508 EVB User's Guide

1. Functional Description

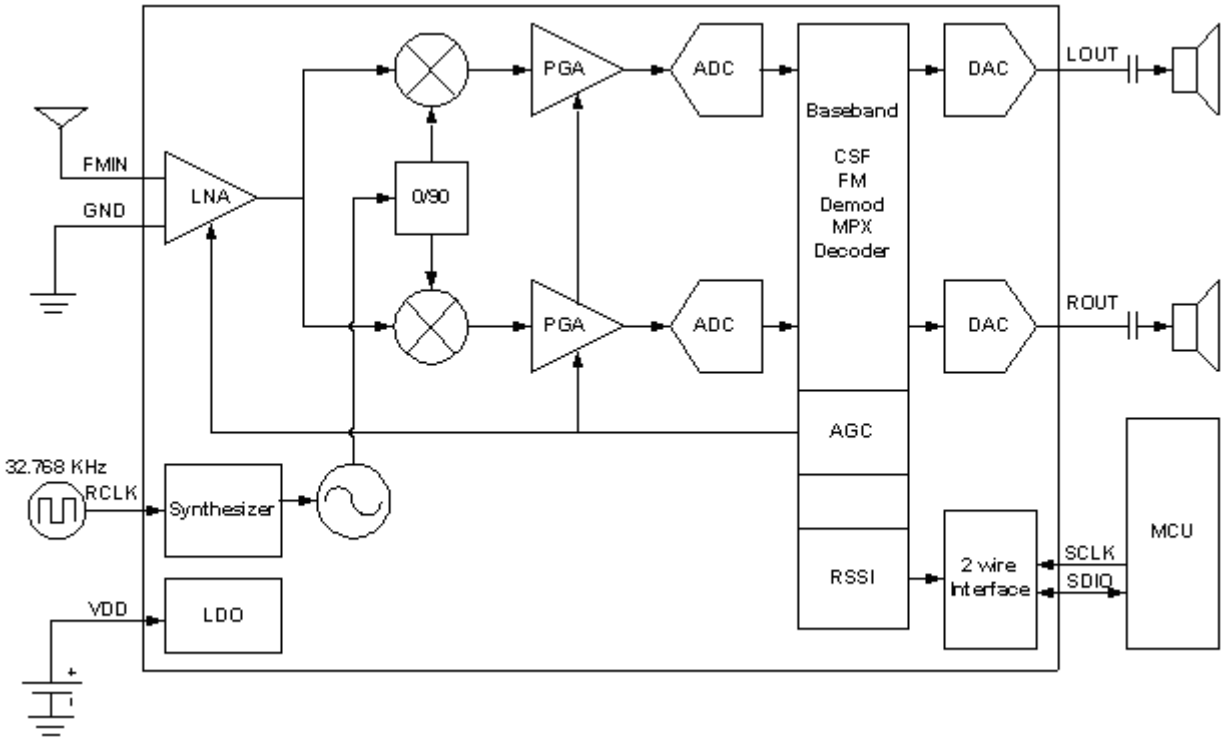


Figure 1. RL508 FM receiver block diagram

1.1. Overview

The RL508 is a monolithic FM receiver. It requires only one external bypass capacitor to minimize BOM cost and design easily for the miniature application.

The RL508 supports only 2-wire interface. With an integrated regulator, it doesn't need an external regulator, and it is allowed to directly supply 2.0 to 3.6 V from battery.

1.2. FM Receiver

It uses optimized system architecture to lower the system cost and area, and recover FM broadcast signal with low power consumption and to eliminate environmental noise with audio algorithm such as soft-mute and stereo-blending.

It integrates a low-noise amplifier (LNA), an automatic gain control (AGC) circuit, a quadrature mixer, two programmable amplifiers (PGA), a pair of analog to digital converters (ADCs). The LNA supports FM broadcast band (64MHz~108MHz). The AGC controls the gain of the LNA and PGA to adjust the input power to optimum signal level for demodulation automatically. Proceeded by LNA, the quadrature mixer down-converts the RF signal to IF signal. The IF signal is amplified, filtered, digitized, and then passed to a baseband processor to perform FM demodulation. A MPX decoder provides stereo digital audio signals to a pair of digital to analog converters (DACs) for generating high-quality stereo analog sound. The RL508 also integrates a frequency synthesizer and a voltage controlled oscillator (VCO). Reference clock of synthesizer is 32.768 kHz, which can be provided by an external clock source or build-in clock oscillator with off-chip crystal.

1.3. Audio Processing

Switching from stereo to mono to limit the output noise is automatically performed by MPX decoder. The blending process from stereo to mono occurs when signal level reaches the threshold which is defined in register bits CSR0_BLNDADJUST[1:0] +CSR0_BLNDOFS[3:0]. Stereo/mono status is shown in the register bit ST. Mono operation can be forced by register bit CSR0_MONO.

A 19 kHz pilot notch filter is implemented to eliminate the distortion from 19 kHz pilot tone for some audio analyzer.

High-frequency interferences and noise can be reduced by pre-emphasis and de-emphasis technology to improve SNR. Since the high audio frequency is accentuated by pre-emphasis universally when FM signal is transmitted, the received FM signal is applied to attenuate high audio frequency using a de-emphasis filter. The CSR0_DEEM bit can be programmed for either 50 or 75us for de-emphasis time constant.

The audio output may be muted by CSR0_DIS_MUTE bit. Volume can be adjusted digitally through CSR0_VOLUME[3:0] bits.

Audio output can be attenuated and audible noise can be minimized during weak-signal level by the software mute function. Four levels of soft-mute tuning (fastest, fast, slow and slowest) are defined in register bits CSR0_SMUTERATE[1:0]. In addition, 4 levels of attenuation (16,14,12 and 10dB) are defined in register bits CSR0_SMUTEATT[1:0]. The soft-mute function can be disabled by register CSR0_DIS_SMUTE.

1.4. Tuning and Seeking

The tuning frequency is defined as:

Frequency (MHz) = Channel Spacing (200kHz or 100kHz or 50kHz) * Channel Number + Band Selection (87.5MHz, 76MHz or 64MHz)

The Channel Spacing is selected by CSR0_CHSPACE[1:0]. The Channel Number is defined by CSR0_CH[9:0]. The CSR0_BAND is used for Band Selection such as Japan, Europe/U.S./Asia or China band. Setting CSR0_TUNE bit is to enable tuning operation. The seek/tune done (STD) bit set when tuning process is done and RSSI level is available.

When seeking process is initiated by setting CSR0_SEEK, the tuning frequency will be seek up or seek down depending on the setting of CSR0_SEEKUP. The RSSI and tuned channel are readable in RSSI[7:0] and READCH[9:0] respectively when the STD bit is set to high to indicate the completion of seek operation. The SF bit is set to high to indicate that the tuned channel is seek failure when the number of RSSI of all seeking channel is less than or equal to the threshold number defined in CSR0_SEEKRSSITH[7:0]. Seek channel can be read by READCH[9:0] during the entire seek operation.

The seek operation can always be deactivated by setting CSR0_SEEK bit to low.

1.5. Reset and Power-up

1.5.1. Reset

RL508 is reset by power on reset (POR), and the internal registers are reset to their default values. Upon POR asserting from low to high, RL508 will leave out reset state.

1.5.2. Power-UP

Power-up can be set by CSR0_ENABLE and CSR0_DISABLE defined in register 06h. When RL508 is reset, CSR0_ENABLE and CSR0_DISABLE are set to default 0. To enable RL508 into power-up mode setting CSR0_ENABLE = 1 and CSR0_DISABLE = 0 and the following chip programming can be performed.

1.6. Initialization Sequence

The initialization sequence can be referenced in Figure 2.

1.6.1. To initialize the device

1. Supply voltage to VDD.
2. Wait 50ms then write 0x96AA to address 0 to power on the device.
3. Wait 100ms then provide RCLK
4..Set CSR0_ENABLE bit high and CSR0_DISABLE bit low to power up device. Normal software operation should not be performed until the completion of power-up time defined in Figure 2.

1.6.2. To power down the device

1. Set CSR0_DISABLE to 1.
2. Wait 10ms before turn off RCLK.
3. Write 0x16AA to address 0 to power down the device. See Figure 3..

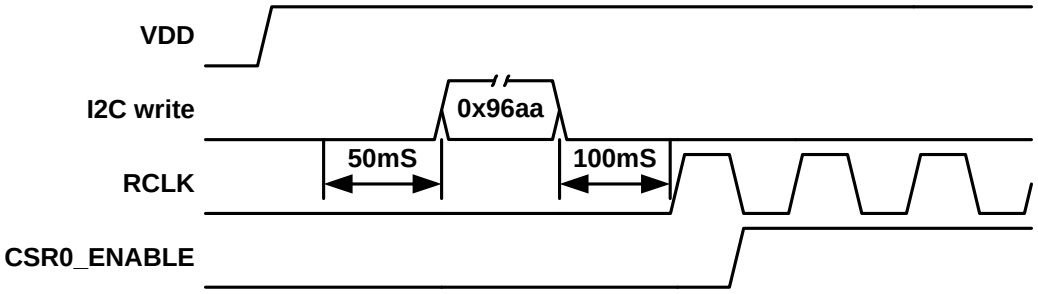


Figure 2. Initialization sequence

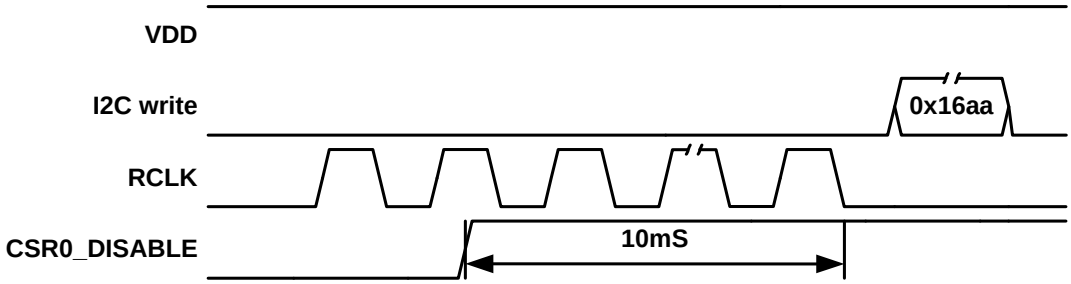


Figure 3. Power down sequence

1.7. Control Interface

RL508 supports only I2C interface. Registers can be operated even RCLK is disappeared. VDD is required for register operation.

1.7.1 2-wire Control Interface

For 2-wire I2C operation, SDIO and SCLK are operated in the open-drain, so external pull-up resistors are required on PCB board. The transfer begins with START condition shown in Table 1. An 8-bits control word is defined in which is A6, A5, A4, A3, A2, A1, A0 and R/W_ where A6:A0=1100100b and R/W_ = 1/0 means read/write operation. This control word is internally latched on rising SCLK edge. To acknowledge control word, SDIO is driven low for one cycle before the next falling SCLK edge.

For write operation (from HOST write to RL508), RL508 latches the incoming serial 8-bit data word on rising SCLK edge. To acknowledge (ACK) each data word, SDIO is driven low for one cycle before the next falling SCLK edge. Host can continue write the following data words with upper byte of register 02h first then lower byte of register 02h until the last register is reached. Host can even further write the following data words because the internal address counter automatically wraps around to the first register.

Data transfer completes when STOP condition happens to make internal address counter rest to 0. Refer to table 1 for STOP condition.

For read operation (host read data from RL508), the serial 8-bit data word is shifted out at each falling SCLK edge and following with acknowledge as Figure 4. Host can continuously read the following data words with upper byte of register 0Ah first then lower byte of register 0Ah until the last register is reached. Host can even further read the following data words because the internal address counter automatically wraps around to the first register. Host should acknowledge each data word but send a non-acknowledge specifically after the data word that occurs before the STOP condition. The internal address counter is reset to 0 when STOP condition happen.

Table 1. 2-Wire control interface characteristics

(VDD = 2 to 3.6 V T_A = –20 to 85 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SCLK Frequency	fSCL		0		400	kHz
SCLK High Time	tC1		600			ns
SCLK Low Time	tC2		1300			ns
Setup Time for START	tC3		600			ns
Hold Time for START	tC4		600			ns
SDIO Input to SCLK ↑ Setup	tC5		100			ns
SDIO Input to SCLK ↓ Hold	tC6		100		900	ns
Setup Time for STOP	tC7		600			ns
STOP to START Time	tC8		1300			ns
SDIO Output to SCLK ↓	tC9		20 + 1*Cb		250	ns
SDIO, SCLK Rising Time	tr		20 + 1*Cb		300	ns
SDIO, SCLK Falling Time	tf		20 + 1*Cb		300	ns
SCLK, SDIO Capacitive Loading	Cb				50	pF

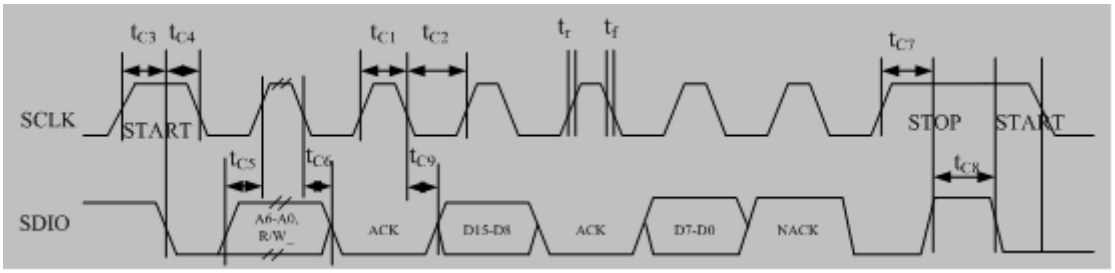


Figure 4(a). 2-Wire control interface read timing parameters

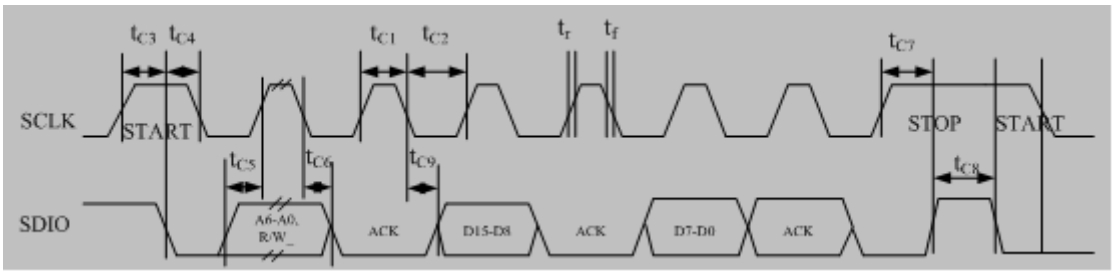


Figure 4(b). 2-Wire control interface write timing parameters

2. Electrical Characteristic

Table 2. Recommended operating conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage	VDD	2		3.6	V
Ambient Temperature	TA	-20	25	85	°C

Table 3. Absolute maximum ratings

PARAMETER	SYMBOL	VALUE	UNIT
Power Supply Voltage	VDD	–0.5 to 3.9	V
Input Current[1]	IIN	±10	mA
Input Voltage[1]	VIN	–0.3 to (VDD + 0.3)	V
Operating Temperature	TOP	–40 to 95	°C
Storage Temperature	TSTG	–40 to 125	°C
RF Input Level[2]		0.4	VpK

Notes:
1. For input pins SCLK, SDIO, RCLK.
2. At RF input pins.

Table 4. DC electrical characteristics
(VDD = 2 to 3.6 V, TA = –20 to 85 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Current[1]	IA	CSR0_ENABLE = 1		17		mA
Logic High Input Voltage[2]	VIH		0.7 x V_{DD}		V_{DD}+ 0.3	V
Logic Low Input Voltage[2]	VIL				0.3 x V_{DD}	V
Logic High Input Current[2]	IIH	VIN = 3.6V VDD = 3.6 V	-10		+10	uA
Logic Low Input Current[2]	IIL	VIN = 0V VDD = 3.6 V	-10		+10	uA
Logic High Output Voltage[3]	VOH	IOUT = 500 µA	0.8 x V_{DD}			V
Logic Low Output Voltage[3]	VOL	IOUT = -500 µA			0.2 x V_{DD}	V

Notes:
1. Refer to Register 02h, for the description of CSR0_ENABLE bit.
2. For input pins SCLK, SDIO, RCLK.
3. For output pins SDIO.

Table5. FM receiver characteristics

(VDD = 2 to 3.6V, T_A = –20 to 85 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Frequency			64	---	108	MHz
Usable Sensitivity		(S+N)/N=26dB	---	1.6	2.0	μV EMF
Adjacent Channel Selectivity		± 200kHz	35	50	---	dB
Alternate Channel Selectivity		± 400kHz	50	60	---	dB
IIP3		Δf1=200 kHz, Δf2=400 kHz	---	91	---	dBuV EMF
IIP3		Δf1=400 kHz, Δf2=800 kHz	---	97	---	dBuV EMF
Audio Output Voltage		Load 10KΩ ‖ 10pF	---	151	---	mVrms
Audio Frequency Response		0 to –3dB	30	---	15K	Hz
Audio (S+N)/N			58	60	---	dB
Stereo Separation			---	42.3	---	dB
Audio Total Harmonic Distortion (THD)		Stereo	---	0.1	0.5	%
Power-up Time		From Power-off to audio out	---	150	---	ms
Tuning/Seeking Time			---	30	---	ms

3. Registers Summary

Table 6. Registers summary

Register Name	Description	Offset Address	Default
DEVICEID	Device ID code	00H	1688H
CHIPID	Chip ID code	01H	14C0H
MPXCONFRG	MPX configuration register	02H	0000H
CHANNEL	Tuning channel setting	03H	0000H
SYSCONFIG	System configuration register	04H	0000H
SEEKCONFIG1	Seek configuration register1	05H	0000H
POWERCONFIG	Power configuration register	06H	0000H
PADCONFIG	PAD configuration register	07H	7000H
Reserved	Reserved	08H	0000H
SEEKCONFIG2	Seek configuration register2	09H	4010H
STATUS	Status register and work channel	0AH	0000H
RSSI	RSSI	0BH	0000H
Reserved	Reserved	0CH	0000H
Reserved	Reserved	0DH	0000H
Reserved	Reserved	0EH	0000H
Reserved	Reserved	0FH	0000H

4. Register Descriptions

DEVICEID (Device ID code), 00H

Field	Bits	Type	Description
PART_NUMBER	15:12	R	Part number
MFGID	11:0	R	Manufacture ID

CHIPID (Chip ID code), 01H

Field	Bits	Type	Description
REVISION_NO	15:10	R	
Reserved	9:0	R	Reserved

MPXCONFRG (MPX configuration register), 02H

Field	Bits	Type	Description
CSR0_DIS_SMUTE	15	R/W	Disable Softmute 0 = Enable Softmute 1 = Disable Softmute(default)
CSR0_DIS_MUTE	14	R/W	Disable Mute 0 = Enable Mute(default) 1 = Disable Mute
CSR0_MONO	13	R/W	Force Mono or Auto Detect 0 = Auto detect Mono or Stereo(default) 1 = Force mono
CSR0_DEEM	12	R/W	De-emphasis 0 = 75us(default) 1 = 50us
Reserved	11:10	R	Reserved
CSR0_BLNDADJUST	9:8	R/W	Stereo/Mono Blend Level Adjustment Set the RSSI range for stereo/mono blend 00 = 31~49 dBuv(default) 01 = 37~55 dBuv 10 = 19~37 dBuv 11 = 25~43 dBuv
CSR0_SMUTERATE	7:6	R/W	Softmute Enter/Recover Rate 00 = fastest(default) 01 = fast 10 = slow 11 = slowest
CSR0_SMUTEATT	5:4	R/W	Softmute Attenuation value 00 = 16dB(default) 01 = 14dB 10 = 12dB 11 = 10dB
CSR0_VOLUME	3:0	R/W	Volume 0000 = mute(default). 0001 = -28dBFS …… 1110 = -2dBFS 1111 = 0dBFS

CHANNEL (Tuning channel setting), 03H

Field	Bits	Type	Description
CSR0_TUNE	15	R/W	Enable Tune function 0 = Disable(default) 1 = Enable
Reserved	14	R	Reserved
CSR0_BAND	13:12	R/W	Band Select 00 = 87.5~108MHz(default) 01 = 76~108MHz 10 = 76~91MHz 11 = 64~76MHz
CSR0_CHSPACE	11:10	R/W	Channel spacing 00 = 200kHz(default) 01 = 100kHz 10 = 50kHz
CSR0_CH	9:0	R/W	Tuning Channel Channel for tune operation

SYSCONFIG (System configuration register), 04H

Field	Bits	Type	Description
Reserved	15:14	R	Reserved
CSR0_DIS_AGC	13	R/W	Disable AGC 0 = Enable AGC (default) 1 = Disable AGC
Reserved	12	R	Reserved
Reserved	11:10	R	Reserved
Reserved	9:8	R	Reserved
Reserved	7:0	R	Reserved

SEEKCONFIG1 (Seek configuration register1), 05H

Field	Bits	Type	Description
CSR0_SEEK	15	R/W	Enable Seek function 0 = Disable(default) 1 = Enable
CSR0_SEEKUP	14	R/W	Seek Direction 0 = Seek down(default) 1 = Seek up
CSR0_SKMODE	13	R/W	Seek Mode. 0 = Wrap at the upper or lower band limit and continue seeking (default). 1 = Stop seeking at the upper or lower band limit.
Reserved	12:8	R	Reserved
CSR0_SEEKRSSITH	7:0	R/W	RSSI Seek Threshold 0x00 = min RSSI(default) 0x7F = max RSSI

POWERCONFIG (Power configuration register), 06H

Field	Bits	Type	Description
CSR0_ENABLE	15	R/W	Power-up Enable Default = 0
CSR0_DISABLE	14	R/W	Power-up Disable Default = 0
Reserved	13:12	R	Reserved
CSR0_BLNDOFS	11:8	R/W	Blending offset value, 2dB per step 0000 = 0 dB (default) 0001 = 2 dB …… 1111 = 30 dB
Reserved	7:4	R	Reserved
CSR0_VOLEXT	3	R/W	0: Volume attenuate 0dB more 1: Volume attenuate 15dB more
CSR0_CLK_TYPE	2:0	R/W	000: 32.768KHz 001: 12MHz 010: 13MHz 011: 19.2MHz 100: 32.768KHz 101: 24MHz 110: 26MHz 111: 38.4MHz

PADCONFIG (PAD configuration register), 07H

Field	Bits	Type	Description
Reserved	15:0	R	Reserved

RESERVED1 (Reserved register1), 08H

Field	Bits	Type	Description
Reserved	15:0	R	Reserved

RESERVED2 (Reserved register2), 09H

Field	Bits	Type	Description
CSR0_OFSTH	15:8	R/W	Seek DC offset fail threshold for 100k/200k spacing 0x00 = min DC value (default: 0x40) 0xFF = max DC value
CSR0_QLTTH	7:0	R/W	Seek audio quality fail threshold 0x00 = best quality (default: 0x10) 0xFF = worst quality

STATUS (Status register and work channel), 0AH

Field	Bits	Type	Description
Reserved	15	R	Reserved
STD	14	R	Seek/Tune Done 0 = Not complete 1 = Done
SF	13	R	Seek Fail 0 = Seek successful 1 = Seek failure
Reserved	12	R	Reserved
Reserved	11	R	Reserved
SI	10	R	Stereo Indicator 0 = Mono 1 = Stereo
READCH	9:0	R	Read Channel

RSSI (RSSI), 0BH

Field	Bits	Type	Description
Reserved	15:8	R	Reserved
RSSI	7:0	R	RSSI RSSI unit is dBuv

RESERVED3 (Reserved register3), 0CH

Field	Bits	Type	Description
Reserved	15:0	R	Reserved

RESERVED4 (Reserved register4), 0DH

Field	Bits	Type	Description
Reserved	15:0	R	Reserved.

RESERVED5 (Reserved register5), 0EH

Field	Bits	Type	Description
Reserved	15:0	R	Reserved.

RESERVED6 (Reserved register6), 0FH

Field	Bits	Type	Description
Reserved	15:0	R	Reserved.

5. Pin Description

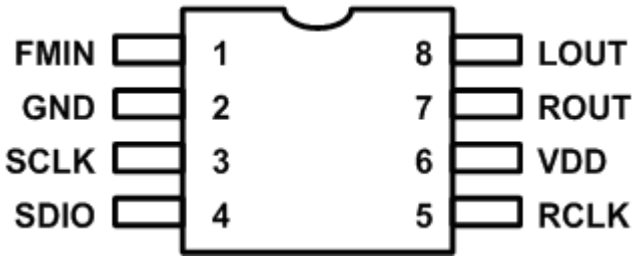


Figure 5. Top View

Table 7. Pin definition

Pin Number	Name	Description
1	FMIN	FM RF input. For single-ended operation
2	GND	Chip RF ground. Connect to ground plane on PCB.
3	SCLK	2-wire serial clock input.
4	SDIO	2-wire serial data input/output.
5	RCLK	External reference clock input.
6	VDD	Power supply voltage.
7	ROUT	Right audio output.
8	LOUT	Left audio output.

6. Package Outline

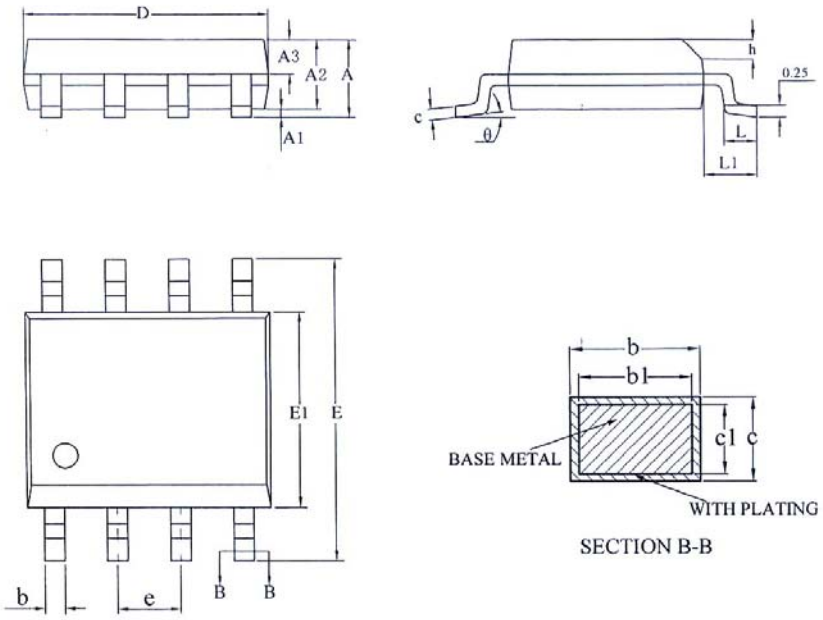


Figure 7. Package outline

Table 8. Package dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	80*80	90*90	95*130

7. PCB Land Pattern

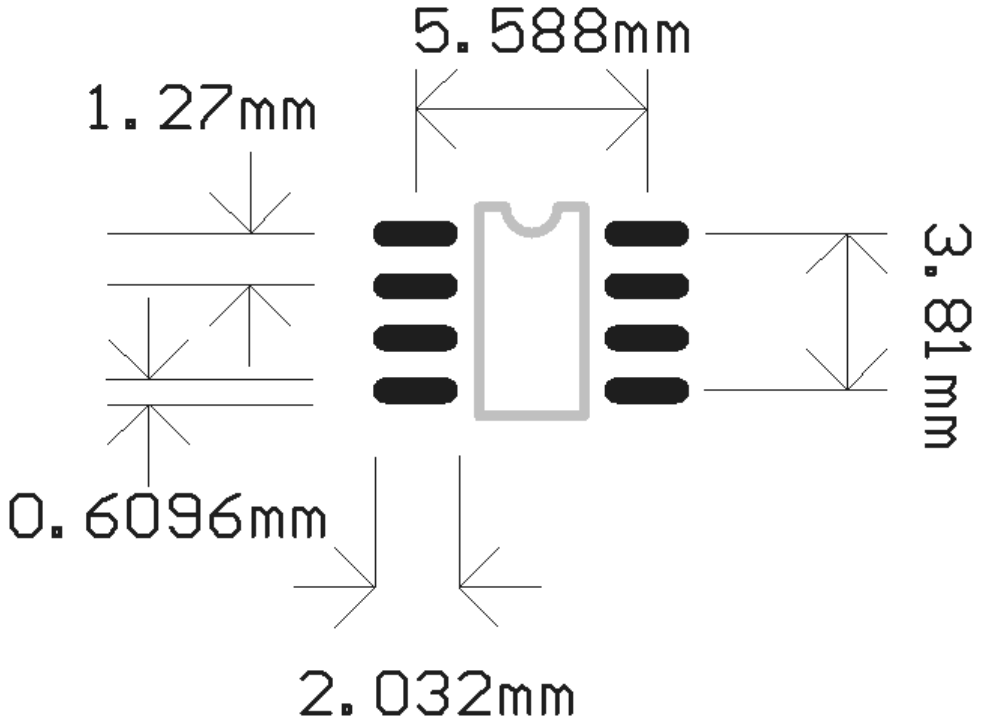
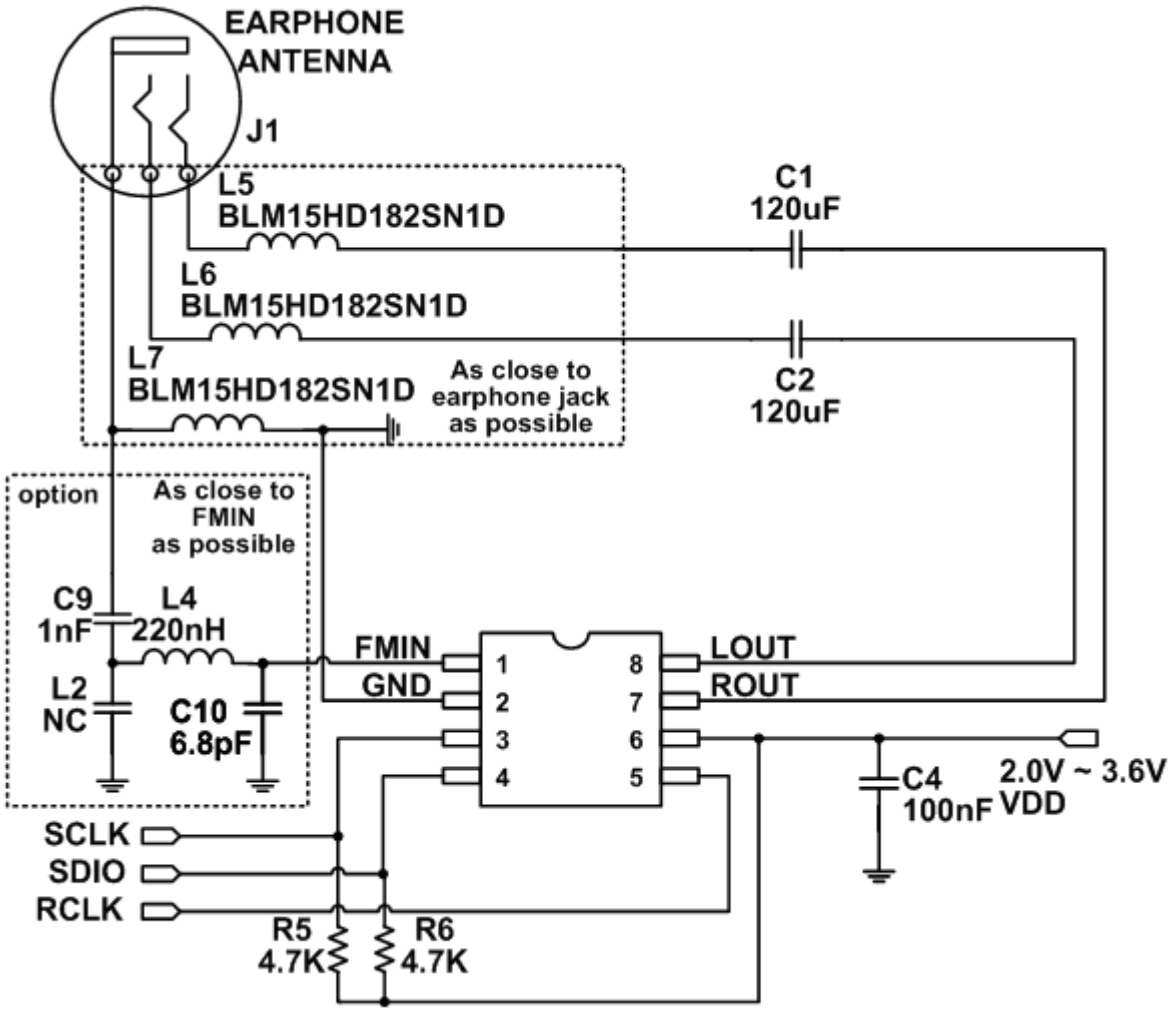


Figure 8. PCB land pattern

8 Application Schematic

8.1 Application Circuit for RCLK and headphone



Notes:
1. Place C4 closed to VDD pin
2. Options: the antenna matching network is kept for high sensitivity mode.
3. Strongly recommended to keep L5, L6, L7 and C9 when applying earphone antennas.

8.1.1 Bill Of Materials

Part Type	Component	Value/Description	Supplier
RL508	U1	RL508 FM Radio Tuner	RichWave
120uF	C1, C2	Audio AC couple capacitors	
BLM15HD182SN1D	L5, L6, L7	Ferrite bead keep high-impedance for RF path	
100nF	C4	Supply bypass capacitor 100nF ,±20%,Z5U/X7R	
4.7K	R5, R6	I2C pull-up resistors	
6.8pF	C10	Antenna matching	
220nH	L4	Antenna matching	
1nF	C9	DC-blocking capacitor	