CMOS Clock Generator – CGS3311

Monolithic crystal controlled CMOS oscillator in bare die form

Rev 1.1
06/05/19

Description

The CGS3311 is a crystal controlled CMOS oscillator requiring a minimum of external components and is designed for Clock Generation and Support applications up to 110 MHz. The device is highly versatile, providing selectable output divide ratios, multiple crystal drive levels and selectable rise and fall timing options. The circuit is designed to operate over a wide frequency range using fundamental model or overtone crystals. The device is a direct electrical and mechanical replacement for the obsolete CGS3311 produced by National Semiconductor.

Features:

- Crystal frequency operation range:
  - fundamental: 10 MHz to 100 MHz typical
  - 3rd or 5th overtone: 10 MHz to 85 MHz
- Programmable oscillator drive
- Selectable fast output edge rates
- Output symmetry circuit to adjust 50% duty cycle point between CMOS and TTL levels
- Output current drive of 48 mA for I_{OL}/I_{OH}
- Output has high speed short circuit protection
- Basic oscillator type: Pierce

Ordering Information

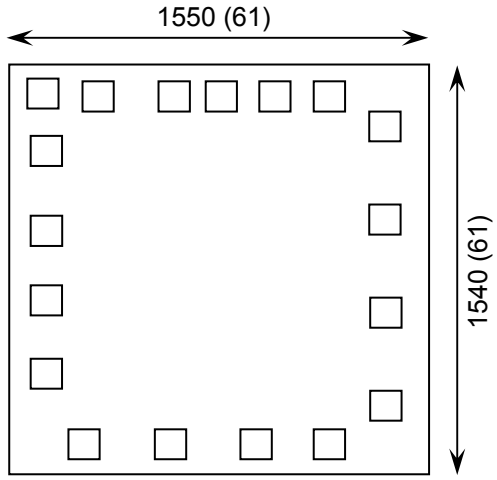
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability version of this product please see

54ACT3301

Die Dimensions in µm (mils)



Supply Formats:

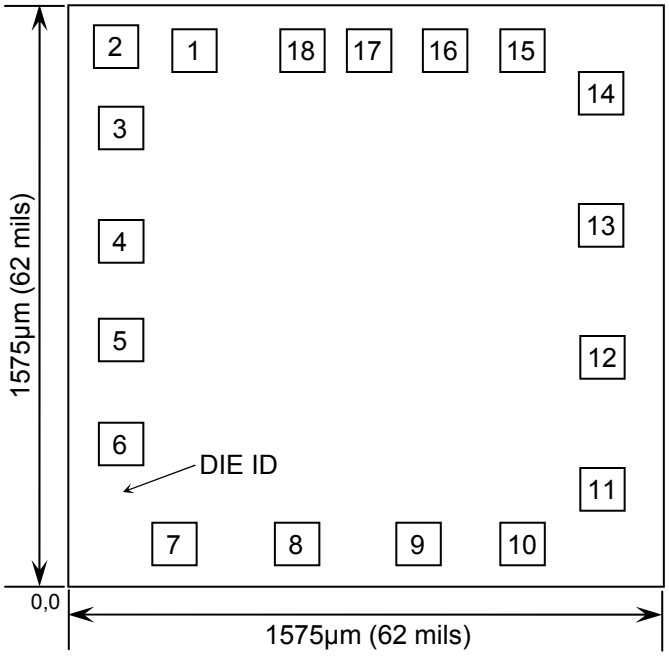
- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1550 x 1540 61 x 61	µm mils
Minimum Bond Pad Size	100 x 100 3.94 x 4	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	OSC_OUT	275	1360
2	NOT USED	70	1370
3	NOT USED	85	1160
4	NOT USED	85	860
5	$\overline{OEL}$	85	605
6	OEH	85	330
7	OSC_LO_1	220	70
8	GND	535	70
9	OUT	845	70
10	V_{CC}	1110	70
11	TRF	1315	215
12	DIVA	1315	560
13	OSC_DR	1315	905
14	DIVB	1315	1250
15	OSC_LO_2	1110	1360
16	DIVBB	915	1360
17	OSC_IN	720	1360
18	NOT USED	550	1360
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Truth Tables

DIVISION SELECTION

DIVB	DIVA	OEL	OEH	DIVIDER OUTPUT
$V_{½}$	0 / F	X	X	Divide-by 1
1	0 / F	0	1	Divide-by 2
0	0 / F	0	1	Divide-by 4
$V_{½}$	1	0	1	Divide-by 8
1	1	0	1	Divide-by 16
0	1	0	1	Divide-by 32
X	X	1	X	Output Reset High at Re-enable
X	X	X	0	Output Reset High at Re-enable

DRIVE SELECTION

OSC_DR	OSC_OUT DRIVE
0	Low
1	Medium
$V_{½}$	High

INPUT LEVEL	
1	High voltage
0	Low voltage
$V_{½}$	$V_{CC/2}$
F	Floating
X	Irrelevant

RISE AND FALL TIME SELECTION

OSC_DR	DIV	TRF	RISE / FALL TIME (ns)
$V_{½}$	N	0 / F	2
$V_{½}$	N	1	<2
$V_{½}$	Y	0 / F	4
$V_{½}$	Y	1	2
0 / 1	X	0 / F	4
0 / 1	X	1	2

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Configuration Options

DIVIDE	ENABLE	DRIVE	OUTPUT RISE / FALL TIME (ns)
1,2,4	OEH	L, M, H	2, 4
1,2,4	OEH	H	2, 4
8, 16, 32	OEH	H	4
8, 16, 32	OEH	L, M, H	4
1,2,4	$\overline{\text{OEL}}$	H	1, 2
4	OEH	H	4
32	OEH	H	4
1,2,4	OEH	H	1, 2
1,2,4	$\overline{\text{OEL}}$	L, M, H	2, 4

Each configuration comprises one output with the choice of selected frequency divide, output enable, crystal drive and output rise/fall time.

Crystal drive options:

- L = Low drive
- M = Medium drive
- H = High drive.

Pad Descriptions

INPUTS

OSC IN (Pad 17) **-** Input to Oscillator Inverter. The output of the crystal would be connected here.

CONTROL INPUTS

DIVA (Pad 12) **-** Input used to select Binary Divide-By Option. This pin has CMOS compatible input levels.
DIVB (Pad 14) **-** 3 Level input used to select Binary Divide-By value.
DIVBB (Pad 16) - This pin is the same signal DIVB and provided as an alternative connection for hybrid assemblies.
OSC_DR (Pad 13**) -** 3 Level input pin that selects Oscillator Drive Level.
OEH (Pad 6) **-** Active High Three-state enable pin. This pin pulls to a high value when left floating and three-states the output when forced low. This pin has TTL compatible input levels.
OEL (Pad 5) **-** Active Low Three-state enable pin. This pin pulls to a low value when left floating and three-states the output when forced high. This pin has TTL compatible input levels.
TRF (Pad 11) **-** Rise and Fall time override pin

OUTPUTS

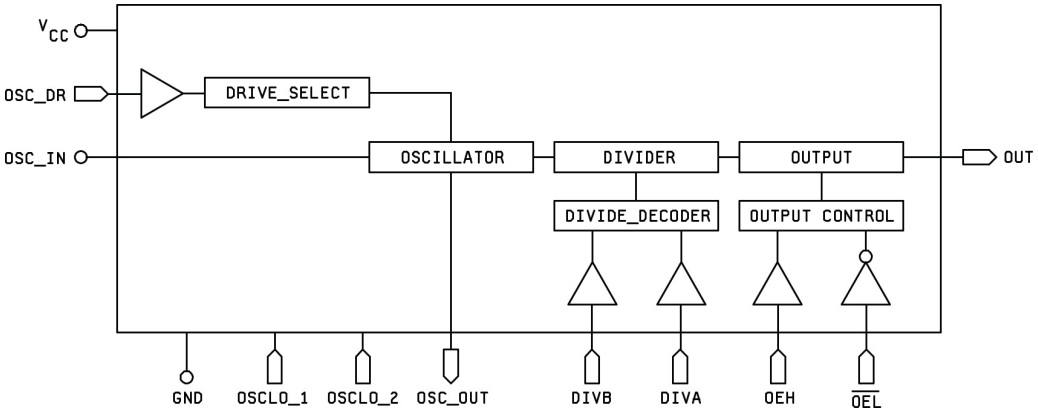
OUT (Pad 9) **-** This pin is the main clock output on the device.
OSC_OUT (Pad 1) **-** Resistive buffered output of the Oscillator inverter

OTHER PADS

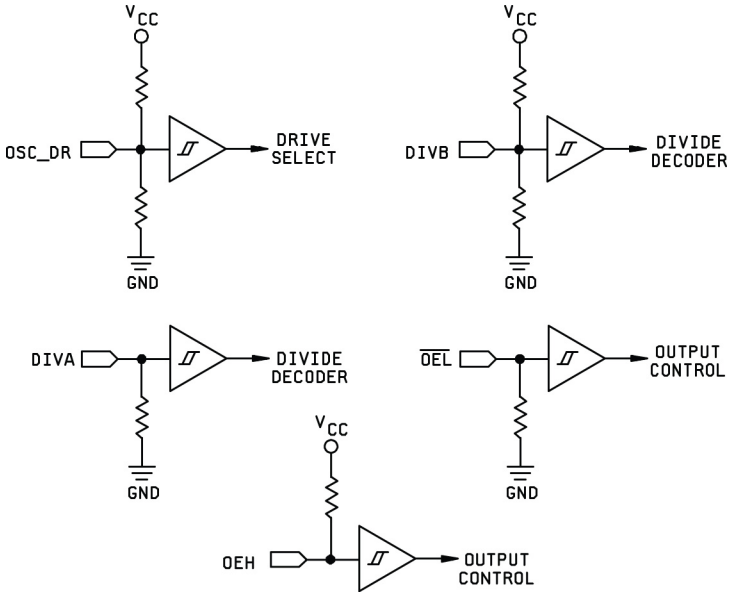
OSC_LO_1 (Pad 7) - The Oscillator Low pin is the ground for the Oscillator.
OSC_LO_2 (Pad 15) **-** This pin is the same signal as OSCLO_1 and provided as an alternative connection for hybrid assemblies.
VCC (Pad 10) **-** The power pin for the chip.
GND (Pad 8) **-** The ground pin for all sections of the circuitry except the oscillator and oscillator related circuitry.

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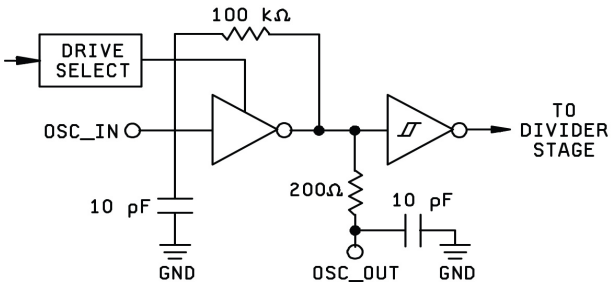
Logic Diagrams



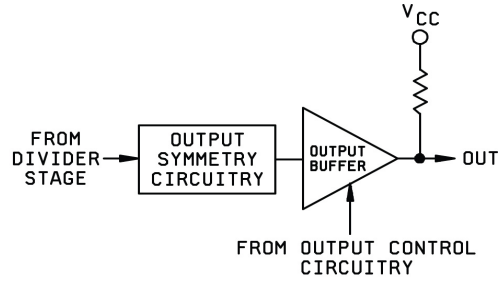
Input Stage



Oscillator Stage



Output Stage



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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 to +7.0	V
Input Voltage Range	V_{IN}	-0.5 to +7.0	V
Output Voltage Range	V_{OUT}	-0.5 to V_{CC} +0.5	V
Input Diode Current	I_{IK}	±9	mA
Output Diode Current	I_{OK}	±20	mA
Output Source or Sink Current	I_{OUT}	±70	mA
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation in Still Air[2]	P_D	500	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.
2. Measured in 16 lead ceramic package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Operating Temperature	T_J	-40	+85	°C
DC Supply Voltage	V_{CC}	+4.5	+5.5	V
Input voltage range	V_{IN}	0	+5.5	V
Output Voltage Range	V_{OUT}	0	V_{CC}	V
Maximum low level input voltage	(V_{IL1}) (OEH, $\overline{OEL}$)	-	0.8	V
Minimum high level input voltage	(V_{IH1}) (OEH, $\overline{OEL}$)	-	2	V
Maximum low level input voltage	(V_{IL2}) (DIVA)	30% V_{CC}		V
Minimum high level input voltage	(V_{IH2}) (DIVA)	70% V_{CC}		V
Maximum low level input voltage	(V_{IL3}) (OSC_DR, DIVB)	10% V_{CC}		V
One-half input voltage level	($V_{½}$) (OSC_DR, DIVB)	50% V_{CC}		V
Minimum high level input voltage	(V_{IH3}) (OSC_DR, DIVB)	90% V_{CC}		V
Maximum high level output current	I_{OH}	-	-48	Ma
Maximum low level output current	I_{OL}	-	+48	mA

DC Electrical Characteristics (+4.5V ≤ V_{CC} ≤ +5.5 V, -40°C ≤ T_J ≤ +85°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Minimum high level input voltage. TTL (OEH, $\overline{OEL}$)	V_{IH1}	V_{CC} = 4.5V	2	-	-	V
		V_{CC} = 5.5V	2	-	-	
Maximum low level input voltage. TTL (OEH, $\overline{OEL}$)	V_{IL1}	V_{CC} = 4.5V	-	-	0.8	V
		V_{CC} = 5.5V	-	-	0.8	

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DC Electrical Characteristics (+4.5V ≤ V_{CC} ≤ +5.5 V, -40°C ≤ T_J ≤ +85°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Minimum high level input voltage. CMOS (DIVA)	V_{IH2}	V_{CC} = 4.5V		3.15	-	-	V
		V_{CC} = 5.5V		3.85	-	-	
Maximum low level input voltage. CMOS (DIVA)	V_{IL2}	V_{CC} = 4.5V		-	-	1.35	V
		V_{CC} = 5.5V		-	-	1.65	
Min. high level input voltage. TRI-STATE (DIVB, OSC_DR)	V_{IH3}	V_{CC} = 4.5V		4.05	-	-	V
		V_{CC} = 5.5V		4.95	-	-	
Max. low level input voltage. TRI-STATE (DIVB, OSC_DR)	V_{IL3}	V_{CC} = 4.5V		-	-	0.45	V
		V_{CC} = 5.5V		-	-	0.55	
½ level input voltage. TRI-STATE (DIVB, OSC_DR)	$V_{½}$	V_{CC} = 4.5V		1.80	-	2.70	V
		V_{CC} = 5.5V		2.20	-	3.30	
High level output voltage (OUT)	V_{OH1}	OEH = V_{IH1}, $\overline{DIVA}$ = V_{IH2}, $\overline{OEL}$ = GND, DIVB = V_{IH3} or $V_{½}$, I_{OH} = -50 µA	V_{CC} = 4.5V	4.40	-	-	V
			V_{CC} = 5.5V	5.40	-	-	
		OEH, DIVA, $\overline{DIVB}$ = V_{CC}; $\overline{OEL}$ = GND; I_{OH} = -48 mA	V_{CC} = 4.5V	3.76	-	-	V
			V_{CC} = 5.5V	4.76	-	-	
		OEH, DIVA, $\overline{DIVB}$ = V_{CC}, $\overline{OEL}$ = GND, I_{OH} = -75 mA[3]	V_{CC} = 5.5V	3.85	-	-	V
High level output voltage, low drive (OSC_OUT)	V_{OH2}	OSC_IN, OSC_DR = 0V, I_{OH} = -150 µA	V_{CC} = 4.5V	3.46	-	-	V
			V_{CC} = 5.5V	4.46	-	-	
High level output voltage, medium drive (OSC_OUT)	V_{OH3}	OSC_IN = 0V, OSC_DR= V_{CC} I_{OH} = -600 µA	V_{CC} = 4.5V	3.46	-	-	V
			V_{CC} = 5.5V	4.46	-	-	
High level output voltage, high drive (OSC_OUT)	V_{OH4}	OSC_IN = 0V, I_{OH} = -1 mA	OSC_DR =2.25V	3.46	-	-	V
			OSC_DR =2.75V	4.46	-	-	
Minimum Dynamic Output Current	I_{OH}	V_{OH} = 3.85V	V_{CC} = 5.5V	-75	-	-	mA

3. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

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DC Electrical Characteristics (+4.5V ≤ V_{CC} ≤ +5.5 V, -40°C ≤ T_J ≤ +85°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		LIMITS			UNITS
				MIN	TYP	MAX	
Low level output voltage (OUT)	V_{OL1}	OEH = V_{CC}, DIVA = V_{IL2}, $\overline{OEL}$ = V_{IL1}, DIVB = V_{IL3} or $V_{½}$, I_{OL} = 50 µA	V_{CC} = 4.5V	-	-	0.10	V
			V_{CC} = 5.5V	-	-	0.10	
		OEH = V_{CC}, DIVA, DIVB = GND, $\overline{OEL}$ = GND, I_{OL} = 48 mA	V_{CC} = 4.5V	-	-	0.44	V
			V_{CC} = 5.5V	-	-	0.44	
		OEH = V_{CC}, DIVA, DIVB = GND, $\overline{OEL}$ = GND, I_{OL} = 75 mA[3]	V_{CC} = 5.5V	-	-	1.65	V
Low level output voltage, low drive (OSC_OUT)	V_{OL2}	OSC_IN = V_{CC} OSC_DR = 0V, I_{OL} = 150 µA	V_{CC} = 4.5V	-	-	0.74	V
			V_{CC} = 5.5V	-	-	0.74	
Low level output voltage, medium drive (OSC_OUT)	V_{OL3}	OSC_IN, OSC_DR =V_{CC}, I_{OL} = 600 µA	V_{CC} = 4.5V	-	-	0.74	V
			V_{CC} = 5.5V	-	-	0.74	
Low level output voltage, high drive (OSC_OUT)	V_{OL4}	OSC_IN = V_{CC}, I_{OL} = 1 mA	OSC_DR =2.25V	-	-	0.74	V
			OSC_DR =2.75V	-	-	0.74	
Minimum Dynamic Output Current	I_{OL}	V_{OL} = 1.65V	V_{CC} = 5.5V	75	-	-	mA
Positive input clamp voltage	V_{IC+}	I_{IN} = 9 mA	V_{CC} = 4.5V	-	-	5.7	V
Negative input clamp voltage	V_{IC-}	I_{IN} = -9 mA	V_{CC} = 4.5V	-	-	-1.2	V
Input current high (DIVB, OSC_DR)	I_{IH}	V_{IN} = 5.5V	V_{CC} = 5.5V	200	-	380	µA
Input current low (DIVB, OSC_DR)	I_{IL}	V_{IN} = 0V	V_{CC} = 5.5V	-200	-	-380	µA
Input current high ($\overline{OEL}$)	I_{IH}	V_{IN} = 5.5V	V_{CC} = 5.5V	85	-	175	µA
Input current low (OEH)	I_{IL}	V_{IN} = 0V	V_{CC} = 5.5V	-85	-	-175	µA
Input current low (DIVA, $\overline{OEL}$)	I_{IL}	V_{IN} = 0V	V_{CC} = 5.5V	-	-	-6	µA
Input current high (OEH)	I_{IH}	V_{IN} = 5.5V	V_{CC} = 5.5V	-	-	6	µA

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DC Electrical Characteristics (+4.5V ≤ V_{CC} ≤ +5.5 V, -40°C ≤ T_J ≤ +85°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		LIMITS			UNITS
				MIN	TYP	MAX	
Input current high (OSC_IN)	I_{IH}	V_{IN} = 5.5V	V_{CC} = 5.5V	20	-	125	µA
Input current low (OSC_IN)	I_{IL}	V_{IN} = 0V	V_{CC} = 5.5V	-20	-	-125	µA
Quiescent supply current, output low	I_{CCL}	$\overline{OEH}$ = 5.5V, $\overline{OEL}$ = 0V, All other inputs V_{IN} = V_{CC} or GND	V_{CC} = 5.5V	-	-	240	µA
Quiescent supply current, output high	I_{CCH}			-	-	45	µA
Quiescent supply current, output three-state	I_{CCZ}	$\overline{OEH}$ = 0V, $\overline{OEL}$ = 5.5V, All other inputs V_{IN} = V_{CC} or GND	V_{CC} = 5.5V	-	-	45	µA
Quiescent supply current delta, OSC_IN Floating	ΔI_{CCO}	OSC_IN = Floating, all other inputs, V_{IN} = V_{CC} or GND	OSC_DR =0.45V V_{CC} = 4.5V	0.6	-	-	mA
			OSC_DR =0.55V V_{CC} = 5.5V	-	-	6.5	mA
			OSC_DR =4.05V V_{CC} = 4.5V	1.7	-	-	mA
			OSC_DR =4.95V V_{CC} = 5.5V	-	-	12.4	mA
			OSC_DR =1.8, 2.7V V_{CC} = 4.5V	5.5	-	-	mA
			OSC_DR =2.2, 3.3V V_{CC} = 5.5V	-	-	31.5	mA
Quiescent supply current delta, input 3 level	ΔI_{CC3L}	DIVB,OSC_DR = 2.75V, all other inputs, V_{IN} = V_{CC} or GND	V_{CC} = 5.5V	-	-	1.5	mA
Quiescent supply current delta, TTL input level	ΔI_{CCT}[4]	$\overline{OEL}$, OEH = V_{CC} - 2.1V, all other inputs, V_{IN} = V_{CC} or GND	V_{CC} = 5.5V	-	-	1.5	mA

4. Performed one input at a time.

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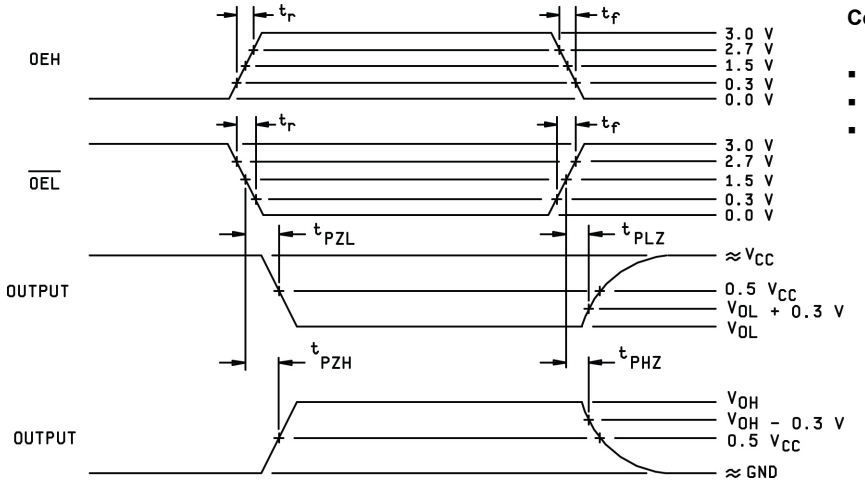
DC Electrical Characteristics (+4.5V ≤ V_{CC} ≤ +5.5 V, -40°C ≤ T_J ≤ +85°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Three-state output leakage current high	I_{OZH}	V_{OUT} = V_{CC}, OEH = 0.8V, $\overline{OEL}$ = 2V, all other inputs, V_{IN} = V_{CC} or GND	V_{CC} = 4.5V	-	-	5	µA
			V_{CC} = 5.5V	-	-	5	
Three-state output leakage current high	I_{OZL}	V_{OUT} = 0V, OEH = 0.8V, $\overline{OEL}$ = 2V, all other inputs, V_{IN} = V_{CC} or GND	V_{CC} = 4.5V	-	-	-150	µA
			V_{CC} = 5.5V	-	-	-180	

AC Electrical Characteristics (+4.5V ≤ V_{CC} ≤ +5.5 V, -40°C ≤ T_J ≤ +85°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Frequency Maximum	f_{MAX}	C_L = 50 pF, R_L = 500Ω, t_r, t_f = 3ns	V_{CC} = 4.5V	100	-	-	MHz
Output enable time, $\overline{OEL}$ or OEH to OUT	t_{PZH}	C_L = 50 pF, R_L = 500Ω, t_r, t_f = 3ns	V_{CC} = 4.5V	1	-	31.5	ns
	t_{PZL}		V_{CC} = 4.5V	1	-	28.0	
Output disable time, $\overline{OEL}$ or OEH to OUT	t_{PHZ}	C_L = 50 pF, R_L = 500Ω, t_r, t_f = 3ns	V_{CC} = 4.5V	1	-	21.5	ns
	t_{PLZ}		V_{CC} = 4.5V	1	-	16.0	

Switching Waveform

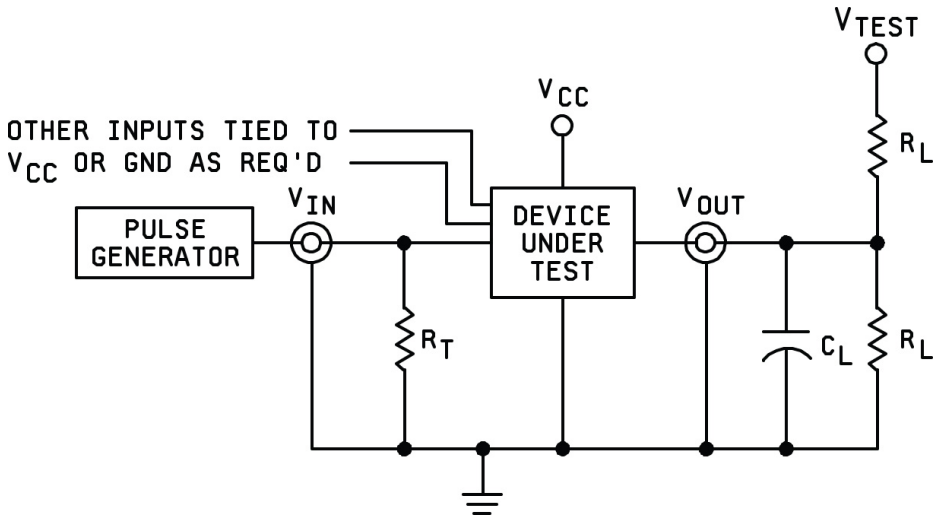


Conditions:

- When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 x V_{CC}.
- When measuring t_{PHZ}, t_{PZH}, t_{PLH} and t_{PHL}: V_{TEST} = open.
- The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.

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Test Circuit



Test Conditions:

- C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance)
- R_L = 500Ω or equivalent, R_T = 50Ω or equivalent
- Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz ; tr ≤ 3.0 ns; tf ≤ 3.0ns
- tr and tf and measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent
- Timing parameters at a minimum input frequency of 1 MHz

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