Document Number: MW7IC3825N
Rev. 1, 11/2010

RoHS

RF LDMOS Wideband Integrated Power Amplifiers

MW7IC3825NR1
MW7IC3825GNR1
MW7IC3825NBR1

3400–3600 MHz, 5 W AVG., 28 V
WiMAX
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

The MW7IC3825N wideband integrated circuit is designed with on–chip matching that makes it usable from 3400–3600 MHz. This multi–stage structure is rated for 26 to 32 Volt operation and covers all typical cellular base station modulation formats.

- Typical WiMAX Performance: V_{DD} = 28 Volts, I_{DQ1} = 130 mA, I_{DQ2} = 230 mA, P_{out} = 5 Watts Avg., f = 3600 MHz, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF.
  - Power Gain — 25 dB
  - Power Added Efficiency — 15%
  - Device Output Signal PAR — 8.5 dB @ 0.01% Probability on CCDF
  - ACPR @ 8.5 MHz Offset — –48 dBc in 1 MHz Channel Bandwidth

Driver Applications

- Typical WiMAX Performance: V_{DD} = 28 Volts, I_{DQ1} = 190 mA, I_{DQ2} = 230 mA, P_{out} = 0.5 Watts Avg., f = 3400 and 3600 MHz, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF.
  - Power Gain — 23.5 dB
  - Power Added Efficiency — 3.5%
  - Device Output Signal PAR — 9.2 dB @ 0.01% Probability on CCDF
  - ACPR @ 8.5 MHz Offset — –55 dBc in 1 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 3500 MHz, 25 Watts CW Output Power
- Stable into a 5:1 VSWR. All Spurs Below –60 dBc @ 0 to 44 dBm CW P_{out}
- Typical P_{out} @ 1 dB Compression Point ≃ 30 Watts CW

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large–Signal Impedance Parameters and Common Source S–Parameters
- On–Chip Matching (50 Ohm Input, RF Choke to Ground)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- Greater Negative Gate–Source Voltage Range for Improved Class C Operation
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13 inch Reel.

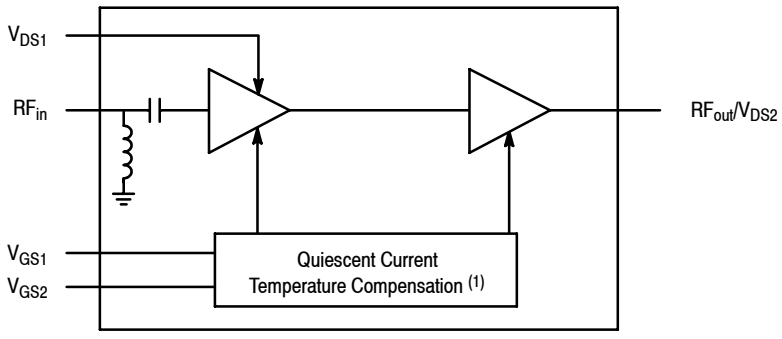
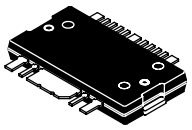
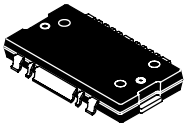


Figure 1. Functional Block Diagram

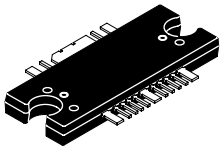
CASE 1886–01
TO–270 WB–16
PLASTIC
MW7IC3825NR1

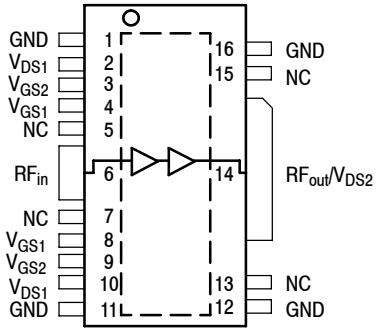


CASE 1887–01
TO–270 WB–16 GULL
PLASTIC
MW7IC3825GNR1



CASE 1329–09
TO–272 WB–16
PLASTIC
MW7IC3825NBR1





(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf.Select Documentation/Application Notes – AN1977 or AN1987.

© Freescale Semiconductor, Inc., 2008, 2010. All rights reserved.

freescale semiconductor

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
Input Power	P_{in}	45	dBm

Table 2. Thermal Characteristics

Characteristic		Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
WiMAX Application	Stage 1, 28 Vdc, I_{DQ1} = 130 mA		4.7	
(Case Temperature 71°C, P_{out} = 5 W CW)	Stage 2, 28 Vdc, I_{DQ2} = 230 mA		1.3	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 - Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 - On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 25 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1} = 130 mA)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (4) (V_{DD} = 28 Vdc, I_{DQ1} = 130 mA, Measured in Functional Test)	$V_{GG(Q)}$	3.5	4.2	5	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. V_{GG} = 1.55 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

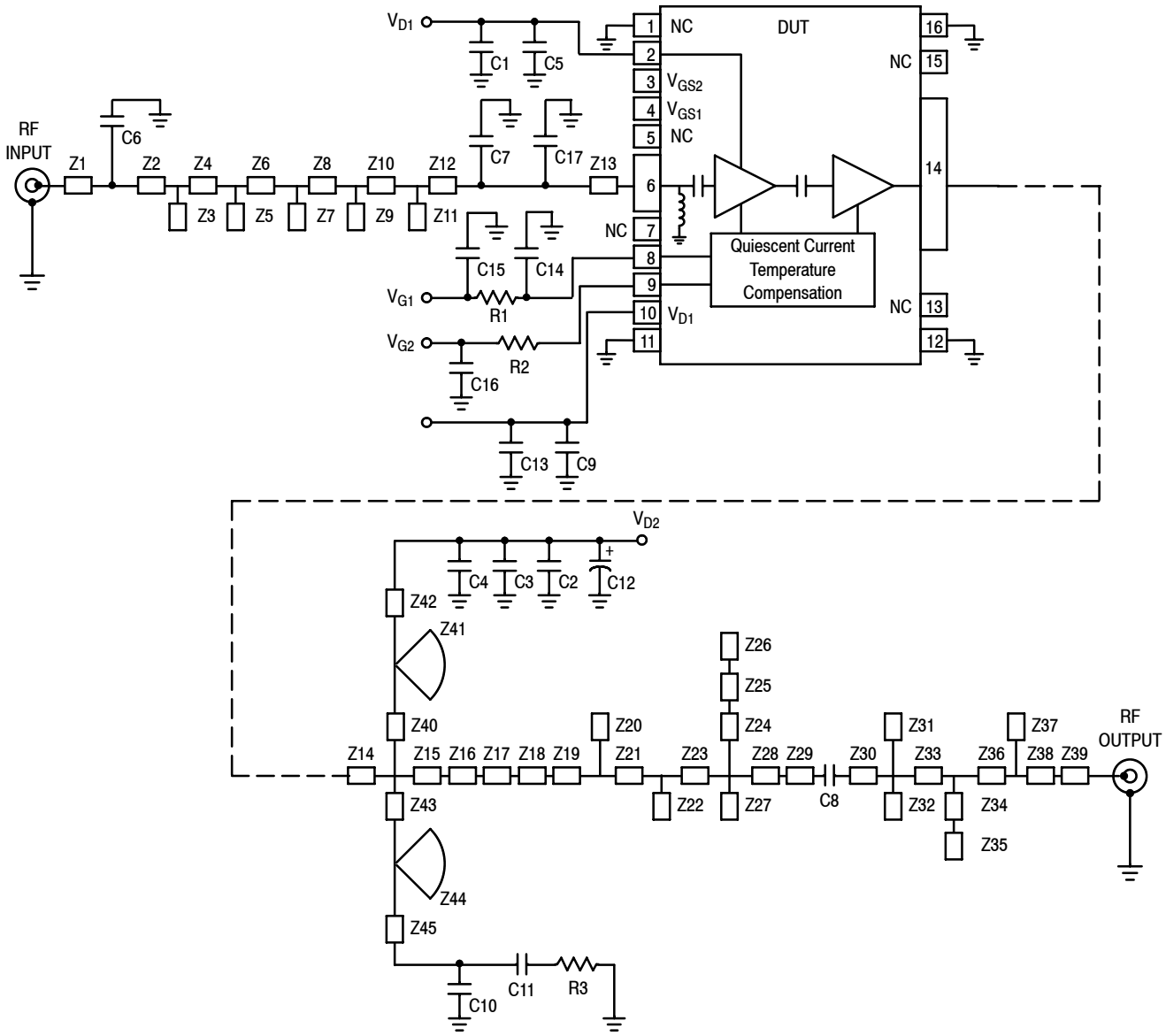
Characteristic	Symbol	Min	Typ	Max	Unit
Stage 2 - Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 - On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 120 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2} = 230 mA)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (1) (V_{DD} = 28 Vdc, I_{DQ2} = 230 mA, Measured in Functional Test)	$V_{GG(Q)}$	2.5	3.3	4	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	0.2	0.5	1.2	Vdc
Stage 2 - Dynamic Characteristics (2)					
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	72.3	—	pF
Functional Tests (3) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 130 mA, I_{DQ2} = 230 mA, P_{out} = 5 W Avg., f = 3600 MHz, WiMAX, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF. ACPR measured in 1 MHz Channel Bandwidth @ ±8.5 MHz Offset.					
Power Gain	G_{ps}	21	25	32	dB
Power Added Efficiency	PAE	12	15	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.5	8.5	—	dB
Adjacent Channel Power Ratio	ACPR	—	-48	-45	dBc
Input Return Loss	IRL	—	-12	-6	dB
Typical Performances OFDM Signal - 10 MHz Channel Bandwidth (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 130 mA, I_{DQ2} = 230 mA, P_{out} = 5 W Avg., f = 3400 MHz and f = 3600 MHz, WiMAX, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF.					
Relative Constellation Error (4)	RCE	—	-33	—	dB
Error Vector Magnitude (4)	EVM	—	2.2	—	% rms

1. V_{GG} = 1.22 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
2. Part internally matched both on input and output.
3. Measurement made with device in straight lead configuration before any lead forming operation is applied.
4. RCE = 20Log(EVM/100).

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 130 mA, I_{DQ2} = 230 mA, 3400–3600 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	30	—	W
IMD Symmetry @ 2 W PEP, P_{out} where IMD Third Order Intermodulation ≧ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	83	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	90	—	MHz
Gain Flatness in 200 MHz Bandwidth @ P_{out} = 5 W Avg.	G_F	—	0.7	—	dB
Average Deviation from Linear Phase in 200 MHz Bandwidth @ P_{out} = 25 W CW	Φ	—	3.15	—	°
Average Group Delay @ P_{out} = 25 W CW, f = 3500 MHz	Delay	—	3.21	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 25 W CW, f = 3500 MHz, Six Sigma Window	ΔΦ	—	13.88	—	°
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.046	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.015	—	dB/°C
Typical Driver Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 190 mA, I_{DQ2} = 230 mA, P_{out} = 0.5 W Avg., f = 3400 MHz and f = 3600 MHz, WiMAX, OFDM 802.16d, 64 QAM $^3/_4$, 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF. ACPR measured in 1 MHz Channel Bandwidth @ ±8.5 MHz Offset.					
Power Gain	G_{ps}	—	23.5	—	dB
Power Added Efficiency	PAE	—	3.5	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	—	9.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	–55	—	dBc
Input Return Loss	IRL	—	–12	—	dB



Z1	0.118″ x 0.044″ Microstrip	Z17	0.230″ x 0.090″ Microstrip	Z32	0.080″ x 0.112″ Microstrip
Z2	0.205″ x 0.044″ Microstrip	Z18	0.125″ x 0.125″ Microstrip	Z33	0.193″ x 0.044″ Microstrip
Z3	0.083″ x 0.096″ Microstrip	Z19	0.228″ x 0.100″ Microstrip	Z34	0.080″ x 0.051″ Microstrip
Z4	0.195″ x 0.044″ Microstrip	Z20	0.076″ x 0.165″ Microstrip	Z35	0.157″ x 0.055″ Microstrip
Z5	0.094″ x 0.132″ Microstrip	Z21	0.289″ x 0.100″ Microstrip	Z36	0.080″ x 0.044″ Microstrip
Z6	0.509″ x 0.044″ Microstrip	Z22	0.083″ x 0.110″ Microstrip	Z37	0.080″ x 0.131″ Microstrip
Z7	0.083″ x 0.091″ Microstrip	Z23	0.375″ x 0.100″ Microstrip	Z38	0.040″ x 0.044″ Microstrip
Z8	0.372″ x 0.044″ Microstrip	Z24	0.185″ x 0.080″ Microstrip	Z39	0.073″ x 0.044″ Microstrip
Z9	0.078″ x 0.192″ Microstrip	Z25	0.079″ x 0.020″ Microstrip	Z40	0.574″ x 0.044″ Microstrip
Z10	0.078″ x 0.044″ Microstrip	Z26	0.185″ x 0.020″ Microstrip	Z41	L = 0.305″ wi = 0.150″ Angle = 130° Microstrip
Z11	0.079″ x 0.141″ Microstrip	Z27	0.185″ x 0.100″ Microstrip	Z42	0.523″ x 0.044″ Microstrip
Z12	0.243″ x 0.044″ Microstrip	Z28	0.093″ x 0.100″ Microstrip	Z43	0.574″ x 0.044″ Microstrip
Z13	0.605″ x 0.044″ Microstrip	Z29	0.063″ x 0.044″ Microstrip	Z44	L = 0.305″ wi = 0.150″ Angle = 130° Microstrip
Z14	0.232″ x 0.340″ Microstrip	Z30	0.103″ x 0.044″ Microstrip	Z45	0.523″ x 0.044″ Microstrip
Z15	0.042″ x 0.340″ Microstrip	Z31	0.080″ x 0.121″ Microstrip	PCB	Taconic TLX8-0300, 0.020″, ε_r = 2.55
Z16	0.112″ x 0.150″ Microstrip				

Figure 3. MW7IC3825NR1(GNR1)(NBR1) Test Circuit Schematic

Table 6. MW7IC3825NR1(GNR1)(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C13, C14	2.2 μF, 50 V Chip Capacitors	C3225X7R1H225M	TDK
C2, C3	10 μF, 50 V Chip Capacitors	C5750X5R1H106M	TDK
C4, C5, C9, C10	2.2 pF Chip Capacitors	ATC100B2R2BT500XT	ATC
C6, C7	0.5 pF Chip Capacitors	ATC100B0R5BT500XT	ATC
C8	2 pF Chip Capacitor	ATC100B2R0BT500XT	ATC
C11	33 pF Chip Capacitor	ATC100B330JT500XT	ATC
C12	220 μF, 63 V Electrolytic Capacitor	222213668221	BC Components
C15, C16	4.7 μF, 50 V Chip Capacitors	C4532X5R1H475M	TDK
C17	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
R1, R2	1 kΩ, 1/8 W Chip Resistors	CRCW08051001FKEA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

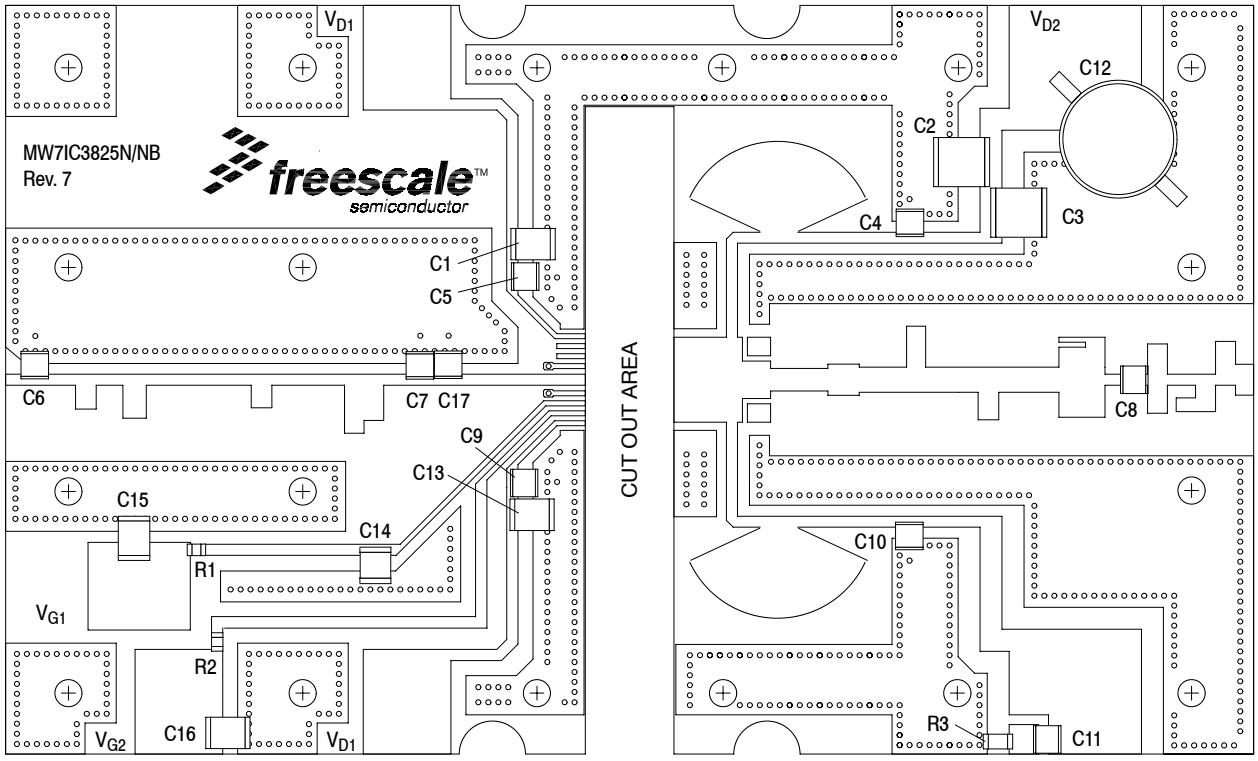


Figure 4. MW7IC3825NR1(GNR1)(NBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

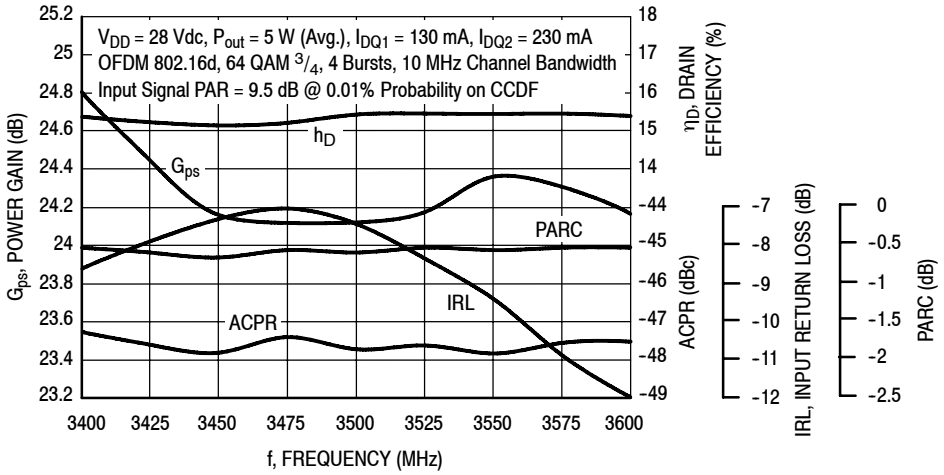


Figure 5. WiMAX Broadband Performance @ P_{out} = 5 Watts Avg.

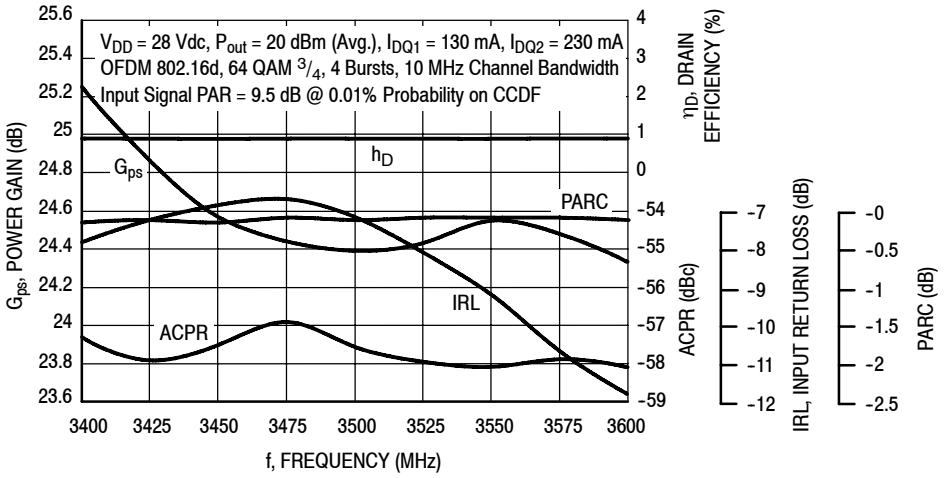


Figure 6. WiMAX Broadband Performance @ P_{out} = 20 dBm Avg.

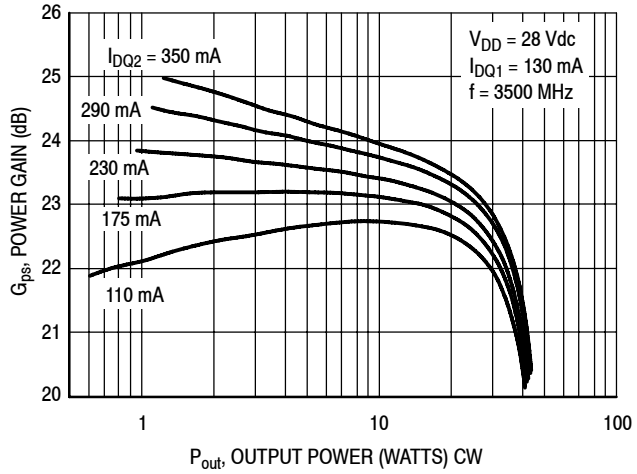


Figure 7. Power Gain versus Output Power @ I_{DQ1} = 130 mA

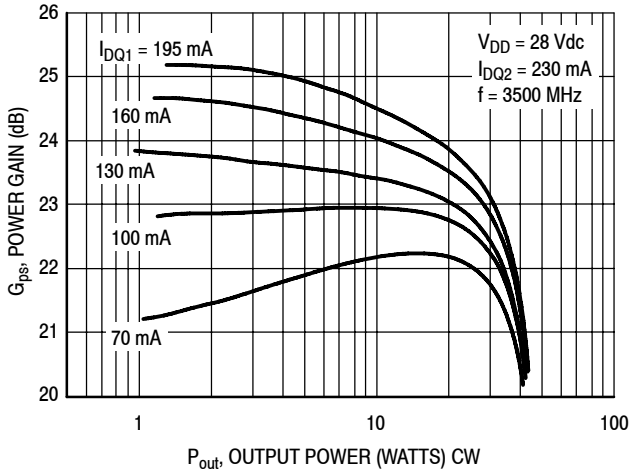


Figure 8. Power Gain versus Output Power @ I_{DQ2} = 230 mA

TYPICAL CHARACTERISTICS

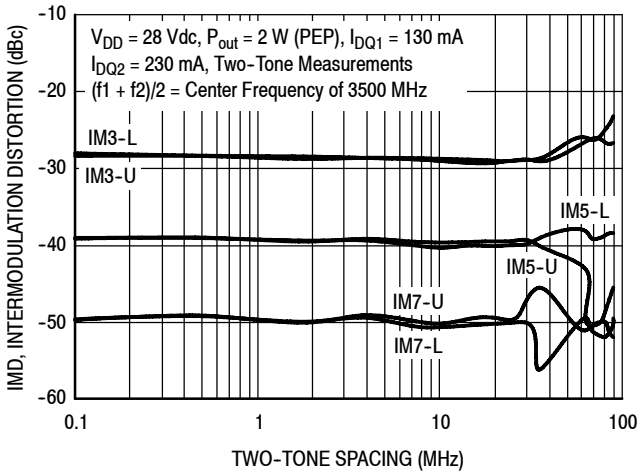


Figure 9. Intermodulation Distortion Products versus Tone Spacing

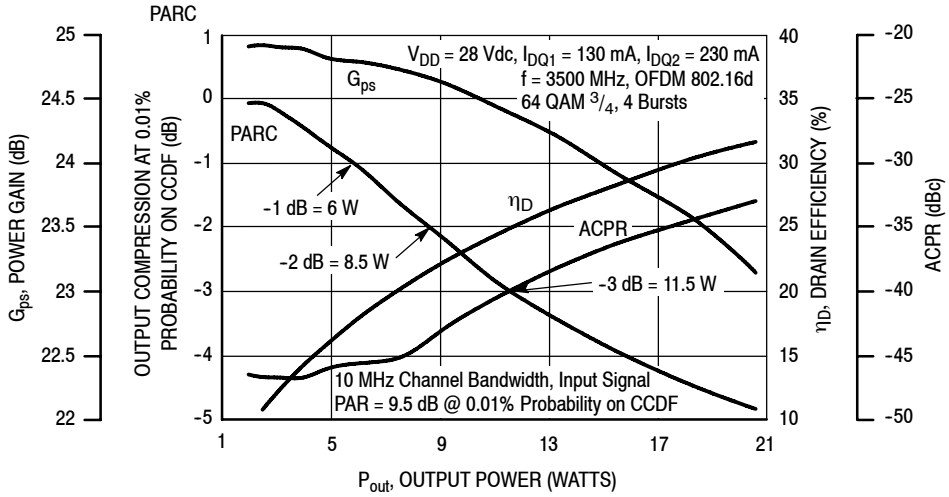


Figure 10. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

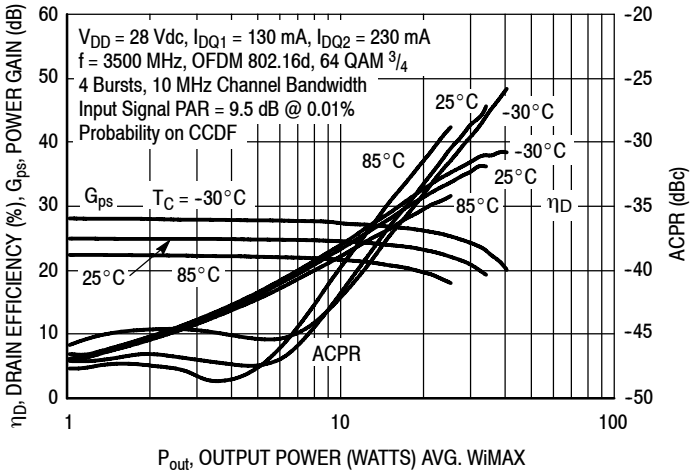


Figure 11. WiMAX, ACPR, Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS

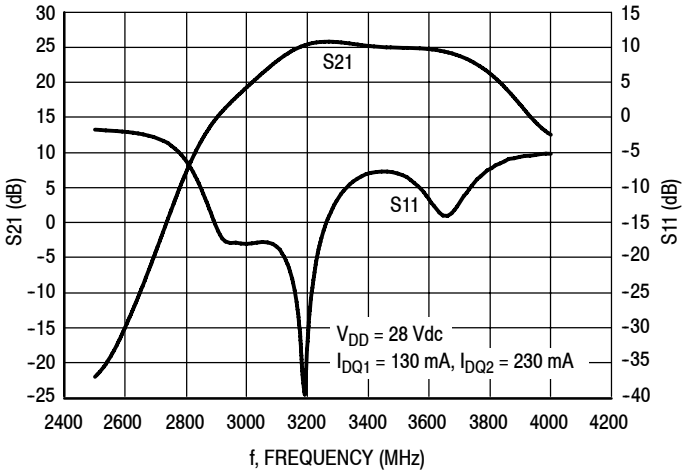
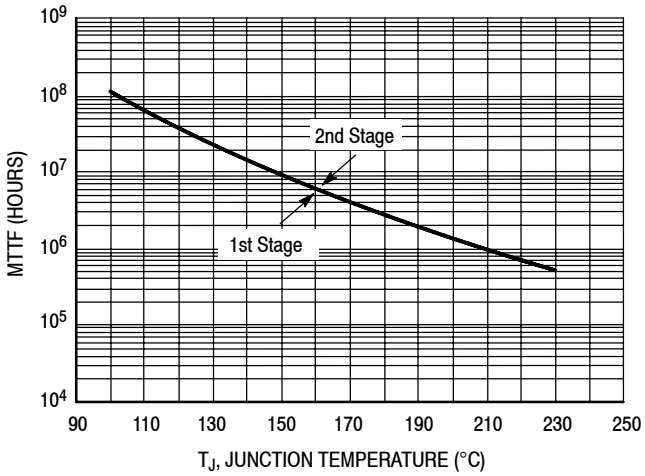


Figure 12. Broadband Frequency Response



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 5 W Avg., and PAE = 15%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 13. MTTF versus Junction Temperature

WIMAX TEST SIGNAL

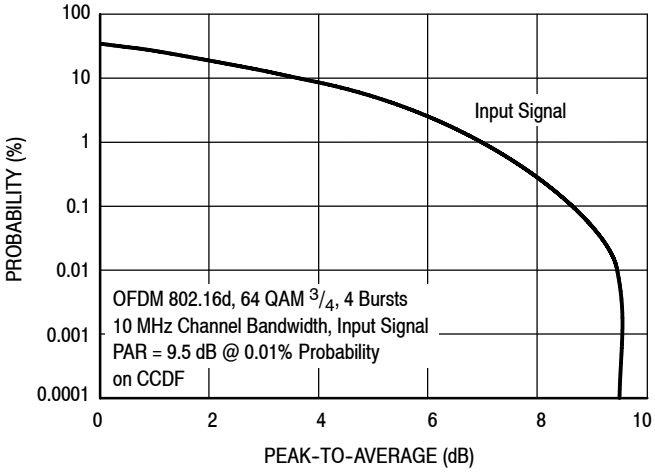


Figure 14. OFDM 802.16d Test Signal

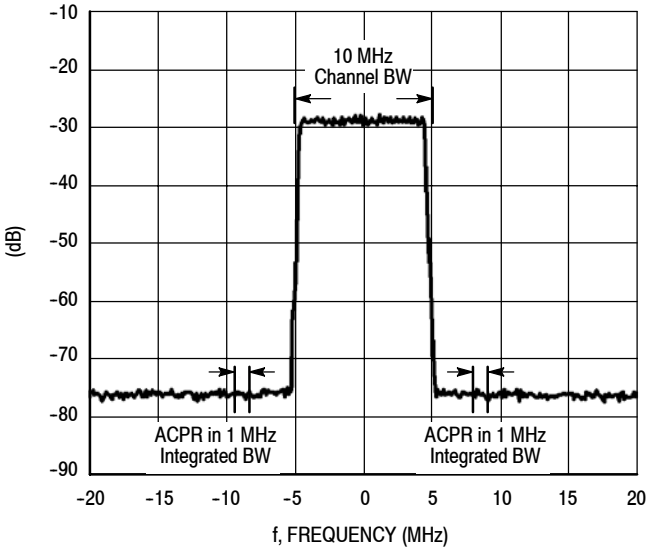
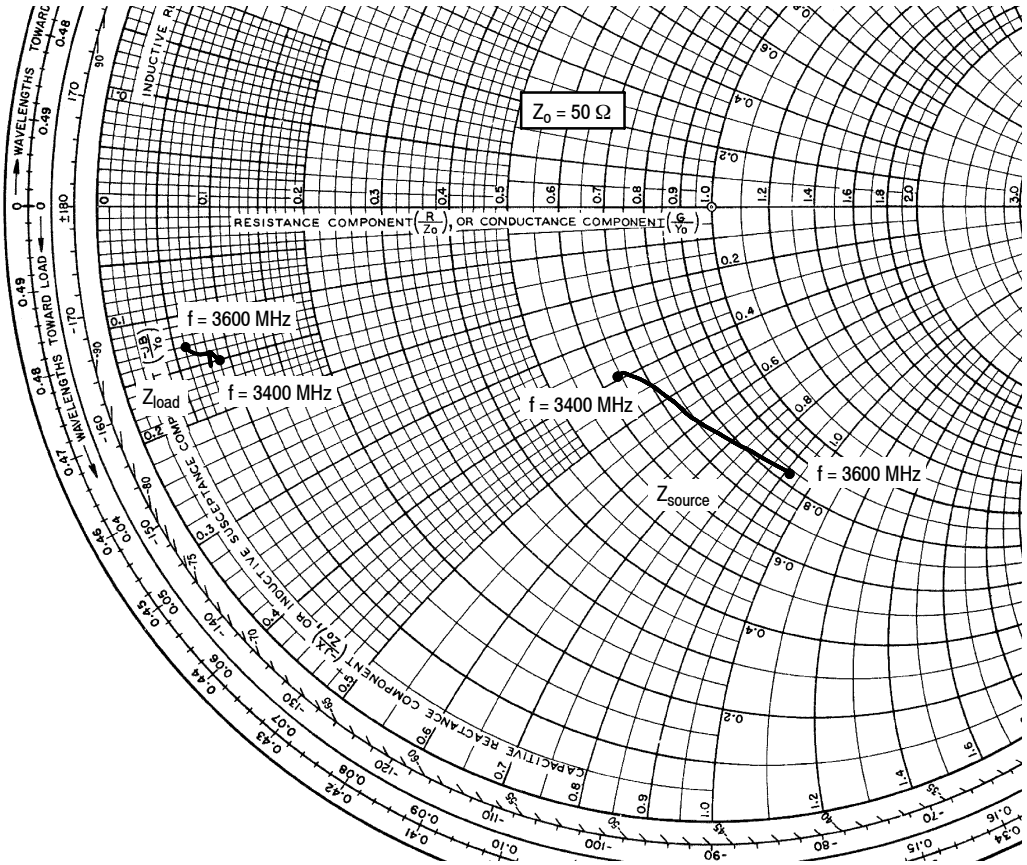


Figure 15. WiMAX Spectrum Mask Specifications



V_{DD} = 28 Vdc, I_{DQ1} = 130 mA, I_{DQ2} = 230 mA, P_{out} = 5 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
3400	31.82 – j19.29	4.58 – j7.62
3425	32.86 – j19.70	4.42 – j7.33
3450	33.95 – j20.93	4.22 – j7.20
3475	35.11 – j22.97	4.13 – j7.22
3500	36.33 – j25.82	4.13 – j7.26
3525	37.61 – j29.49	4.07 – j7.20
3550	38.95 – j33.97	3.81 – j6.99
3575	40.35 – j39.26	3.48 – j6.77
3600	41.81 – j45.37	3.21 – j6.72

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

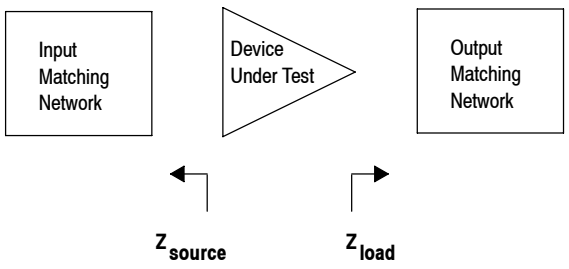
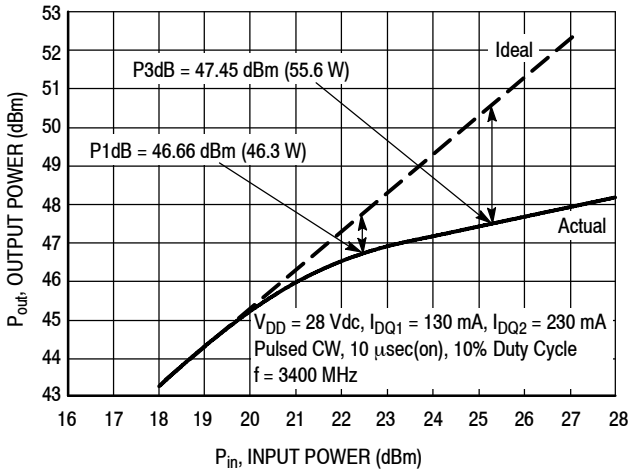


Figure 16. Series Equivalent Source and Load Impedance

Table 7. Common Source S-Parameters (V_{DD} = 28 V, I_{DQ1} = 130 mA, I_{DQ2} = 230 mA, T_A = 25°C, 50 Ohm System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
3000	0.260	-47.0	7.550	-61.6	0.00485	-43.9	0.724	-87.7
3050	0.177	-63.4	8.610	-102.0	0.00423	-72.7	0.713	-113.0
3100	0.139	-68.0	10.000	-143.0	0.00424	-98.1	0.675	-141.0
3150	0.117	-59.6	11.300	177.0	0.00293	-122.0	0.612	-166.0
3200	0.190	-61.1	13.600	139.0	0.00322	-98.2	0.627	171.0
3250	0.283	-85.6	16.800	95.7	0.00533	-118.0	0.629	138.0
3300	0.395	-118.0	19.900	49.1	0.00762	-146.0	0.547	102.0
3350	0.493	-155.0	22.300	0.9	0.00950	-178.0	0.421	65.9
3400	0.575	166.0	24.000	-48.3	0.0116	148.0	0.235	23.1
3450	0.603	126.0	23.800	-99.4	0.0132	111.0	0.053	-130.0
3500	0.537	82.8	19.900	-155.0	0.0135	58.2	0.409	124.0
3550	0.479	56.7	15.600	165.0	0.00994	27.0	0.509	80.6
3600	0.458	29.8	12.900	128.0	0.00810	1.1	0.585	49.7
3650	0.465	1.3	11.200	94.1	0.00680	-19.7	0.637	21.3
3700	0.427	-27.1	9.830	58.3	0.00636	-42.4	0.672	-4.3
3750	0.429	-53.0	8.600	25.7	0.00546	-65.7	0.707	-28.9
3800	0.407	-81.6	7.770	-7.2	0.00476	-82.1	0.730	-53.8
3850	0.395	-110.0	7.020	-39.8	0.00445	-97.7	0.752	-77.2
3900	0.388	-139.0	6.380	-71.8	0.00421	-113.0	0.761	-102.0
3950	0.384	-167.0	5.900	-104.0	0.00454	-126.0	0.779	-125.0
4000	0.389	165.0	5.460	-135.0	0.00531	-145.0	0.779	-150.0

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

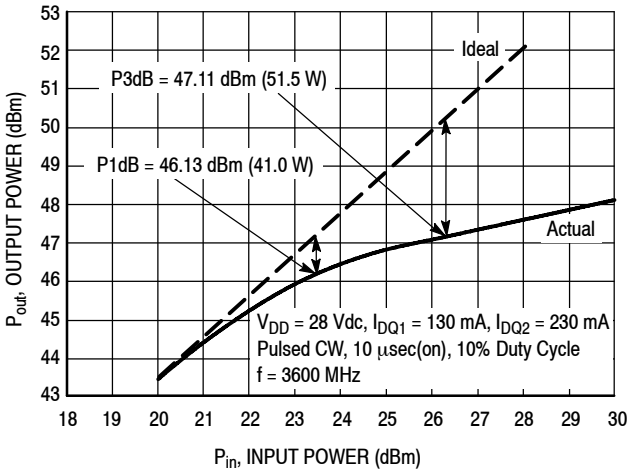


NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	52.4 – j42.5	3.5 – j8.5

Figure 17. Pulsed CW Output Power versus Input Power @ 28 V @ 3400 MHz



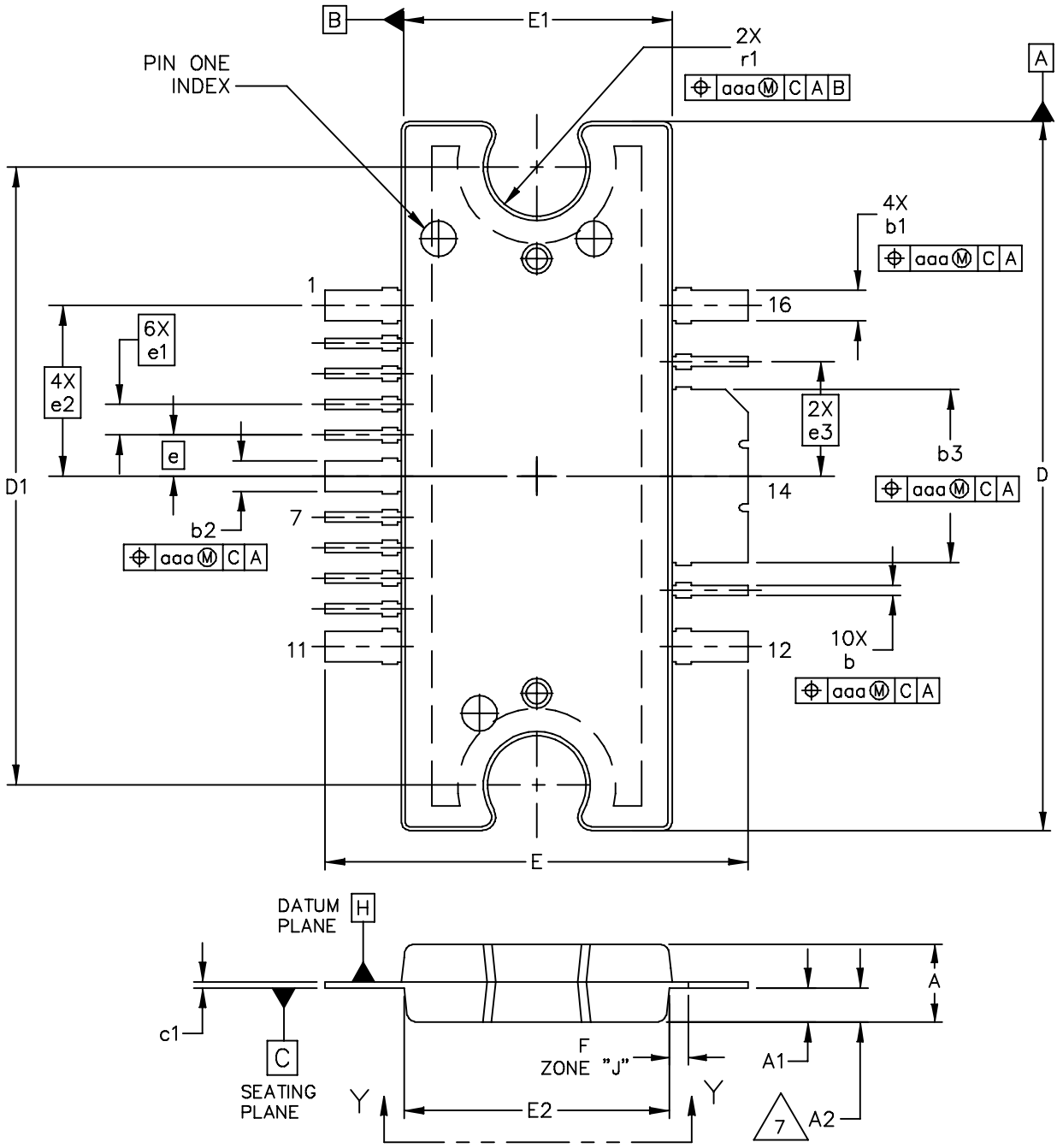
NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

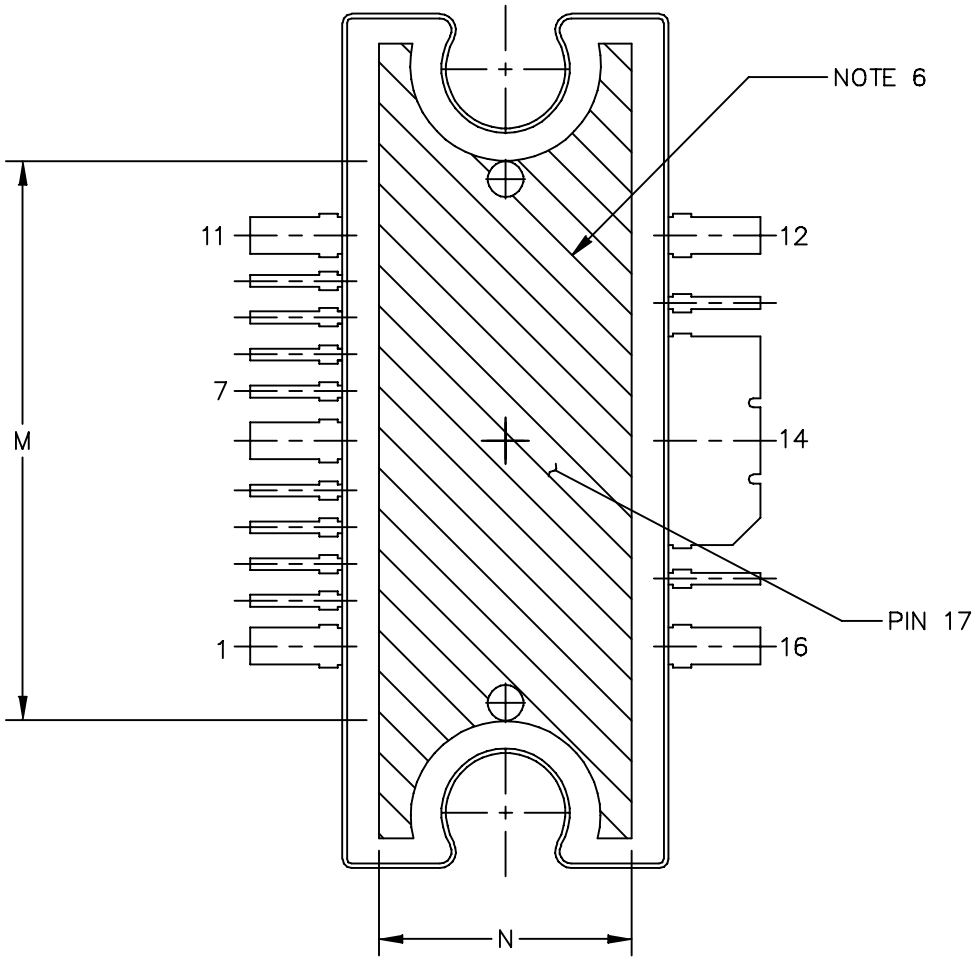
	Z_{source} Ω	Z_{load} Ω
P1dB	126.6 – j41.9	3.3 – j8.3

Figure 18. Pulsed CW Output Power versus Input Power @ 28 V @ 3600 MHz

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-272 WIDE BODY MULTI-LEAD	DOCUMENT NO: 98ARH99164A	REV: P
	CASE NUMBER: 1329-09	18 MAY 2010
	STANDARD: NON-JEDEC	



VIEW Y–Y

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–272 WIDE BODY MULTI–LEAD	DOCUMENT NO: 98ARH99164A	REV: P
	CASE NUMBER: 1329–09	18 MAY 2010
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----					
					aaa	.004		.10	

© FREESCALE SEMICONDUCTOR, INC.
ALL RIGHTS RESERVED.

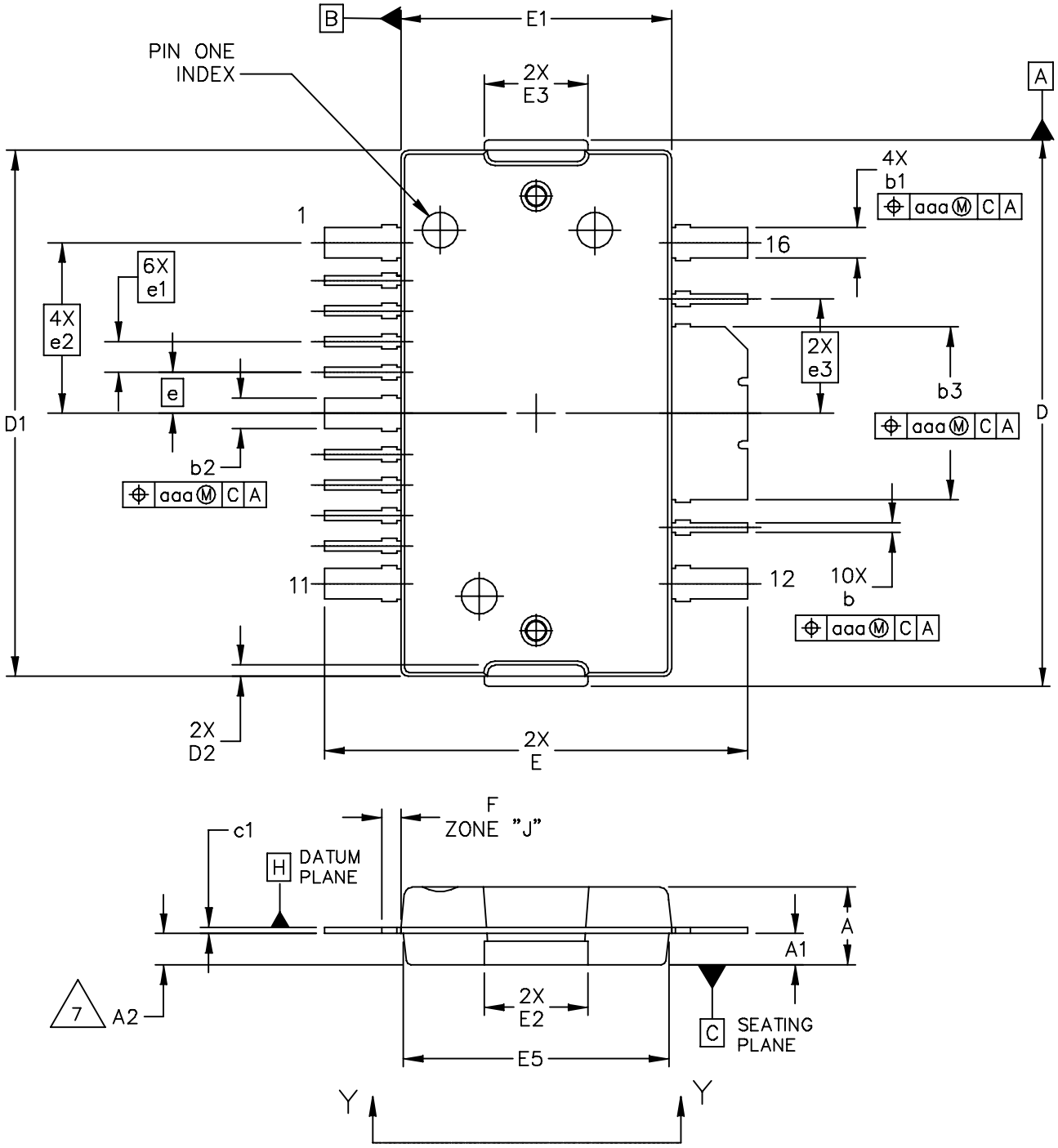
MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: TO–272 WIDE BODY MULTI–LEAD

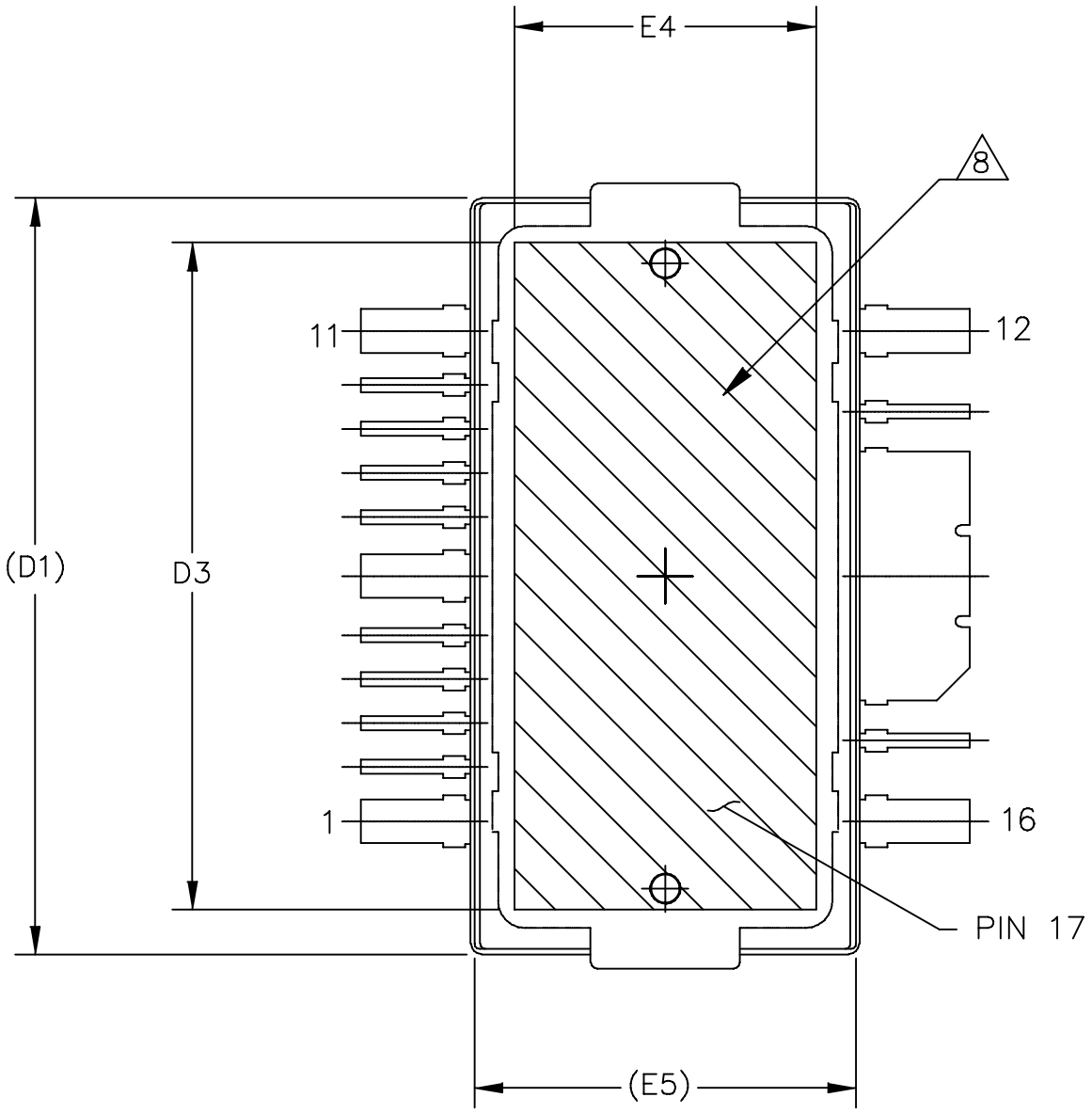
DOCUMENT NO: 98ARH99164A | REV: P

CASE NUMBER: 1329–09 | 18 MAY 2010

STANDARD: NON–JEDEC



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-270 WIDE BODY 16 LEAD	DOCUMENT NO: 98ASA10754D	REV: A
	CASE NUMBER: 1886-01	31 AUG 2007
	STANDARD: NON-JEDEC	



VIEW Y–Y

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270 WIDE BODY 16 LEAD	DOCUMENT NO: 98ASA10754D	REV: A
	CASE NUMBER: 1886–01	31 AUG 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUM –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.011	.017	0.28	0.43
A2	.040	.042	1.02	1.07	b1	.037	.043	0.94	1.09
D	.712	.720	18.08	18.29	b2	.037	.043	0.94	1.09
D1	.688	.692	17.48	17.58	b3	.225	.231	5.72	5.87
D2	.011	.019	0.28	0.48	c1	.007	.011	.18	.28
D3	.600	---	15.24	---	e	.054 BSC		1.37 BSC	
E	.551	.559	14	14.2	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.224 BSC		5.69 BSC	
E2	.132	.140	3.35	3.56	e3	.150 BSC		3.81 BSC	
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

© FREESCALE SEMICONDUCTOR, INC.
ALL RIGHTS RESERVED.

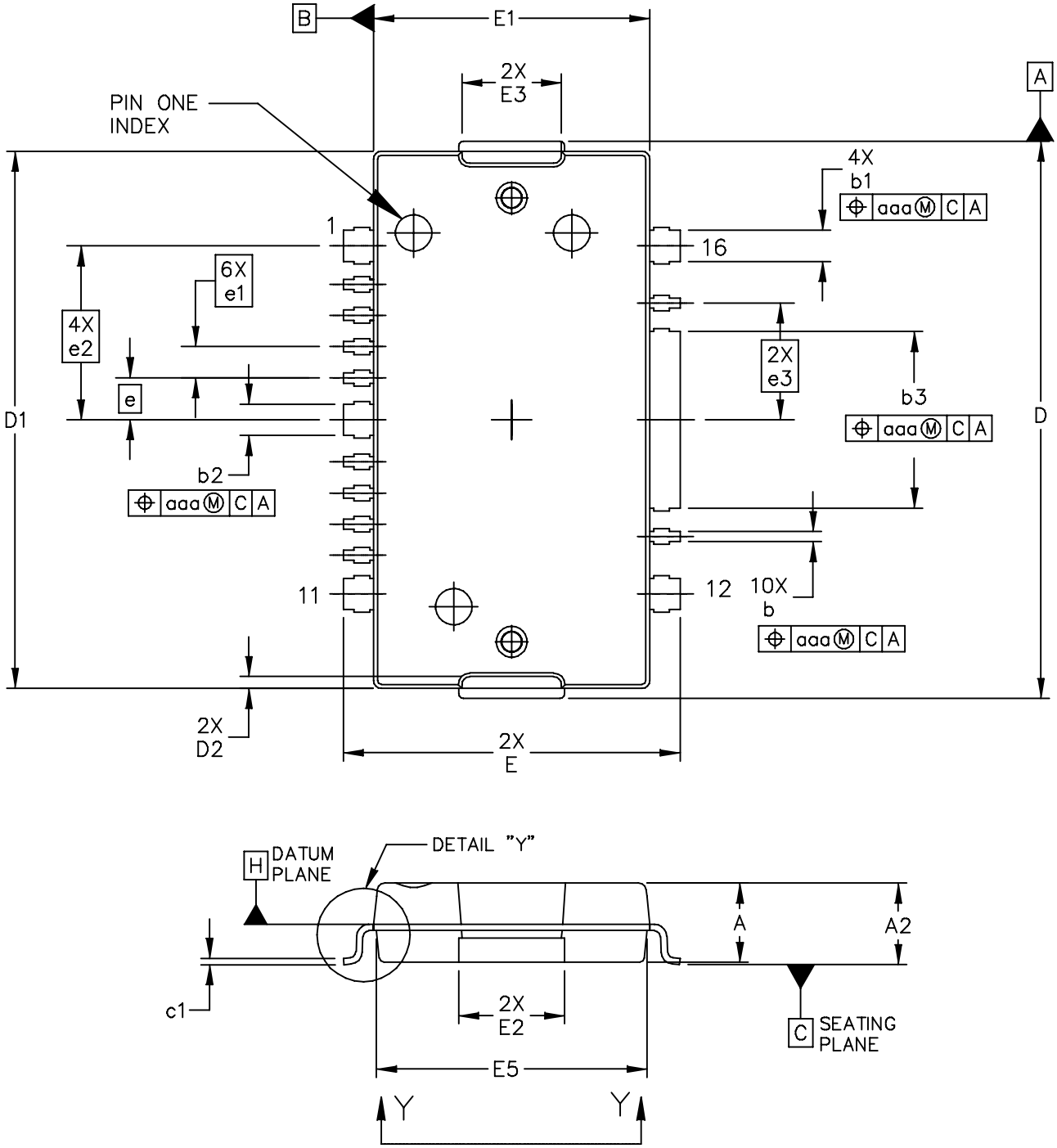
MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: TO–270 WIDE BODY 16 LEAD

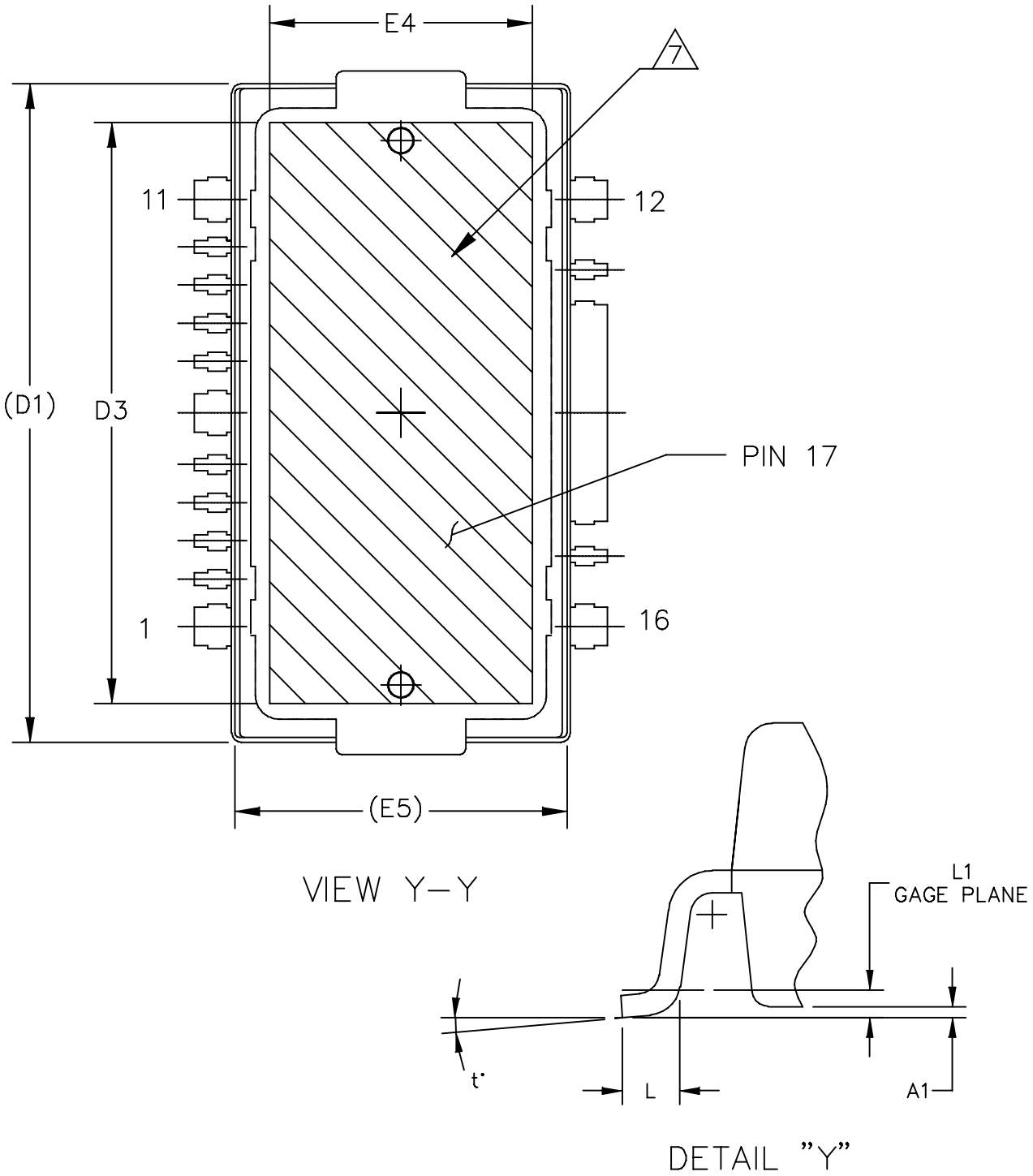
DOCUMENT NO: 98ASA10754D | REV: A

CASE NUMBER: 1886–01 | 31 AUG 2007

STANDARD: NON–JEDEC



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-270 WIDE BODY 16 LEAD, GULL WING	DOCUMENT NO: 98ASA10755D	REV: A
	CASE NUMBER: 1887-01	31 AUG 2007
	STANDARD: NON-JEDEC	



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO–270 WIDE BODY 16 LEAD, GULL WING	DOCUMENT NO: 98ASA10755D	REV: A	
	CASE NUMBER: 1887–01	31 AUG 2007	
	STANDARD: NON–JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUM –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.011	.017	0.28	0.43
D	.712	.720	18.08	18.29	b1	.037	.043	0.94	1.09
D1	.688	.692	17.48	17.58	b2	.037	.043	0.94	1.09
D2	.011	.019	0.28	0.48	b3	.225	.231	5.72	5.87
D3	.600	---	15.24	---	c1	.007	.011	0.18	0.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.132	.140	3.35	3.56	e2	.224 BSC		5.69 BSC	
E3	.124	.132	3.15	3.35	e3	.150 BSC		3.81 BSC	
E4	.270	---	6.86	---	t	2°	8°	2°	8°
E5	.346	.350	8.79	8.89	aaa	.004		0.10	

© FREESCALE SEMICONDUCTOR, INC.
ALL RIGHTS RESERVED.

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10755D	REV: A
TO–270 WIDE BODY 16 LEAD, GULL WING	CASE NUMBER: 1887–01	31 AUG 2007
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2008	• Initial Release of Data Sheet
1	Nov. 2010	• Corrected data sheet to remove “DC Block” from On-chip Matching feature bullet and replaced with “RF Choke to Ground”, p. 1 • Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13628, p. 1, 3 • Added “RF Input Choke to Ground” circuitry to Functional Block Diagram and Test Circuit Schematic, p. 1, 5 • Added Electromigration MTTF Calculator and RF High Power Model availability to Product Software, p. 22

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals”, must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.
© Freescale Semiconductor, Inc. 2008, 2010. All rights reserved.

Document Number: MW7IC3825N
Rev. 1, 11/2010