

# SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

- Meet or Exceed the Requirements of ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.10 and V.11
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noise Environments
- Driver Positive- and Negative-Current Limiting
- Thermal Shutdown Protection
- Driver 3-State Outputs
- Receiver Common-Mode Input Voltage Range of –12 V to 12 V
- Receiver Input Sensitivity . . .  $\pm 200$  mV
- Receiver Hysteresis . . . 50 mV Typ
- Receiver Input Impedance . . . 12 k $\Omega$  Min
- Receiver 3-State Outputs (SN751177 Only)
- Operate From Single 5-V Supply

## description

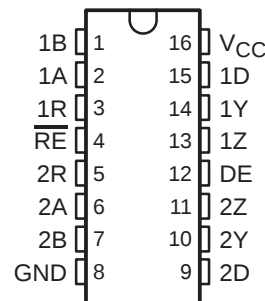
The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits that are designed for balanced multipoint bus transmission at rates up to 10 Mbit/s. They are designed to improve the performance of full-duplex data communications over long bus lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.10 and V.11.

The SN751177 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal-shutdown protection from line-fault conditions on the transmission bus line.

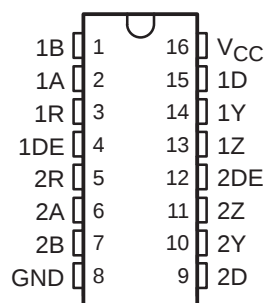
The receiver features high input impedance of at least 12 k $\Omega$ , an input sensitivity of  $\pm 200$  mV over a common-mode input voltage range of –12 V to 12 V, and typical input hysteresis of 50 mV. Fail-safe design ensures that if the receiver inputs are open, the receiver outputs always will be high.

The SN751177 and SN751178 are characterized for operation from –20°C to 85°C.

SN751177 . . . N OR NS<sup>†</sup> PACKAGE  
(TOP VIEW)



SN751178 . . . N OR NS<sup>†</sup> PACKAGE  
(TOP VIEW)



<sup>†</sup> The NS package is only available taped and reeled.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN751177, SN751178

## DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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### Function Tables

**SN751177, SN751178**  
(each driver)

| INPUT<br>D | ENABLE<br>DE | OUTPUTS |   |
|------------|--------------|---------|---|
|            |              | Y       | Z |
| H          | H            | H       | L |
| L          | H            | L       | H |
| X          | L            | Z       | Z |

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off)

**SN751177**  
(each receiver)

| DIFFERENTIAL INPUTS<br>A – B              | ENABLE<br>RE | OUTPUT<br>R |
|-------------------------------------------|--------------|-------------|
| $V_{ID} \geq 0.2 \text{ V}$               | L            | H           |
| $-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$ | L            | ?           |
| $V_{ID} \leq -0.2 \text{ V}$              | L            | L           |
| X                                         | H            | Z           |
| Open                                      | L            | H           |

H = high level, L = low level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)

**SN751178**  
(each receiver)

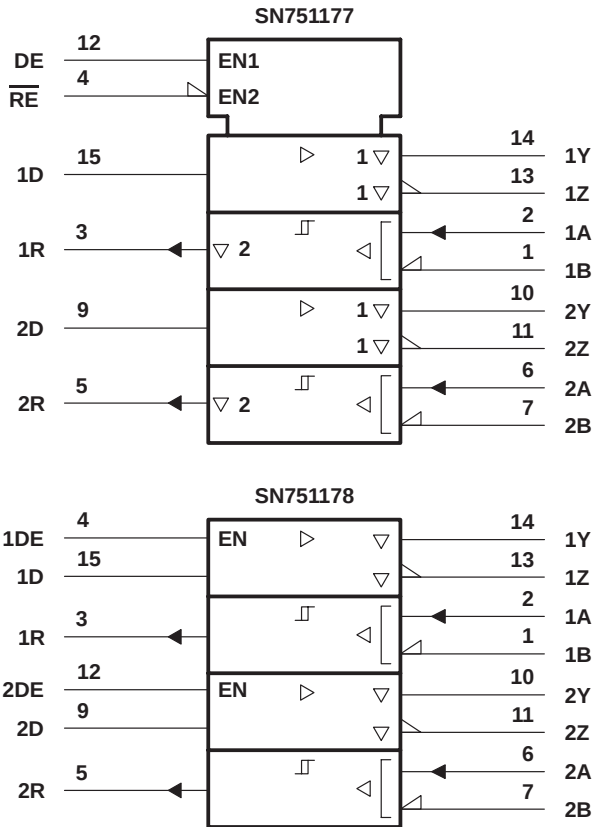
| DIFFERENTIAL INPUTS<br>A – B              | OUTPUT<br>R |
|-------------------------------------------|-------------|
| $V_{ID} \geq 0.2 \text{ V}$               | H           |
| $-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$ | ?           |
| $V_{ID} \leq -0.2 \text{ V}$              | L           |

H = high level, L = low level,  
? = indeterminate

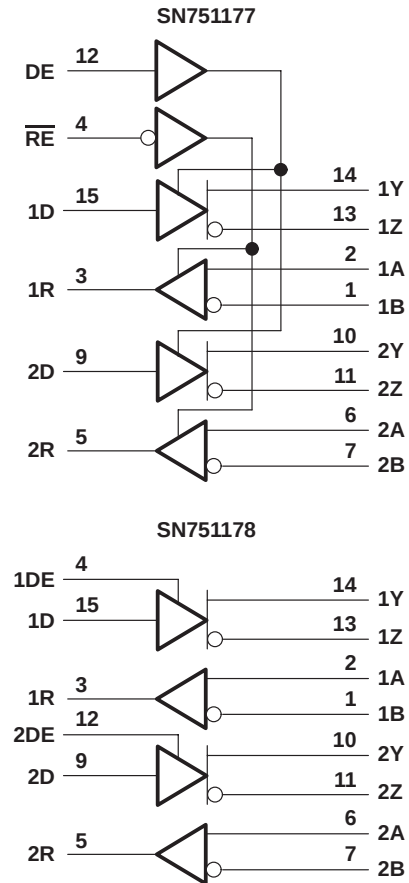
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## logic symbols†

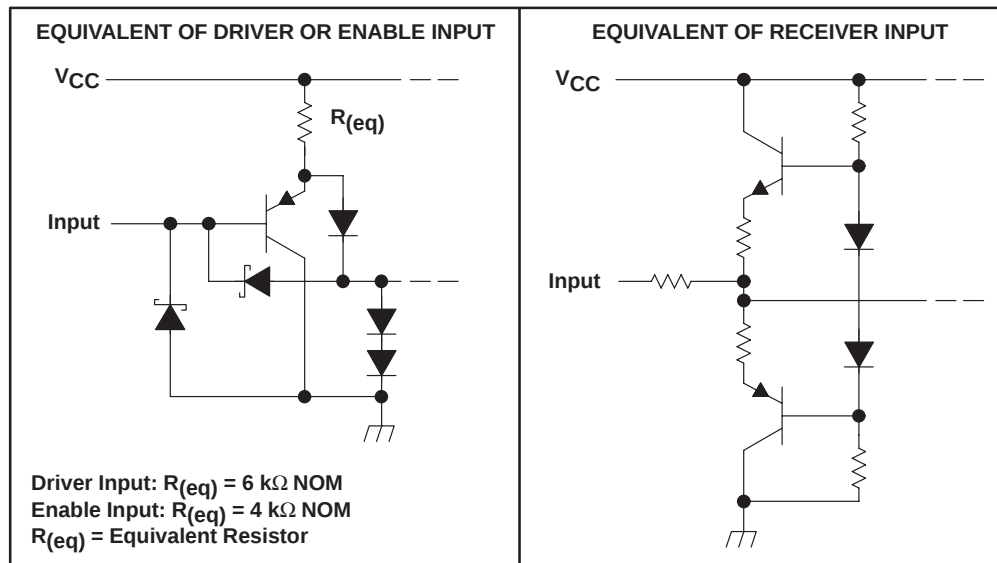


## logic diagrams (positive logic)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## schematics of inputs

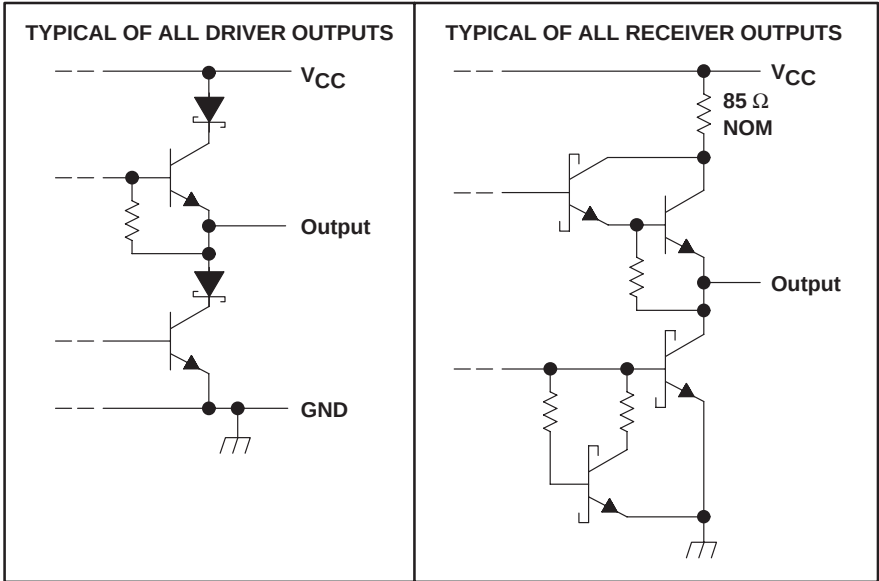


All resistor values are nominal.

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DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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schematics of outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                  |                |
|------------------------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)                            | 7 V            |
| Input voltage, $V_I$ (DE, RE, and D inputs)                      | 7 V            |
| Receiver input voltage range, $V_I$ (A or B inputs)              | –25 V to 25 V  |
| Receiver differential input voltage range, $V_{ID}$ (see Note 2) | –25 V to 25 V  |
| Driver output voltage range, $V_O$                               | –10 V to 15 V  |
| Receiver low-level output current, $I_{OL}$                      | 50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): N package | 78°C/W         |
| NS package                                                       | 111°C/W        |
| Storage temperature range, $T_{stg}$                             | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds     | 260°C          |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.  
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.  
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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## recommended operating conditions

|                                                |                                    | MIN             | NOM | MAX  | UNIT  |
|------------------------------------------------|------------------------------------|-----------------|-----|------|-------|
| Supply voltage, V <sub>CC</sub>                |                                    | 4.75            | 5   | 5.25 | V     |
| High-level input voltage, V <sub>IH</sub>      | DE, $\overline{RE}$ , and D inputs | 2               |     |      | V     |
| Low-level input voltage, V <sub>IL</sub>       |                                    | 0.8             |     |      | V     |
| Common-mode output voltage, V <sub>OC</sub>    | Driver                             | −7 <sup>†</sup> |     |      | V     |
| High-level output current, I <sub>OH</sub>     |                                    | −60             |     |      | mA    |
| Low-level output current, I <sub>OL</sub>      |                                    | 60              |     |      | mA    |
| Common-mode input voltage, V <sub>IC</sub>     | Receiver                           | ±12             |     |      | V     |
| Differential input voltage, V <sub>ID</sub>    |                                    | ±12             |     |      | V     |
| High-level output current, I <sub>OH</sub>     |                                    | −400            |     |      | μA    |
| Low-level output current, I <sub>OL</sub>      |                                    | 16              |     |      | mA    |
| Operating free-air temperature, T <sub>A</sub> |                                    | −20             |     |      | 85 °C |

<sup>†</sup> The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

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## DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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### DRIVER SECTIONS

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

| PARAMETER                                                                        | TEST CONDITIONS                                                               | MIN                         | TYP† | MAX       | UNIT          |
|----------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-----------------------------|------|-----------|---------------|
| $V_{IK}$ Input clamp voltage                                                     | $I_I = -18 \text{ mA}$                                                        |                             |      | -1.5      | V             |
| $V_{OH}$ High-level output voltage                                               | $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -33 \text{ mA}$ |                             | 3.7  |           | V             |
| $V_{OL}$ Low-level output voltage                                                | $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = 33 \text{ mA}$  |                             | 1.1  |           | V             |
| $ V_{OD1} $ Differential output voltage                                          | $I_O = 0$                                                                     | 1.5                         |      | 6         | V             |
| $ V_{OD2} $ Differential output voltage                                          | $R_L = 100 \Omega$ , See Figure 1                                             | 2 or $1/2 V_{OD1}^\ddagger$ |      |           | V             |
|                                                                                  | $R_L = 54 \Omega$ , See Figure 1                                              | 1.5                         |      | 5         |               |
| $V_{OD3}$ Differential output voltage                                            | See Note 4                                                                    | 1.5                         |      | 5         | V             |
| $\Delta V_{OD} $ Change in magnitude of differential output voltage (see Note 5) | $R_L = 54 \Omega$ or $100 \Omega$ , See Figure 1                              |                             |      | $\pm 0.2$ | V             |
| $V_{OC}$ Common-mode output voltage                                              |                                                                               | -1 <sup>§</sup>             |      | 3         | V             |
| $\Delta V_{OC} $ Change in magnitude of common-mode output voltage (see Note 5)  |                                                                               |                             |      | $\pm 0.2$ | V             |
| $I_O$ Output current with power off                                              | $V_{CC} = 0$ , $V_O = -7 \text{ V to } 12 \text{ V}$                          |                             |      | $\pm 100$ | $\mu\text{A}$ |
| $I_{OZ}$ High-impedance-state output current                                     | $V_O = -7 \text{ V to } 12 \text{ V}$                                         |                             |      | $\pm 100$ | $\mu\text{A}$ |
| $I_{IH}$ High-level input current                                                | $V_{IH} = 2.7 \text{ V}$                                                      |                             |      | 20        | $\mu\text{A}$ |
| $I_{IL}$ Low-level input current                                                 | $V_{IL} = 0.4 \text{ V}$                                                      |                             |      | -100      | $\mu\text{A}$ |
| $I_{OS}$ Short-circuit output current (see Note 6)                               | $V_O = -7 \text{ V}$                                                          |                             |      | -250      | mA            |
|                                                                                  | $V_O = V_{CC}$                                                                |                             |      | 250       |               |
|                                                                                  | $V_O = 12 \text{ V}$                                                          |                             |      | 250       |               |
| $I_{CC}$ Supply current                                                          | No load                                                                       | Outputs enabled             |      | 80        | mA            |
|                                                                                  |                                                                               | Outputs disabled            |      | 50        |               |

† All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

‡ The minimum  $V_{OD2}$  with a  $100\text{-}\Omega$  load is either  $1/2 V_{OD1}$  or  $2 \text{ V}$ , whichever is greater.

§ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 4. See TIA/EIA-485-A Figure 3.5, Test Termination Measurement 2

5.  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from a high level to a low level.

6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

### switching characteristics at $V_{CC} = 5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$

| PARAMETER                                                   | TEST CONDITIONS                   | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------|-----------------------------------|-----|-----|-----|------|
| $t_d(\text{OD})$ Differential output delay time             | $R_L = 54 \Omega$ , See Figure 3  |     | 20  | 25  | ns   |
| $t_t(\text{OD})$ Differential output transition time        |                                   |     | 27  | 35  | ns   |
| $t_{PLH}$ Propagation delay time, low- to high-level output | $R_L = 27 \Omega$ , See Figure 4  |     | 20  | 25  | ns   |
| $t_{PHL}$ Propagation delay time, high- to low-level output |                                   |     | 20  | 25  | ns   |
| $t_{PZH}$ Output enable time to high level                  | $R_L = 110 \Omega$ , See Figure 5 |     | 80  | 120 | ns   |
| $t_{PZL}$ Output enable time to low level                   | $R_L = 110 \Omega$ , See Figure 6 |     | 40  | 60  | ns   |
| $t_{PHZ}$ Output disable time from high level               | $R_L = 110 \Omega$ , See Figure 5 |     | 90  | 120 | ns   |
| $t_{PLZ}$ Output disable time from low level                | $R_L = 110 \Omega$ , See Figure 6 |     | 30  | 45  | ns   |



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## SYMBOL EQUIVALENTS

| DATA-SHEET<br>PARAMETER | TIA/EIA-422-B             | TIA/EIA-485-A                          |
|-------------------------|---------------------------|----------------------------------------|
| $ V_{OD1} $             | $V_O$                     | $V_O$                                  |
| $ V_{OD2} $             | $V_t (R_L = 100 \Omega)$  | $V_t (R_L = 54 \Omega)$                |
| $ V_{OD3} $             |                           | $V_t$ (Test Termination Measurement 2) |
| $\Delta V_{OD} $        | $ V_t  -  \bar{V}_t $     | $ V_t  -  \bar{V}_t $                  |
| $V_{OC}$                | $ V_{OS} $                | $ V_{OS} $                             |
| $\Delta V_{OC} $        | $ V_{OS} - \bar{V}_{OS} $ | $ V_{OS} - \bar{V}_{OS} $              |
| $I_{OS}$                | $ I_{sa} ,  I_{sb} $      |                                        |
| $I_O$                   | $ I_{xa} ,  I_{xb} $      | $I_{ia}, I_{ib}$                       |

## RECEIVER SECTIONS

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER |                                                  | TEST CONDITIONS             |                                         | MIN               | TYP <sup>†</sup> | MAX      | UNIT          |
|-----------|--------------------------------------------------|-----------------------------|-----------------------------------------|-------------------|------------------|----------|---------------|
| $V_{IT+}$ | Positive-going input threshold voltage           | $V_O = 2.7 \text{ V}$ ,     | $I_O = -0.4 \text{ mA}$                 |                   |                  | 0.2      | V             |
| $V_{IT-}$ | Negative-going input threshold voltage           | $V_O = 0.5 \text{ V}$ ,     | $I_O = 16 \text{ mA}$                   | -0.2 <sup>‡</sup> |                  |          | V             |
| $V_{hys}$ | Input hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) |                             |                                         |                   | 50               |          | mV            |
| $V_{IK}$  | Enable clamp voltage                             | SN751177                    | $I_I = -18 \text{ mA}$                  |                   |                  | -1.5     | V             |
| $V_{OH}$  | High-level output voltage                        | $V_{ID} = 200 \text{ mV}$ , | $I_{OH} = -400 \mu\text{A}$             | 2.7               |                  |          | V             |
| $V_{OL}$  | Low-level output voltage                         | $V_{ID} = -200 \text{ mV}$  | $I_{OL} = 8 \text{ mA}$                 |                   |                  | 0.45     | V             |
|           |                                                  |                             | $I_{OL} = 16 \text{ mA}$                |                   |                  | 0.5      |               |
| $I_{OZ}$  | High-impedance-state output current              | SN751177                    | $V_O = 0.4 \text{ V to } 2.4 \text{ V}$ |                   |                  | $\pm 20$ | $\mu\text{A}$ |
| $I_I$     | Line input current (see Note 7)                  | Other input at 0 V          | $V_I = 12 \text{ V}$                    |                   |                  | 1        | mA            |
|           |                                                  |                             | $V_I = -7 \text{ V}$                    |                   |                  | -0.8     |               |
| $I_{IH}$  | High-level enable input current                  | SN751177                    | $V_{IH} = 2.7 \text{ V}$                |                   |                  | 20       | $\mu\text{A}$ |
| $I_{IL}$  | Low-level enable input current                   | SN751177                    | $V_{IL} = 0.4 \text{ V}$                |                   |                  | -100     | $\mu\text{A}$ |
| $I_{OS}$  | Short-circuit output current (see Note 6)        |                             |                                         | -15               |                  | -85      | $\mu\text{A}$ |
| $I_{CC}$  | Supply current                                   | No load,                    | Outputs enabled                         |                   | 80               | 110      | mA            |
| $r_i$     | Input resistance                                 |                             |                                         | 12                |                  |          | k $\Omega$    |

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

7. Refer to ANSI Standards TIA/EIA-422-B, TIA/EIA-423-A, and TIA/EIA-485-A for exact conditions.



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switching characteristics at  $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^{\circ}\text{C}$

| PARAMETER |                                                   | TEST CONDITIONS                                         | MIN | TYP | MAX | UNIT |
|-----------|---------------------------------------------------|---------------------------------------------------------|-----|-----|-----|------|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $V_{ID} = -1.5\text{ V to }1.5\text{ V}$ , See Figure 7 |     | 20  | 35  | ns   |
| $t_{PHL}$ | Propagation delay time, high- to low-level output |                                                         |     | 22  | 35  | ns   |
| $t_{PZH}$ | Output enable time to high level                  | SN751177 See Figure 8                                   |     | 17  | 25  | ns   |
| $t_{PZL}$ | Output enable time to low level                   |                                                         |     | 20  | 27  | ns   |
| $t_{PHZ}$ | Output disable time from high level               |                                                         |     | 25  | 40  | ns   |
| $t_{PLZ}$ | Output disable time from low level                |                                                         |     | 30  | 40  | ns   |

## PARAMETER MEASUREMENT INFORMATION

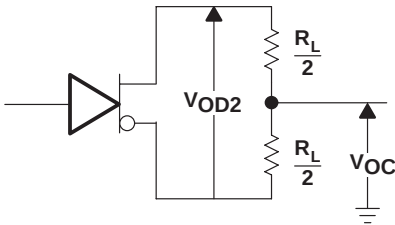


Figure 1. Driver Test Circuit,  $V_{OD}$  and  $V_{OC}$

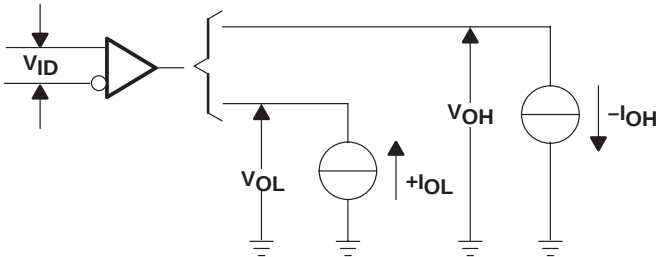
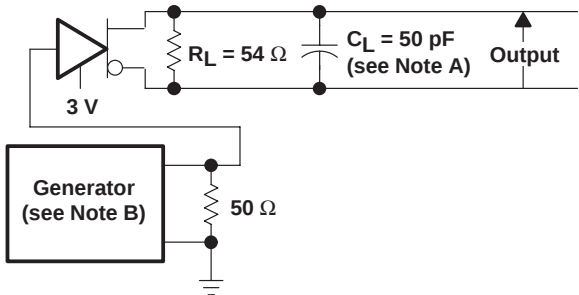
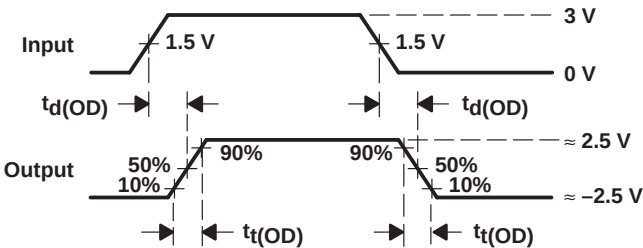


Figure 2. Receiver Test Circuit,  $V_{OH}$  and  $V_{OL}$



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics:  $PRR \leq 1\text{ MHz}$ , 50% duty cycle,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$ .

Figure 3. Driver Differential Output-Delay and Transition-Time Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION

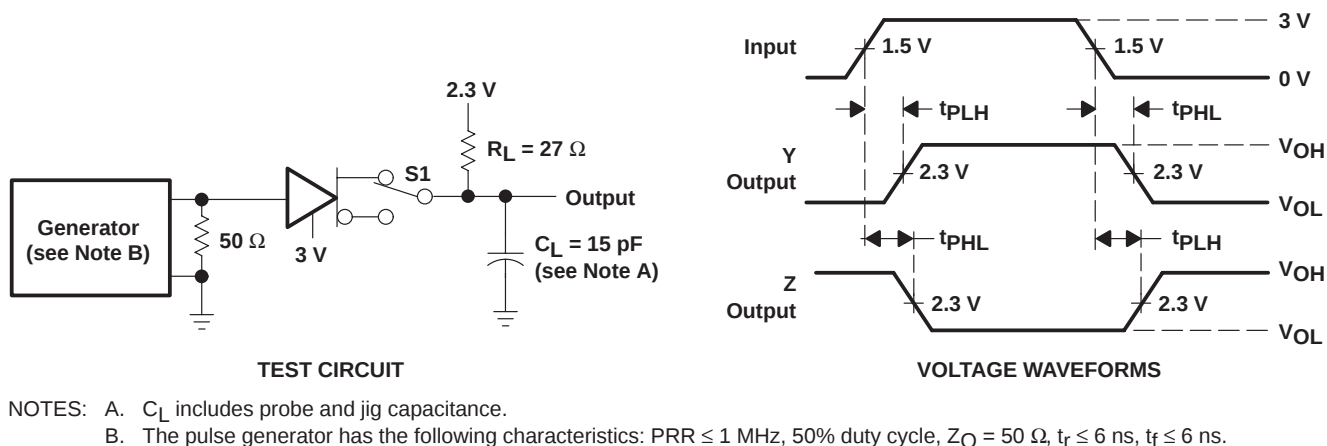


Figure 4. Driver Propagation-Time Test Circuit and Voltage Waveforms

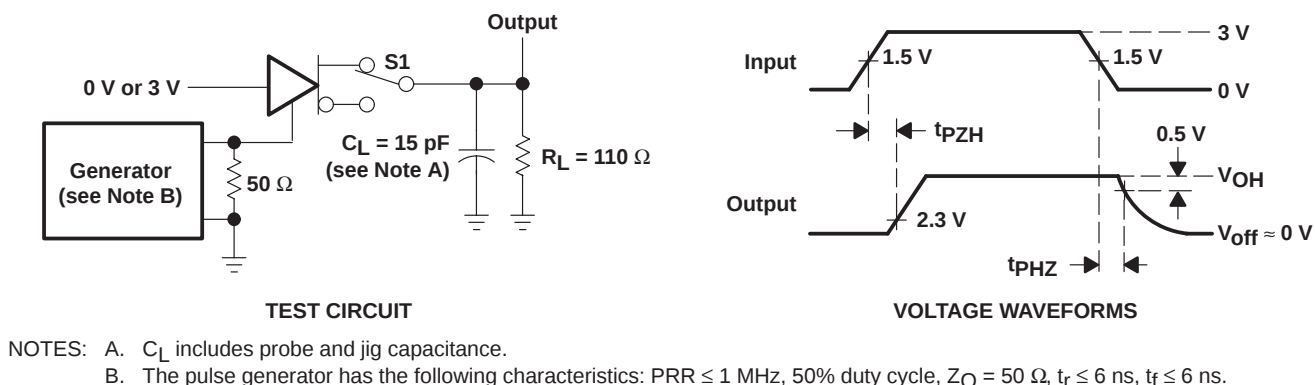


Figure 5. Driver Enable- and Disable-Time Test Circuit and Voltage Waveforms

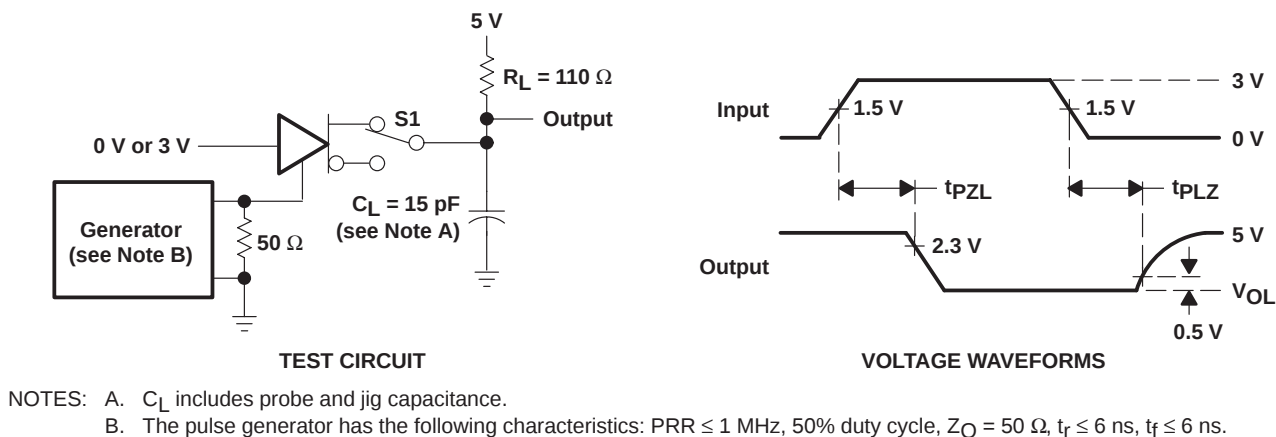
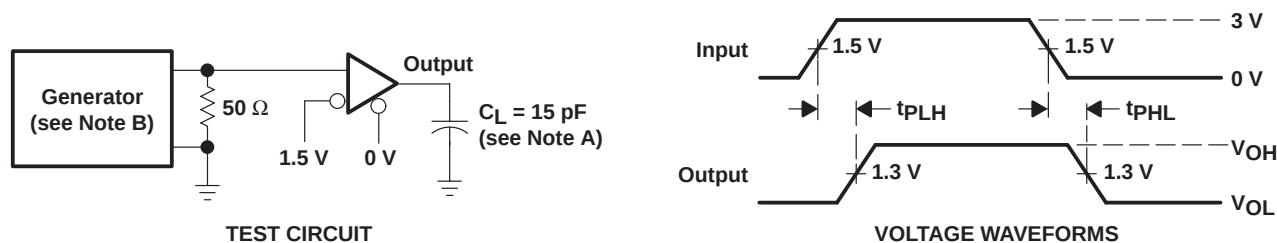


Figure 6. Driver Enable- and Disable-Time Test Circuit and Voltage Waveforms

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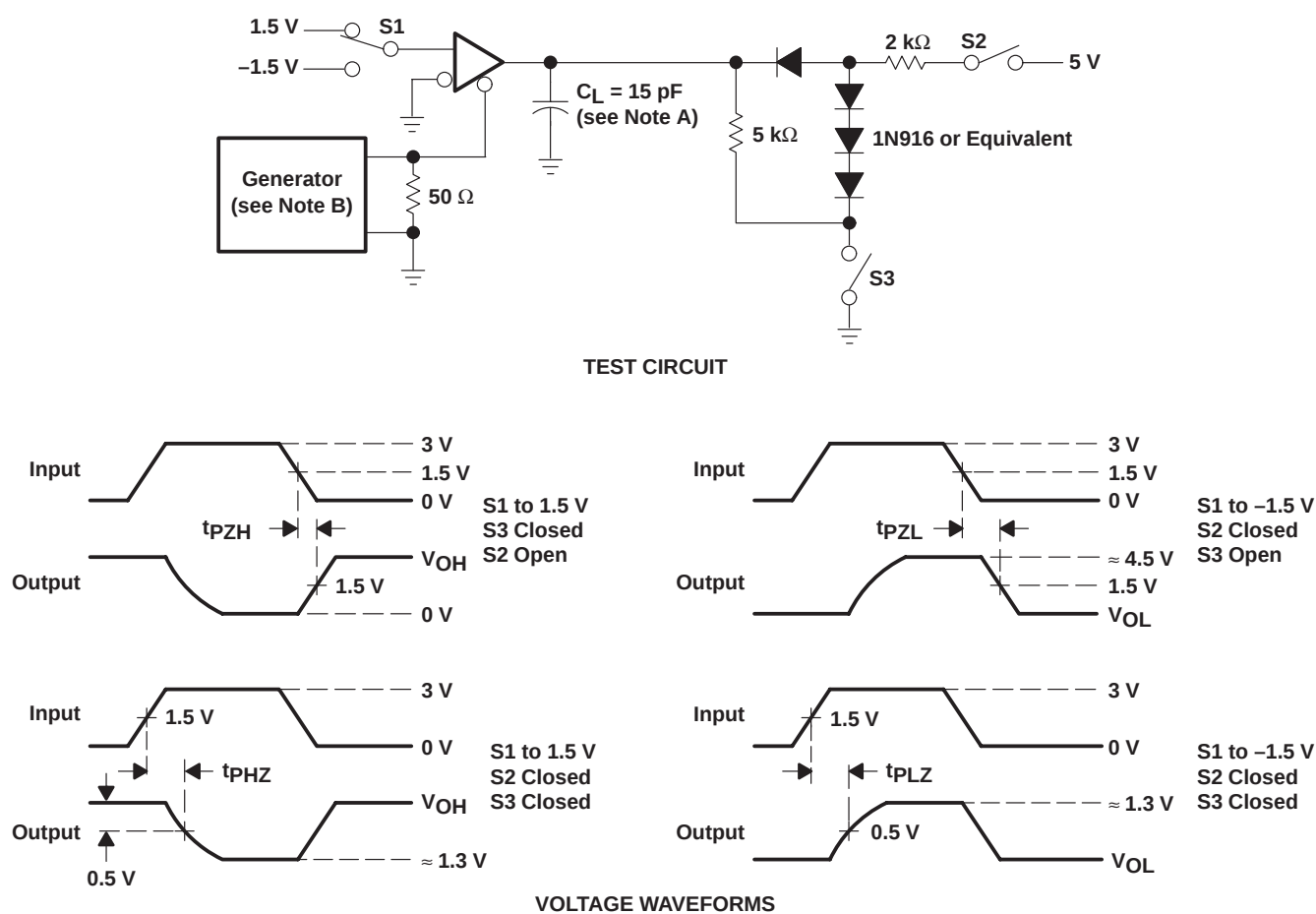
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## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics:  $PRR \leq 1 \text{ MHz}$ , 50% duty cycle,  $Z_O = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ .

Figure 7. Receiver Propagation-Time Test Circuit and Voltage Waveforms



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics:  $PRR \leq 1 \text{ MHz}$ , 50% duty cycle,  $Z_O = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ .

Figure 8. Receiver Output Enable- and Disable-Time Test Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN751177N        | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN751177NE4      | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN751177NSR      | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN751177NSRE4    | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN751177NSRG4    | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN751178N        | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN751178NE4      | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN751178NSR      | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN751178NSRE4    | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN751178NSRG4    | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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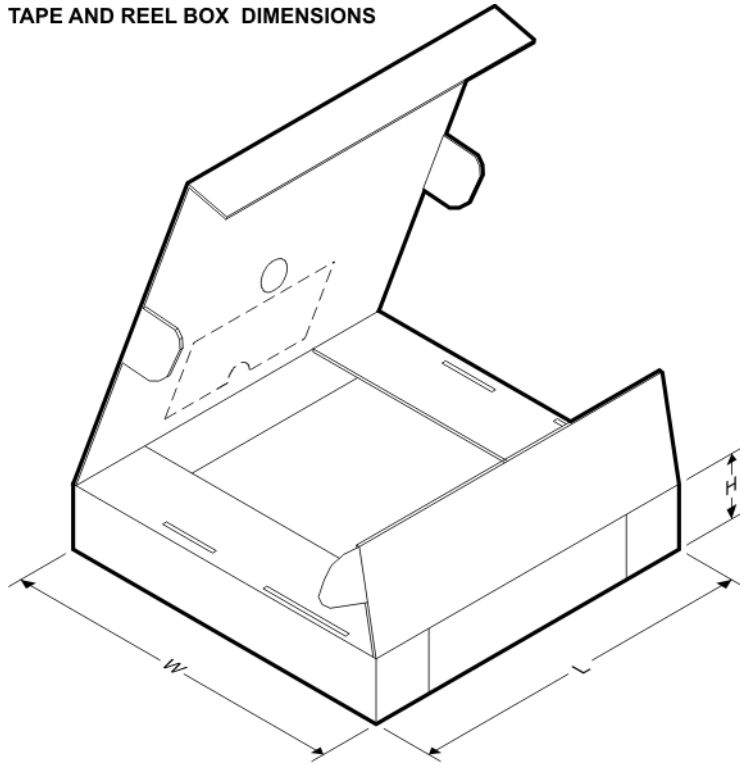
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN751177NSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN751178NSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN751177NSR | SO           | NS              | 16   | 2000 | 346.0       | 346.0      | 33.0        |
| SN751178NSR | SO           | NS              | 16   | 2000 | 346.0       | 346.0      | 33.0        |

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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