NCV4274, NCV4274A

400 mA 2% and 4%Voltage Regulator Family

ON Semiconductor®

http://onsemi.com

Description

The NCV4274 and NCV4274A is a precision micro−power voltage regulator with an output current capability of 400 mA available in the DPAK and D2PAK packages.

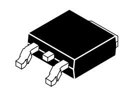
The output voltage is accurate within ±2.0% or ±4.0% depending on the version with a maximum dropout voltage of 0.5 V with an input up to 40 V. Low quiescent current is a feature drawing only 150 μA with a 1 mA load. This part is ideal for automotive and all battery operated microprocessor equipment.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

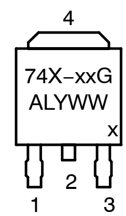
Features

- 2.5, 3.3 V, 5.0 V, ±2.0% and ±4.0% Output Options
- Low 150 μA Quiescent Current at 1 mA load current
- 400 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage with Respect to GND
  - −40 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Very Low Dropout Voltage
- AEC−Q100 Qualified
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- These are Pb−Free Devices

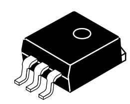
MARKING DIAGRAMS



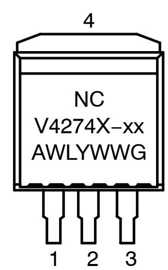
DPAK
DT SUFFIX
CASE 369C



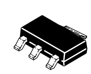
1 Input
2, 4 Ground
3 Output



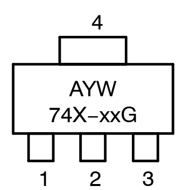
D2PAK
DS SUFFIX
CASE 418AF



1 Input
2, 4 Ground
3 Output



SOT−223
ST SUFFIX
CASE 318E



1 Input
2, 4 Ground
3 Output

X	= A or blank
xx	= Voltage Ratings
A	= Assembly Location
L, WL	= Wafer Lot
Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

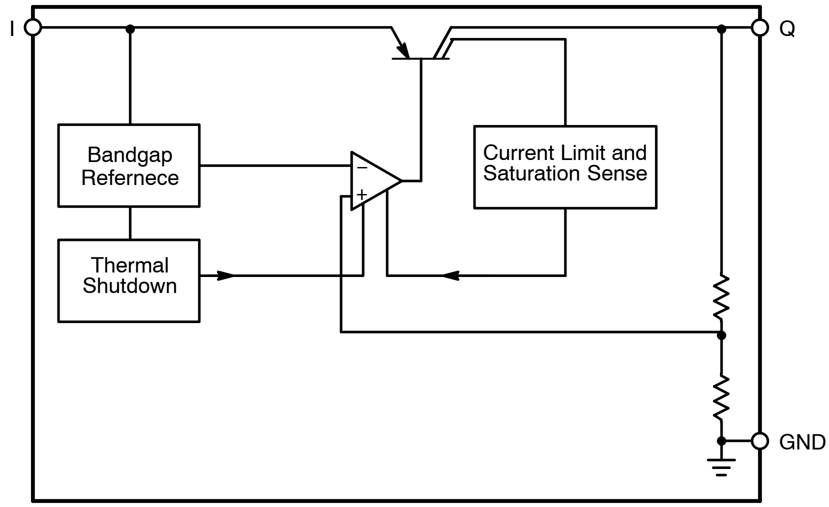


Figure 1. Block Diagram

Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	Input; Bypass directly at the IC a ceramic capacitor to GND.
2,4	GND	Ground
3	Q	Output; Bypass with a capacitor to GND.

1. DPAK 3LD package code 6025
2. D2PAK 3LD package code 6083

ABSOLUTE MAXIMUM RATINGS

Pin Symbol, Parameter		Symbol	Condition	Min	Max	Unit
I, Input−to−Regulator	Voltage	V_I		−42	45	V
	Current	I_I		Internally Limited	Internally Limited	
I, Input peak Transient Voltage to Regulator with Respect to GND		V_I			60	V
Q, Regulated Output	Voltage	V_Q		−1.0	40	V
	Current	I_Q		Internally Limited	Internally Limited	
GND, Ground Current		I_{GND}		–	100	mA
Junction Temperature Storage Temperature		T_J T_{Stg}		– −50	150 150	°C °C
ESD Capability, Human Body Model		ESD_{HB}		4		kV
ESD Capability, Machine Model		ESD_{MM}		200		V
ESD Capability, Charged Device Model		ESD_{CDM}		1		kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD CDM tested per EIA/JES D22/C101, Field Induced Charge Model

OPERATING RANGE

Parameter	Symbol	Condition	Min	Max	Unit
Input Voltage (5.0 V Version)	V_I		5.5	40	V
Input Voltage (3.3 V, and 2.5 V Version)	V_I		4.5	40	V
Junction Temperature	T_J		−40	150	°C

THERMAL RESISTANCE

Parameter		Symbol	Condition	Min	Max	Unit
Junction−to−Ambient	DPAK	R_{thja}		–	70 (Note 4)	°C/W
Junction−to−Ambient	D2PAK	R_{thja}		–	60 (Note 4)	°C/W
Junction−to−Case	DPAK	R_{thjc}		–	4	°C/W
Junction−to−Case	D2PAK	R_{thjc}		–	3	°C/W
Junction−to−Tab	SOT−223	Ψ−JLX, Ψ_{LX}		–	14.5 (Note 5)	°C/W
Junction−to−Ambient	SOT−223	$R_{\theta JA}$, θ_{JA}		–	169.7 (Note 5)	°C/W

4. Soldered in, minimal footprint, FR4
5. 1 oz copper, 5 mm^2 copper area, FR4

LEAD FREE SOLDERING TEMPERATURE AND MSL

Parameter		Symbol	Condition	Min	Max	Unit
Lead Free Soldering, (Note 6) Reflow (SMD styles only),	Pb−Free	T_{sld}	60s – 150s Above 217s 40s Max at Peak	–	265 pk	°C
Moisture Sensitivity Level		MSL	DPAK and D2PAK SOT−223	1 3	– –	

6. Per IPC/JEDEC J−STD−020C

ELECTRICAL CHARACTERISTICS NCV4274A and NCV4274 5.0 V
$-40°C < T_J < 150°C$; $V_I = 13.5$ V unless otherwise noted.

Parameter	Symbol	Test Conditions	NCV4274A Min	NCV4274A Typ	NCV4274A Max	NCV4274 Min	NCV4274 Typ	NCV4274 Max	Unit
REGULATOR									
Output Voltage (5.0 V Version)	V_Q	5 mA < I_Q < 400 mA 6V < V_I < 28 V	4.9	5.0	5.1	4.8	5.0	5.2	V
Output Voltage (5.0 V Version)	V_Q	5 mA < I_Q < 200 mA 6 V < V_I < 40 V	4.9	5.0	5.1	4.8	5.0	5.2	V
Output Voltage (3.3 V Version)	V_Q	5 mA < I_Q < 400 mA 4.5 V < V_I < 28 V	3.23	3.3	3.37	3.17	3.3	3.43	V
Output Voltage (3.3 V Version)	V_Q	5 mA < I_Q < 200 mA 4.5 V < V_I < 40 V	3.23	3.3	3.37	3.17	3.3	3.43	V
Output Voltage (2.5 V Version)	V_Q	5 mA < I_Q < 400 mA 4.5 V < V_I < 28 V	2.45	2.5	2.55	2.4	2.5	2.6	V
Output Voltage (2.5 V Version)	V_Q	5 mA < I_Q < 200 mA 4.5 V < V_I < 40 V	2.45	2.5	2.55	2.4	2.5	2.6	V
Current Limit	I_Q	–	400	600	–	400	600	–	mA
Quiescent Current	I_q	I_q = 1 mA V_Q = 5.0 V V_Q = 3.3 V V_Q = 2.5 V I_q = 250 mA V_Q = 5.0 V V_Q = 3.3 V V_Q = 2.5 V I_q = 400 mA V_Q = 5.0 V V_Q = 3.3 V V_Q = 2.5 V	 – – – – – – – – –	 190 145 140 10 13 12 20 30 28	 250 250 250 15 20 15 35 45 35	 – – – – – – – – –	 190 145 140 10 13 12 20 30 28	 250 250 250 15 20 15 35 45 35	 μA μA μA mA mA mA mA mA mA
Dropout Voltage 5.0 V Version 3.3 V Version 2.5 V Version	V_{DR}	I_Q = 250 mA, $V_{DR} = V_I - V_Q$ V_I = 5.0 V V_I = 4.5 V V_I = 4.5 V	 – – –	 250 – –	 500 1.23 2.05	 – – –	 250 – –	 500 1.33 2.1	 mV V V
Load Regulation	DV_Q	I_Q = 5 mA to 400 mA	–	7	20	–	7	30	mV
Line Regulation	DV_Q	DV_I = 12 V to 32 V I_Q = 5 mA	–	10	25	–	10	25	mV
Power Supply Ripple Rejection	P_{SRR}	fr = 100 Hz, V_r = 0.5 V_{PP}	–	60	–	–	60	–	dB
Temperature output voltage drift	dV_Q/dT		–	0.5	–	–	0.5	–	mV/K
Thermal Shutdown Temperature*	T_{SD}	I_Q = 5 mA	165	–	210	165	–	210	°C

*Guaranteed by design, not tested in production

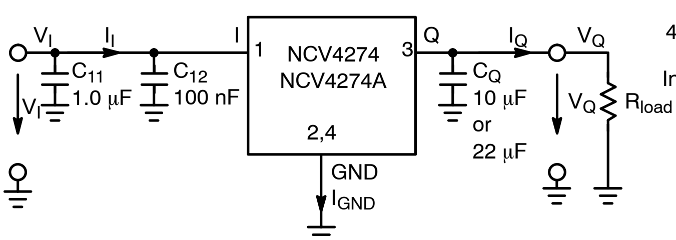


Figure 2. Measuring Circuit

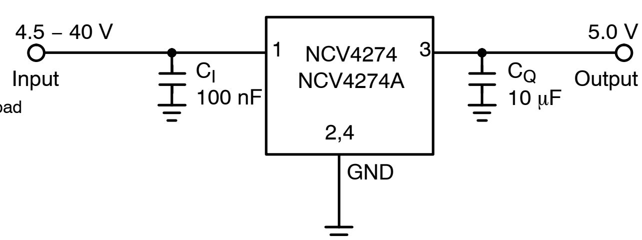


Figure 3. Application Circuit

TYPICAL CHARACTERISTIC CURVES

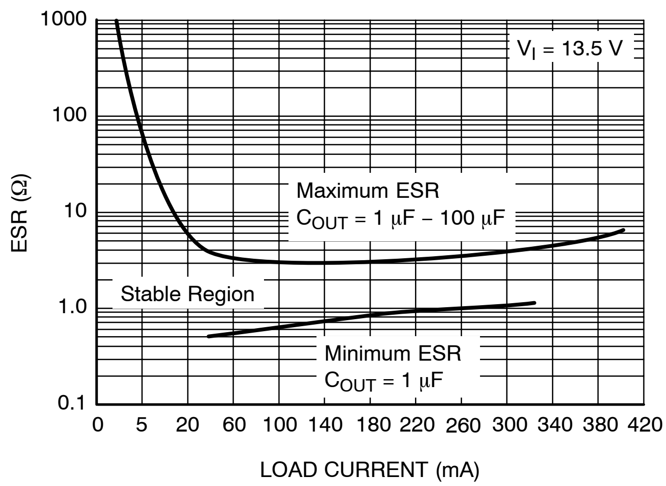


Figure 4. ESR Characterization

TYPICAL CHARACTERISTIC CURVES – 5.0 V Version

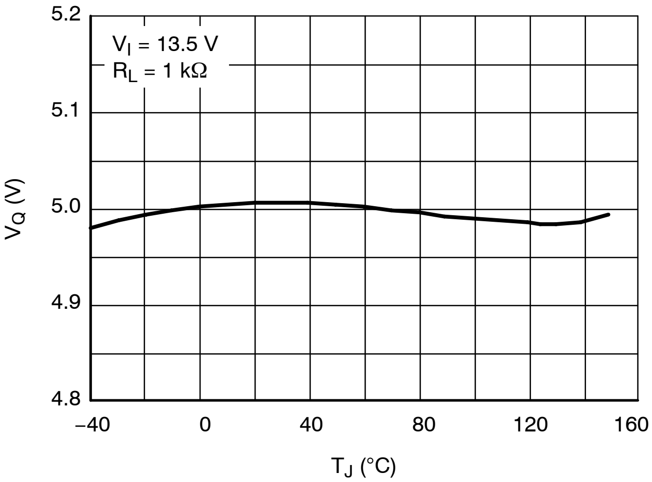


Figure 5. Output Voltage vs. Junction Temperature

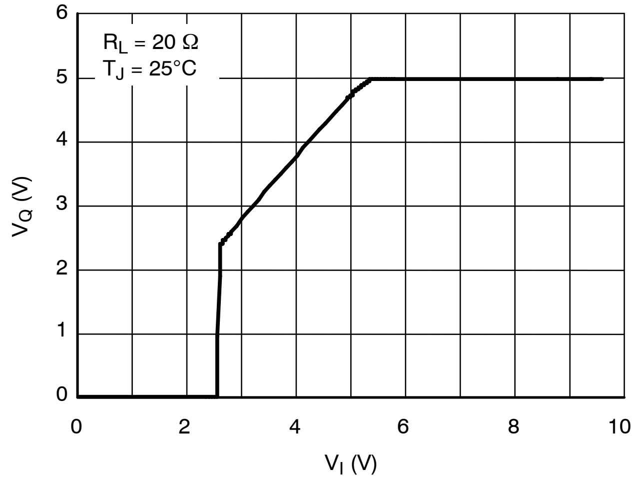


Figure 6. Output Voltage vs. Input Voltage

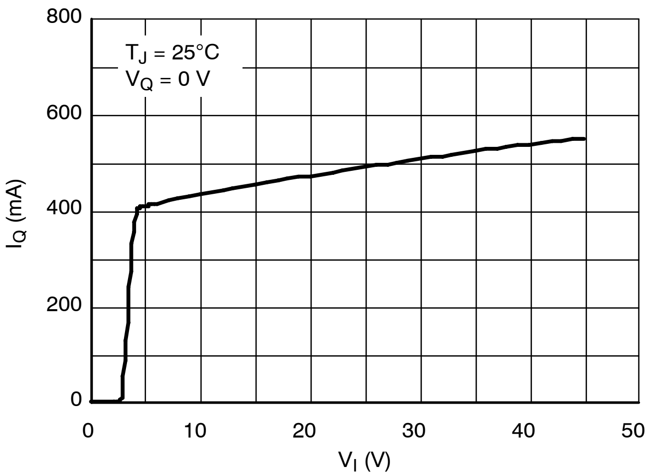


Figure 7. Output Current vs. Input Voltage

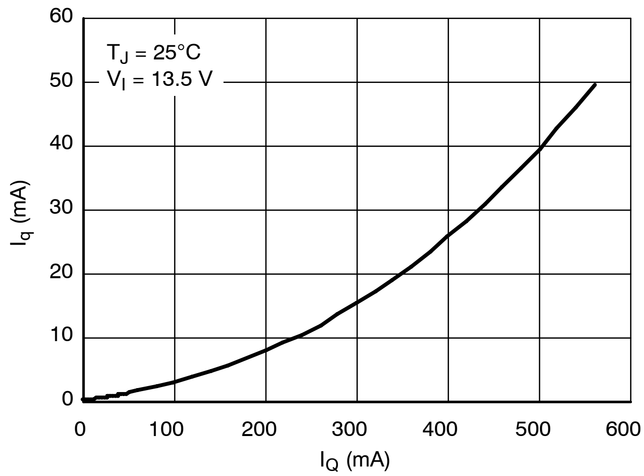


Figure 8. Current Consumption vs. Output Current (High Load)

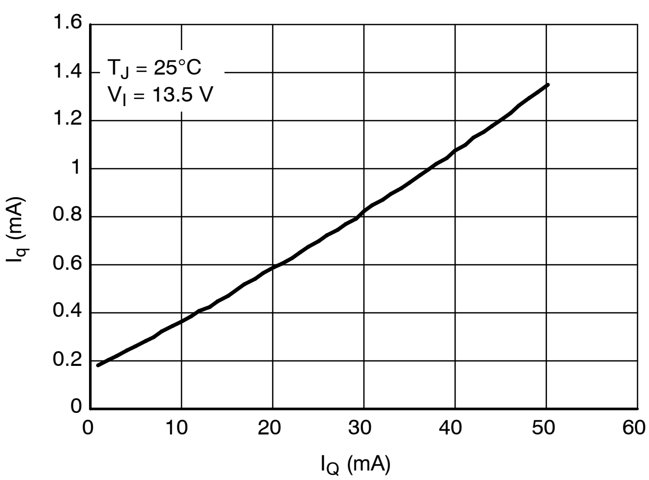


Figure 9. Current Consumption vs. Output Current (Low Load)

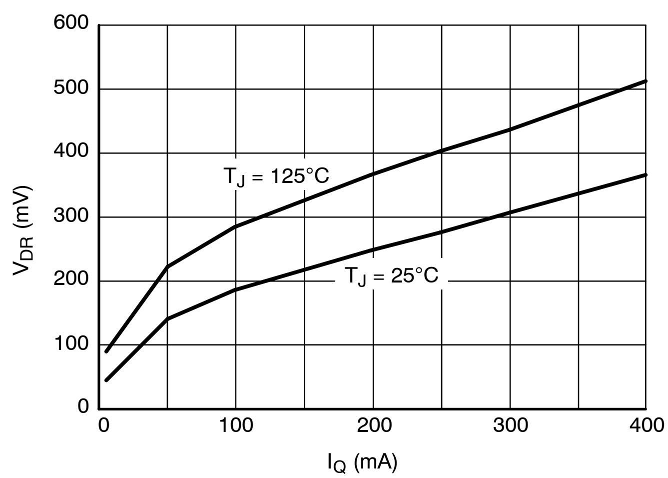


Figure 10. Drop Voltage vs. Output Current

TYPICAL CHARACTERISTIC CURVES – 5.0 V Version

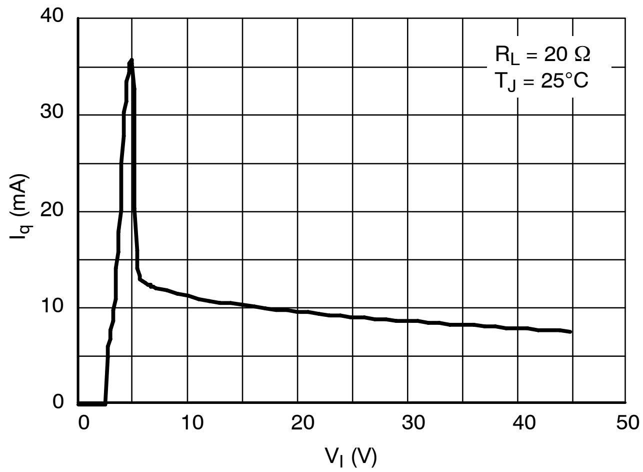


Figure 11. Current Consumption vs. Input Voltage

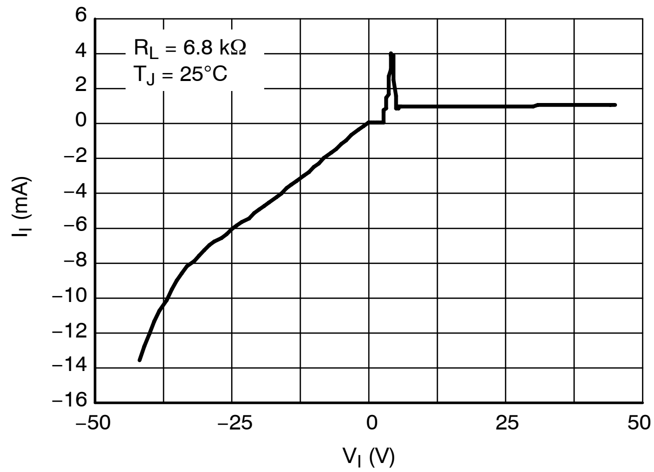


Figure 12. Input Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES – 3.3 V Version

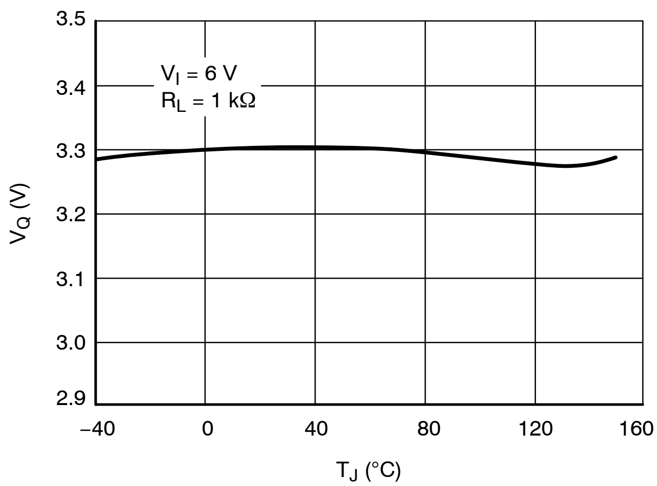


Figure 13. Output Voltage vs. Junction Temperature

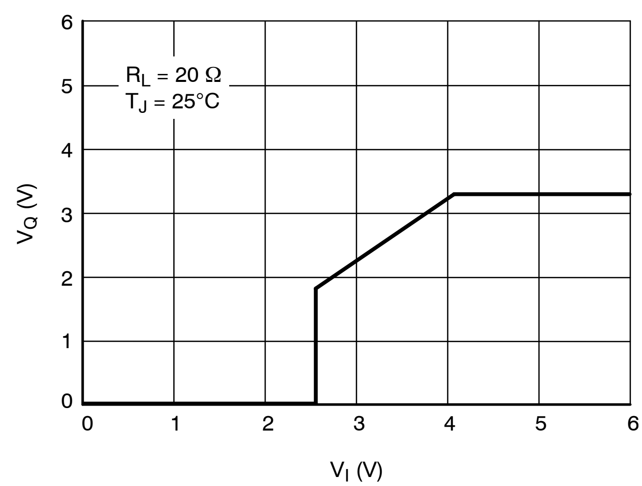


Figure 14. Output Voltage vs. Input Voltage

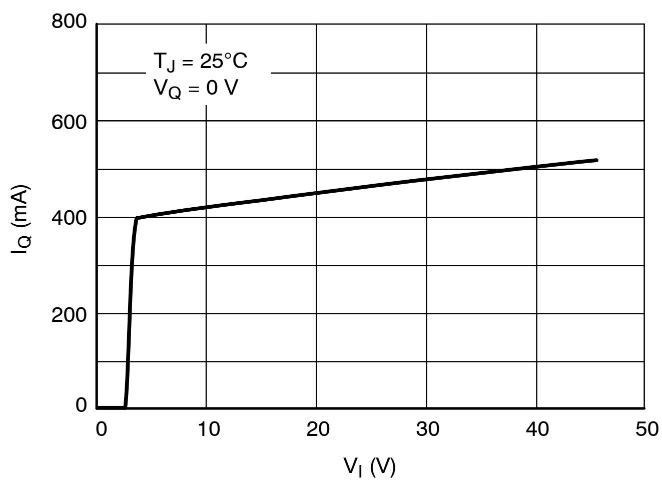


Figure 15. Output Current vs. Input Voltage

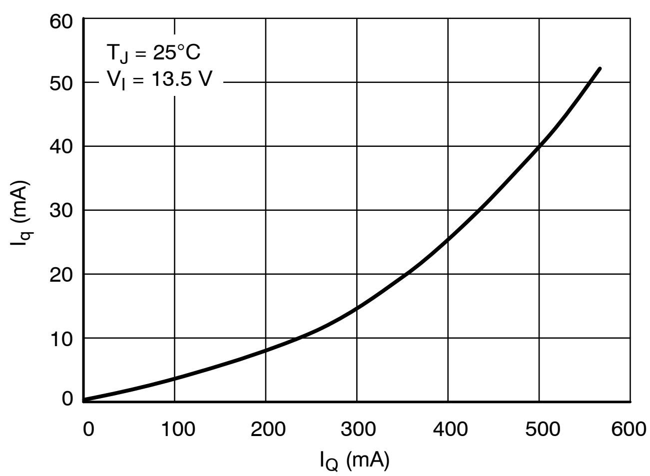


Figure 16. Current Consumption vs. Output Current (High Load)

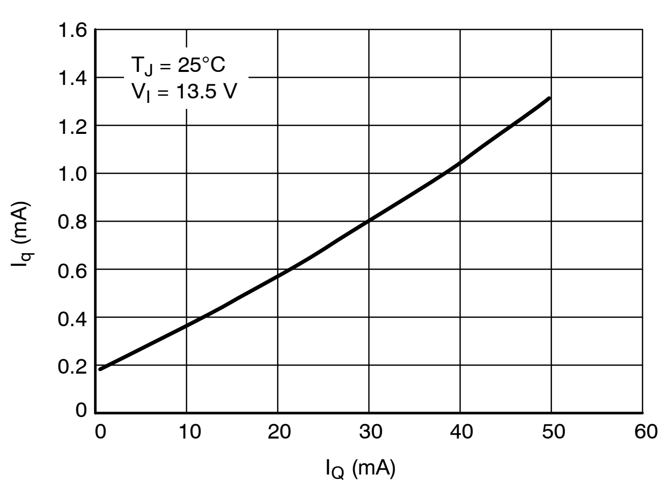


Figure 17. Current Consumption vs. Output Current (Low Load)

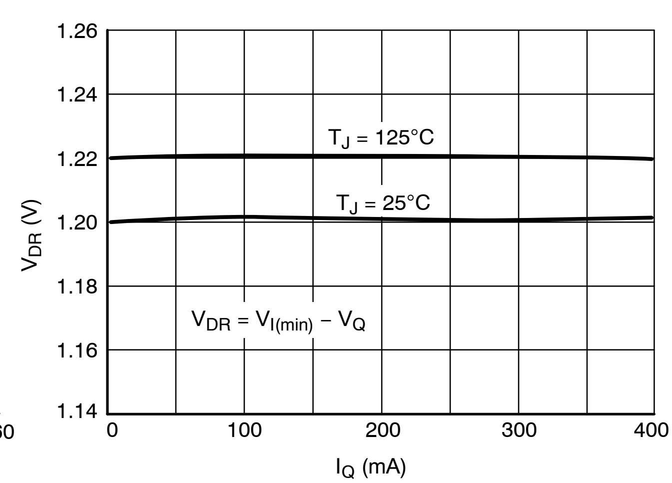


Figure 18. Voltage Drop vs. Output Current

TYPICAL CHARACTERISTIC CURVES − 3.3 V Version

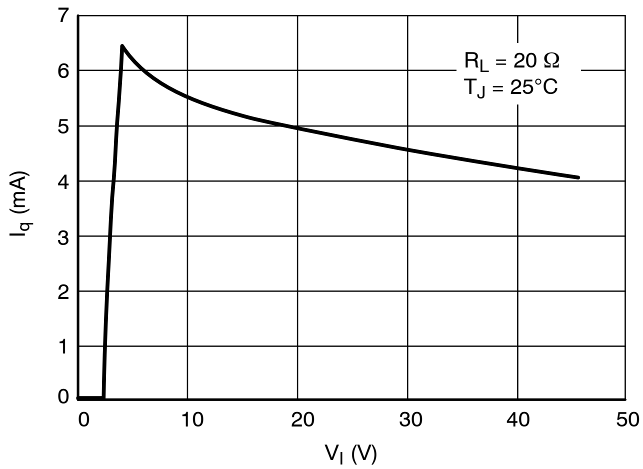


Figure 19. Current Consumption vs. Input Voltage

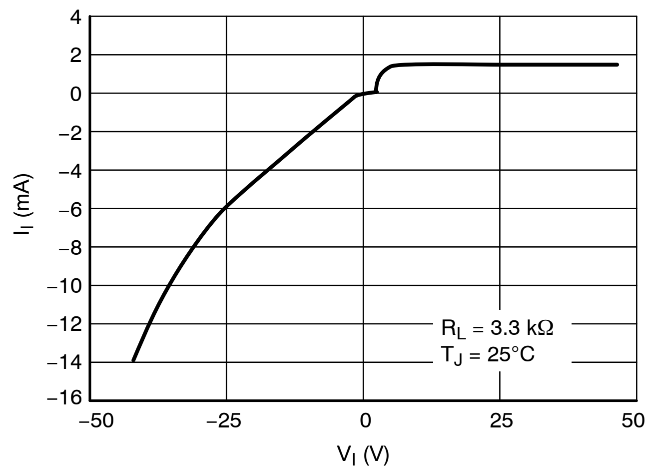


Figure 20. Input Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES – 2.5 V Version

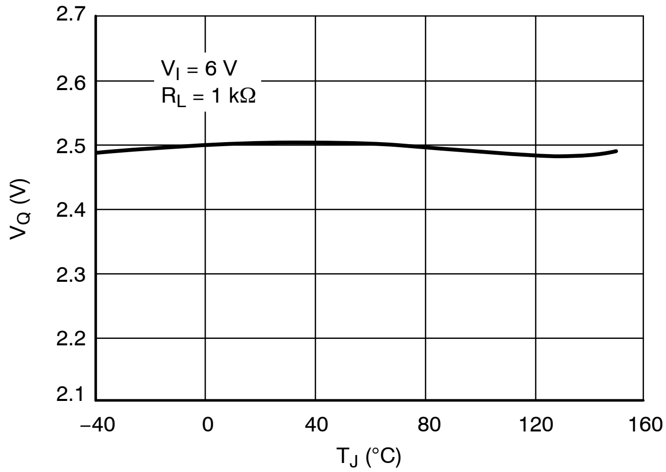


Figure 21. Output Voltage vs. Junction Temperature

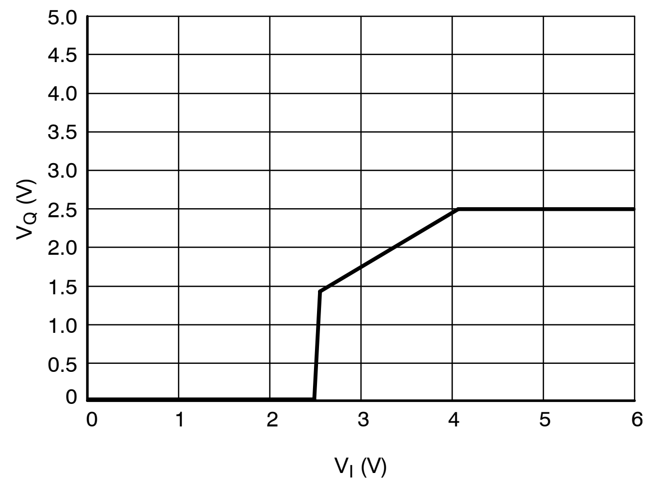


Figure 22. Output Voltage vs. Input Voltage

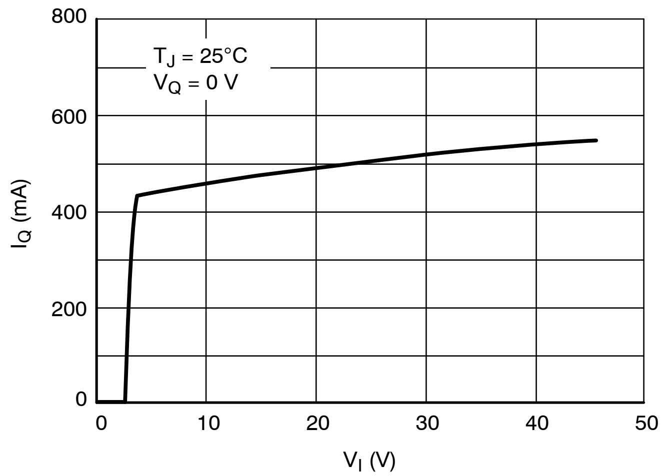


Figure 23. Output Current vs. Input Voltage

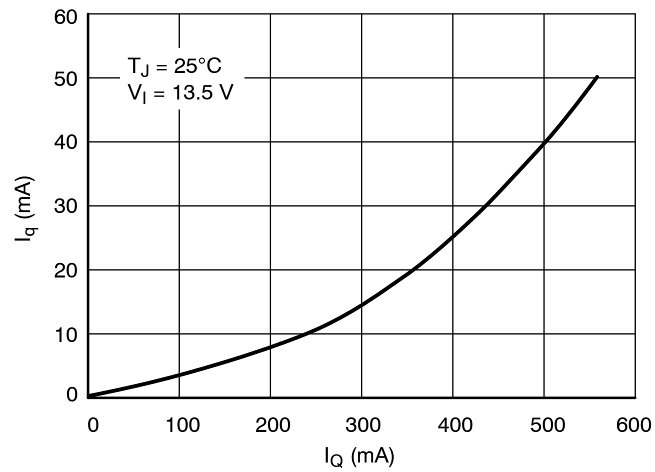


Figure 24. Current Consumption vs. Output Current (High Load)

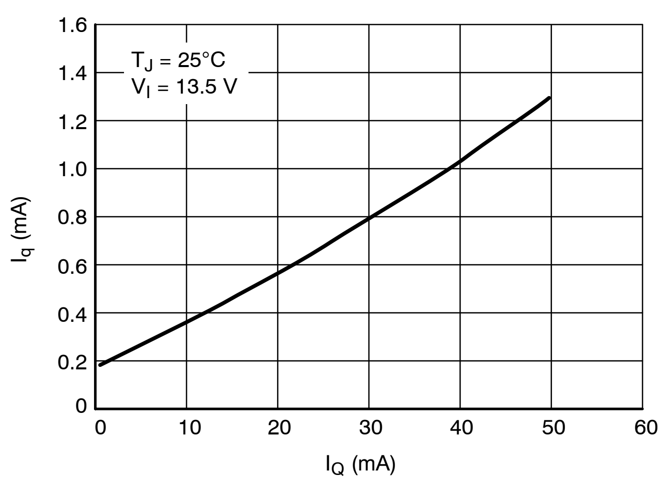


Figure 25. Current Consumption vs. Output Current (Low Load)

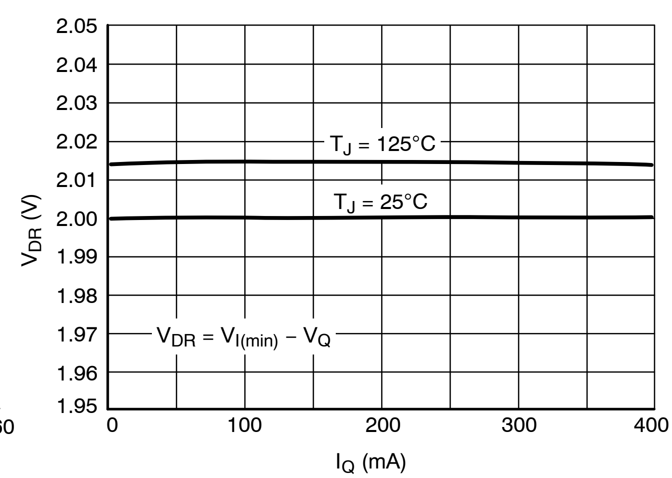


Figure 26. Voltage Drop vs. Output Current

TYPICAL CHARACTERISTIC CURVES – 2.5 V Version

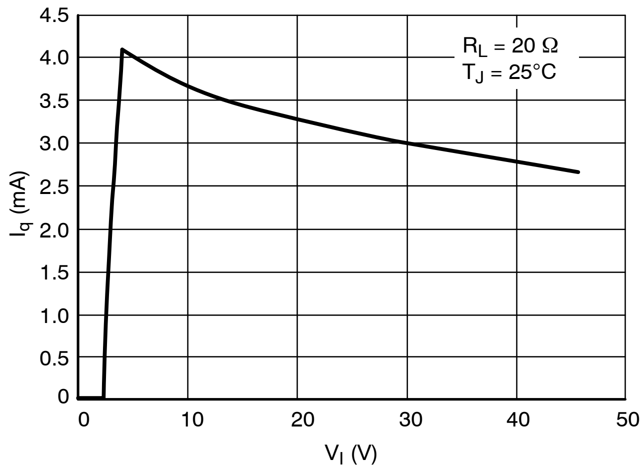


Figure 27. Current Consumption vs. Input Voltage

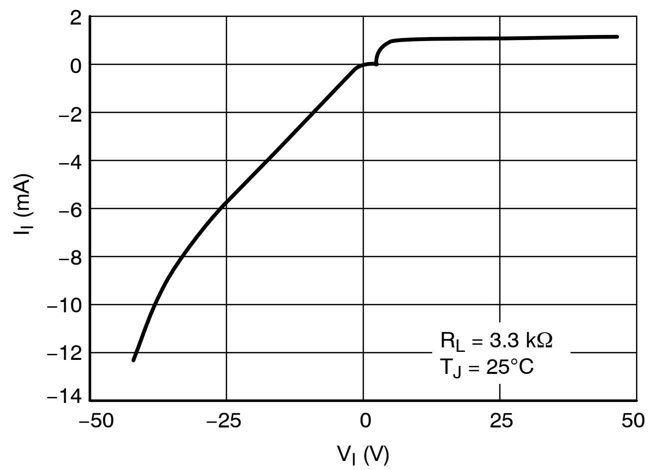


Figure 28. Input Current vs. Input Voltage

APPLICATION DESCRIPTION

Output Regulator

The output is controlled by a precision trimmed reference and error amplifier. The PNP output has saturation control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

Stability Considerations

The input capacitor C_{I1} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{I2}.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor C_Q shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values $C_Q \geq 2.2\ \mu F$ and an ESR $\leq 2.5\ \Omega$ within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]I_{Q(max)} + V_{I(max)}I_q \quad \text{(eq. 1)}$$

Where:

$V_{I(max)}$ is the maximum input voltage,
$V_{Q(min)}$ is the minimum output voltage,
$I_{Q(max)}$ is the maximum output current for the application, and
I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta_{JA}} = \frac{(150\ C - T_A)}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

Where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and
$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.
$R_{\theta JC}$ appears in the package section of the data sheet.

Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.

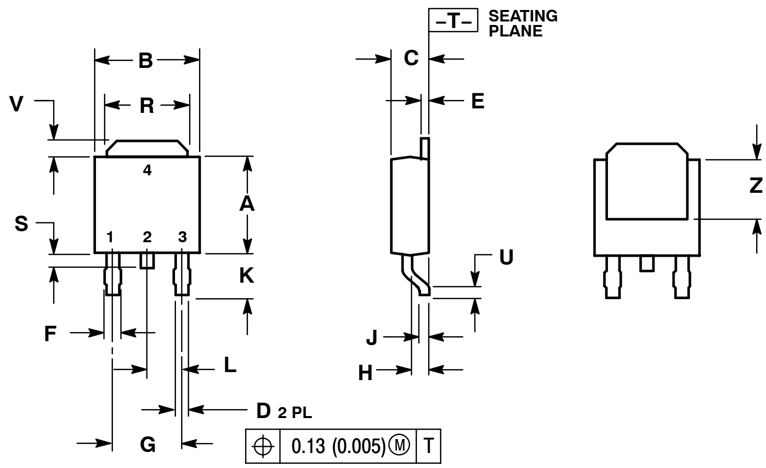
ORDERING INFORMATION4

Device	Output Voltage Accuracy	Output Voltage	Package	Shipping†
NCV4274DS50G	4%	5.0 V	D2PAK (Pb−Free)	50 Units / Rail
NCV4274DS50R4G	4%	5.0 V	D2PAK (Pb−Free)	800 / Tape & Reel
NCV4274DT50G	4%	5.0 V	DPAK (Pb−Free)	75 Units / Rail
NCV4274DT50RKG	4%	5.0 V	DPAK (Pb−Free)	2500 / Tape & Reel
NCV4274ADS50G	2%	5.0 V	D2PAK (Pb−Free)	50 Units / Rail
NCV4274ADS50R4G	2%	5.0 V	D2PAK (Pb−Free)	800 / Tape & Reel
NCV4274ADT50G	2%	5.0 V	DPAK (Pb−Free)	75 Units / Rail
NCV4274ADT50RKG	2%	5.0 V	DPAK (Pb−Free)	2500 / Tape & Reel
NCV4274ST33T3G	4%	3.3 V	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV4274DT33RKG	4%	3.3 V	DPAK (Pb−Free)	2500 / Tape & Reel
NCV4274AST33T3G	2%	3.3 V	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV4274ADT33RKG	2%	3.3 V	DPAK (Pb−Free)	2500 / Tape & Reel
NCV4274ST25T3G	4%	2.5 V	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV4274AST25T3G	2%	2.5 V	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

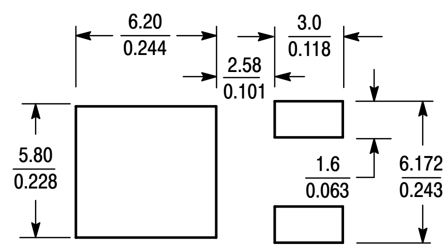
DPAK (SINGLE GAUGE)
CASE 369C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*

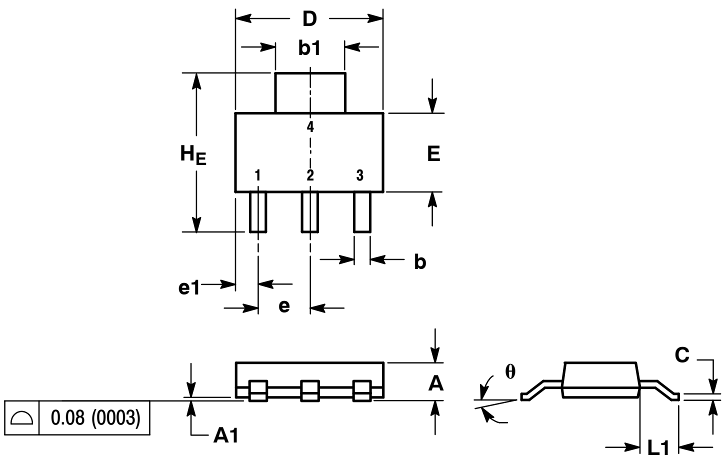


SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

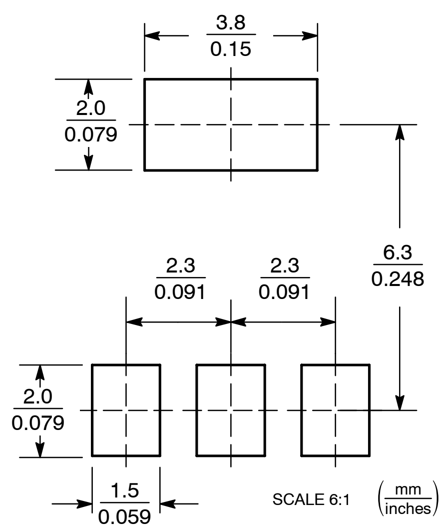
SOT−223 (TO−261)
CASE 318E−04
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

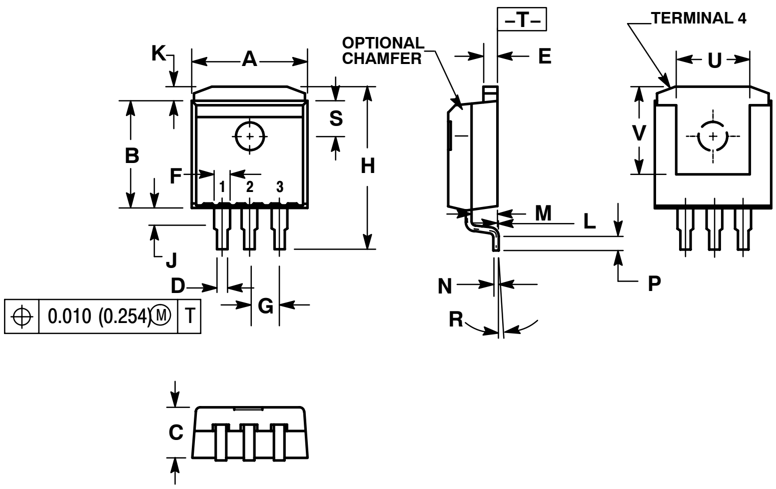
	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

D2PAK
CASE 418AF−01
ISSUE O



NOTES:
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.
5. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
6. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
7. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

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