Z80 CMOS Microprocessors

Z84C90 KIO Serial/ Parallel Counter/Timer

Product Specification

PS011804-0612

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Revision History

Each instance in the following revision history table reflects a change to this document from its previous version. For more details, refer to the corresponding pages or appropriate links provided in the table.

Date	Revision Level	Description	Page Number
Jun 2013	04	Corrected to remove internal discussion tags.	N/A
Jun 2012	03	Updated to include missing information covered in the DC8321-00 Databook (2Q94).	All
Sep 2002	02	Added Z84C90 KIO Peripheral: Serial/Parallel Counter/ Timer Packages table, modified AC Characteristics of the Z84C90 table.	2, 38
Sep 2002	01	Original issue.	All

Table of Contents

Revision History iii
List of Figures v
List of Tables vii
Introduction 1
Features 1
Block Descriptions 3
Pin Signals 8
Pin Descriptions 10
Register Address Decoding for the KIO 13
Register Programming 16
PIO Registers 16
CTC Registers 18
SIO Registers 20
PIA Registers 26
KIO Command Register 27
Z84C90 KIO: Enhanced Version 27
Electrical Characteristics 29
Absolute Maximum Ratings 29
Standard Test Conditions 29
DC Characteristics 30
Capacitance 37
AC Characteristics 37
Packaging 45
Ordering Information 46
Part Number Suffix Designations 46
Precautions & Limitations 47
Customer Support 49

List of Figures

Figure 1. A Block Diagram of the Z84C90 KIO Peripheral 2
Figure 2. Z84C20 Parallel Input/Output Block Diagram 3
Figure 3. Parallel Interface Adapter Block Diagram 4
Figure 4. Counter/Timer Block Diagram 5
Figure 5. SIO Block Diagram 6
Figure 6. Crystal Connection 7
Figure 7. Z84C90 84-Pin PLCC Configuration 8
Figure 8. 100-Pin LQFP Configuration 9
Figure 9. KIO Register Addressing 15
Figure 10. PIO Interrupt Vector Word Register 16
Figure 11. PIO Mode Control Word Register 16
Figure 12. PIO I/O Register Control Word 17
Figure 13. PIO Interrupt Control Word 17
Figure 14. PIO Mask Control Word 18
Figure 15. PIO Interrupt Disable Word 18
Figure 16. CTC Channel Control Word 19
Figure 17. CTC Time Constant Word 20
Figure 18. CTC Interrupt Vector Word 20
Figure 19. SIO Read Register 0 21
Figure 20. SIO Read Register 1** 21
Figure 21. SIO Read Register 2 (Channel B only) 22
Figure 22. SIO Write Register 0 23
Figure 23. SIO Write Register 1 23
Figure 24. SIO Write Register 2 (Channel B only) 24
Figure 25. SIO Write Register 3 24
Figure 26. SIO Write Register 4 25
Figure 27. SIO Write Register 5 25
Figure 28. SIO Write Register 6 26

Figure 29. SIO Write Register 7 26
Figure 30. PIA Control Register 27
Figure 31. KIO Command Register A 27
Figure 32. KIO Register 15: KIO Command Register B 28
Figure 33. Test Load Diagram 30
Figure 34. I/O Read/Write Timing (M1 = 1) 31
Figure 35. Interrupt Acknowledge Cycle 32
Figure 36. Counter/Timer Timing 32
Figure 37. RETI Timing Standard Function 33
Figure 38. RETI Timing Interrupt Pending 34
Figure 39. Port I/O Read/Write Timing 35
Figure 40. Serial I/O Timing 36
Figure 41. Op Code Fetch Cycle 37
Figure 42. Internal Daisy Chain Configuration 42

List of Tables

Table 1. Z84C90 KIO Peripheral: Serial/Parallel Counter/Timer Packages 2
Table 2. KIO Registers 13
Table 3. DC Characteristics of the Z84C90 30
Table 4. Capacitance 37
Table 5. AC Characteristics of the Z84C90 38
Table 6. Daisy Chain Parameters 43
Table 7. Daisy Chain Calculation Data* 43
Table 8. Z84C90 KIO Ordering Matrix 46

Introduction

Zilog's Z84C90 Serial/Parallel Counter/Timer KIO is a multichannel, multipurpose I/O peripheral device designed to provide the end user with a cost-effective and powerful solution to meet an assortment of peripherals requirements. The Z84C90 KIO Peripheral combines the features of one Z84C30 CTC, one Z84C20 PIO and a Z84C4x SIO, plus an 8-bit, bit-programmable I/O port and a crystal oscillator into a single 84-pin PLCC or 100-pin LQFP package. Utilizing fifteen internal registers for data and programming information, the KIO can easily be configured to any given system environment. Although optimum performance is obtained with a Z84C00 CPU, the KIO can just as easily be used with any other CPU.

Features

The Z84C90 Serial/Parallel Counter/Timer KIO offers the following features:

- Two independent synchronous/asynchronous serial channels
- Three 8-bit parallel ports
- Four independent counter/timer channels
- On-chip clock oscillator/driver
- Software/hardware resets
- Designed in CMOS for low power operations
- Supports Z80 Family interrupt daisy chain
- Programmable interrupt priorities
- 8, 10 and 12.5MHz bus clock frequency
- Single +5V power supply

Table 1 lists the differing frequencies offered for the Z84C90 KIO Peripheral by package and part number.

Table 1. Z84C90 KIO Peripheral: Serial/Parallel Counter/Timer Packages

Part Number	Package	Frequency (MHz)
Z84C9008ASC	100-pin LQFP	8
Z84C9010ASC	100-pin LQFP	10
Z84C9008VEC	84-pin PLCC	8
Z84C9008VSC	84-pin PLCC	8
Z84C9010VSC	84-pin PLCC	10
Z84C9012VSC	84-pin PLCC	12

Figure 1 illustrates a block diagram of the Z84C90 KIO Peripheral.

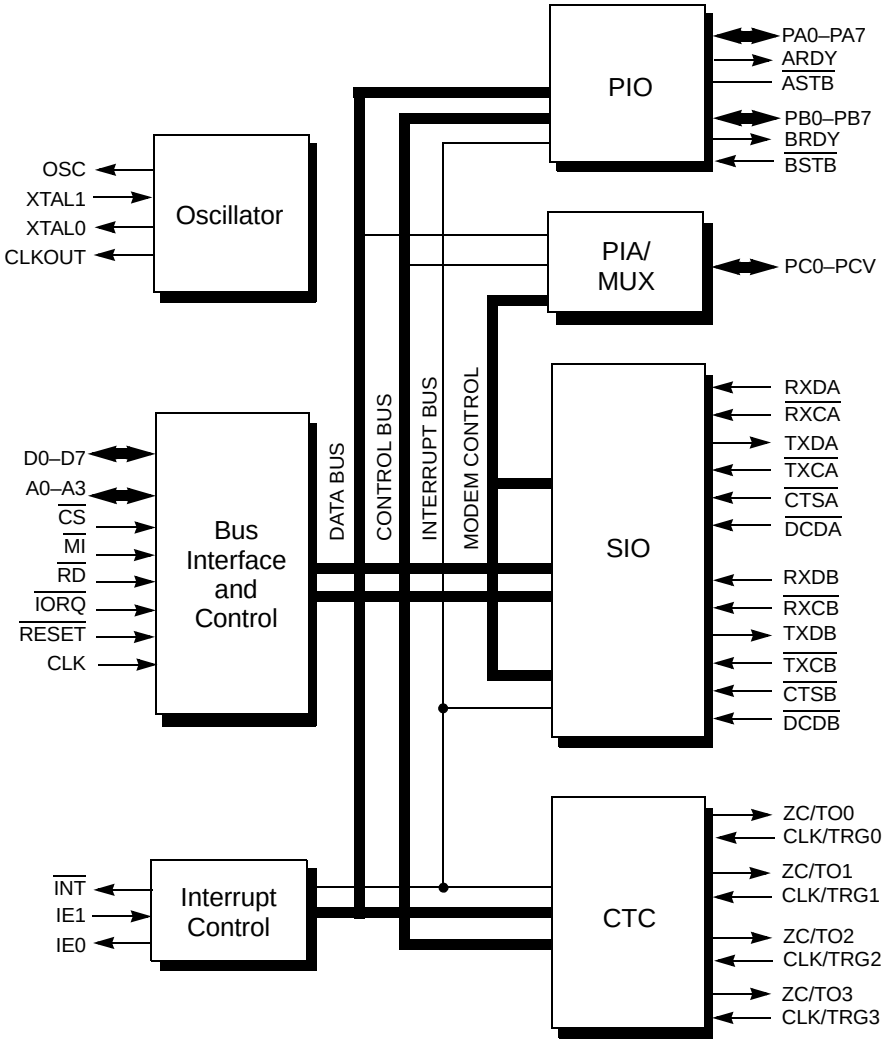


Figure 1. A Block Diagram of the Z84C90 KIO Peripheral

Block Descriptions

Z84C20 Parallel Input/Output Logic Unit. This logic unit provides both TTL- and CMOS-compatible interfaces between peripheral devices and a CPU through the use of two 8-bit parallel ports. The CPU configures the logic to interface to a wide range of peripheral devices with no external logic. Typical devices that are compatible with this interface are keyboards, printers and EPROM/PAL programmers.

The parallel ports (designated Port A and Port B) are byte-wide and completely compatible with the Z84C90 PIO (see Figure 2). These two ports feature several modes of operation: input, output, bidirectional or bit control. Each port features two handshake signals (RDY and $\overline{STB}$) which can be used to control data transfers. The RDY (ready) indicates that the port is ready for data transfer while $\overline{STB}$ (strobe) is an input to the port that indicates when data transfer has occurred. Each of the ports can also be programmed to interrupt the CPU upon the occurrence of specified status conditions and generate unique interrupt vectors when the CPU responds.

For more information about the operation of this portion of the logic, please refer to the Z8420/Z84C20 PIO Product Specification (PS0180).

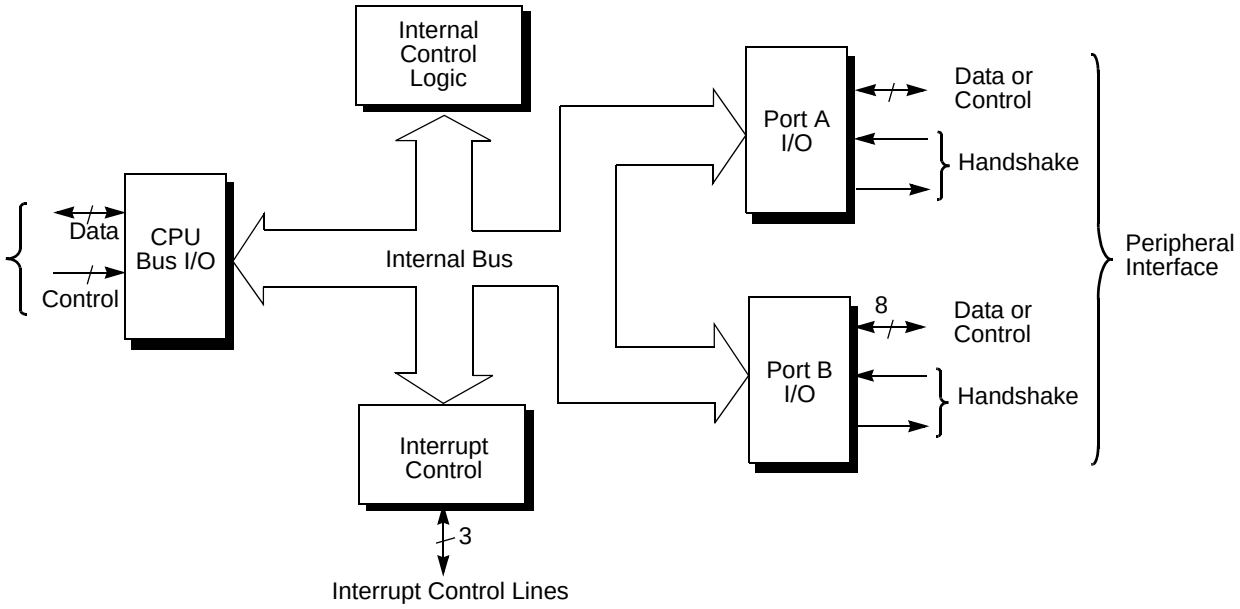


Figure 2. Z84C20 Parallel Input/Output Block Diagram

Parallel Interface Adapter (PIA) Logic Unit. This logic also offers an additional 8 bits of I/O to the user, referred to as the PIA port (see Figure 3). This port, designated as Port C, is bit-programmable for data transfers; each bit can be individually programmed as either an input or an output. Bit direction control is performed through the programming of the PIA Control Register. When programmed as outputs, the output data latches are programmed with an I/O write cycle; their state can be read with an I/O read cycle. When programmed as inputs, the state of the external pin is read with the I/O read cycle. This port does not have handshake capabilities and offers no interrupt capabilities. This port is multiplexed to provide the additional modem and CPU control signals for the serial I/O logic unit, when appropriate.

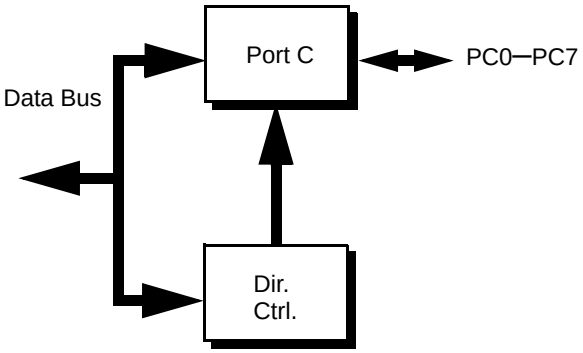


Figure 3. Parallel Interface Adapter Block Diagram

When a read from the PIA port occurs, input data will be latched when $\overline{\text{IORQ}}$, $\overline{\text{CS}}$ and $\overline{\text{RD}}$ all detected as active. The data bus will display this data as a result of the rising edge of the clock input after this occurrence. When a write to the PIA port occurs, data will be written as a result of the rising edge of the clock input after $\overline{\text{IORQ}}$ and $\overline{\text{CS}}$ have been detected as active and $\overline{\text{RD}}$ has been detected as inactive.

Counter/Timer Logic (CTC) Unit. This logic unit provides the user with four individual 8-bit counter/timer channels that are compatible with the Z84C30 CTC (see Figure 4). The counter/timers can be programmed by the CPU for a broad range of counting and timing applications. Typical applications include event counting, interrupt and interval timing and serial baud rate clock generation.

Each of the counter/timer channels, designated Channels 0 through 3, have an 8-bit prescaler (when used in timer mode) as well as its own 8-bit counter to provide a wide range of count resolution. Each of the channels also have their own clock/trigger input to quantify the counting process and an output to indicate zero crossing/time-out conditions. With only one interrupt vector programmed into this logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.

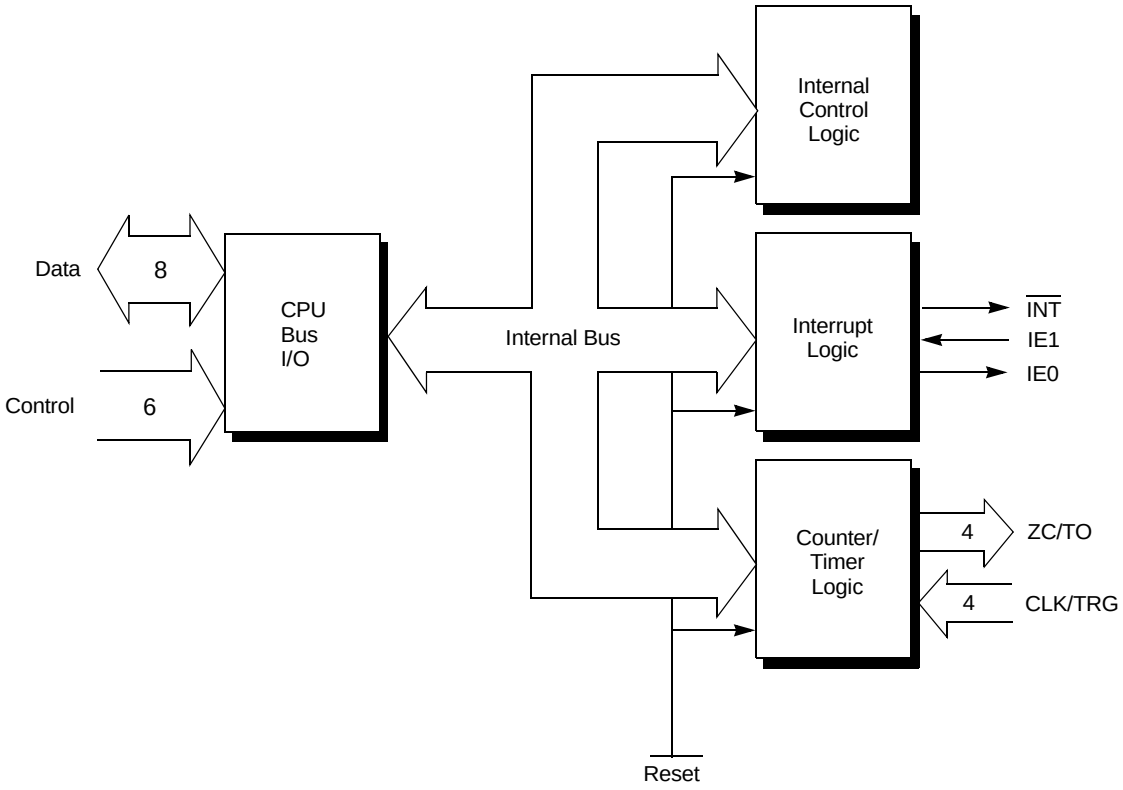


Figure 4. Counter/Timer Block Diagram

Serial I/O Logic Unit. This logic unit provides the user with two separate serial I/O channels that are completely compatible with the Z84C4x SIO (see Figure 5). Their basic functions as serial-to-parallel and parallel-to-serial converters can be programmed by a CPU for a broad range of serial communications applications. Each channel, designated Channel A and Channel B, is capable of supporting all common asynchronous and synchronous protocols (Monosync, Bisync and SDLC/HDLC), byte- or bit-oriented.

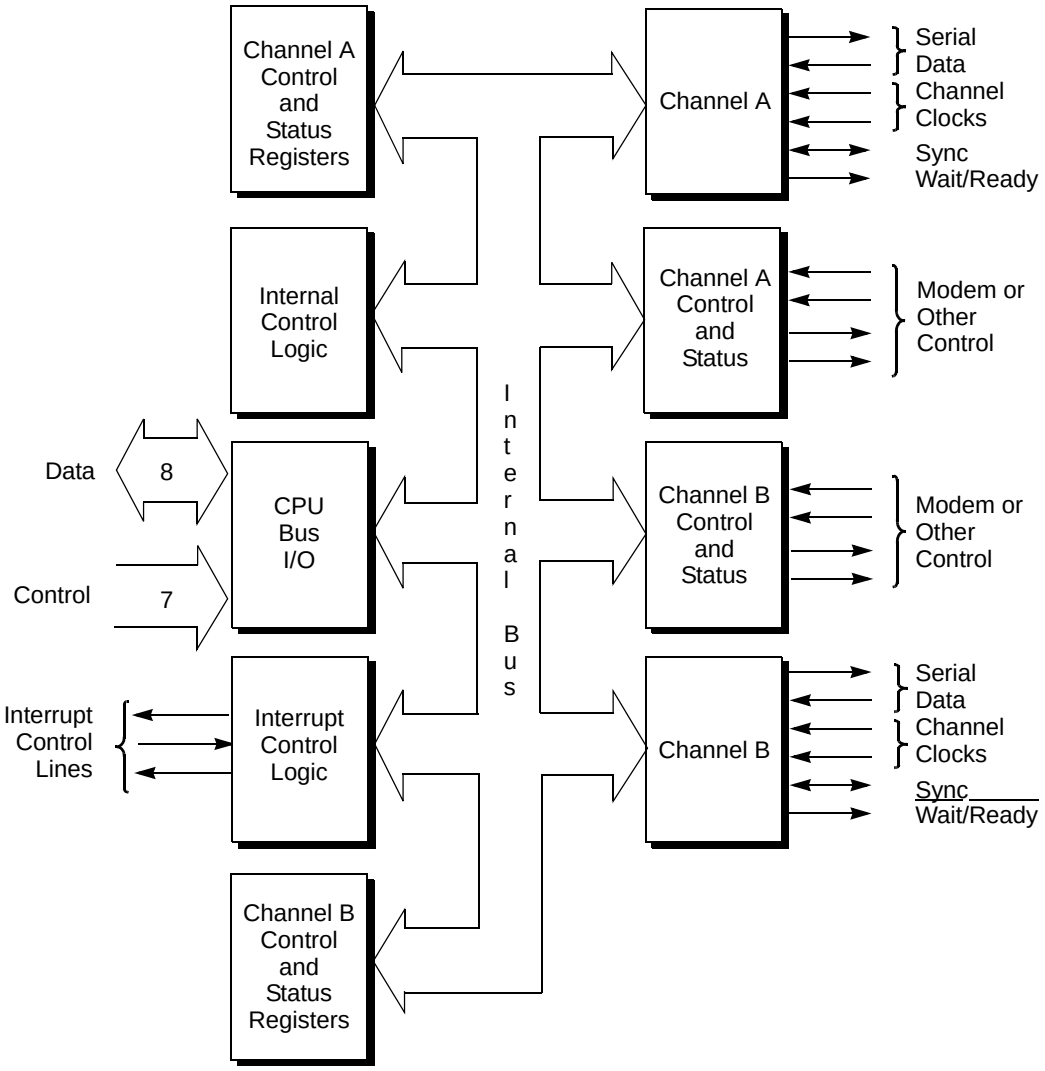


Figure 5. SIO Block Diagram

In the default state of the KIO, each serial channel supports full duplex communication with separate transmit and receive data lines, two modem control signals ($\overline{CTS}$ and $\overline{DCD}$) and separate transmit and receive clock inputs. Optionally, additional modem and CPU/DMA control signals can be obtained through the PIA port.

For more information about the operation of this portion of the logic, please refer to the Z8420/Z84C20 PIO Product Specification (PS0180).

Clock Oscillator/Driver Logic Unit. A clock oscillator/driver is available that will allow the user to eliminate circuitry with in a new design, or that can be used as another oscillator within the system. This logic will accept either a crystal ceramic resonator or TTL-compatible clock input and generate a MOS-compatible clock output and also an oscillator reference output. Zilog recommends a fundamental parallel resonant crystal; see Figure 6. The preferred value of the two capacitors C1 and C2 is 33pF each.

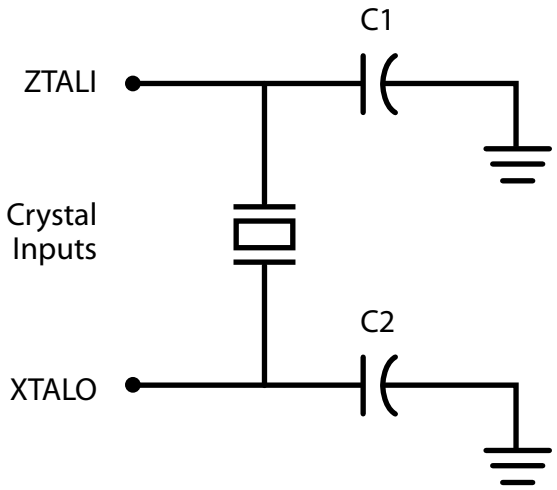


Figure 6. Crystal Connection

Command Logic Unit. This logic unit provides for much more than just controlling the interface between the KIO and the CPU. The main function provided by this unit is to allow the user to configure the internal interrupt daisy chain of the KIO into a preferred sequence of peripherals to interrupt. Any one of the three devices (SIO, CTC, PIO) can be the highest priority, while another can be second priority and the remaining device the third. The user can even configure the daisy chain such that no internal peripherals are involved in the chain. Programming of the daisy chain configuration is performed by programming the Command Register with the appropriate 3-bit pattern in addresses D0–D2, with D3 set to 1.

A second function of this logic unit is to provide software-controllable hardware resets to each of the individual devices. As a result, an individual peripheral is allowed to be reset without having to reset the entire KIO. Requiring bit D3 to be set to a 1 to program the daisy chain configuration allows the user to reset the individual devices without changing the daisy chain. The software reset commands for the individual devices still remain available to the user.

A third function of the Command Register allows the user to obtain use of the additional control signals of the SIO logic instead of the PIA port by programming bit D7 of the Command Register with a 1.

Pin Signals

Figure 7 shows the pin-outs for the 84-pin PLCC Z84C90 KIO Peripheral package; Figure 8 shows the 100-pin LQFP pin-outs.

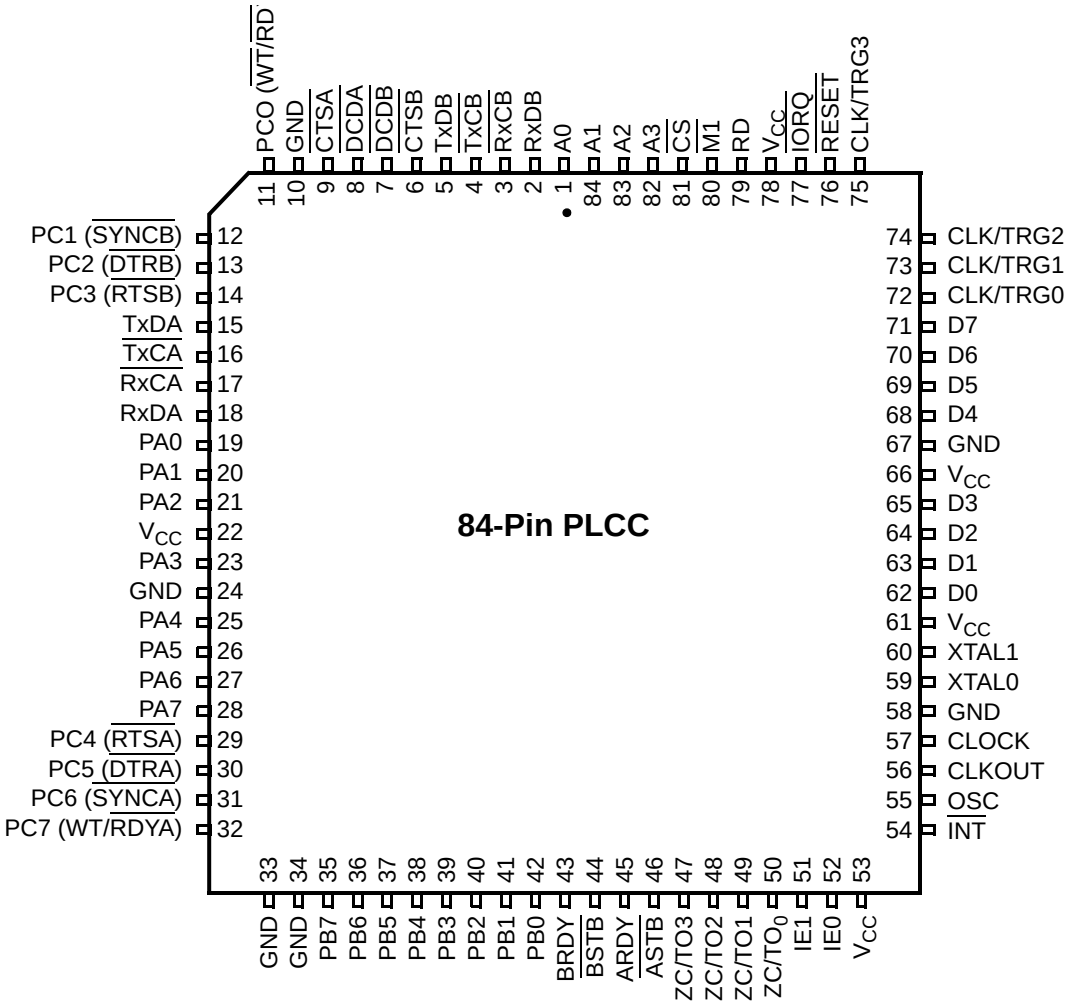


Figure 7. Z84C90 84-Pin PLCC Configuration

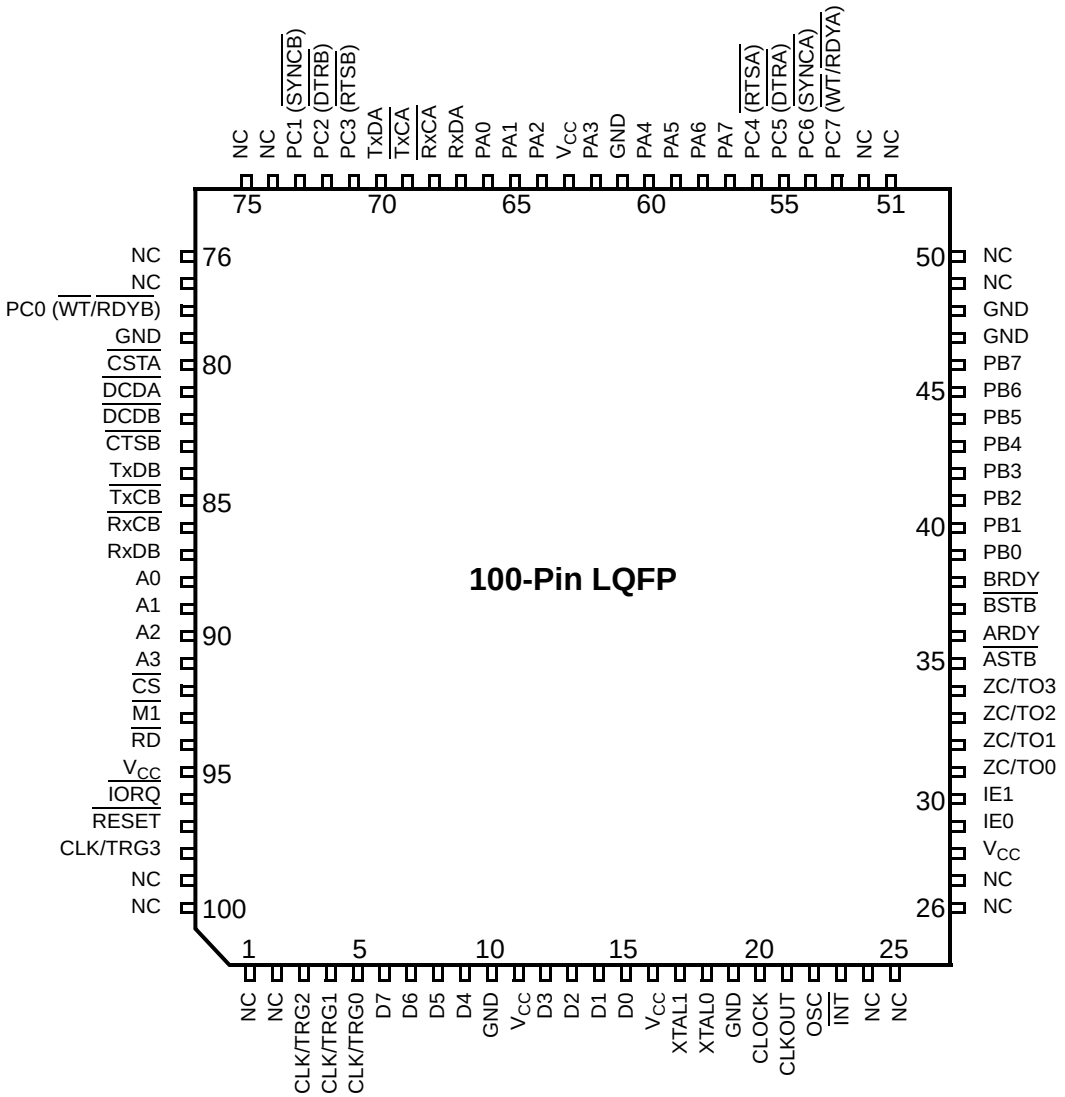


Figure 8. 100-Pin LQFP Configuration

Pin Descriptions

A0–A3. Address bus (inputs). Used to select the port/register for each bus cycle.

ARDY, BRDY. Port Ready (outputs, active High). These signals indicate that the port is ready for a data transfer. In Mode 0, the signal indicates that the port has data available to the peripheral device. In Mode 1, the signal indicates that the port is ready to accept data from the peripheral device. In Mode 2, ARDY indicates that Port A has data available for the peripheral device, but that the data is not be placed onto PA0–PA7 until the $\overline{\text{ASTB}}$ signal is Active. BRDY indicates that Port A is able to accept data from a peripheral device.

Note: Port B does not support Mode 2 operation and can only be used in Mode 3 when Port A is programmed for Mode 2. BRDY is not associated with Port B when it is operating in Mode 3.

$\overline{\text{ASTB}}$, $\overline{\text{BSTB}}$. Port Strobe (inputs, active Low). These signals indicate that the peripheral device has performed a transfer. In Mode 0, the signal indicates that the peripheral device has accepted the data present on the port pins. In Mode 1, the signal causes the data on the port pins to be latched onto Port A. In Mode 2, $\overline{\text{ASTB}}$ Low causes the data in the output data latch of Port A to be placed onto the Port A pins. $\overline{\text{BSTB}}$ Low causes the data present on the Port A pins to be latched into the Port A input data latch. The end of the current transaction is noted by the rising edge of these signals.

Note: Port B does not support Mode 2 operation, and can only be used in Mode 3 when Port A is programmed for Mode 2. $\overline{\text{BSTB}}$ is not associated with Port B when it is operating in Mode 3.

CLK/TRG0–CLK/TRG3. External Clock/Timer Trigger (inputs, user-selectable active High or Low). These four pins correspond to the four counter/timer channels of the KIO. In Counter mode, each active edge causes the downcounter to decrement. In Timer mode, an active edge starts the timer.

CLKOUT. Clock Out (output). This output is a divide-by-two of the oscillator (XTAL) input.

CLOCK. System Clock (input). This clock must be the same as (or a derivative of) the CPU clock. If the CLKOUT is to be used as the system clock, then these two pins must be connected together.

CS. Chip Select (input, active Low). Used to activate the internal register decoding mechanism and allow the KIO to perform a data transfer to/from the CPU.

$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$. Clear to Send (inputs, active Low). These signals are modem control signals for the serial channels. When programmed for Auto Enable, a Low on these pins enables their respective transmitters. If not programmed as Auto Enable, these pins may be used as general-purpose input signals.

D0–D7. Data Bus (bidirectional, active High, tristated). Used for data exchanges between the CPU and the KIO for programming and data transfer. The KIO also monitors the data bus for Return from Interrupt (RETI) instructions to maintain its Interrupt Under Service (IUS) status.

$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$. Data Carrier Detect (inputs, active Low). These signals are modem control signals for the serial channels. When programmed for Auto Enable, a Low on these pins enables their respective receivers. If not programmed as Auto Enable, these pins may be used as general-purpose input signals.

$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$. Data Terminal Ready (outputs, active Low). These signals are modem control signals for the serial channels. They follow the state programmed into their respective serial channels, and are multiplexed with Port C, bits 5 and 2, respectively.

IEI. Interrupt Enable In (input, active High). This signal is used with Interrupt Enable Out (IEO) to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no higher-priority device is requesting an interrupt.

IEO. Interrupt Enable Out (output, active High). This signal is used with Interrupt Enable In (IEI) to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that this device is requesting an interrupt, and that no higher-priority device, is not requesting an interrupt. A Low blocks any lower-priority devices from requesting an interrupt.

IORQ. Input/Output Request (input, active Low). $\overline{\text{IORQ}}$ is used with $\overline{\text{RD}}$, A0–A3, and $\overline{\text{CS}}$ to transfer data between the KIO and the CPU. When $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, and $\overline{\text{CS}}$ are active Low, the device selected by A0–A3 transfers data to the CPU. When $\overline{\text{IORQ}}$ and $\overline{\text{CS}}$ are active Low, but $\overline{\text{RD}}$ is active High, the device selected by A0–A3 is written into by the CPU. When $\overline{\text{IORQ}}$ and $\overline{\text{M1}}$ are both active Low, the KIO may respond with an interrupt vector from its highest-priority interrupting device.

M1. Machine Cycle 1 (input, active Low). When $\overline{\text{M1}}$ and $\overline{\text{RD}}$ are Low, the Z80 CPU fetches an instruction from memory; the KIO decodes this cycle to determine if the RETI instruction sequence is being executed. When $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ are both active, the KIO decodes the cycle to be an interrupt acknowledge, and may respond with a vector from its highest-priority interrupting device.

OSC. Oscillator (output). This output is a reference clock for the oscillator.

PA0–PA7. Port A Bus (bidirectional, tristated). One of the 8-bit ports of the PIO. PA0 is the least-significant bit of the bus.

PB0–PB7. Port B Bus (bidirectional, tristated). One of the 8-bit ports of the PIO. PB_0 is the least-significant bit of the bus. This port can also supply 1.5mA at 1.5V to drive Darlington transistors.

PC0–PC7. Port C Bus (bidirectional, tristated). PC_0 is the least-significant bit of the bus. These pins are multiplexed between the 8-bit PIA and additional modem control signals for the serial channels.

RD. Read (input, active Low). When $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with A0–A3, $\overline{CS}$ and $\overline{IORQ}$ to transfer data between the KIO and CPU.

RESET. Reset (input, active Low). A Low on this pin forces the KIO into a Reset condition. This signal must be active for a minimum of three clock cycles. When the KIO is reset, the following events occur:

- The PIO ports are in Mode 1 operation
- Handshakes are inactive and interrupts are disabled
- The PIA port is in Input mode and active
- CTC channel counting is terminated and interrupts are disabled
- SIO channels are disabled
- Marking with interrupts is disabled

All control registers must be rewritten after a hardware reset.

$\overline{RTSA}$, $\overline{RTSB}$. Request to Send (outputs, active Low). These signals are modem control signals for their serial channels. They follow the inverse state programmed into their respective serial channels, and are multiplexed with Port C, bits 4 and 3, respectively.

$\overline{RxCA}$, $\overline{RxCB}$. Receive Clock (inputs, active Low). These clocks are used to assemble the data in the receiver shift register for their serial channels. Data is sampled on the rising edge of the clock.

RxDA, RxDB. Receive Data (inputs, active High). These pins are the input data pins to the receive shift register for their serial channels.

$\overline{SYNCA}$, $\overline{SYNCB}$. Synchronization (bidirectional, active Low). In the Asynchronous mode of operation, these pins act much like the $\overline{CTS}$ and $\overline{DCD}$ pins. Transitions affect the Sync/

Hunt status bit for their respective serial channels, but serve no other purpose. These pins are multiplexed with Port C, bits 6 and 1, respectively.

$\overline{\text{TxCA}}$, $\overline{\text{TxCB}}$. Transmit Clock (inputs, active Low). These clocks are used to transmit data from the transmit shift register for their serial channels. Data is transmitted on the falling edge of the clock.

TxDA, TxDB. Transmit Data (outputs, active High). These pins are the output data pins from the transmitter for their serial channels.

$\overline{\text{WT}}$/$\overline{\text{RDYA}}$, $\overline{\text{WT}}$/$\overline{\text{RDYB}}$. Wait/Ready (outputs, open-drain when programmed as Wait; tristated when programmed as Ready). These pins may be programmed as Ready lines for a DMA controller or Wait lines for interfacing to a CPU. As a Ready line, these pins indicate (when active Low) that the transmitter or the receiver requests a transfer between the serial channel and the DMA. As a Wait line, these pins dictate (when Low) that the CPU must wait until the transmitter or receiver can complete the requested transaction. These pins are multiplexed with Port C, bit 7 and 0, respectively.

XTALI. Crystal/Clock Connection. (input).

XTALO. Crystal Connection. (output).

ZC/TO0–ZC/TO3. Zero count/Time-Out (outputs, active High). These four pins are outputs from the four counter/timer channels of the KIO. Each pin pulses High when its corresponding downcounter reaches 0.

Register Address Decoding for the KIO

Address lines A0–A3 determine which one of the 16 control registers is being accessed. Table 2 shows the address decoding of each of the KIO control registers; also see Figure 9 on page 15.

Table 2. KIO Registers

Address	A3	A2	A1	A0
Register 0: PIO Port A Data	0	0	0	0
Register 1: PIO Port A Command	0	0	0	1
Register 2: PIO Port B Data	0	0	1	0
Register 3: PIO Port B Command	0	0	1	1
Register 4: CTC Channel 0	0	1	0	0

Note: Additionally, $\overline{\text{IORQ}}$ and $\overline{\text{CS}}$ must be Low. Registers are written to or read from by the CPU, applying a 1 or a 0 respectively on the $\overline{\text{RD}}$ pin.

Table 2. KIO Registers (Continued)

Address	A3	A2	A1	A0
Register 5: CTC Channel 1	0	1	0	1
Register 6: CTC Channel 2	0	1	1	0
Register 7: CTC Channel 3	0	1	1	1
Register 8: SIO Port A Data	1	0	0	0
Register 9: SIO Port A Command/Status	1	0	0	1
Register 10: SIO Channel B Data	1	0	1	0
Register 11: SIO Channel B Command/Status	1	0	1	1
Register 12: PIA Port C Data	1	1	0	0
Register 13: PIA Port C Command	1	1	0	1
Register 14: KIO Command	1	1	1	0
Register 15: KIO Command B	1	1	1	1

Note: Additionally, $\overline{IORQ}$ and $\overline{CS}$ must be Low. Registers are written to or read from by the CPU, applying a 1 or a 0 respectively on the $\overline{RD}$ pin.

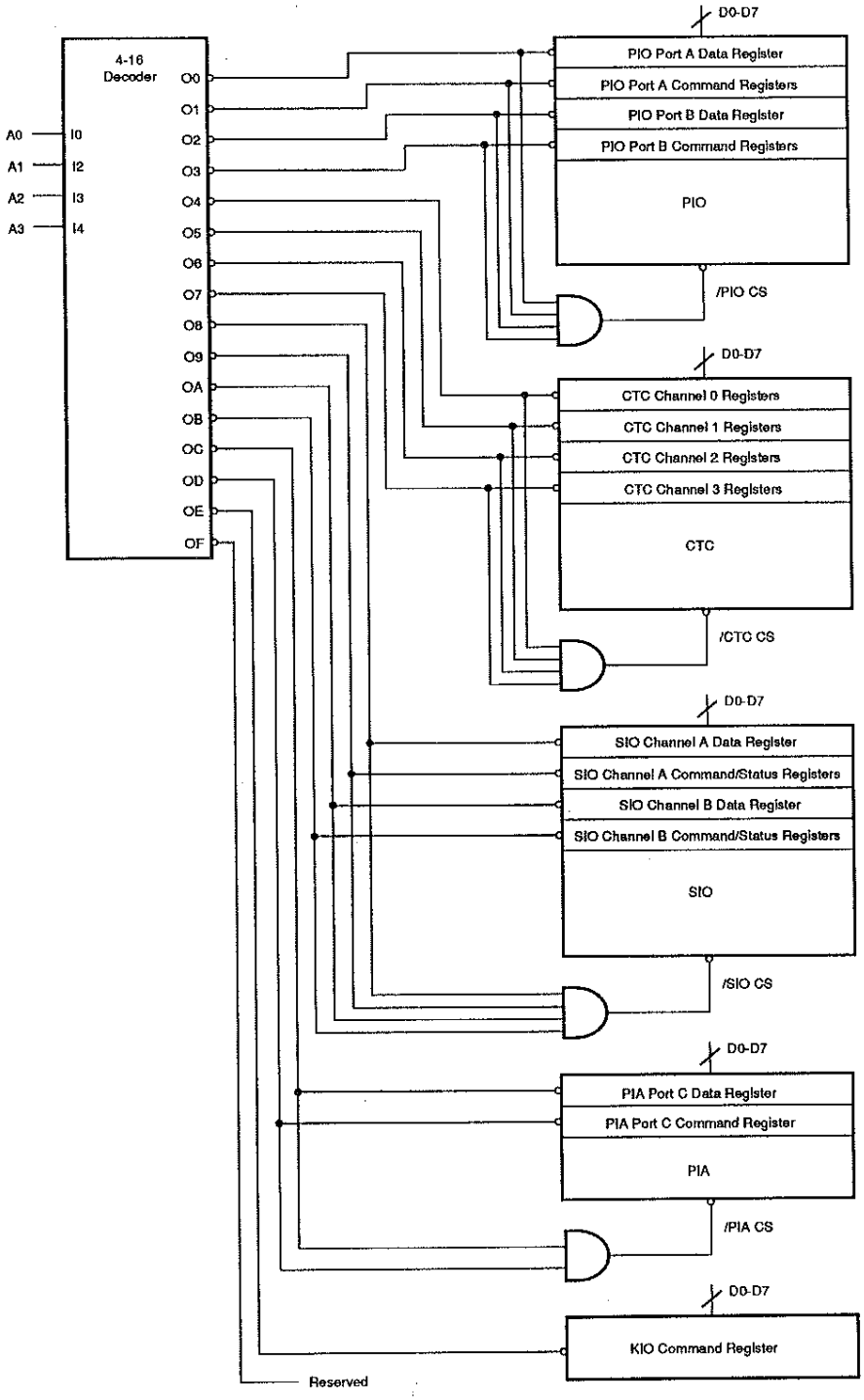


Figure 9. KIO Register Addressing

Register Programming

This section describes how the bits within each of the Z84C90 KIO's command registers change their respective command register functions, as well as the effects of such changes.

PIO Registers

The PIO registers described in this section apply to channels A and B (additionally, see the Register Address Decoding for the KIO section on page 13). For more information about these PIO registers, please consult the Z80 CPU Peripherals User Manual (UM0081).

Interrupt Vector Word. When Bit 0 of the command register is cleared to 0, the command register functions as the Interrupt Vector Word Register. The PIO logic unit is designed to work with the Z80 CPU in Interrupt Mode 2. This word must be programmed if interrupts are to be used; bit D0 must be 0. See Figure 10.

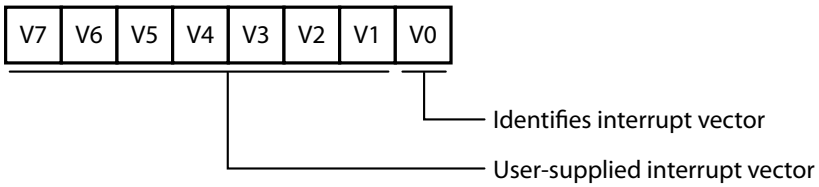


Figure 10. PIO Interrupt Vector Word Register

Mode Control Word. When bits B2 to B0 are set to 1, the command register functions as the Mode Control Word Register. Selects the port operating mode. This word is required and can be written at any time. See Figure 11.

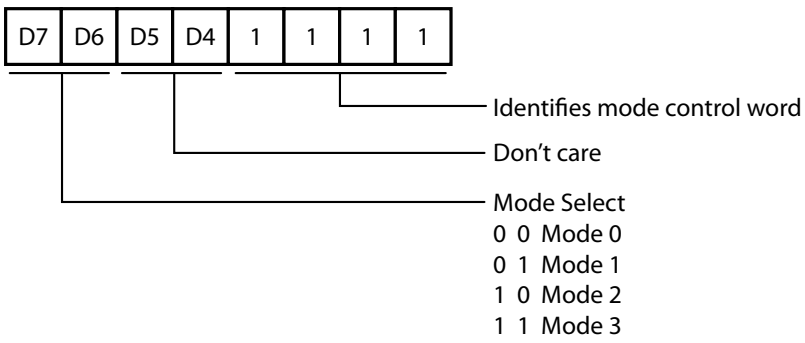


Figure 11. PIO Mode Control Word Register

I/O Register Control Word. When Mode 3 is selected, the Mode Control Word data must be followed by the loading of the I/O Register Control Word data. This word configures the I/O Register, which defines which port lines are inputs or outputs. A 1 indicates input, while a 0 indicates output. this word is required with in Mode 3. See Figure 12.

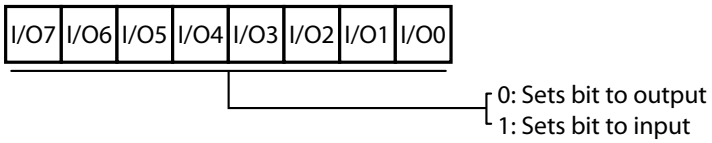
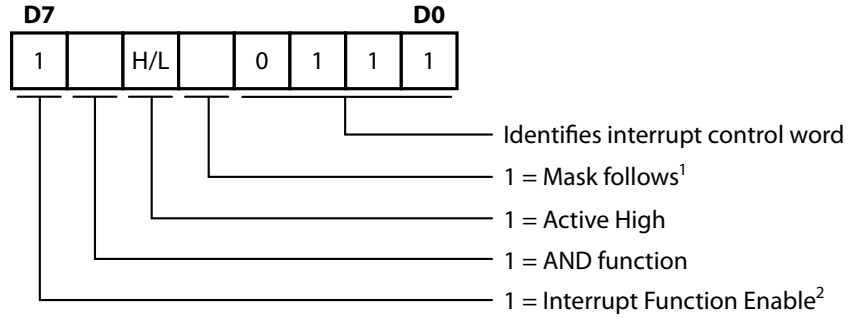


Figure 12. PIO I/O Register Control Word

PIO Interrupt Control Word. When bits D3 to D0 are loaded with 0111, the command register functions as the PIO Interrupt Control Word Register. In Mode 3 operation, handshake signals are not used. Interrupts are generated as a logic function of the input signal levels. The Interrupt Control Word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered) and OR (if any one of the input bits change to the active logic level, an interrupt is triggered). The user can also program which input bits are to be considered as part of this logic function. bit D6 sets the logic function, bit D5 sets the logic level and bit D4 specifies the mask control word data to follow. See Figure 13.



Notes:
1. Regardless of the operating mode, setting bit D4 = 1 causes any pending interrupts to be cleared.
2. The port interrupt is not enabled until the interrupt function enable is followed by an active M1.

Figure 13. PIO Interrupt Control Word

Mask Control Word. This words sets the Mask Control Register, thus allowing any unused bits to be masked off. If any bits are to be masked, bit D4 of the Interrupt Control

Word must be set. When bit D4 of the Interrupt Control Word is set, the next word loaded into the command register must be the Mask Control Word. To mask an input bit, the corresponding Mask Control Word bit must be a 1. See Figure 14.

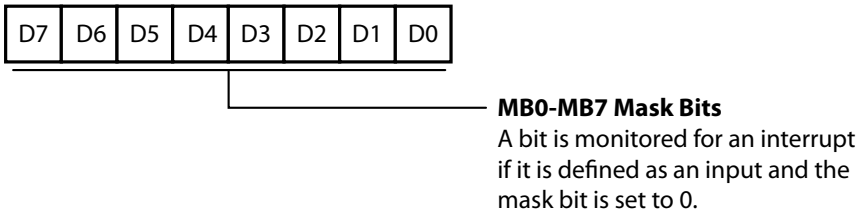


Figure 14. PIO Mask Control Word

Interrupt Disable Word. When bits B3 to B0 are loaded with 0011, the command register functions as the Interrupt Disable Word Register. This word can be used to enable or disable a port's interrupts without change the remainder of the port's interrupt conditions. See Figure 15.

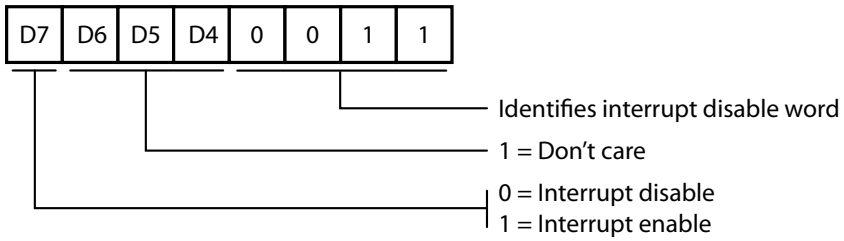


Figure 15. PIO Interrupt Disable Word

CTC Registers

The CTC registers apply to channels 0, 1, 2 and 3 (additionally, see the Register Address Decoding for the KIO section on page 13). For more information about these CTC registers, please consult the Z80 CPU Peripherals User Manual (UM0081).

Channel Control Word. This word sets the operating modes and parameters as described in the following paragraphs. Bit D0 of the CTC Register must be a 1 to indicate a Control Word; otherwise, it is an Interrupt Vector Word. See Figure 16.

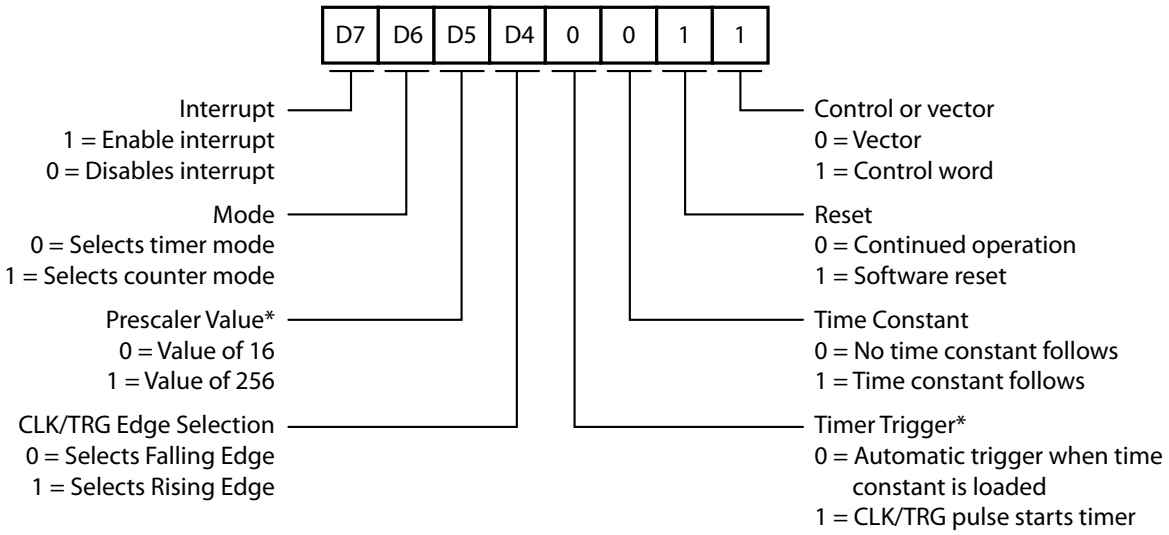


Figure 16. CTC Channel Control Word

Interrupt Enable. Bit D7 enables the interrupt logic so that an interrupt output ($\overline{INT}$) can be generated at zero count. Interrupts can be programmed in either mode and can be enabled or disabled at any time.

Mode. Bit D6 selects either Timer Mode or Counter Mode.

Prescale Factor. Bit D5 selected the prescale factor for use in Timer Mode. Either divide-by-16 or divide-by-256 is available.

Clock/Trigger Edge Selector. Bit D4 selects the active edge of the CLK/TRG input pulses.

Timer Trigger. Bit D3 selects the trigger mode for timer operation. Either an automatic or an external trigger can be selected.

Time Constant. Bit D2 indicates that the next word loaded into this register is the time constant data for the downcounter.

Software Reset. Setting bit D1 indicates a software reset operation.

Time Constant Word. Before a channel can start counting, it must receive a time constant word. The time constant value can be anywhere between 1 and 256, with 0 being accepted as a count of 256. See Figure 17.

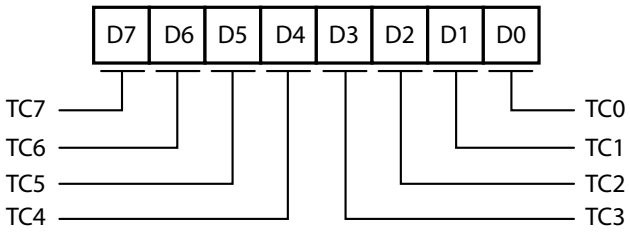


Figure 17. CTC Time Constant Word

Interrupt Vector Word. If one or more of the CTC channels have interrupts enabled, the Interrupt Vector Word must be programmed into the CTC Register. Only the five most significant bits of this word are programmed, and bit D0 must be 0. Bits D2–D1 are automatically modified by the CTC channel when it responds with an interrupt vector. See Figure 18.

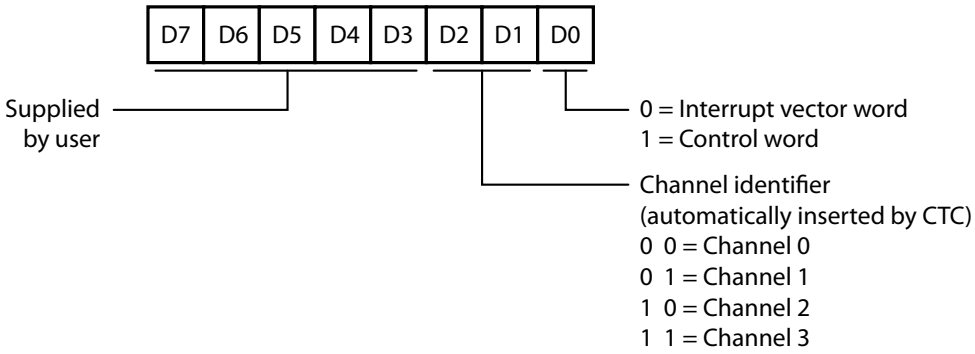


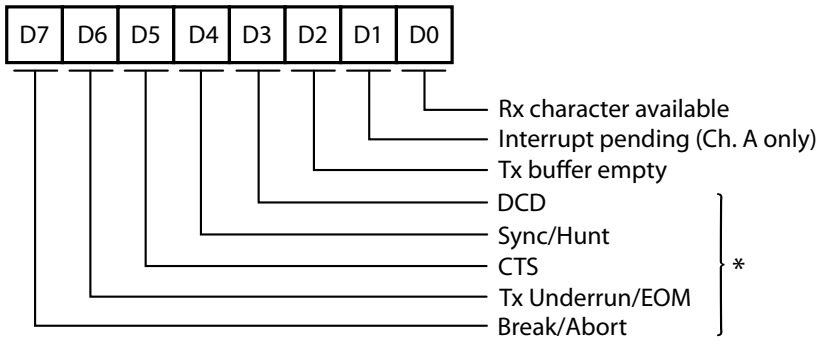
Figure 18. CTC Interrupt Vector Word

SIO Registers

These registers apply to channels A and B (additionally, see the Register Address Decoding for the KIO section on page 13). The Command/Status Register initially functions as Write Register 0 (WR0) and operates as a pointer to the read registers or to the write registers. The read register for Write Register 0 is RR0. The read registers for Write Register 1 and Write Register 2 are RR1 and RR2, respectively.

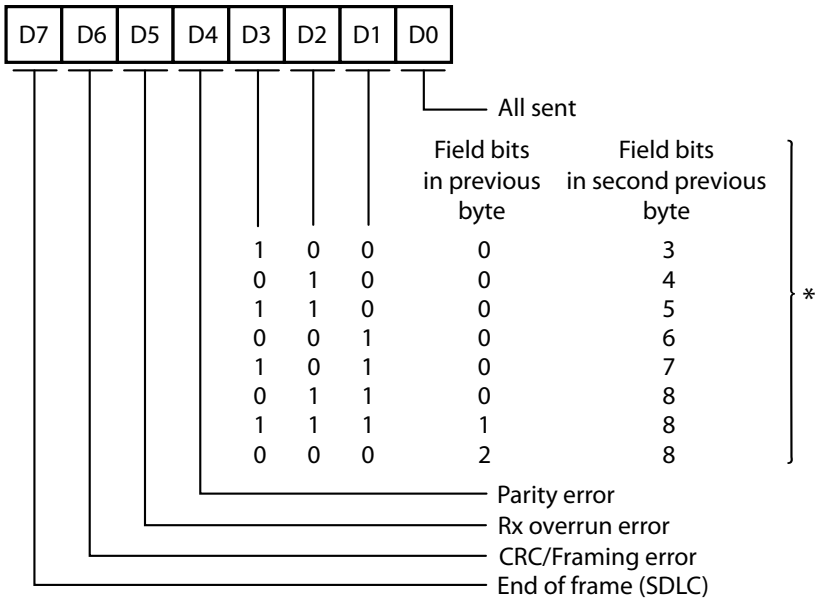
For more information about these SIO registers, please consult the Z80 CPU Peripherals User Manual (UM0081).

Read Registers. SIO Channel B contains three read registers while Channel A contains only two that can be read to obtain status information. To read the contents of a register (other than RR0), the program must first write a pointer to WR0 in exactly the same manner as a write register operation. The next I/O read cycle will place the contents of the selected read register onto the data bus. See Figures 19 through 21.



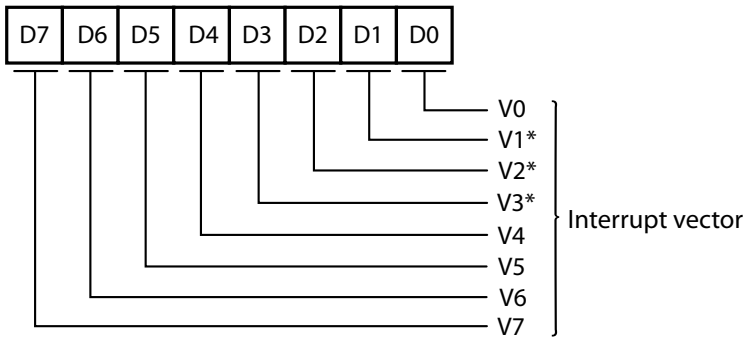
Note: *Used with External/Status Interrupt modes.

Figure 19. SIO Read Register 0



Notes: *Residue data for eight Rx bits/character programmed.
**Used with a special receive condition mode.

Figure 20. SIO Read Register 1**



Note: *Variable if Status Affects Vector is also programmed.

Figure 21. SIO Read Register 2 (Channel B only)

Write Registers. SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating modes and characteristics of each channel. With the exception of WR0, programming the write registers is a two-step operation. The first operation is a pointer written to WR0 that points to the selected register. The second operation is the actual control word data that is written into the register to configure the SIO channel. See Figures 22 through 29 to examine the details of these write registers.

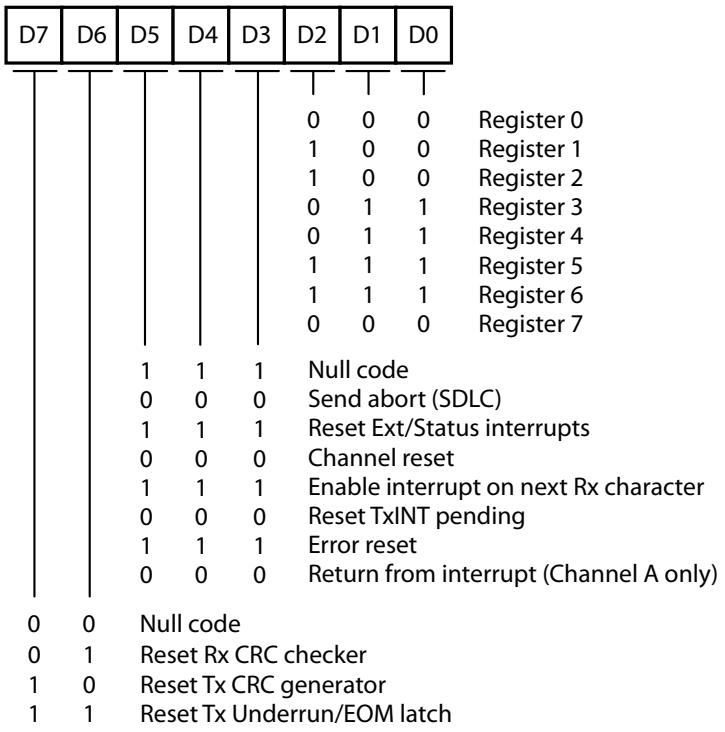
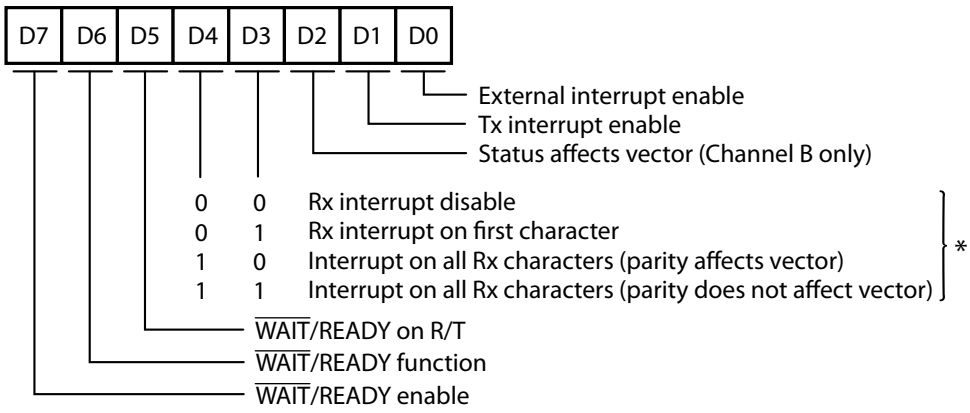


Figure 22. SIO Write Register 0



Note: *Or on special condition.

Figure 23. SIO Write Register 1

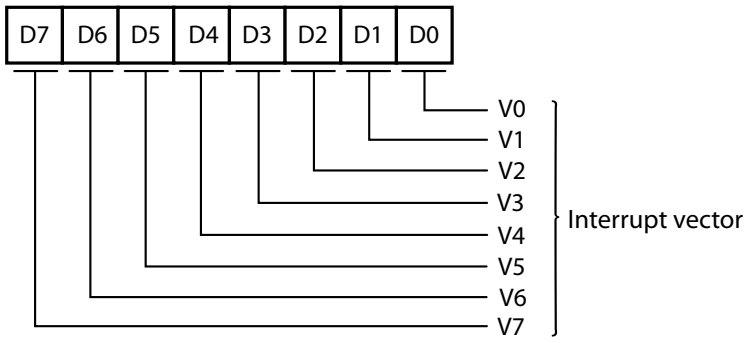


Figure 24. SIO Write Register 2 (Channel B only)

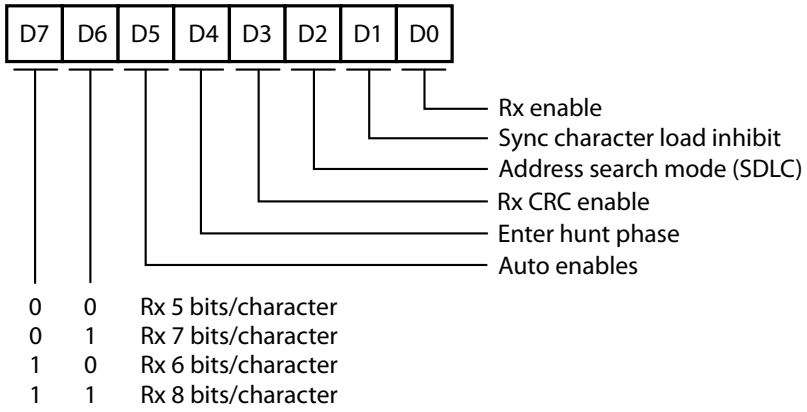


Figure 25. SIO Write Register 3

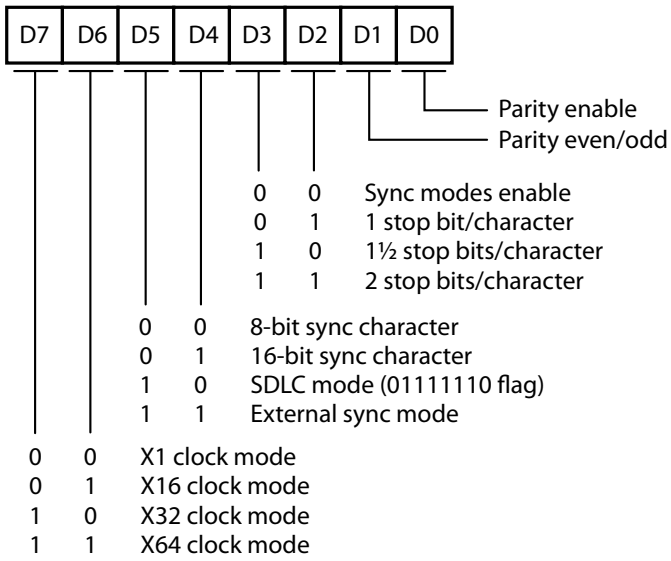


Figure 26. SIO Write Register 4

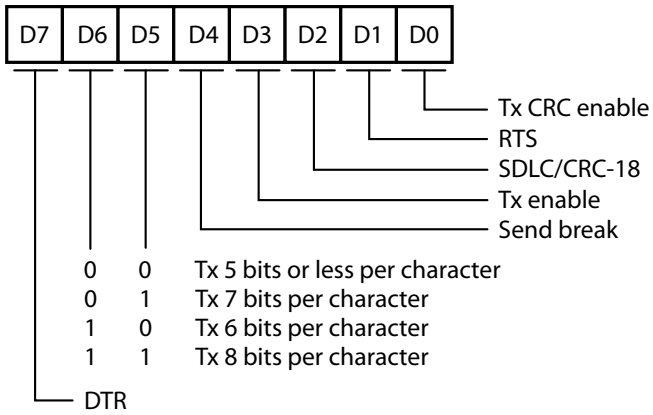
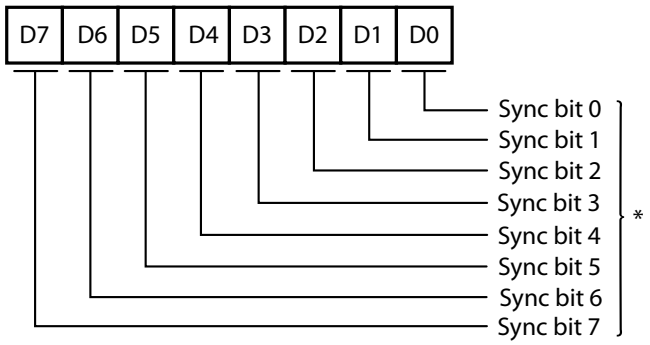
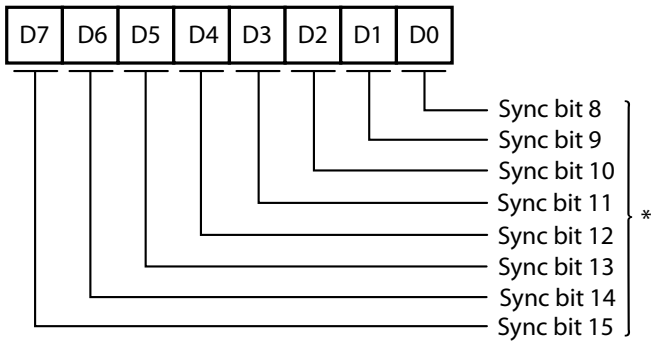


Figure 27. SIO Write Register 5



Note: *Also SDLC address field.

Figure 28. SIO Write Register 6



Note: For SDLC, these bits must be programmed to 01111110 for flag recognition.

Figure 29. SIO Write Register 7

PIA Registers

The PIA port can be configured for any combination of input and output bits. The direction is controlled by writing to the PIA Control Register. A 1 written to a bit position indicates that the respective bit should be an input (see Figure 30). All bits are inputs upon reset.

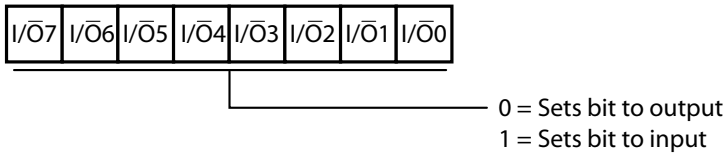


Figure 30. PIA Control Register

KIO Command Register

Command Register A is used to program software resets and to configure the internal interrupt daisy chain priority (see Figure 31). *This register should be programmed before all others.* The reset control bits are momentary; writing a 1 pulses an internal reset signal to the appropriate device.

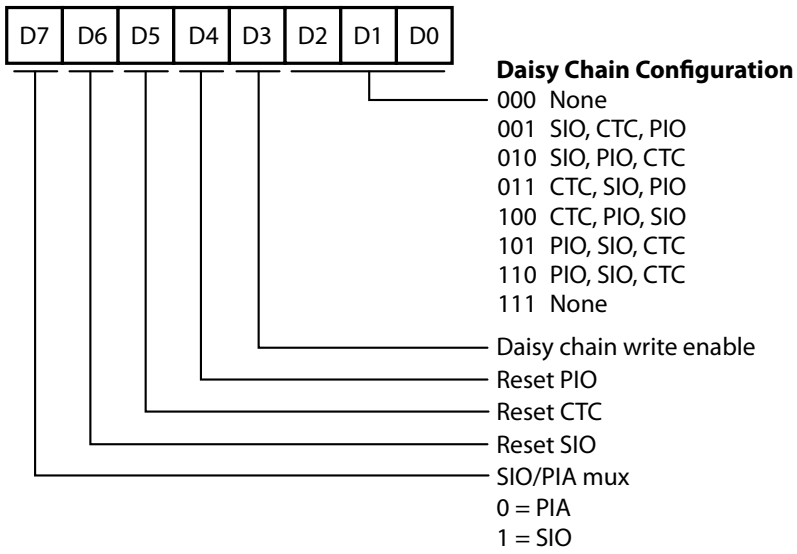


Figure 31. KIO Command Register A

Z84C90 KIO: Enhanced Version

A subsequent revision of the Z84C90 MCU features an enhancement which allows users to simulate the Return From Interrupt sequence with software. This feature allows the interfacing of the CPU to other devices in addition to the Z80 CPU (or the Z180/Z280).

Command Register B. Writing a 1 to a particular command bit location of the KIO generates a RETI sequence internally. Every time a RETI is required, a 1 is written to this bit to allow software control of the RETI.

Programming of this Feature. This revision has one newly assigned register at Register Address 15 (this location is *reserved* on the original version). The bit assignments for this register are shown in Figure 32.

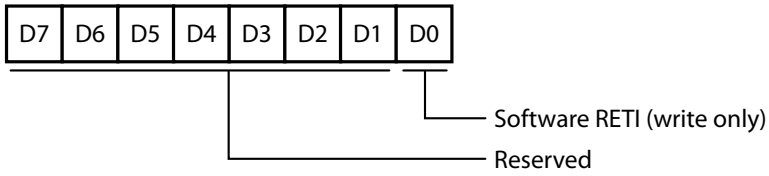


Figure 32. KIO Register 15: KIO Command Register B

Writing a 1 to the bit D0 location of this register enables the KIO to simulate a RETI sequence. Writing a 0 to this bit yields no effect. The upper 7 bits of this register (D7–D1) are reserved and should be programmed to 0. If this register is read, unpredictable data is returned.

Notes: After writing a 1 to this bit, 8 clock cycles of access recovery time is required before additional access to the KIO can occur. If accessing the KIO within this recovery period, the KIO ignores the transaction on the bus.

When simulating RETI, the status of the IEI pin is ignored with an internally forced H. If there are other peripherals on the upper interrupt daisy chain, caution must be exercised.

Electrical Characteristics

The data in this chapter represents all known data prior to qualification and characterization of the Z84C90 KIO device and is therefore subject to change. Additional electrical characteristics can be found in the individual chapters of this document.

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Voltage on V_{CC} with respect to V_{SS}	–0.3V to +7.0V
Voltages on all inputs with respect to V_{SS}	–0.3V to V_{CC} +0.3V
Operating Ambient Temperature	See Ordering Information
Storage Temperature	–65°C to +150°C

Standard Test Conditions

The DC Characteristics and Capacitance sections that follow apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature ranges are:

- S = 0°C to +70°C
- E = –40°C to +100°C

Voltage Supply Range: +5.0V ±10%

All AC parameters assume a load capacitance of 100 pF, as shown in Figure 33. Add a 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points.

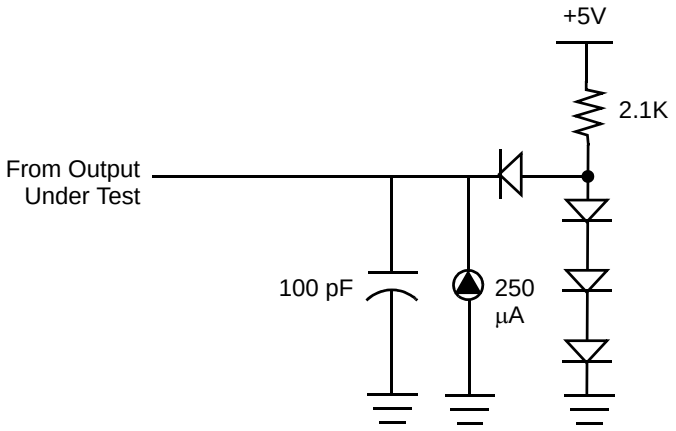


Figure 33. Test Load Diagram

DC Characteristics

Table 3 lists the direct current characteristics for the Z84C90 KIO Peripheral. In this table, V_{CC} = 5.0V ±10% unless otherwise specified.

Table 3. DC Characteristics of the Z84C90

Symbol	Item	Min	Max	Unit	Condition
V_{ILC}	Clock Input Low Voltage	–0.3	+0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC}–0.6	V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	–0.3	+0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 2.0mA
V_{OH1}	Output High Voltage 1	2.4		V	I_{OH} = –1.6mA
V_{OH2}	Output High Voltage 2	V_{CC}–0.8		V	I_{OH} = –250mA
I_{LI}	Input Leakage Current		±10.0	µA	V_{IN} = 0.4~V_{CC}
I_{OL}	3-State Leakage Current		±10.0	µA	V_{IN} = 0.4~V_{CC}
$I_{L(SY)}$	SYNC Pin Leakage Current	–40	+10	µA	V_{IN} = 0.4~V_{CC}

Note: *Measurement made with output floating over specified temperature and voltage ranges with V_{CC} = 5V, V_{IH} = V_{CC}–0.2V and V_{IL} = 0.2V.

Table 3. DC Characteristics of the Z84C90 (Continued)

Symbol	Item	Min	Max	Unit	Condition
I_{OHD}	Darlington Drive Current (Port B and ZC/T00~3)	–1.5		mA	V_{OH} = 1.5V R_{EXT} = 390Ω
I_{CC}	Power Supply Current*				
	8MHz		15	mA	
	10MHz		15	mA	
	12.5MHz		15	mA	

Note: *Measurement made with output floating over specified temperature and voltage ranges with V_{CC} = 5V, V_{IH} = V_{CC}–0.2V and V_{IL} = 0.2V.

Figure 34 shows the timing of reads and writes for the Z84C90 KIO Peripheral's I/O block.

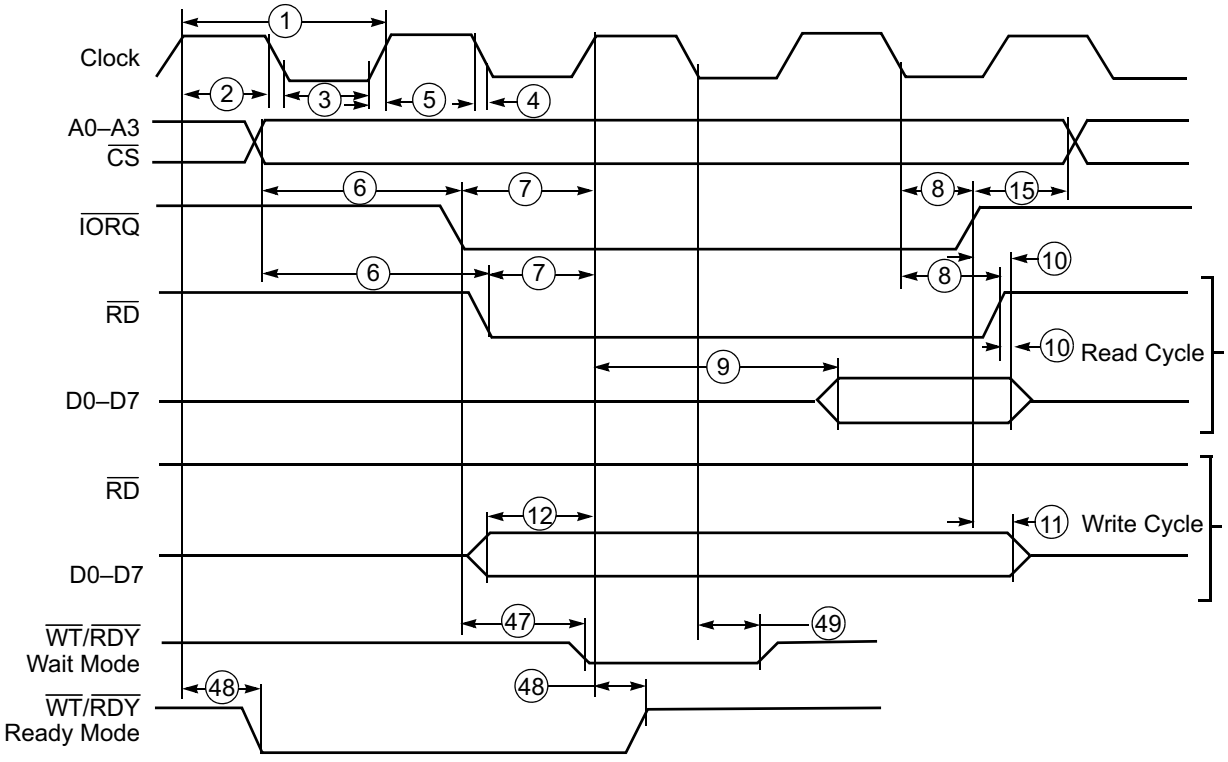
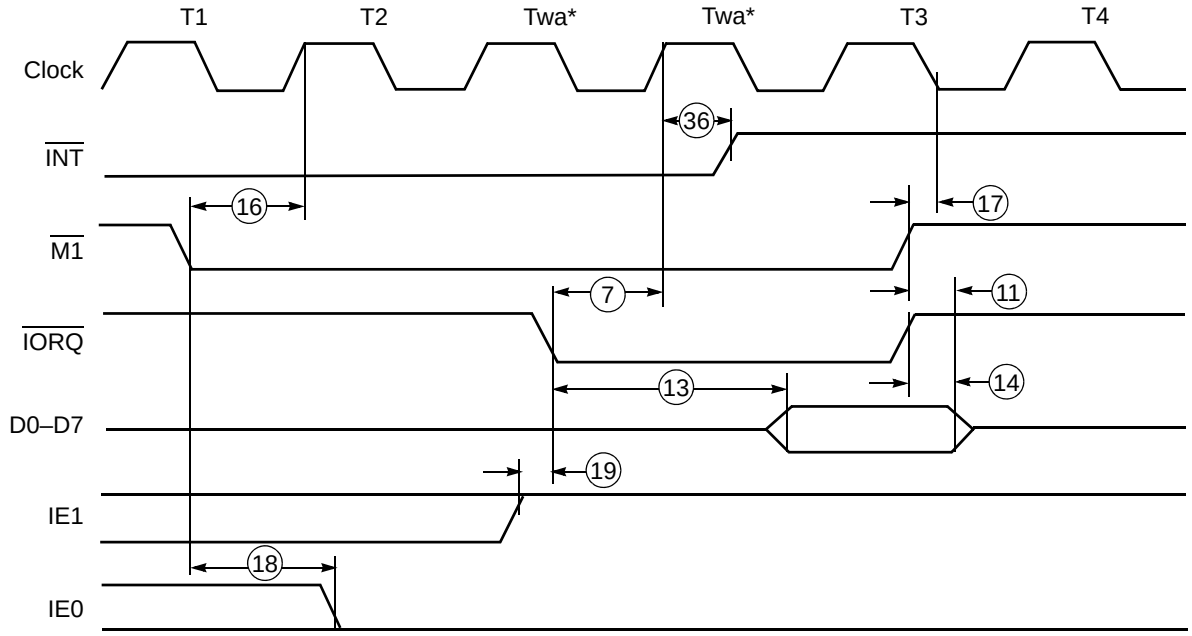


Figure 34. I/O Read/Write Timing ($\overline{M1}$ = 1)

Figure 35 shows the timing of the Z84C90 KIO Peripheral's interrupts.



*Wait state.

Figure 35. Interrupt Acknowledge Cycle

Figure 36 shows the timing of the Z84C90 KIO Peripheral's counter/timer.

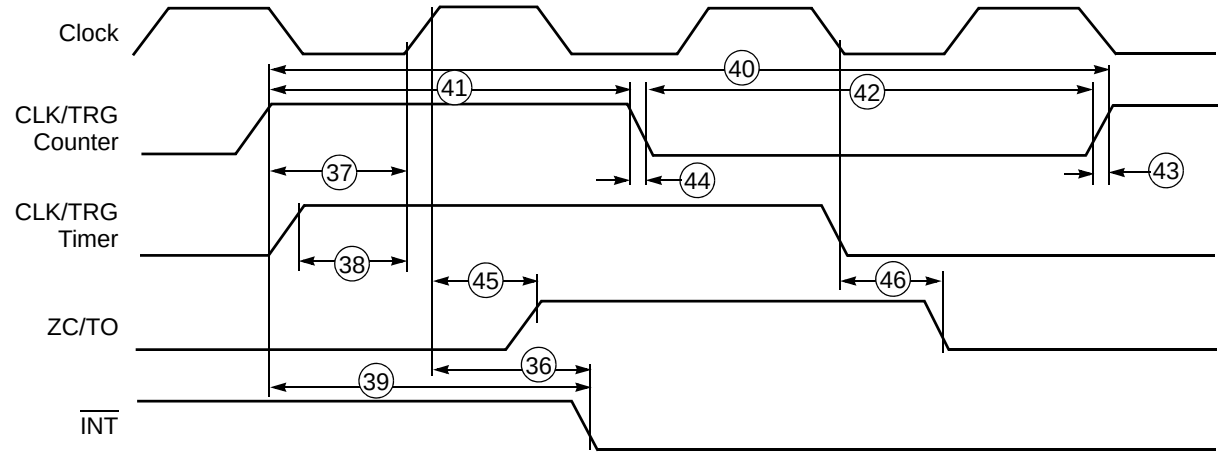


Figure 36. Counter/Timer Timing

Figure 37 shows the timing for the RETI sequence.

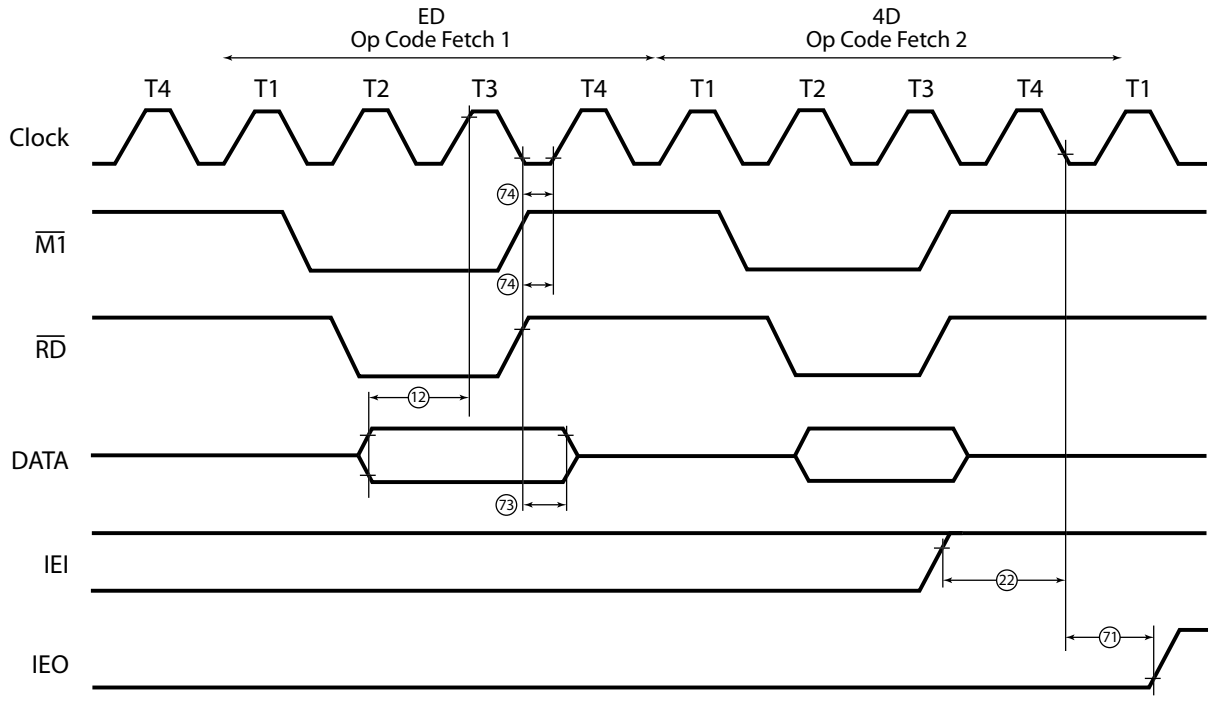


Figure 37. RETI Timing Standard Function

Figure 38 shows the interrupt timing that occurs when a RETI sequence is pending.

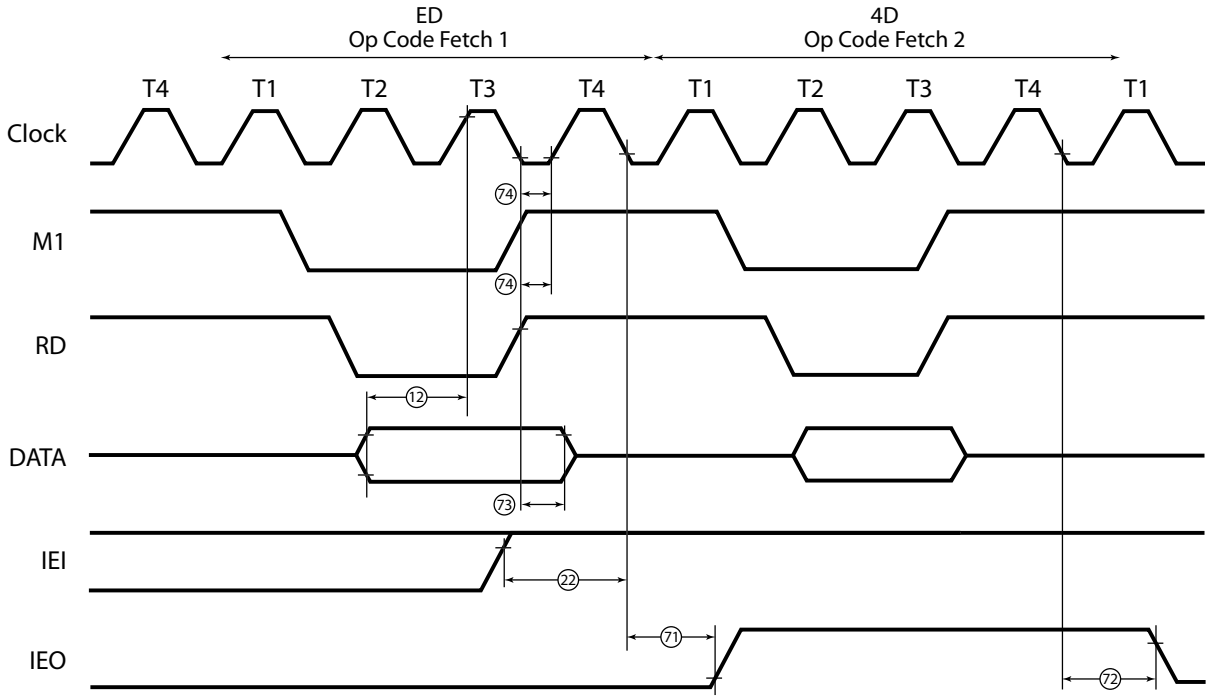


Figure 38. RETI Timing Interrupt Pending

Figure 39 shows the read and write timing of the Z84C90 KIO Peripheral's GPIO ports.

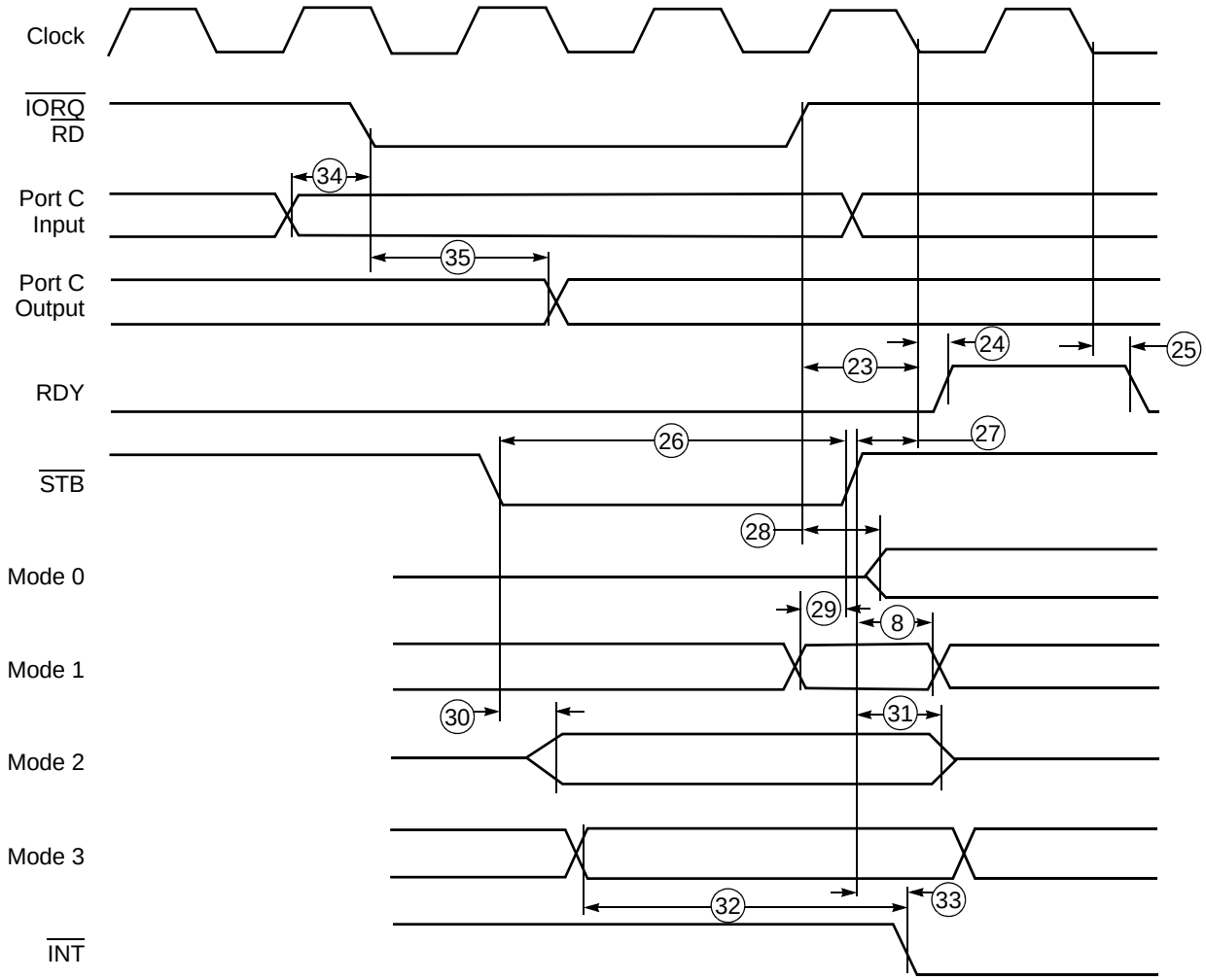


Figure 39. Port I/O Read/Write Timing

Figure 40 shows the serial timing of the Z84C90 KIO Peripheral's I/O block.

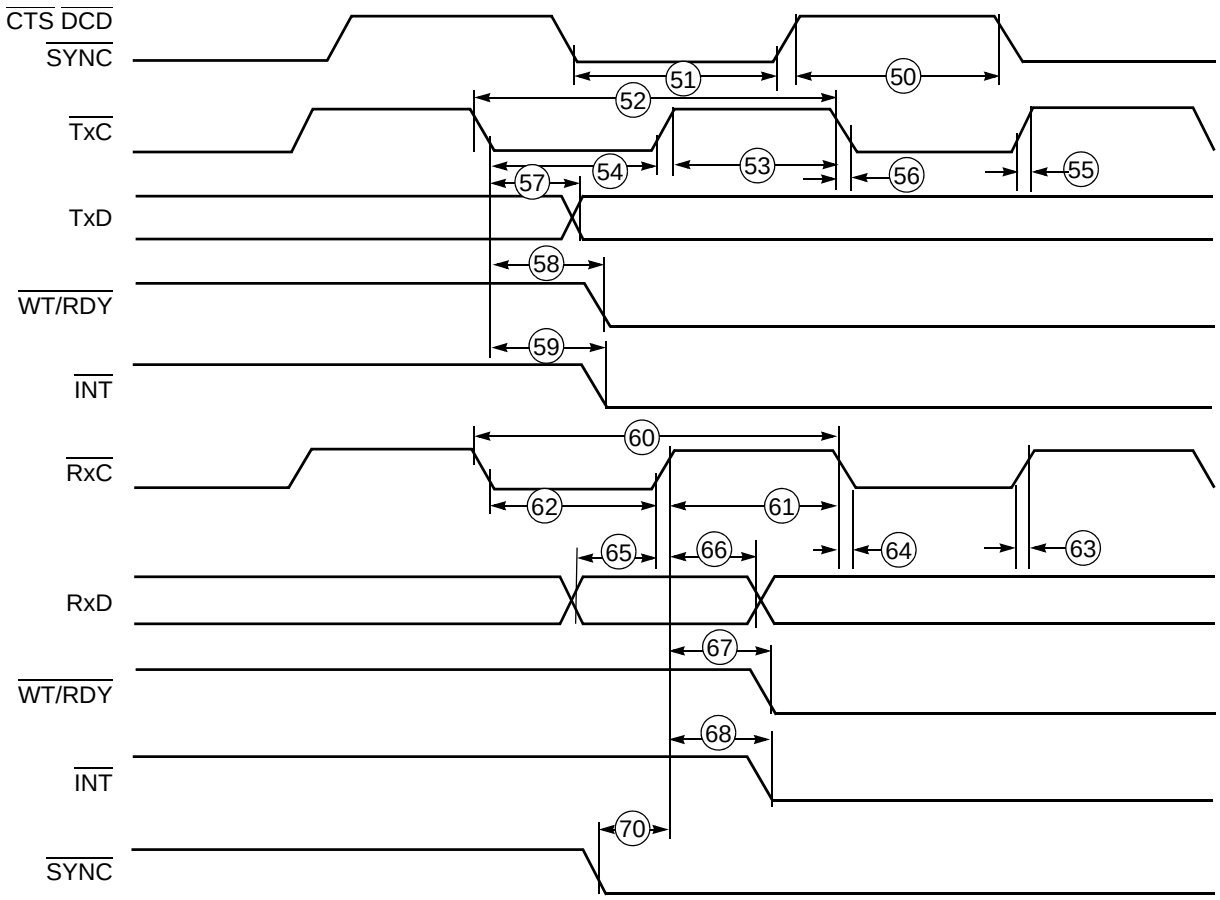


Figure 40. Serial I/O Timing

Figure 41 shows the Z84C90 KIO Peripheral operation code fetch timing.

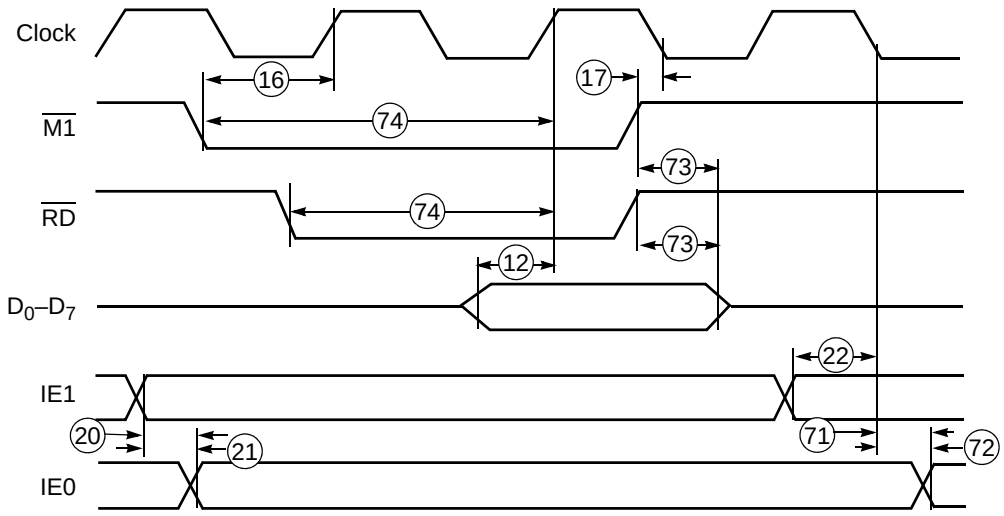


Figure 41. Op Code Fetch Cycle

Capacitance

Table 4 lists the clock and input/output capacitance values for the Z84C90 KIO Peripheral.

Table 4. Capacitance

Symbol	Parameter	Minimum	Maximum	Unit
C_{CLOCK}	Clock Capacitance		10	cF
CI_N	Input Capacitance		10	cF
C_{OUT}	Output Capacitance		15	cF
Note: T_A = 25°C, f = 1MHz.				

AC Characteristics

Table 5 lists the alternating current characteristics for the Z84C90 KIO Peripheral.

Table 5. AC Characteristics of the Z84C90

			8MHz		10MHz[1,6]		12.5MHz[1,6]		
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**U/M**
Bus Interface Timing									
1	TcC	Clock Cycle Time	125	DC	100	DC	80	DC	ns
2	TwCh	Clock Pulse Width (High)	55	DC	42	DC	32	DC	ns
3	TwCl	Clock Pulse Width (Low)	55	DC	42	DC	32	DC	ns
4	TfC	Clock Fall Time		10		10		10	ns
5	TrC	Clock Rise Time		10		10		10	ns
6	TsA(Rlf)	Address, $\overline{CS}$ Setup to $\overline{RD}$, $\overline{IORQ}$ Fall	50		40		30		ns
7	TsRl(Cr)	$\overline{RD}$, $\overline{IORQ}$ to Clock Rise Setup	50		50		40		ns
8	Th	Hold Time for Specified Setup	15		15		15		ns
9	TdCr(DO)	CLOCK Rise to Data Out Delay		100		80		65	ns
10	TdRlr(DOz)	$\overline{RD}$, $\overline{IORQ}$ Rise to Data Out Float Delay		75		60		55	ns
11	ThRDr(D)	$\overline{M1}$,$\overline{RD}$,$\overline{IORQ}$ Rise to Data Float	15		15		15		ns
12	TsD(Cr)	Data in to Clock Rise Setup	30		25		22		ns
13	TdIOI(DOI)	$\overline{IORQ}$ Fall to Data Out Delay (INTACK Cycle)[2]		95		95		95	ns
14	ThIOr(D)	$\overline{IORQ}$ Rise to Data Float (INTACK)	15		15		15		ns
15	THIOr(A)	$\overline{IORQ}$ Rise to Address Hold	15		15		15		ns
16	TsM1f(Cr)	$\overline{M1}$ Fall to Clock Rise Setup	40		40		40		ns
17	TsM1r(Cf)	$\overline{M1}$ Rise to Clock Fall Setup (M1 Cycle)	–15		–15		–15		ns
18	TdM1f(IEOf)	$\overline{M1}$ Fall to IEO Fall Delay (Interrupt Immediately preceding M1 Fall)[3]	–		–		–		ns
19	TsIEI(IOf)	IEI to $\overline{IORQ}$ Fall Setup[3]							ns

Notes:
1. Maximum SIO data rate is f_{CLOCK} ÷ by 5, in which $f_{CLOCK} = 1 \div T_CC$.
2. For a Z80 CPU operating above 8MHz, one wait state is required to meet this parameter.
3. These daisy chain parameters include contributions from the PIO, SIO and CTC cells, and vary slightly depending on how they are ordered by the KIO Command Register.
4. Counter mode only; when using a cycle time less than 3 TcC, parameter #37 must be met.
5. Units are TcC.
6. If the CPU is a Z80 CPU and if it is required to have multiple Z80 peripherals in the system, then the time period between $\overline{M1}$ to $\overline{IORQ}$ must be extended.
7. Any open-drain output must add a Register-Capacitor (RC) time constant to the specification value.

Table 5. AC Characteristics of the Z84C90 (Continued)

No.	Symbol	Parameter	8MHz		10MHz[1,6]		12.5MHz[1,6]		U/M
			Min	Max	Min	Max	Min	Max	
Bus Interface Timing (continued)									
20	TdIEIf(IEOf)	IEI Fall to IEO Fall Delay[3]		160		150		125	ns
21	TdIEIf(IEOr)	IEI Rise to IEO Rise Delay (after ED Decode)[3]		160		150		125	ns
22	TsIEI(Cf)	IEI to Clock Fall Setup (for 4D Decode)	50		40		30		ns
23	TsIOr(Cf)	$\overline{IORQ}$ Rise to Clock Fall Setup (to activate $\overline{RDY}$ on next clock)	100		100		100		ns
PIO Timing									
24	TdCf(RDYr)	Clock Fall to $\overline{RDY}$ Rise Delay		100		100		100	ns
25	TdCf(RDYf)	Clock Fall to $\overline{RDY}$ Fall Delay		100		100			ns
26	TwSTB	$\overline{STB}$ Pulse Width	100		80		60		ns
27	TsSTBr(Cf)	$\overline{STB}$ Rise to Clock Fall Setup (to activate $\overline{RDY}$ on next clock cycle)	100		100				ns
28	TdIOf(PD)	$\overline{IORQ}$ Fall to Port Data Valid (Mode 0)		140		120		110	ns
29	TsPD(STBr)	Port A,B Data to $\overline{STB}$ Rise Setup Time (Mode 1)	140		75		75		ns
30	TdSTBI(PD)	$\overline{STB}$ Fall to Port A,B Data Valid Delay (Mode 2)		150		120		110	ns
31	TdSTBr(PDz)	$\overline{STB}$ Rise to Port Data Float Delay (Mode 2)		140		120		110	ns
32	TdPD(INTf)	Port Data Match to $\overline{INT}$ Fall Delay (Mode 3)		250		200		160	ns
33	TdSTBr(INTf)	$\overline{STB}$ Rise to $\overline{INT}$ Fall Delay		290		220		190	ns
34	TsPD(RIf)	PIA Port Data to $\overline{RD}$, $\overline{IORQ}$ Fall Setup	TBD		TBD			TBD	–

Notes:
1. Maximum SIO data rate is f_{CLOCK} ÷ by 5, in which $f_{CLOCK} = 1 \div T_CC$.
2. For a Z80 CPU operating above 8MHz, one wait state is required to meet this parameter.
3. These daisy chain parameters include contributions from the PIO, SIO and CTC cells, and vary slightly depending on how they are ordered by the KIO Command Register.
4. Counter mode only; when using a cycle time less than 3 TcC, parameter #37 must be met.
5. Units are TcC.
6. If the CPU is a Z80 CPU and if it is required to have multiple Z80 peripherals in the system, then the time period between M1 to IORQ must be extended.
7. Any open-drain output must add a Register-Capacitor (RC) time constant to the specification value.

Table 5. AC Characteristics of the Z84C90 (Continued)

No.	Symbol	Parameter	8MHz		10MHz[1,6]		12.5MHz[1,6]		U/M
			Min	Max	Min	Max	Min	Max	
PIO Timing (continued)									
35	TdCr(PD)	Clock Rise to Port Data Valid Delay		80		80		80	ns
CTC Timing									
36	TdCr(INTf)	Clock Rise to $\overline{INT}$ Rise Delay	TcC+100		TcC+80		TcC+75		ns
37	TsCTRr(Cr)c	CLK/TRG Rise to Clock Rise Setup (for immediate count, Counter mode)	90		90		75		ns
38	TsCTRr(Cr)t	CLK/TRG Rise to Clock Rise Setup (for enabling prescaler on following Clock Rise, Timer mode)	90		90		75		ns
39	TdCTRr(INTf)	CLK/TRG Rise to INT Fall Delay TsCTRr(Cr) satisfied TsCTRr(Cr) not satisfied	 (36)+(38) (1)+(36)+(38)		 (36)+(38) (1)+(36)+(38)		 (36)+(38) (1)+(36)+(38)		ns
40	TcCTR	CLK/TRG Cycle Time[4]	(2TcC)	DC	(2TcC)	DC	(2TcC)	DC	ns
41	TwCTRh	CLK/TRG Width High	90	DC	90	DC	75	DC	ns
42	TwCTRl	CLK/TRG Width Low	90	DC	90	DC	75	DC	ns
43	TrCTR	CLK/TRG Rise Time		30		30		30	ns
44	TfCTR	CLK/TRG Fall Time		30		30		30	ns
45	TdCr(ZCr)	Clock Rise to ZC/TO Rise Delay		80		80		80	ns
46	TdCf(ZCf)	Clock Fall to ZC/TO Fall Delay		80		80		80	ns
SIO Timing									
47	TdIOf(W/Rf)	$\overline{IORQ}$ Fall to $\overline{WT}$/$\overline{RDY}$ Fall Delay (Wait Mode)		130		110		110	ns
48	TdCr(W/Rf)	Clock Rise to $\overline{WT}$/$\overline{RDY}$ Delay (Ready Mode)		85		85		85	ns
49	TdCf(W/Rz)	Clock Fall to $\overline{WT}$/$\overline{RDY}$ Float Delay (Wait Mode)[7]		90+RC		80+RC		75+RC	ns

Notes:
1. Maximum SIO data rate is f_{CLOCK} ÷ by 5, in which $f_{CLOCK} = 1 \div T_CC$.
2. For a Z80 CPU operating above 8MHz, one wait state is required to meet this parameter.
3. These daisy chain parameters include contributions from the PIO, SIO and CTC cells, and vary slightly depending on how they are ordered by the KIO Command Register.
4. Counter mode only; when using a cycle time less than 3 TcC, parameter #37 must be met.
5. Units are TcC.
6. If the CPU is a Z80 CPU and if it is required to have multiple Z80 peripherals in the system, then the time period between M1 to IORQ must be extended.
7. Any open-drain output must add a Register-Capacitor (RC) time constant to the specification value.

Table 5. AC Characteristics of the Z84C90 (Continued)

No.	Symbol	Parameter	8MHz		10MHz[1,6]		12.5MHz[1,6]		U/M
			Min	Max	Min	Max	Min	Max	
SIO Timing (continued)									
50	TwPh	Pulse Width High	150		120		100		ns
51	TwPl	Pulse Width Low	150		120		100		ns
52	TcTxC	$\overline{TxC}$ Cycle Time	250	DC	200	DC	160	DC	ns
53	TwTxCh	$\overline{TxC}$ Width High	85	DC	80	DC	70	DC	ns
54	TwTxCl	$\overline{TxC}$ Width Low	85	DC	80	DC	70	DC	ns
55	TrTxC	$\overline{TxC}$ Rise Time		60		60		60	ns
56	TfTxC	$\overline{TxC}$ Fall Time		60		60		60	ns
57	TdTxCf(TxD)	$\overline{TxC}$ Fall to TxD Delay (x1 mode)		160		120		115	ns
58	TdTxCf(W/Rf)	$\overline{TxC}$ Fall to $\overline{WT}$/$\overline{RDY}$ Fall Delay (Ready Mode)[5]	5	9	5	9		59	ns
59	TdTxCf(INTf)	$\overline{TxC}$ Fall to $\overline{INT}$ Fall Delay[5]	5	9	5	9		59	ns
60	TcRxC	$\overline{RxC}$ Cycle Time	250	DC	200	DC	160	DC	ns
61	TwRxCh	$\overline{RxC}$ Width High	85	DC	80	DC	70	DC	ns
62	TwRxCl	$\overline{RxC}$ Width Low	85	DC	80	DC	70	DC	ns
63	TrRxC	$\overline{RxC}$ Rise Time		60		60		60	ns
64	TfRxC	$\overline{RxC}$ Fall Time		60		60		60	ns
65	TsRxD(RxCr)	RxD to $\overline{RxC}$ Rise Setup	0		0		0		ns
66	ThRxCr(RxD)	$\overline{RxC}$ Rise to RxD Hold Time	80		60		50		ns
67	TdRxCr(W/Rf)	$\overline{RxC}$ Rise to $\overline{W}$/$\overline{RDY}$ Fall Delay (Ready Mode)[5]	10	13	10	13	10	13	ns
68	TdRxCf(INTf)	$\overline{RxC}$ to $\overline{INT}$ Fall Delay[5]	10	13	10	13	10	13	ns
69	TdRxCr (SYNCf)	$\overline{RxC}$ Rise to $\overline{SYNC}$ Fall Delay (Output Mode)	4	7	4	7	4	7	ns

Notes:
1. Maximum SIO data rate is $f_{CLOCK} \div$ by 5, in which $f_{CLOCK} = 1 \div T_CC$.
2. For a Z80 CPU operating above 8MHz, one wait state is required to meet this parameter.
3. These daisy chain parameters include contributions from the PIO, SIO and CTC cells, and vary slightly depending on how they are ordered by the KIO Command Register.
4. Counter mode only; when using a cycle time less than 3 TcC, parameter #37 must be met.
5. Units are TcC.
6. If the CPU is a Z80 CPU and if it is required to have multiple Z80 peripherals in the system, then the time period between M1 to IORQ must be extended.
7. Any open-drain output must add a Register-Capacitor (RC) time constant to the specification value.

Table 5. AC Characteristics of the Z84C90 (Continued)

No.	Symbol	Parameter	8MHz		10MHz[1,6]		12.5MHz[1,6]		U/M
			Min	Max	Min	Max	Min	Max	
SIO Timing (continued)									
70	TsSYNCf (RxCr)	$\overline{SYNC}$ Fall to $\overline{RxC}$ Rise Setup (External Sync Mode)	–100		–100		–100		ns
71	TdCf(IEOr)	Clock Fall to IEO Rise Delay		90		75		60	ns
72	TdCf(IEOf)	Clock Fall to IEO Fall Delay		110		90		75	ns
73	ThDI(M1r,Rdr)	Data Hold Time to $\overline{M1}$ Rise or $\overline{RD}$ Rise	0		0		0		ns
74	TsM1/RD(C)	Setup time for M1 and RD to clock Rising (with Data Valid)	20		20		20		ns

Notes:
1. Maximum SIO data rate is $f_{CLOCK} \div$ by 5, in which $f_{CLOCK} = 1 \div T_CC$.
2. For a Z80 CPU operating above 8MHz, one wait state is required to meet this parameter.
3. These daisy chain parameters include contributions from the PIO, SIO and CTC cells, and vary slightly depending on how they are ordered by the KIO Command Register.
4. Counter mode only; when using a cycle time less than 3 TcC, parameter #37 must be met.
5. Units are TcC.
6. If the CPU is a Z80 CPU and if it is required to have multiple Z80 peripherals in the system, then the time period between $\overline{M1}$ to $\overline{IORQ}$ must be extended.
7. Any open-drain output must add a Register-Capacitor (RC) time constant to the specification value.

Figure 42 offers a visual representation of the daisy chain sequence; Table 6 lists 8MHz, 10MHz and 12MHz daisy chain parameters.

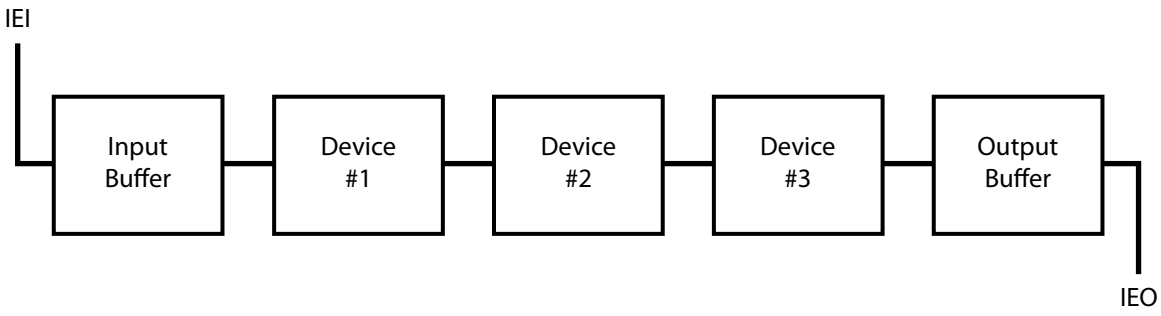


Figure 42. Internal Daisy Chain Configuration

Table 6. Daisy Chain Parameters

No.	Symbol	Parameter	8MHz		10MHz		12.5MHz		Unit
			Min	Max	Min	Max	Min	Max	
18[1]	TdM1(IEO)	(PIO at #1)		160		150		125	ns
		(CTC at #1)		180		150		125	ns
		(SIO at #1)		230		200		160	ns
19[2]	TsIEI (IO)	(PIO at #3)	170		140		115		ns
		(CTC at #3)	170		160		135		ns
		(SIO at #3)	180		160		130		ns
20[3]	TdIEI(IEOf)			160		150		125	ns
21[4]	TdIEI(IEOr)			160		150		125	ns

Notes: To calculate Z80 KIO daisy-chain timing, use the Z80 PIO, CTC, and SIO with I/O buffers on the chain. Consider the following calculation formulas:

1. Parameter 18: M1 falling to IEO delay TdM1(IEO) = TdM1(IEO)#1 + TdIEI(IEO)#2 + TdIEI(IEO)#3 + Output Buffer Delay), in which TdIEI(IEO) refers to the worst-case number value between TdIEI(IEOr) and TdIEI(IEOf).
2. Parameter 19: IEI to IORQ falling setup time TsIEI(IO) = TdIEI(IEO)#1 + TdIEI(IEO)#2 + TdIEI(IEO)#3 + Input Buffer Delay), in which TdIEI(IEO) refers to the worst-case number value between TdIEI(IEOr) and TdIEI(IEOf).
3. Parameter 20: IEI falling delay = TdIEI(IEOf) = TdIEI(IEOf)PIO + TdIEI(IEOf)CTC + TdIEI(IEOf)SIO + (Input buffer Delay) + (Output Buffer Delay).
4. Parameter 21: IEI rising to IEO rising delay (after ED decode) – TdIEI(IEOr) = TdIEI(IEOr)PIO + TdIEI(IEOr)CTC + TdIEI(IEOr)SIO + ((Input buffer Delay) + (Output Buffer Delay).
5. In notes 1–4, TdIEI(IEO) refers to the worst-case number value between the parameters TdIEI(IEOr) and TdIEI(IEOf).

The data that support the calculations in Table 6 are tabulated in Table 7.

Table 7. Daisy Chain Calculation Data*

	8MHz		10MHz		12.5MHz		Unit
	Min	Max	Min	Max	Min	Max	
Input Buffer Delay	10		10		10		ns
Output Buffer Delay	10		10		10		ns
8MHz	**PIO Part**		**CTC Part**		**SIO Part**		ns
TdM1(IEO)	60		80		120		ns
TsIEI(IO)	70		70		70		ns
TdIEI(IEOf)		50		50		40	ns
TdIEI(IEOr)		50		50		40	ns

Note: *When using an interrupt from only a portion of the Z84C90 KIO, the numbers in this table are smaller than the actual values. For example, in Figure 42 on page 42, if Device #1 is PIO, Device #2 is CTC, and Device #3 is SIO, then at 12.5MHz, Parameter #18 in Table 6, TdM1(IEO), is PIO TdM1(IEO) + CTC TdIEI(IEO) + SIO (TdIEI(IEO) + Output Buffer. = 50ns + 40ns + 25ns + 10ns = 125ns.

Table 7. Daisy Chain Calculation Data* (Continued)

	8MHz		10MHz		12.5MHz		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
10MHz	**PIO Part**		**CTC Part**		**SIO Part**		ns
TdM1(IEO)	60		60		90		ns
TsIEI(IO)	50		70		50		ns
TdIEI(IEOf)		50		50		30	ns
TdIEI(IEOr)		50		50		30	ns
12.5MHz	**PIO Part**		**CTC Part**		**SIO Part**		ns
TdM1(IEO)	50		50		70		ns
TsIEI(IO)	40		60		40		
TdIEI(IEOf)		40		40		25	
TdIEI(IEOr)		40		40		25	

Note: *When using an interrupt from only a portion of the Z84C90 KIO, the numbers in this table are smaller than the actual values. For example, in Figure 42 on page 42, if Device #1 is PIO, Device #2 is CTC, and Device #3 is SIO, then at 12.5MHz, Parameter #18 in Table 6, TdM1(IEO), is PIO TdM1(IEO) + CTC TdIEI(IEO) + SIO (TdIEI(IEO) + Output Buffer. = 50ns + 40ns + 25ns + 10ns = 125ns.

Packaging

Zilog's Z84C90 KIO is available in the following packages:

- 84-pin Plastic Chip Carrier (PLCC)
- 100-Pin Quad Flat Pack (LQFP)

Current diagrams for each of these packages are published in Zilog's Packaging Product Specification (PS0072), which is available free for download from the Zilog website.

Ordering Information

Order your Z84C90 KIO Serial/Parallel Counter/Timer products from Zilog using the part numbers shown in Table 8. For more information about ordering, please consult your local Zilog sales office. The Sales Location page on the Zilog website lists all regional offices.

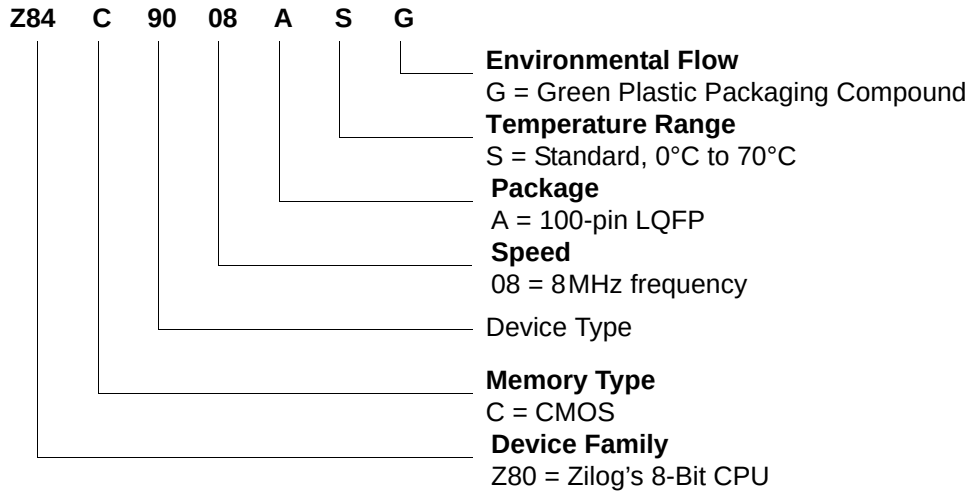
Table 8. Z84C90 KIO Ordering Matrix

Part Number	Frequency	Package	Temperature Range
Z84C9008ASG	8MHz	100-Pin LQFP	0°C to 70°C
Z84C9008VEG	8MHz	84-Pin PLCC	–40°C to +105°C
Z84C9008VSG	8MHz	84-Pin PLCC	0°C to 70°C
Z84C9010ASG	10MHz	100-Pin LQFP	0°C to 70°C
Z84C9010VEG	10MHz	84-Pin PLCC	–40°C to +105°C
Z84C9010VSG	10MHz	84-Pin PLCC	0°C to 70°C
Z84C9012VSG	12.5MHz	84-Pin PLCC	0°C to 70°C

Part Number Suffix Designations

Zilog part numbers consist of a number of components, as indicated in the following example.

Example. Part number Z84C9008ASG is an 8-bit Z80-powered MCU operating at an 8MHz frequency in a 100-pin LQFP package, operating within a 0ºC to +70ºC temperature range and built using lead-free solder.



Precautions & Limitations

The following issues describe the possible limitations and resulting workarounds when working with Revision A of the Z84C90 KIO Peripheral.

Daisy-Chain

If the KIO has an interrupt pending during an Interrupt Acknowledge cycle, the KIO misses the status of the IE1 pin. As a result, vector contention is produced if there is a higher interrupting device. However, operation is as expected if only one device is in the system.

Workaround: There is no problem if the application has only one peripheral in the daisy chain. For two or more peripherals in the system, a *hardware workaround circuit* is required. Please contact your local Zilog representative to obtain more information.

Reset

KIO requires the $\overline{M1}$ signal to exit from a Reset state. If the $\overline{M1}$ signal is not received, the KIO cannot be programmed. This problem does not exist for users of the Z80 CPU.

Workaround: If the CPU is other than a Z80 CPU, an $\overline{M1}$ signal is required to exit RESET status. Otherwise, the KIO cannot be programmed.

Port C

When Port C is used as a parallel I/O (and not as modem signals for an SIO) and there is a status change on PC1 or PC6, the status of $\overline{SYNCA}$ or $\overline{SYNCB}$ (SIO cell) also changes.

Workaround: Before using Port C as a parallel port, set the SIO modem signal mode back to Port C. This procedure avoids the problem.

Interrupt Acknowledge Cycle

The KIO modifies the contents of the KIO Control Register (specifically, the KIO modifies the daisy-chain configuration) if the $\overline{CE}$ pin is active during the Interrupt Acknowledge cycle (assuming other conditions are satisfied).

This problem can occur under the following narrowly-defined conditions:

- The $\overline{CE}$ signal is active throughout the Interrupt Acknowledge cycle
- The address on the bus, A3–A0, is `110b`
- Bit D3 is 1

- At the end of the Interrupt Acknowledge cycle, M1 goes inactive prior to the $\overline{\text{IORQ}}$ signal
- During the time period in which $\overline{\text{CE}}$ is active, $\overline{\text{IORQ}}$ is active, and $\overline{\text{M1}}$ returns to the inactive state, all of which occur during the rising edge of the clock.

This problem does not exist with the Z80 CPU; however, other CPUs could be affected. One of the possible workarounds is to add the $\overline{\textit{M1}}$ *not active* condition to generate a $\overline{\text{CE}}$ signal.

Customer Support

To share comments, get your technical questions answered, or report issues you may be experiencing with our products, please visit Zilog's Technical Support page at http://support.zilog.com.

To learn more about this product, find additional documentation, or to discover other facets about Zilog product offerings, please visit the Zilog Knowledge Base at http://zilog.com/kb or consider participating in the Zilog Forum at http://zilog.com/forum.

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