

**i5141-TG**

**SD/MMC Memory Card Controller**

**Datasheet**

**Version 1.1**

**iCreate Technologies Corporation**

**2006/9/28**

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## Revision History

Date	Revision	Description
2006/9/25	1.0	Initial release version
2006/9/28	1.1	Update new package outline

## 1. Introduction

### 1.1. General description

i5141-TG is a high performance flash memory controller for SD/MMC interface flash memory cards. This chip is based on iCreate 3rd-generation flash engine to achieve high data transfer rate. The enhanced designs include high performance CPU, multi-bank flash access, 8/16-bit flash interface, and Reed-Solomon based ECC capability. Voltage-Regulator, Power-on-reset and RC oscillator are integrated to reduce BOM cost and PCB area. Typical applications of i5141-TG are SD, miniSD, MMC and RS-MMC memory card.

### 1.2. Features

- ◆ Compliant to SD1.1, MMC4.1 standards
- ◆ 1/4/8-bit host data transfer
- ◆ SD/MMC Clock frequency 0 ~ 52 MHz
- ◆ Integrated power-on-reset and RC oscillator
- ◆ On-the-fly ECC (4 Byte per 528 Byte)
- ◆ Wear-leveling mechanism
- ◆ Support large block NAND type flash
- ◆ Support small block NAND type flash
- ◆ Support AG-AND type flash
- ◆ 4 flash chips enable
- ◆ Auto-suspend to conserve energy

### 1.3. Block diagram

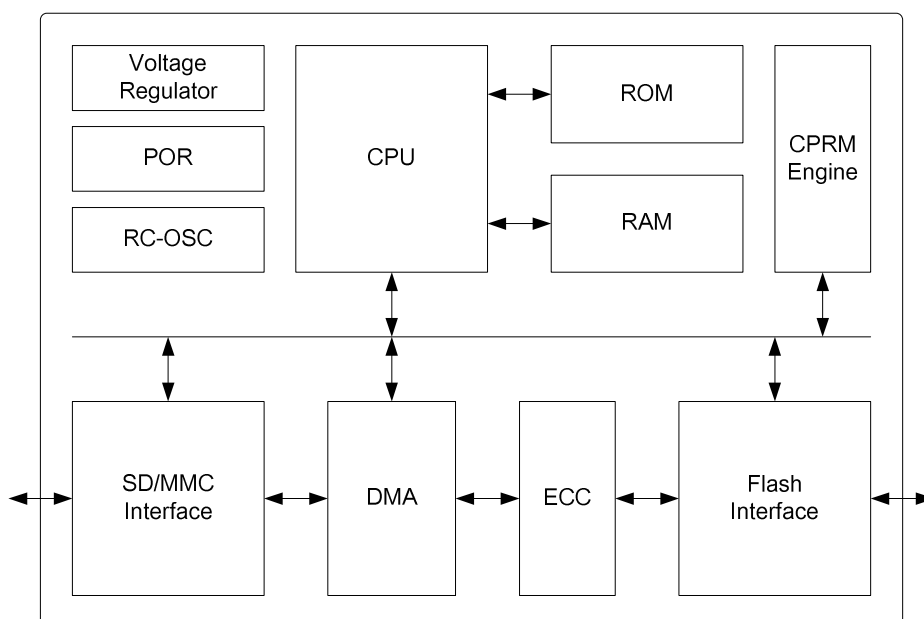


Figure 1. Block diagram

## 2. Pin Diagram and Description

### 2.1. Pin Diagram

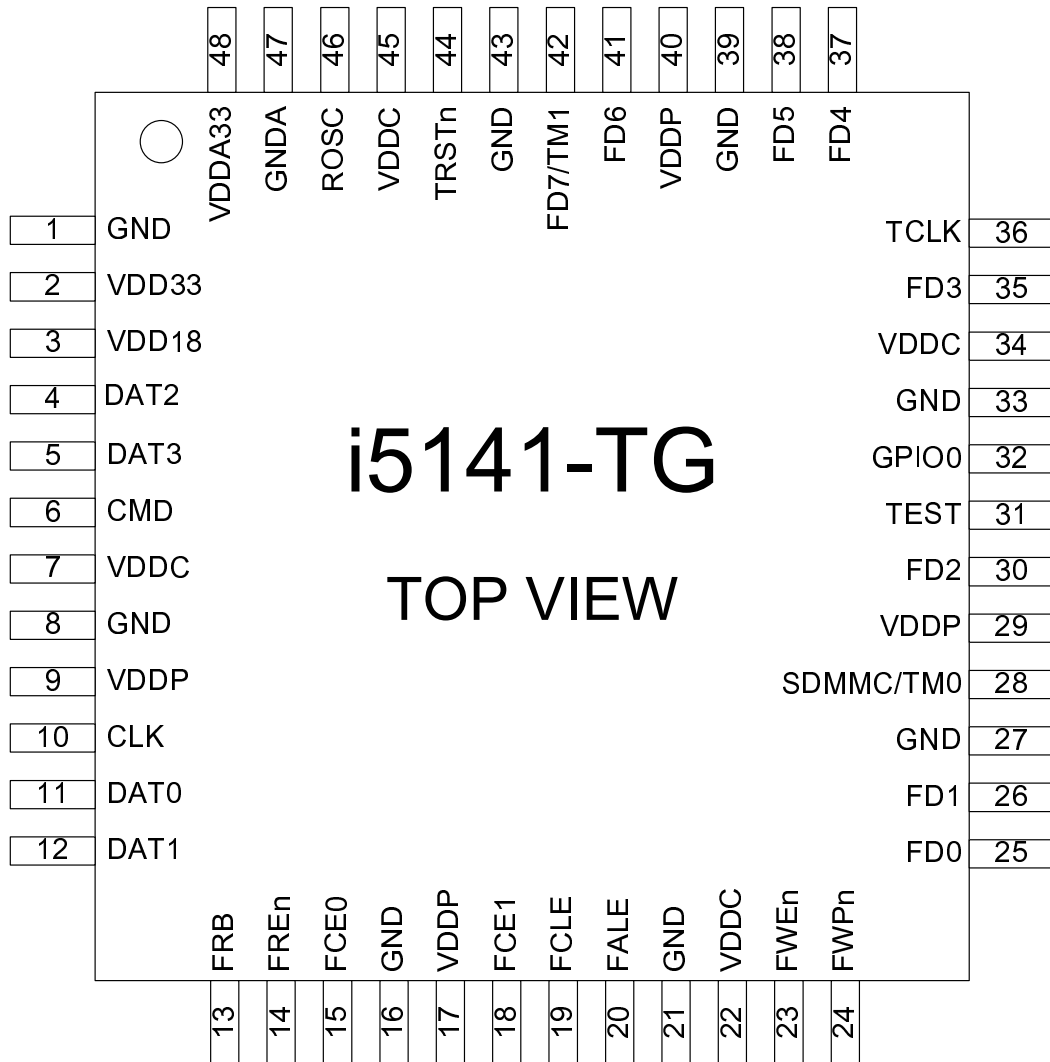


Figure 2. Pin Diagram

## 2.2. Pin Description

Pin Name	Type <sup>*1</sup>	Description
VDD33	Power	Internal regulator 3.3V input pin.
VDD18	Power	Internal regulator 1.8V output pin.
VDDC	Power	1.8V power supply for core.
VDDP	Power	3.3V power supply for I/O.
GND	Power	Power supply ground.
VDDA33	Power	3.3V power supply for analog block.
GNDA	Power	Power supply ground for analog block.
ROSC	Analog	Connect 3.9K Ohm resistor to VDD18 for internal 50MHz clock generator.
DAT0~3	IO/ST/PUC	SD/MMC Data Bus
CMD	IO/ST/PUC	SD/MMC Command/Response signal
CLK	I/ST	SD/MMC Clock input.
FCE0~1	IO/ST/PUC	Flash chip enable signal.
FRBn	IO/ST/PUC	Flash Ready/Busy signal
FCLE	IO/ST/PUC	Flash command latch enable
FALE	IO/ST/PUC	Flash address latch enable.
FREn	IO/ST/PUC	Flash read enable.
FWEn	IO/ST/PUC	Flash write enable.
FWPn	IO/ST/PUC	Flash write protect.
FD0~FD7	IO/ST/PUC	Flash data bus.
SDMMC	I	SD/MMC Selection. MMC Mode when Tie-High and SD Mode when Tie-Low.
TEST	I/PD	Test mode enable. This pin must floating or tie-low when normal operation.
TCLK	I/ST	Clock for test mode.
TRSTn	I/PD	Reset for test mode.
GPIO0	IO/ST/PUC	General purpose I/O pin.

\*1: I/O Type I: Input pin. IO: Bidirectional pin. ST: pin with S Trigger. Analog: Analog pin

PD: pin with pull-down resistor. PUC: pin with controllable pull-up resistor. Power: Power Pin

Table 1. Pin Description

### 3. Internal Regulator, Power-ON Reset and RC oscillator

#### 3.1. Regulator

The internal voltage regulator input 3.3V and output 1.8V used for core power supply as shown in Figure 3.

#### 3.2. Power-on-reset and brown-out-reset

The internal reset control unit has power-on-reset (POR). To use internal POR, only provide 3.3V to VDDA33 and GNDA connected to ground as shown in Figure 3.

#### 3.3. RC oscillator

An integrated RC oscillator can be used to reduce BOM cost. ROSC must be connected to 1.8V through a resistor, as shown in Figure 3.

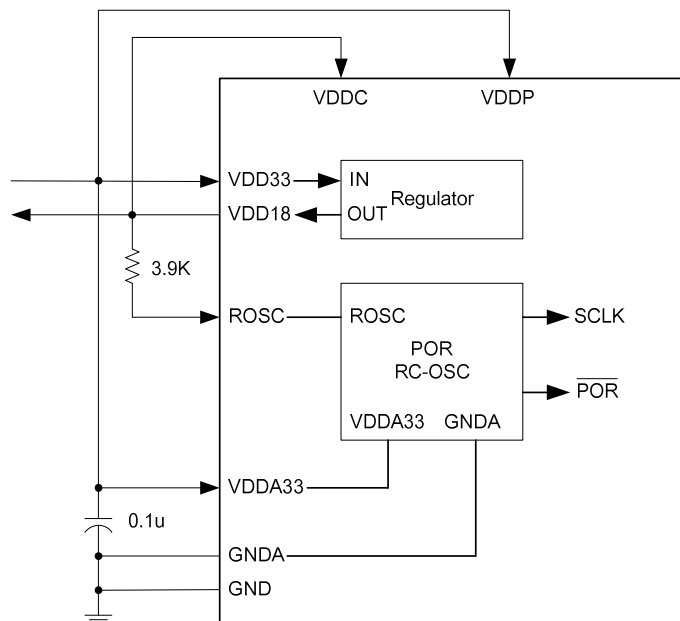


Figure 3. Pin connection to use internal Regulator, Power-ON Reset and Oscillator

## 4. Electrical specifications

### 4.1. Absolute maximum ratings

Symbol	Description	Value	Unit	Notes
$V_{DD}$	I/O Power Supply Voltage	- 0.3 to +3.6	V	VDDP, VDD33, VDD33A
$V_{DDC}$	Core Power Supply Voltage	- 0.3 to +1.98	V	VDDC
$V_{IN}, V_{OUT}$	All input/output voltages	- 0.3 to VDD + 0.3	V	
$T_{stg}$	Storage temperature range	- 45 to +85	°C	

Table 2. Absolute maximum ratings

### 4.2. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{DD}$	I/O Power Supply Voltage	2.7	3.3	3.6	V
$V_{DDC}$	Core Power Supply Voltage	1.62	1.8	1.98	V
$T_{OPR}$	Operating temperature	0		70	°C

Table 3. Recommended operation conditions

### 4.3. Power-on-reset characteristics

Symbol	Parameter	Typ.	Unit
$V_T(POR)$	Threshold voltage of power-on-reset	2.6	V

Table 4. Power-on-reset characteristics



## 4.4. Bus Operating Conditions

### 4.4.1. General

Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines		-0.5	3.6	V	
<b>All inputs</b>					
Input Leakages Current		-10	10	$\mu\text{A}$	
<b>All outputs</b>					
Output Leakages Current		-10	10	$\mu\text{A}$	

Table 5. Bus Operating Conditions – General

### 4.4.2. Bus Signal Level

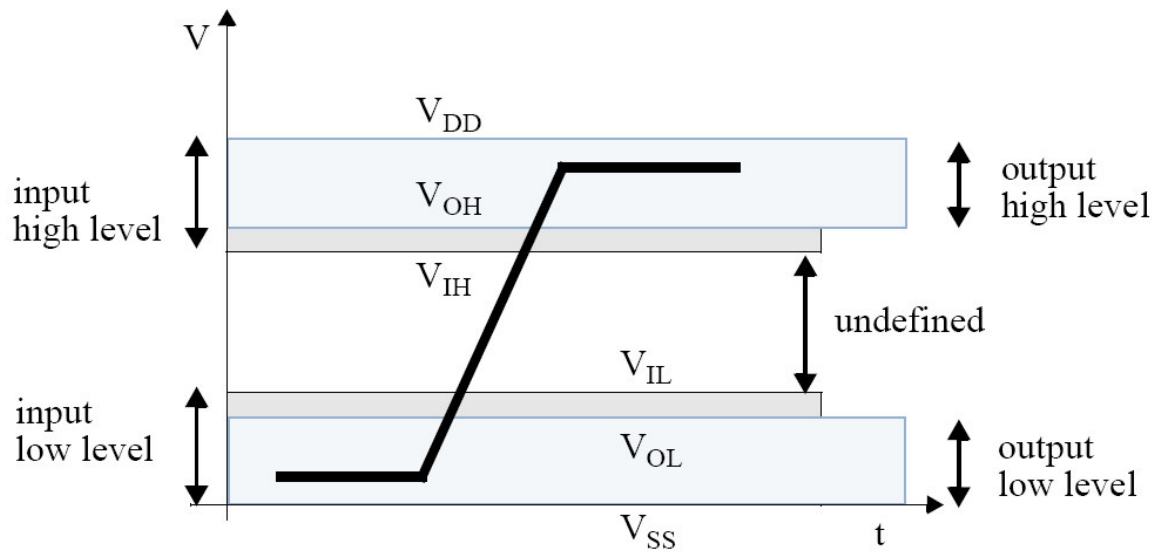


Figure 4. Bus Signal Level

## 4.5. SD Mode Bus Operating Conditions

### 4.5.1. Deault

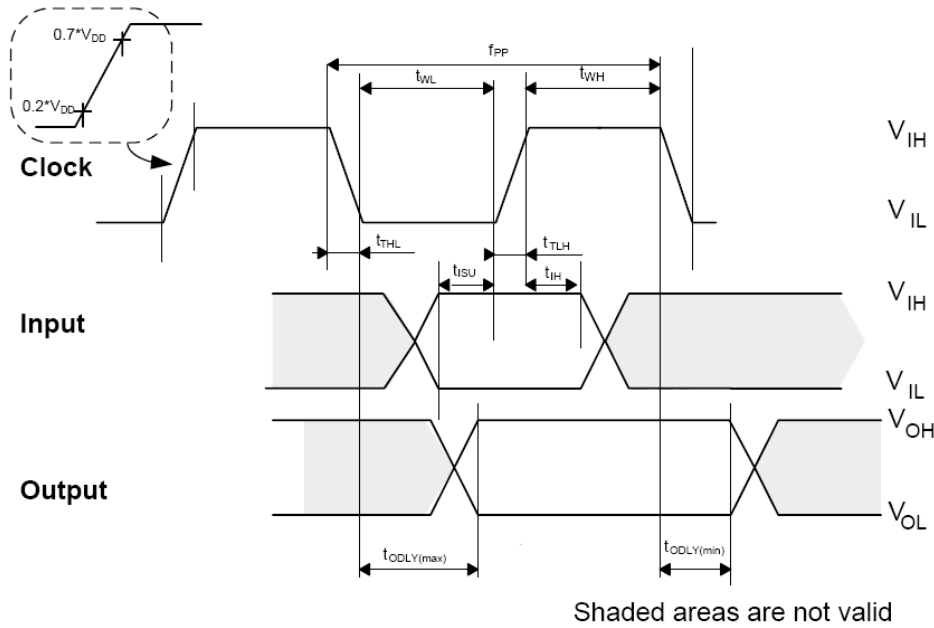


Figure 5. SD Mode: Timing Diagram Data Input/Output Referenced to Clock (Default)

Parameter	Symbol	Min.	Max.	Unit	Remark
<b>Clock CLK</b> (All values are referred to $\min(V_{IH})$ and $\max(V_{IL})$ ,					
Clock frequency Data Transfer Mode	$f_{PP}$	0	25	MHz	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock frequency Identification Mode	$f_{OD}$	$0_{(1)}/100$	400	KHz	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock low time	$t_{WL}$	10		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock high time	$t_{WH}$	10		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock rise time	$t_{TLH}$		10	ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock fall time	$t_{THL}$		10	ns	$C_{CARD} \leq 10\text{pF}$ (1 card)

Parameter	Symbol	Min.	Max.	Unit	Remark
<b>Input CMD, DAT (referenced to CLK)</b>					
Input set-up time	$t_{ISU}$	5		ns	$C_{CARD} \leq 10pF$ (1 card)
Input hold time	$t_{IH}$	5		ns	$C_{CARD} \leq 10pF$ (1 card)
<b>Outputs CMD, DAT (referenced to CLK)</b>					
Output Delay time during Data Transfer Mode	$t_{ODLY}$	0	14	ns	$C_L \leq 40pF$ (1 card)
Output Delay time during Identification Mode	$t_{ODLY}$	0	50	ns	$C_L \leq 40pF$ (1 card)

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

Table 6. SD Mode: Bus Timing – Parameters Value (Default)

## 4.5.2. High Speed

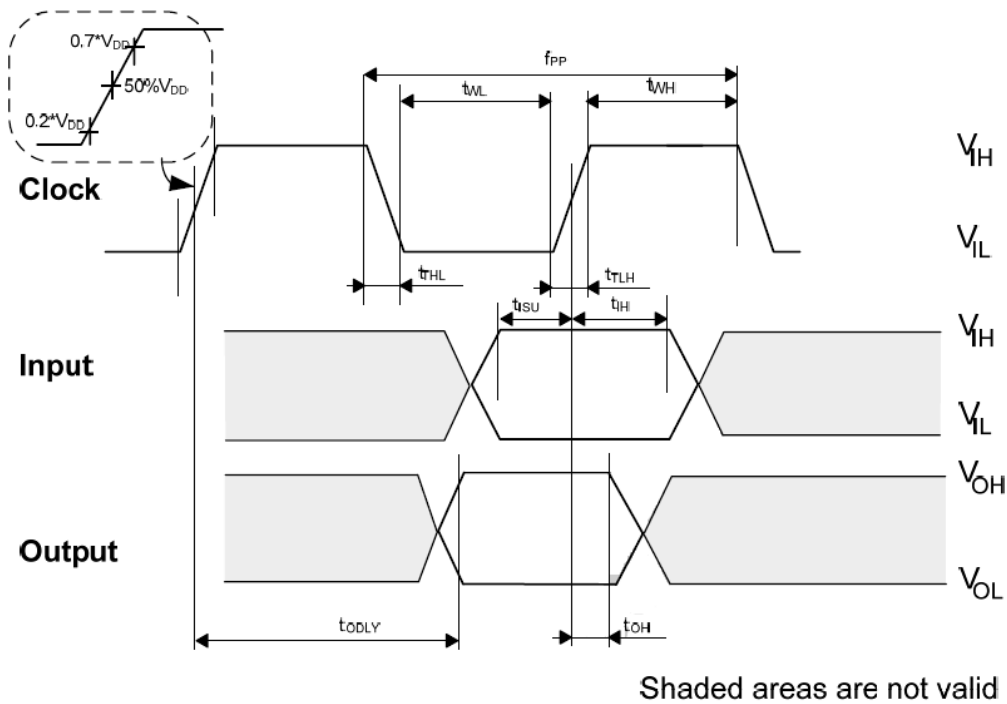


Figure 6. SD Mode: Timing Diagram Data Input/Output Referenced to Clock (High-Speed)

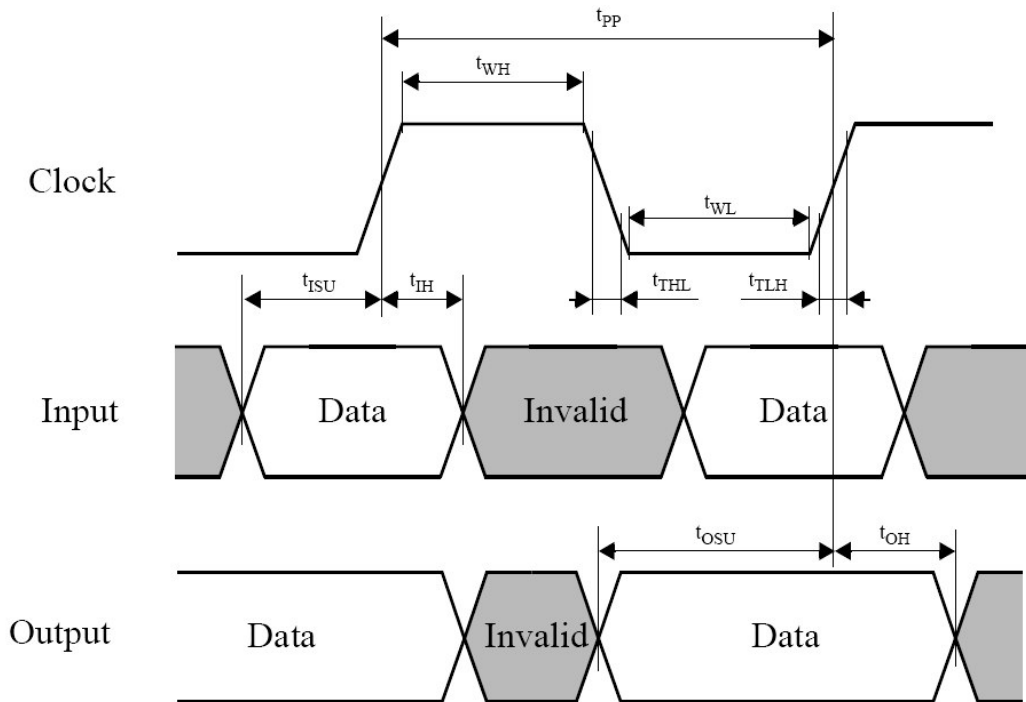
Parameter	Symbol	Min.	Max.	Unit	Remark
<b>Clock CLK</b> (All values are referred to $\min(V_{IH})$ and $\max(V_{IL})$ ,					
Clock frequency Data Transfer Mode	$f_{PP}$	0	50	MHz	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock low time	$t_{WL}$	7		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock high time	$t_{WH}$	7		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock rise time	$t_{TLH}$		3	ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock fall time	$t_{THL}$		3	ns	$C_{CARD} \leq 10\text{pF}$ (1 card)

Parameter	Symbol	Min.	Max.	Unit	Remark
<b>Input CMD, DAT (referenced to CLK)</b>					
Input set-up time	$t_{ISU}$	6		ns	$C_{CARD} \leq 10pF$ (1 card)
Input hold time	$t_{IH}$	2		ns	$C_{CARD} \leq 10pF$ (1 card)
<b>Outputs CMD, DAT (referenced to CLK)</b>					
Output Delay time during Data Transfer Mode	$t_{ODLY}$		14	ns	$C_L \leq 40pF$ (1 card)
Output Hold time	$t_{OH}$	2.5		ns	$C_L \geq 15pF$ (1 card)
Total System capacitance for each line	$C_L$		40	pF	1 card

(1) In order to satisfy severe timing, host shall drive only one card.

Table 7. SD Mode: Bus Timing – Parameters Values (High-Speed)

## 4.6. MMC Mode Bus Operating Conditions



Data must always be sampled on the rising edge of the clock.

Figure 7. MMC Mode: Timing Diagram - Data Input/Output

### 4.6.1. Card Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
<b>Clock CLK<sup>1</sup></b>					
Clock frequency Data Transfer Mode (PP) <sup>2</sup>	$f_{PP}$	0	26/52	MHz	$C_L \leq 30$ pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	$f_{OD}$	0	400	kHz	Tolerance: +20KHz
Clock low time	$t_{WL}$	6.5		ns	$C_L \leq 30$ pF
Clock rise time <sup>3</sup>	$t_{TLH}$		3	ns	$C_L \leq 30$ pF
Clock fall time	$t_{THL}$		3	ns	$C_L \leq 30$ pF
<b>Inputs CMD, DAT (referenced to CLK)</b>					
Input set-up time	$t_{ISU}$	3		ns	$C_L \leq 30$ pF
Input hold time	$t_{IH}$	3		ns	$C_L \leq 30$ pF
<b>Outputs CMD, DAT (referenced to CLK)</b>					
Output set-up time	$t_{OSU}$	5		ns	$C_L \leq 30$ pF
Output hold time	$t_{OH}$	5		ns	$C_L \leq 30$ pF

Parameter	Symbol	Min	Max.	Unit	Remark
Signal rise time <sup>4</sup>	$t_{rise}$		3	ns	$C_L \leq 30$ pF
Signal fall time	$t_{fall}$		3	ns	$C_L \leq 30$ pF

Table 8. MMC Mode: High-Speed Card Interface Timing

- 1) All timing values are measured relative to 50% of voltage level
- 2) A MultiMediaCard shall support the full frequency range from 0-26Mhz, or 0-52MHz
- 3) Rise and fall times are measured from 10%-90% of voltage level
- 4) Rise and fall times are measured from 10%-90% of voltage level

Parameter	Symbol	Min	Max.	Unit	Remark
<b>Clock CLK<sup>1</sup></b>					
Clock frequency Data Transfer Mode (PP)	$f_{PP}$	0	20	MHz	$C_L \leq 30$ pF
Clock frequency Identification Mode (OD)	$f_{OD}$	0	400	kHz	
Clock low time	$t_{WL}$	10		ns	$C_L \leq 30$ pF
Clock rise time <sup>2</sup>	$t_{TLH}$		10	ns	$C_L \leq 30$ pF
Clock fall time	$t_{THL}$		10	ns	$C_L \leq 30$ pF
<b>Inputs CMD, DAT (referenced to CLK)</b>					
Input set-up time	$t_{ISU}$	3		ns	$C_L \leq 30$ pF
Input hold time	$t_{IH}$	3		ns	$C_L \leq 30$ pF
<b>Outputs CMD, DAT (referenced to CLK)</b>					
Output set-up time	$t_{OSU}$	13.1		ns	$C_L \leq 30$ pF
Output hold time	$t_{OH}$	9.7		ns	$C_L \leq 30$ pF

- 1) All timing values are measured relative to 50% of voltage level
- 2) Clock rise and fall times are measured from VIL to VIH of voltage level

Table 9. MMC Mode: Backwards Compatible Card Interface Timing

## 4.7. Flash Interface Command Write AC characteristics

Symbol	Parameter	Min.	Max.	Unit
tCLS	FCLE setup time	0		ns
tCLH	FCLE hold time	10		ns
tCS	FCE# setup time	0		ns
tCH	FCE# hold time	10		ns
tWP	FWE# pulse width	25		ns
tALS	FALE setup time	0		ns
tALH	FALE hold time	10		ns
tDS	Data Setup time	20		ns
tDH	Data hold time	10		ns

Table 10. Timing Parameters: Flash Interface Command Write

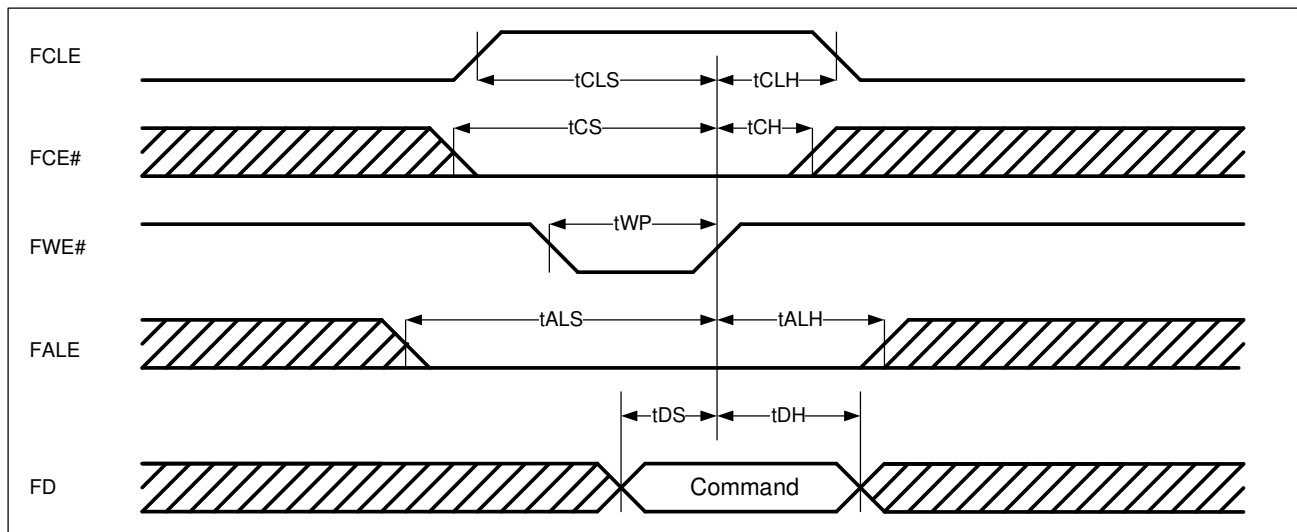


Figure 8. Timing Diagram: Flash Interface Command Write



## 4.8. Flash Interface Address Write AC characteristics

Symbol	Parameter	Min.	Max.	Unit
tCLS	FCLE setup time	0		ns
tCS	FCE# setup time	0		ns
tCH	FCE# hold time	10		ns
tWP	FWE# pulse width	25		ns
tWH	FWE# high hold time	15		ns
tALS	FALE setup time	0		ns
tALH	FALE hold time	10		ns
tDS	Data Setup time	20		ns
tDH	Data hold time	10		ns
tWC	Flash write cycle time	50		

Table 11. Timing Parameters: Flash Interface Address Write

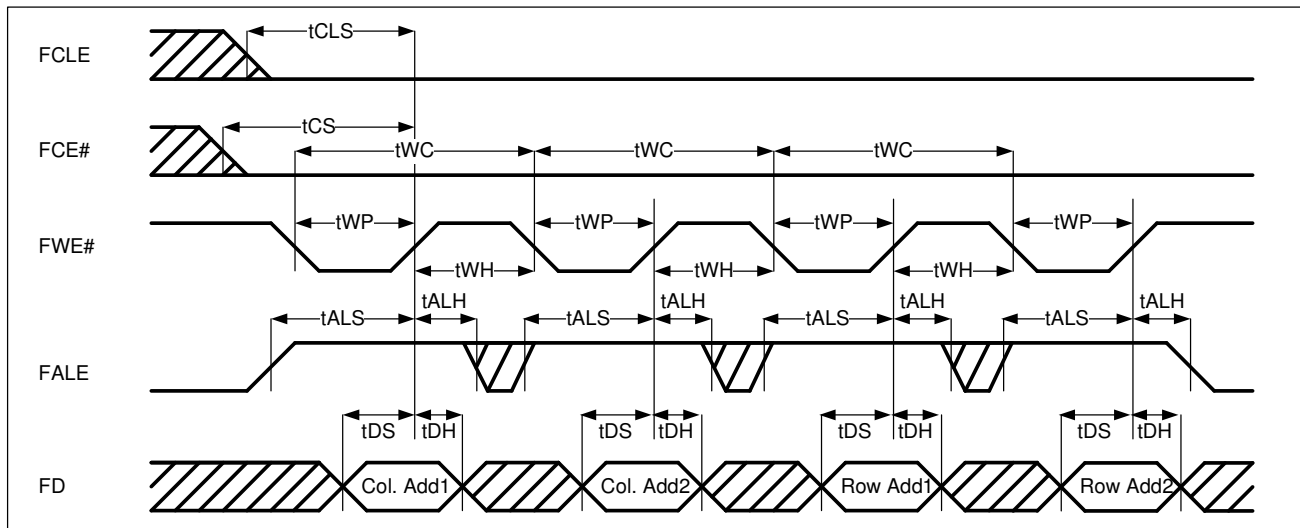


Figure 9. Timing Diagram: Flash Interface Address Write

## 4.9. Flash Interface Data Write AC characteristics

Symbol	Parameter	Min.	Max.	Unit
tCLH	FCLE hold time	10		ns
tCH	FCE# hold time	10		ns
tWP	FWE# pulse width	25		ns
tWH	FWE# high hold time	15		ns
tALS	FALE setup time	0		ns
tDS	Data setup time	20		ns
tDH	Data hold time	10		ns
tWC	Flash write cycle time	50		ns

Table 12. Timing Parameters: Flash Interface Data Write

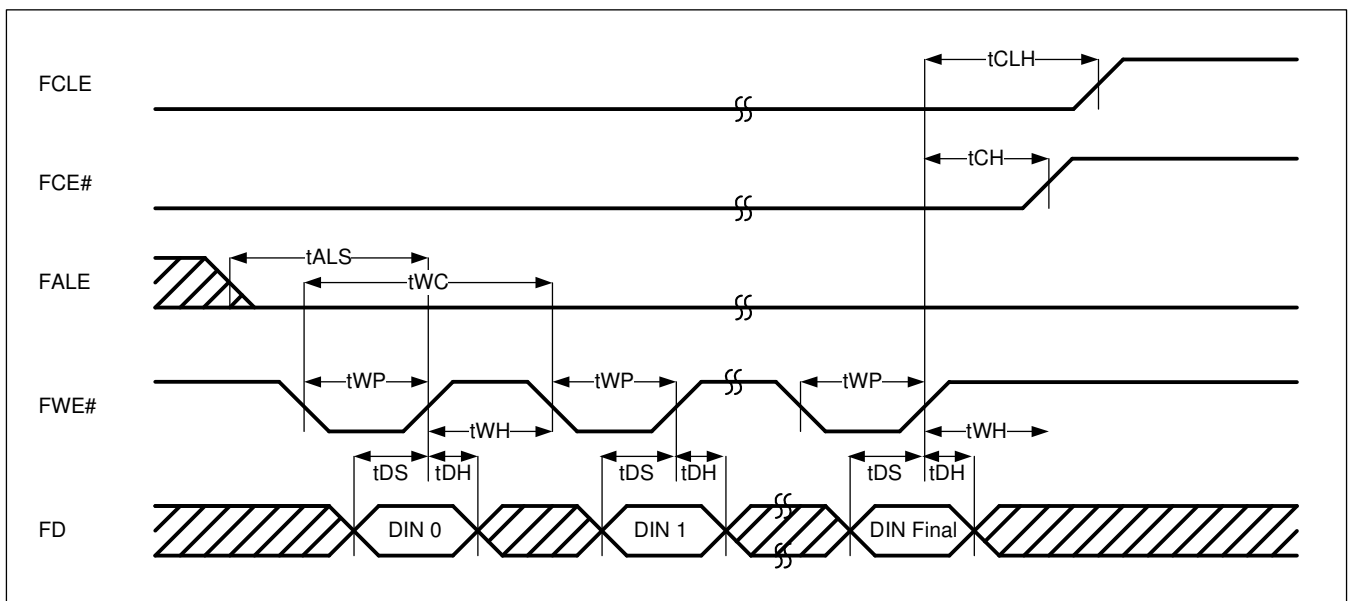


Figure 10. Timing Diagram: Flash Interface Data Write

### 4.10. Flash Interface Data Read AC characteristics

Symbol	Parameter	Min.	Max.	Unit
tCLR	FCLE to FRE# delay	10		ns
tAR	ALE to FRE# delay	10		ns
tRR	Ready to FRE# low	20		ns
tRC	Read cycle time	30		ns

Table 13. Timing Parameters: Flash Interface Data Read

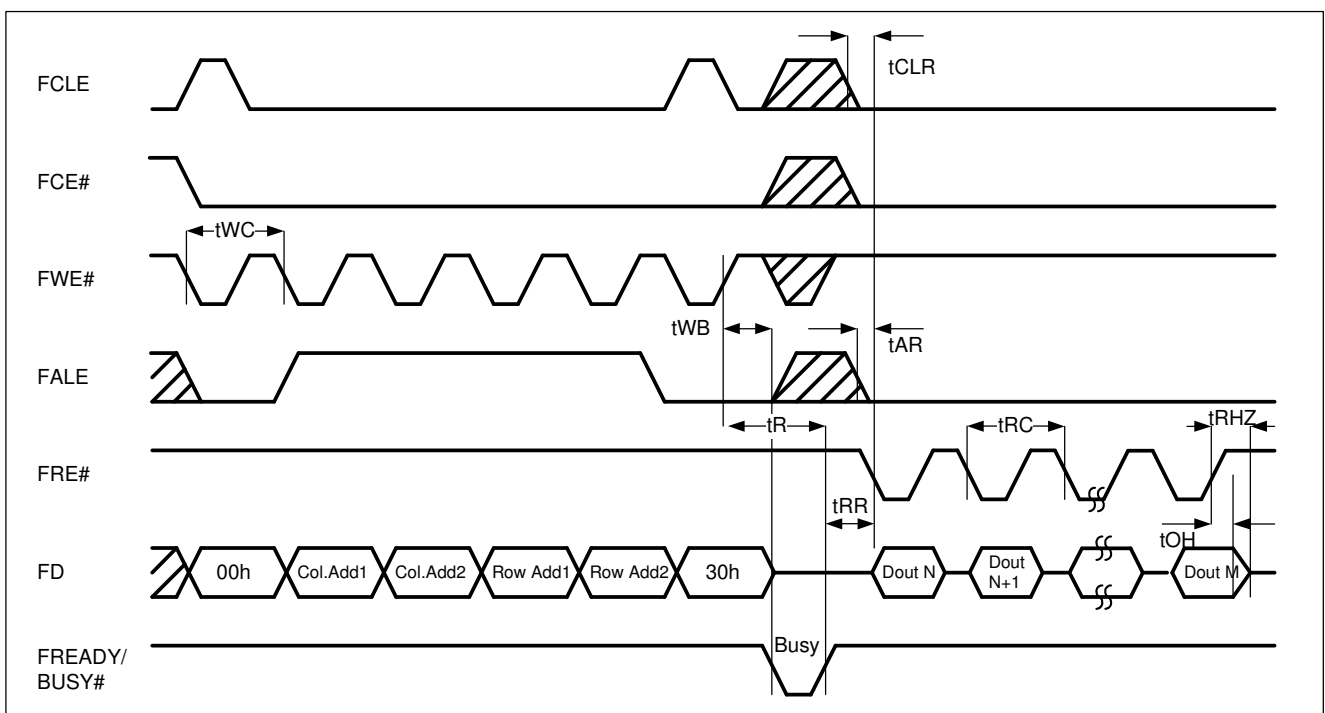


Figure 11. Timing Diagram: Flash Interface Data Read

## 5. Package Dimensions

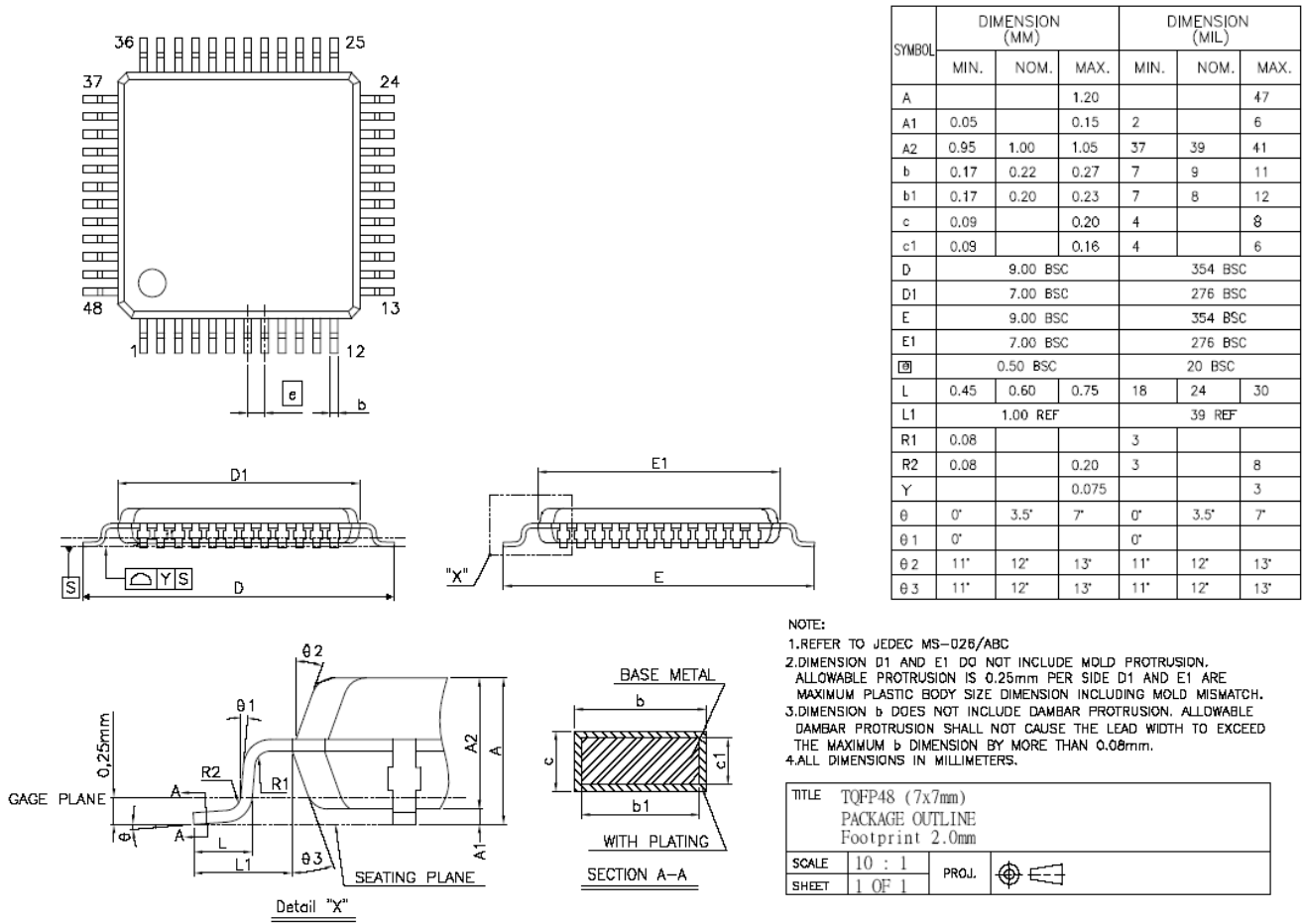


Figure 12. i5141-TG Package Diagram