

Features

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
 - High-performance 32-bit RISC Architecture
 - High-density 16-bit Instruction Set
 - Leader in MIPS/Watt
 - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
- Internal High-speed Flash
 - 512 Kbytes (AT91SAM7X512) Organized in Two Banks of 1024 Pages of 256 Bytes (Dual Plane)
 - 256 Kbytes (AT91SAM7X256) Organized in 1024 Pages of 256 Bytes (Single Plane)
 - 128 Kbytes (AT91SAM7X128) Organized in 512 Pages of 256 Bytes (Single Plane)
 - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
 - Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
 - Page Programming Time: 6 ms, Including Page Auto-erase, Full Erase Time: 15 ms
 - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
 - Fast Flash Programming Interface for High Volume Production
- Internal High-speed SRAM, Single-cycle Access at Maximum Speed
 - 128 Kbytes (AT91SAM7X512)
 - 64 Kbytes (AT91SAM7X256)
 - 32 Kbytes (AT91SAM7X128)
- Memory Controller (MC)
 - Embedded Flash Controller, Abort Status and Misalignment Detection
- Reset Controller (RSTC)
 - Based on Power-on Reset Cells and Low-power Factory-calibrated Brownout Detector
 - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
 - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and one PLL
- Power Management Controller (PMC)
 - Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
 - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
 - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
 - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
 - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
 - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)
 - 12-bit key-protected Programmable Counter
 - Provides Reset or Interrupt Signals to the System
 - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode



Product Description

AT91SAM7X512
AT91SAM7X256
AT91SAM7X128

Preliminary Summary

NOTE: This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

6120ES-ATARM-08-Oct-07



- **Real-time Timer (RTT)**
 - 32-bit Free-running Counter with Alarm
 - Runs Off the Internal RC Oscillator
- **Two Parallel Input/Output Controllers (PIO)**
 - Sixty-two Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
 - Input Change Interrupt Capability on Each I/O Line
 - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- **Thirteen Peripheral DMA Controller (PDC) Channels**
- **One USB 2.0 Full Speed (12 Mbits per second) Device Port**
 - On-chip Transceiver, 1352-byte Configurable Integrated FIFOs
- **One Ethernet MAC 10/100 base-T**
 - Media Independent Interface (MII) or Reduced Media Independent Interface (RMII)
 - Integrated 28-byte FIFOs and Dedicated DMA Channels for Transmit and Receive
- **One Part 2.0A and Part 2.0B Compliant CAN Controller**
 - Eight Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- **One Synchronous Serial Controller (SSC)**
 - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
 - I²S Analog Interface Support, Time Division Multiplex Support
 - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- **Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)**
 - Individual Baud Rate Generator, IrDA[®] Infrared Modulation/Demodulation
 - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
 - Full Modem Line Support on USART1
- **Two Master/Slave Serial Peripheral Interfaces (SPI)**
 - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- **One Three-channel 16-bit Timer/Counter (TC)**
 - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
 - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- **One Four-channel 16-bit Power Width Modulation Controller (PWMC)**
- **One Two-wire Interface (TWI)**
 - Master Mode Support Only, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported
- **One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os**
- **SAM-BA[™] Boot Assistance**
 - Default Boot program
 - Interface with SAM-BA Graphic User Interface
- **IEEE[®] 1149.1 JTAG Boundary Scan on All Digital Pins**
- **5V-tolerant I/Os, Including Four High-current Drive I/O lines, Up to 16 mA Each**
- **Power Supplies**
 - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
 - 3.3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
 - 1.8V VDDCORE Core Power Supply with Brownout Detector
- **Fully Static Operation: Up to 55 MHz at 1.65V and 85°C Worst Case Conditions**
- **Available in 100-lead LQFP Green and 100-ball TFBGA Green Packages**

1. Description

Atmel's AT91SAM7X512/256/128 is a member of a series of highly integrated Flash microcontrollers based on the 32-bit ARM RISC processor. It features 512/256/128 Kbyte high-speed Flash and 128/64/32 Kbyte SRAM, a large set of peripherals, including an 802.3 Ethernet MAC and a CAN controller. A complete set of system functions minimizes the number of external components.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserve its confidentiality.

The AT91SAM7X512/256/128 system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

By combining the ARM7TDMI processor with on-chip Flash and SRAM, and a wide range of peripheral functions, including USART, SPI, CAN Controller, Ethernet MAC, Timer Counter, RTT and Analog-to-Digital Converters on a monolithic chip, the AT91SAM7X512/256/128 is a powerful device that provides a flexible, cost-effective solution to many embedded control applications requiring communication over, for example, Ethernet, CAN wired and Zigbee™ wireless networks.

1.1 Configuration Summary of the AT91SAM7X512/256/128

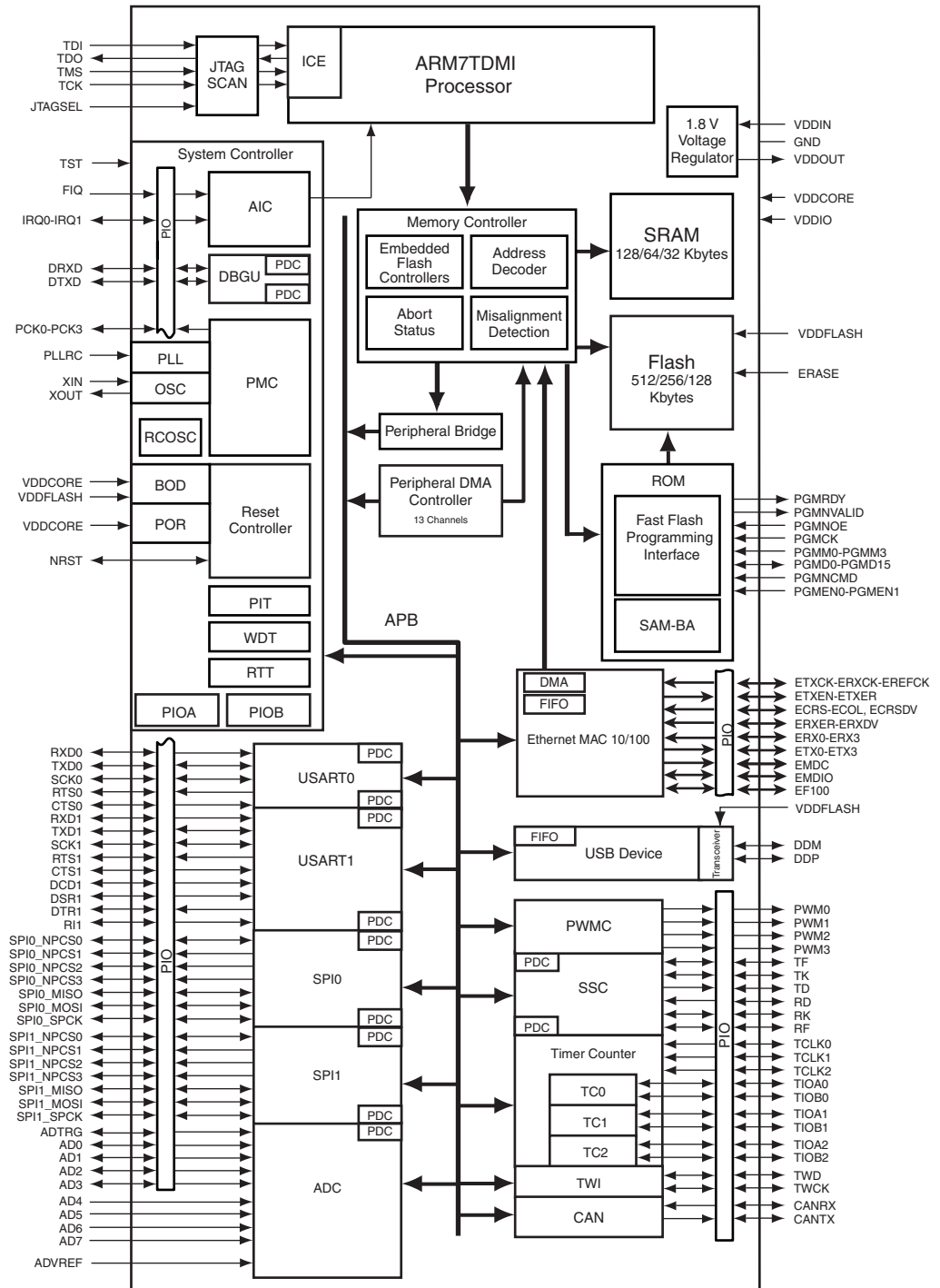
The AT91SAM7X512, AT91SAM7X256 and AT91SAM7X128 differ only in memory sizes. [Table 1-1](#) summarizes the configurations of the three devices.

Table 1-1. Configuration Summary

| Device | Flash | Flash Organization | SRAM |
|--------------|------------|--------------------|------------|
| AT91SAM7X512 | 512 Kbytes | dual plane | 128 Kbytes |
| AT91SAM7X256 | 256 Kbytes | single plane | 64 Kbytes |
| AT91SAM7X128 | 128 Kbytes | single plane | 32 Kbytes |

2. AT91SAM7X512/256/128 Block Diagram

Figure 2-1. AT91SAM7X512/256/128 Block Diagram



3. Signal Description

Table 3-1. Signal Description List

| Signal Name | Function | Type | Active Level | Comments |
|-------------------------------------|--|--------|--------------|-------------------------------------|
| Power | | | | |
| VDDIN | Voltage Regulator and ADC Power Supply Input | Power | | 3V to 3.6V |
| VDDOUT | Voltage Regulator Output | Power | | 1.85V |
| VDDFLASH | Flash and USB Power Supply | Power | | 3V to 3.6V |
| VDDIO | I/O Lines Power Supply | Power | | 3V to 3.6V |
| VDDCORE | Core Power Supply | Power | | 1.65V to 1.95V |
| VDDPLL | PLL | Power | | 1.65V to 1.95V |
| GND | Ground | Ground | | |
| Clocks, Oscillators and PLLs | | | | |
| XIN | Main Oscillator Input | Input | | |
| XOUT | Main Oscillator Output | Output | | |
| PLLRC | PLL Filter | Input | | |
| PCK0 - PCK3 | Programmable Clock Output | Output | | |
| ICE and JTAG | | | | |
| TCK | Test Clock | Input | | No pull-up resistor |
| TDI | Test Data In | Input | | No pull-up resistor. |
| TDO | Test Data Out | Output | | |
| TMS | Test Mode Select | Input | | No pull-up resistor. |
| JTAGSEL | JTAG Selection | Input | | Pull-down resistor. |
| Flash Memory | | | | |
| ERASE | Flash and NVM Configuration Bits Erase Command | Input | High | Pull-down resistor |
| Reset/Test | | | | |
| NRST | Microcontroller Reset | I/O | Low | Pull-up resistor, Open Drain Output |
| TST | Test Mode Select | Input | High | Pull-down resistor |
| Debug Unit | | | | |
| DRXD | Debug Receive Data | Input | | |
| DTXD | Debug Transmit Data | Output | | |
| AIC | | | | |
| IRQ0 - IRQ1 | External Interrupt Inputs | Input | | |
| FIQ | Fast Interrupt Input | Input | | |
| PIO | | | | |
| PA0 - PA30 | Parallel IO Controller A | I/O | | Pulled-up input at reset |
| PB0 - PB30 | Parallel IO Controller B | I/O | | Pulled-up input at reset |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Comments |
|---|-----------------------------------|--------|--------------|----------|
| USB Device Port | | | | |
| DDM | USB Device Port Data - | Analog | | |
| DDP | USB Device Port Data + | Analog | | |
| USART | | | | |
| SCK0 - SCK1 | Serial Clock | I/O | | |
| TXD0 - TXD1 | Transmit Data | I/O | | |
| RXD0 - RXD1 | Receive Data | Input | | |
| RTS0 - RTS1 | Request To Send | Output | | |
| CTS0 - CTS1 | Clear To Send | Input | | |
| DCD1 | Data Carrier Detect | Input | | |
| DTR1 | Data Terminal Ready | Output | | |
| DSR1 | Data Set Ready | Input | | |
| RI1 | Ring Indicator | Input | | |
| Synchronous Serial Controller | | | | |
| TD | Transmit Data | Output | | |
| RD | Receive Data | Input | | |
| TK | Transmit Clock | I/O | | |
| RK | Receive Clock | I/O | | |
| TF | Transmit Frame Sync | I/O | | |
| RF | Receive Frame Sync | I/O | | |
| Timer/Counter | | | | |
| TCLK0 - TCLK2 | External Clock Inputs | Input | | |
| TIOA0 - TIOA2 | I/O Line A | I/O | | |
| TIOB0 - TIOB2 | I/O Line B | I/O | | |
| PWM Controller | | | | |
| PWM0 - PWM3 | PWM Channels | Output | | |
| Serial Peripheral Interface - SPIx | | | | |
| SPIx_MISO | Master In Slave Out | I/O | | |
| SPIx_MOSI | Master Out Slave In | I/O | | |
| SPIx_SPCK | SPI Serial Clock | I/O | | |
| SPIx_NPCS0 | SPI Peripheral Chip Select 0 | I/O | Low | |
| SPIx_NPCS1-NPCS3 | SPI Peripheral Chip Select 1 to 3 | Output | Low | |
| Two-wire Interface | | | | |
| TWD | Two-wire Serial Data | I/O | | |
| TWCK | Two-wire Serial Clock | I/O | | |

AT91SAM7X512/256/128 Preliminary Summary

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Comments |
|---|------------------------------|--------|--------------|-----------------------------------|
| Analog-to-Digital Converter | | | | |
| AD0-AD3 | Analog Inputs | Analog | | Digital pulled-up inputs at reset |
| AD4-AD7 | Analog Inputs | Analog | | Analog Inputs |
| ADTRG | ADC Trigger | Input | | |
| ADVREF | ADC Reference | Analog | | |
| Fast Flash Programming Interface | | | | |
| PGMEN0-PGMEN1 | Programming Enabling | Input | | |
| PGMM0-PGMM3 | Programming Mode | Input | | |
| PGMD0-PGMD15 | Programming Data | I/O | | |
| PGMRDY | Programming Ready | Output | High | |
| PGMNVALID | Data Direction | Output | Low | |
| PGMNOE | Programming Read | Input | Low | |
| PGMCK | Programming Clock | Input | | |
| PGMNCMD | Programming Command | Input | Low | |
| CAN Controller | | | | |
| CANRX | CAN Input | Input | | |
| CANTX | CAN Output | Output | | |
| Ethernet MAC 10/100 | | | | |
| EREFCK | Reference Clock | Input | | RMII only |
| ETXCK | Transmit Clock | Input | | MII only |
| ERXCK | Receive Clock | Input | | MII only |
| ETXEN | Transmit Enable | Output | | |
| ETX0 - ETX3 | Transmit Data | Output | | ETX0 - ETX1 only in RMII |
| ETXER | Transmit Coding Error | Output | | MII only |
| ERXDV | Receive Data Valid | Input | | MII only |
| ECRSDV | Carrier Sense and Data Valid | Input | | RMII only |
| ERX0 - ERX3 | Receive Data | Input | | ERX0 - ERX1 only in RMII |
| ERXER | Receive Error | Input | | |
| ECRS | Carrier Sense | Input | | MII only |
| ECOL | Collision Detected | Input | | MII only |
| EMDC | Management Data Clock | Output | | |
| EMDIO | Management Data Input/Output | I/O | | |
| EF100 | Force 100 Mbits/sec. | Output | High | RMII only |

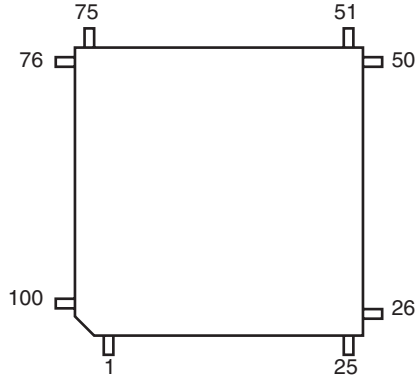
4. Package

The AT91SAM7X512/256/128 is available in 100-lead LQFP Green and 100-ball TFBGA RoHS-compliant packages.

4.1 100-lead LQFP Package Outline

Figure 4-1 shows the orientation of the 100-lead LQFP package. A detailed mechanical description is given in the Mechanical Characteristics section.

Figure 4-1. 100-lead LQFP Package Outline (Top View)



AT91SAM7X512/256/128 Preliminary Summary

4.2 100-lead LQFP Pinout

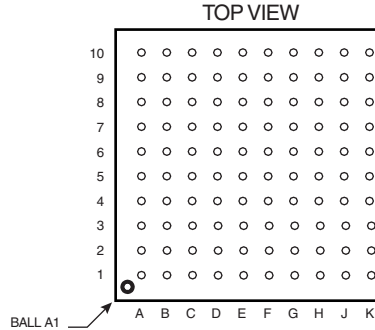
Table 4-1. Pinout in 100-lead LQFP Package

| | | | | | | | |
|----|------------|----|-------------|----|-------------|-----|---------------|
| 1 | ADVREF | 26 | PA18/PGMD6 | 51 | TDI | 76 | TDO |
| 2 | GND | 27 | PB9 | 52 | GND | 77 | JTAGSEL |
| 3 | AD4 | 28 | PB8 | 53 | PB16 | 78 | TMS |
| 4 | AD5 | 29 | PB14 | 54 | PB4 | 79 | TCK |
| 5 | AD6 | 30 | PB13 | 55 | PA23/PGMD11 | 80 | PA30 |
| 6 | AD7 | 31 | PB6 | 56 | PA24/PGMD12 | 81 | PA0/PGMEN0 |
| 7 | VDDOUT | 32 | GND | 57 | NRST | 82 | PA1/PGMEN1 |
| 8 | VDDIN | 33 | VDDIO | 58 | TST | 83 | GND |
| 9 | PB27/AD0 | 34 | PB5 | 59 | PA25/PGMD13 | 84 | VDDIO |
| 10 | PB28/AD1 | 35 | PB15 | 60 | PA26/PGMD14 | 85 | PA3 |
| 11 | PB29/AD2 | 36 | PB17 | 61 | VDDIO | 86 | PA2 |
| 12 | PB30/AD3 | 37 | VDDCORE | 62 | VDDCORE | 87 | VDDCORE |
| 13 | PA8/PGMM0 | 38 | PB7 | 63 | PB18 | 88 | PA4/PGMNCMD |
| 14 | PA9/PGMM1 | 39 | PB12 | 64 | PB19 | 89 | PA5/PGMRDY |
| 15 | VDDCORE | 40 | PB0 | 65 | PB20 | 90 | PA6/PGMNOE |
| 16 | GND | 41 | PB1 | 66 | PB21 | 91 | PA7/PGMNVALID |
| 17 | VDDIO | 42 | PB2 | 67 | PB22 | 92 | ERASE |
| 18 | PA10/PGMM2 | 43 | PB3 | 68 | GND | 93 | DDM |
| 19 | PA11/PGMM3 | 44 | PB10 | 69 | PB23 | 94 | DDP |
| 20 | PA12/PGMD0 | 45 | PB11 | 70 | PB24 | 95 | VDDFLASH |
| 21 | PA13/PGMD1 | 46 | PA19/PGMD7 | 71 | PB25 | 96 | GND |
| 22 | PA14/PGMD2 | 47 | PA20/PGMD8 | 72 | PB26 | 97 | XIN/PGMCK |
| 23 | PA15/PGMD3 | 48 | VDDIO | 73 | PA27/PGMD15 | 98 | XOUT |
| 24 | PA16/PGMD4 | 49 | PA21/PGMD9 | 74 | PA28 | 99 | PLLRC |
| 25 | PA17/PGMD5 | 50 | PA22/PGMD10 | 75 | PA29 | 100 | VDDPLL |

4.3 100-ball TFBGA Package Outline

Figure 4-2 shows the orientation of the 100-ball TFBGA package. A detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

Figure 4-2. 100-ball TFBGA Package Outline (Top View)



4.4 100-ball TFBGA Pinout

Pinout in 100-ball TFBGA Package

| Pin | Signal Name |
|-----|-------------|
| A1 | PA22/PGMD10 |
| A2 | PA21/PGMD9 |
| A3 | PA20/PGMD8 |
| A4 | PB1 |
| A5 | PB7 |
| A6 | PB5 |
| A7 | PB8 |
| A8 | PB9 |
| A9 | PA18/PGMD6 |
| A10 | VDDIO |
| B1 | TDI |
| B2 | PA19/PGMD7 |
| B3 | PB11 |
| B4 | PB2 |
| B5 | PB12 |
| B6 | PB15 |
| B7 | PB14 |
| B8 | PA14/PGMD2 |
| B9 | PA16/PGMD4 |
| B10 | PA17/PGMD5 |
| C1 | PB16 |
| C2 | PB4 |
| C3 | PB10 |
| C4 | PB3 |
| C5 | PB0 |

| Pin | Signal Name |
|-----|-------------|
| C6 | PB17 |
| C7 | PB13 |
| C8 | PA13/PGMD1 |
| C9 | PA12/PGMD0 |
| C10 | PA15/PGMD3 |
| D1 | PA23/PGMD11 |
| D2 | PA24/PGMD12 |
| D3 | NRST |
| D4 | TST |
| D5 | PB19 |
| D6 | PB6 |
| D7 | PA10/PGMM2 |
| D8 | VDDIO |
| D9 | PB27/AD0 |
| D10 | PA11/PGMM3 |
| E1 | PA25/PGMD13 |
| E2 | PA26/PGMD14 |
| E3 | PB18 |
| E4 | PB20 |
| E5 | TMS |
| E6 | GND |
| E7 | VDDIO |
| E8 | PB28/AD1 |
| E9 | VDDIO |
| E10 | GND |

| Pin | Signal Name |
|-----|-------------|
| F1 | PB21 |
| F2 | PB23 |
| F3 | PB25 |
| F4 | PB26 |
| F5 | TCK |
| F6 | PA6/PGMNOE |
| F7 | ERASE |
| F8 | VDDCORE |
| F9 | GND |
| F10 | VDDIN |
| G1 | PB22 |
| G2 | PB24 |
| G3 | PA27/PGMD15 |
| G4 | TDO |
| G5 | PA2 |
| G6 | PA5/PGMRDY |
| G7 | VDDCORE |
| G8 | GND |
| G9 | PB30/AD3 |
| G10 | VDDOUT |
| H1 | VDDCORE |
| H2 | PA28 |
| H3 | JTAGSEL |
| H4 | PA3 |
| H5 | PA4/PGMNCMD |

| Pin | Signal Name |
|-----|----------------|
| H6 | PA7/PGMINVALID |
| H7 | PA9/PGMM1 |
| H8 | PA8/PGMM0 |
| H9 | PB29/AD2 |
| H10 | PLLRC |
| J1 | PA29 |
| J2 | PA30 |
| J3 | PA0/PGMEN0 |
| J4 | PA1/PGMEN1 |
| J5 | VDDFLASH |
| J6 | GND |
| J7 | XIN/PGMCK |
| J8 | XOUT |
| J9 | GND |
| J10 | VDDPLL |
| K1 | VDDCORE |
| K2 | VDDCORE |
| K3 | DDP |
| K4 | DDM |
| K5 | GND |
| K6 | AD7 |
| K7 | AD6 |
| K8 | AD5 |
| K9 | AD4 |
| K10 | ADVREF |

5. Power Considerations

5.1 Power Supplies

The AT91SAM7X512/256/128 has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator and the ADC; voltage ranges from 3.0V to 3.6V, 3.3V nominal. In order to decrease current consumption, if the voltage regulator and the ADC are not used, VDDIN, ADVREF, AD4, AD5, AD6 and AD7 should be connected to GND. In this case, VDDOUT should be left unconnected.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDFLASH pin. It powers the USB transceivers and a part of the Flash and is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.
- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

5.2 Power Consumption

The AT91SAM7X512/256/128 has a static current of less than 60 μA on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset when the brownout detector is deactivated. Activating the brownout detector adds 28 μA static current.

The dynamic power consumption on VDDCORE is less than 90 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

5.3 Voltage Regulator

The AT91SAM7X512/256/128 embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100 μA static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 25 μA static current and draws 1 mA of output current.

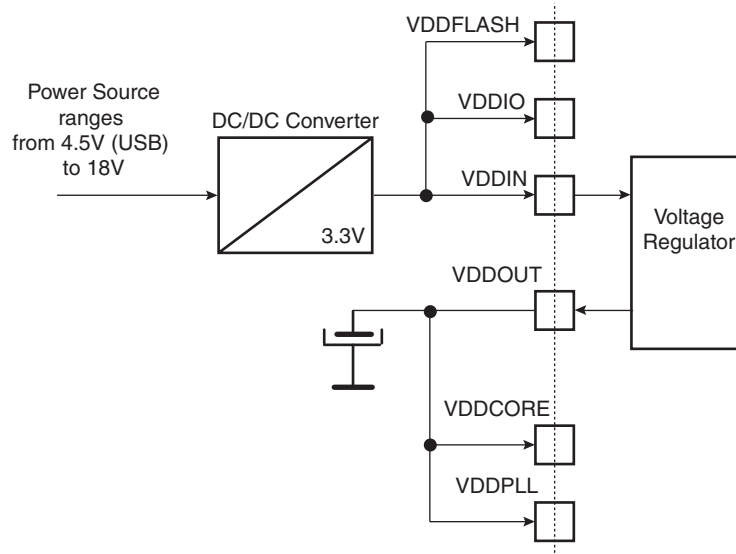
Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel: one external 470 pF (or 1 nF) NPO capacitor should be connected between VDDOUT and GND as close to the chip as possible. One external 2.2 μF (or 3.3 μF) X7R capacitor should be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 μ F X7R.

5.4 Typical Powering Schematics

The AT91SAM7X512/256/128 supports a 3.3V single supply mode. The internal regulator input connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. [Figure 5-1](#) shows the power schematics to be used for USB bus-powered systems.

Figure 5-1. 3.3V System Single Power Supply Schematic



6. I/O Lines Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs and are not 5-V tolerant. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 k Ω to GND, so that it can be left unconnected for normal operations.

6.2 Test Pin

The TST pin is used for manufacturing test or fast programming mode of the AT91SAM7X512/256/128 when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 k Ω to GND, so that it can be left unconnected for normal operations.

To enter fast programming mode, the TST pin and the PA0 and PA1 pins should be tied high and PA2 tied to low.

Driving the TST pin at a high level while PA0 or PA1 is driven at 0 leads to unpredictable results.

6.3 Reset Pin

The NRST pin is bidirectional with an open drain output buffer. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the NRST pin as system user reset, and the use of the signal NRST to reset all the components of the system.

The NRST pin integrates a permanent pull-up resistor to VDDIO.

6.4 ERASE Pin

The ERASE pin is used to re-initialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 k Ω to GND, so that it can be left unconnected for normal operations.

This pin is debounced by the RC oscillator to improve the glitch tolerance. When the pin is tied to high during less than 100 ms, ERASE pin is not taken into account. The pin must be tied high during more than 220 ms to perform the re-initialization of the Flash.

6.5 PIO Controller Lines

All the I/O lines, PA0 to PA30 and PB0 to PB30, are 5V-tolerant and all integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers.

5V-tolerant means that the I/O lines can drive voltage level according to VDDIO, but can be driven with a voltage of up to 5.5V. However, driving an I/O line with a voltage over VDDIO while the programmable pull-up resistor is enabled will create a current path through the pull-up resistor from the I/O line to VDDIO. Care should be taken, in particular at reset, as all the I/O lines default to input with pull-up resistor enabled at reset.

6.6 I/O Lines Current Drawing

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 200 mA.

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
 - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
 - ARM high-performance 32-bit instruction set
 - Thumb high code density 16-bit instruction set
- Three-stage pipeline architecture
 - Instruction Fetch (F)
 - Instruction Decode (D)
 - Execute (E)

7.2 Debug and Test Features

- Integrated embedded in-circuit emulator
 - Two watchpoint units
 - Test access port accessible through a JTAG protocol
 - Debug communication channel
- Debug Unit
 - Two-pin UART
 - Debug communication channel interrupt handling
 - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Programmable Bus Arbiter
 - Handles requests from the ARM7TDMI, the Ethernet MAC and the Peripheral DMA Controller
- Address decoder provides selection signals for
 - Three internal 1 Mbyte memory areas
 - One 256 Mbyte embedded peripheral area
- Abort Status Registers
 - Source, Type and all parameters of the access leading to an abort are saved
 - Facilitates debug by detection of bad pointers
- Misalignment Detector
 - Alignment checking of all data accesses
 - Abort generation in case of misalignment
- Remap Command
 - Remaps the SRAM in place of the embedded non-volatile memory
 - Allows handling of dynamic exception vectors

- Embedded Flash Controller
 - Embedded Flash interface, up to three programmable wait states
 - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
 - Key-protected program, erase and lock/unlock sequencer
 - Single command for erasing, programming and locking operations
 - Interrupt generation in case of forbidden operation

7.4 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Thirteen channels
 - Two for each USART
 - Two for the Debug Unit
 - Two for the Serial Synchronous Controller
 - Two for each Serial Peripheral Interface
 - One for the Analog-to-digital Converter
- Low bus arbitration overhead
 - One Master Clock cycle needed for a transfer from memory to peripheral
 - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements
- Peripheral DMA Controller (PDC) priority is as follows (from the highest priority to the lowest):

| | |
|----------|--------|
| Receive | DBGU |
| Receive | USART0 |
| Receive | USART1 |
| Receive | SSC |
| Receive | ADC |
| Receive | SPI0 |
| Receive | SPI1 |
| Transmit | DBGU |
| Transmit | USART0 |
| Transmit | USART |
| Transmit | SSC |
| Transmit | SPI0 |
| Transmit | SPI1 |

8. Memories

8.1 AT91SAM7X512

- 512 Kbytes of dual-plane Flash Memory
 - 2 contiguous banks of 1024 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 32 lock bits, protecting 32 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 128 Kbytes of Fast SRAM
 - Single-cycle access at full speed

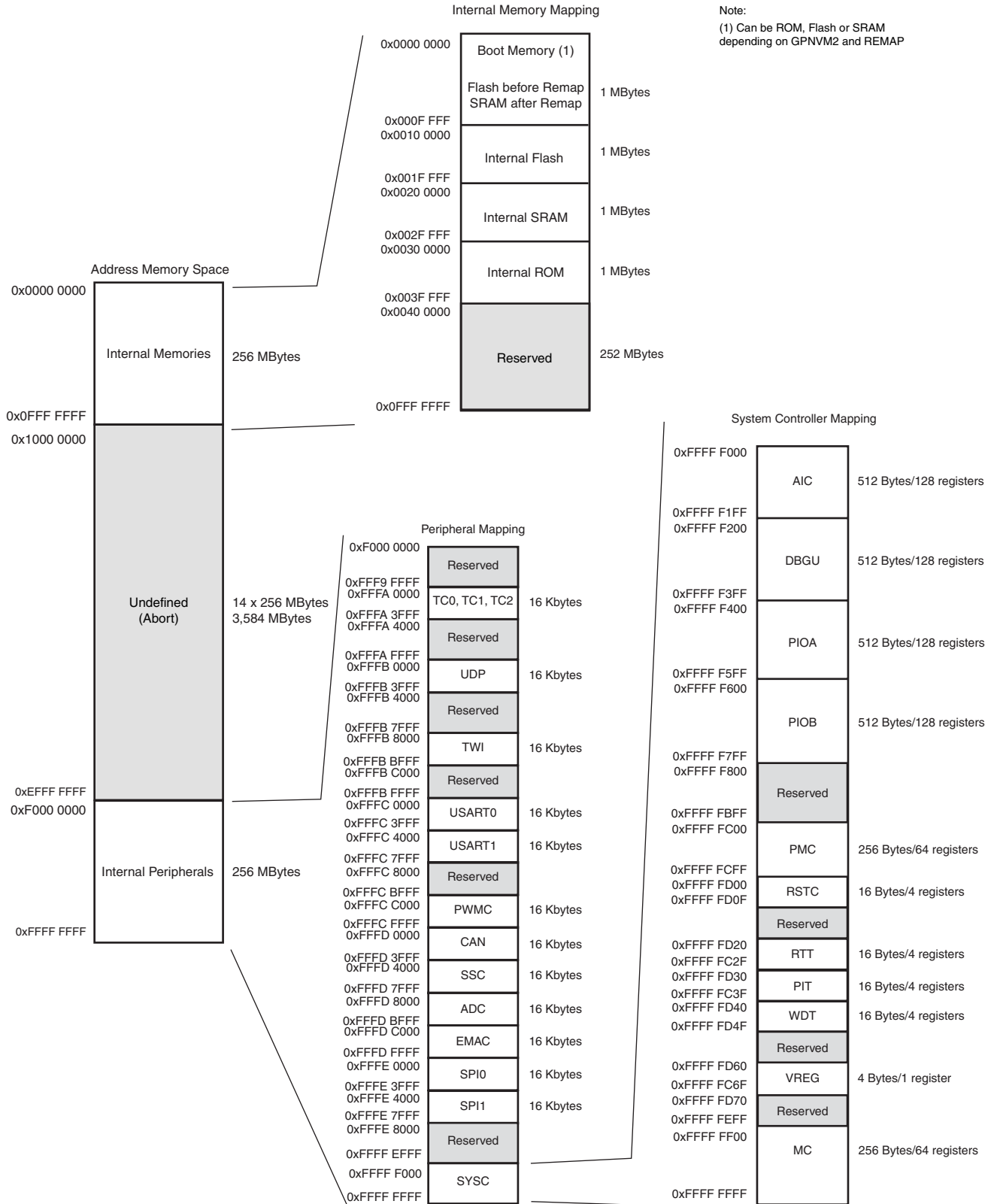
8.2 AT91SAM7X256

- 256 Kbytes of Flash Memory
 - 1024 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 16 lock bits, each protecting 16 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
 - Single-cycle access at full speed

8.3 AT91SAM7X128

- 128 Kbytes of Flash Memory
 - 512 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 8 lock bits, each protecting 8 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 32 Kbytes of Fast SRAM
 - Single-cycle access at full speed

Figure 8-1. AT91SAM7X512/256/128 Memory Mapping



8.4 Memory Mapping

8.4.1 Internal SRAM

- The AT91SAM7X512 embeds a high-speed 128 Kbyte SRAM bank.
- The AT91SAM7X256 embeds a high-speed 64 Kbyte SRAM bank.
- The AT91SAM7X128 embeds a high-speed 32 Kbyte SRAM bank.

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

8.4.2 Internal ROM

The AT91SAM7X512/256/128 embeds an Internal ROM. At any time, the ROM is mapped at address 0x30 0000. The ROM contains the FFPI and the SAM-BA program.

8.4.3 Internal Flash

- The AT91SAM7X512 features two banks (dual plane) of 256 Kbytes of Flash.
- The AT91SAM7X256 features one bank (single plane) of 256 Kbytes of Flash.
- The AT91SAM7X128 features one bank (single plane) of 128 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000. It is also accessible at address 0x0 after the reset, if GPNVM bit 2 is cleared and before the Remap Command.

A general purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

This GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

Setting the GPNVM Bit 2 selects the boot from the Flash. Asserting ERASE clears the GPNVM Bit 2 and thus selects the boot from the ROM by default.

Figure 8-2. Internal Memory Mapping with GPNVM Bit 2 = 0 (default)

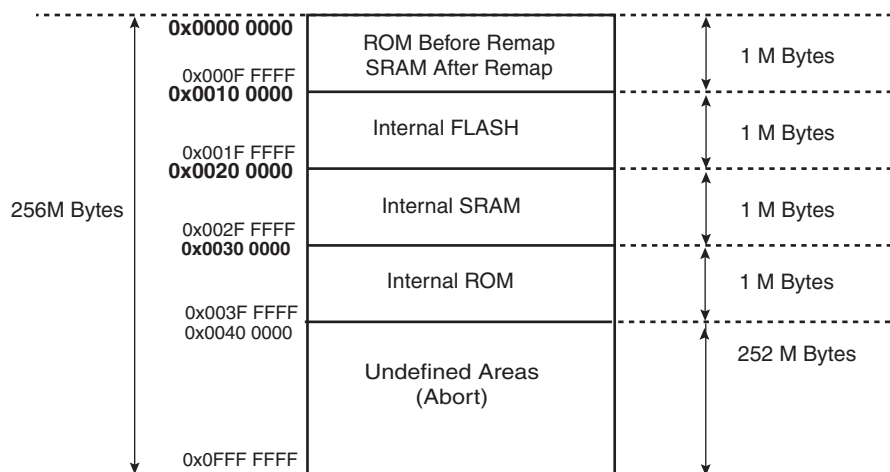
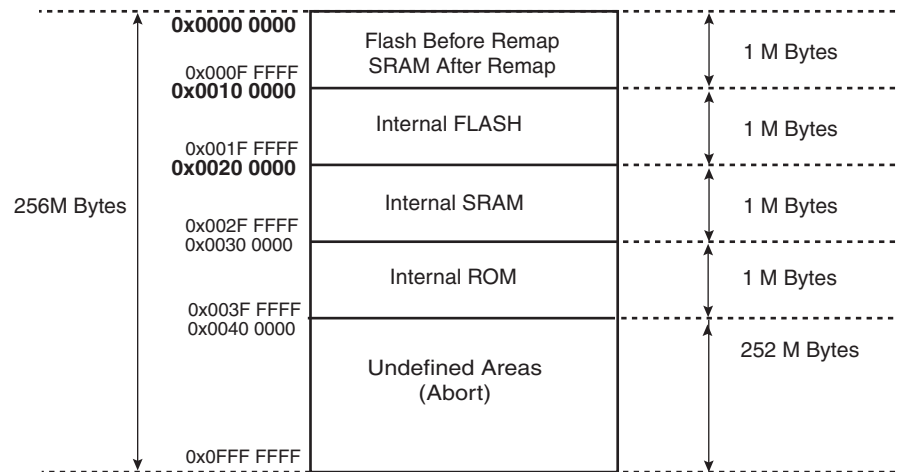


Figure 8-3. Internal Memory Mapping with GPNVM Bit 2 = 1



8.5 Embedded Flash

8.5.1 Flash Overview

- The Flash of the AT91SAM7X512 is organized in two banks (dual plane) of 1024 pages of 256 bytes. The 524,288 bytes are organized in 32-bit words.
- The Flash of the AT91SAM7X256 is organized in 1024 pages of 256 bytes (single plane). It reads as 65,536 32-bit words.
- The Flash of the AT91SAM7X128 is organized in 512 pages of 256 bytes (single plane). It reads as 32,768 32-bit words.

The Flash contains a 256-byte write buffer, accessible through a 32-bit interface.

The Flash benefits from the integration of a power reset cell and from the brownout detector. This prevents code corruption during power supply changes, even in the worst conditions.

When Flash is not used (read or write access), it is automatically placed into standby mode.

8.5.2 Embedded Flash Controller

The Embedded Flash Controller (EFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB. The User Interface allows:

- programming of the access parameters of the Flash (number of wait states, timings, etc.)
- starting commands such as full erase, page erase, page program, NVM bit set, NVM bit clear, etc.
- getting the end status of the last command
- getting error status
- programming interrupts on the end of the last commands or on errors

The Embedded Flash Controller also provides a dual 32-bit Prefetch Buffer that optimizes 16-bit access to the Flash. This is particularly efficient when the processor is running in Thumb mode.

Two EFCs are embedded in the AT91SAM7X512 to control each bank of 256 KBytes. Dual-plane organization allows concurrent read and program functionality. Read from one memory

plane may be performed even while program or erase functions are being executed in the other memory plane.

One EFC is embedded in the AT91SAM7X256/128 to control the single plane of 256/128 KBytes.

8.5.3 Lock Regions

8.5.3.1 AT91SAM7X512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7X512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 32 NVM bits are software programmable through both of the EFC User Interfaces. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.3.2 AT91SAM7X256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7X256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.3.3 AT91SAM7X128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7X128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.4 Security Bit Feature

The AT91SAM7X512/256/128 features a security bit, based on a specific NVM-Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast

Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 220 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

8.5.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.
- The GPNVM Bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM Bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM Bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

8.5.6 Calibration Bits

Eight NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

8.6 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high.

8.7 SAM-BA Boot Assistant

The SAM-BA Boot Assistant is a default Boot Program that provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

- Communication via the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.

AT91SAM7X512/256/128 Preliminary Summary

- Communication via the USB Device Port is limited to an 18.432 MHz crystal.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped at address 0x0 when the GPNVM Bit 2 is set to 0.

When GPNVM bit 2 is set to 1, the device boots from the Flash.

When GPNVM bit 2 is set to 0, the device boots from ROM (SAM-BA).

9. System Controller

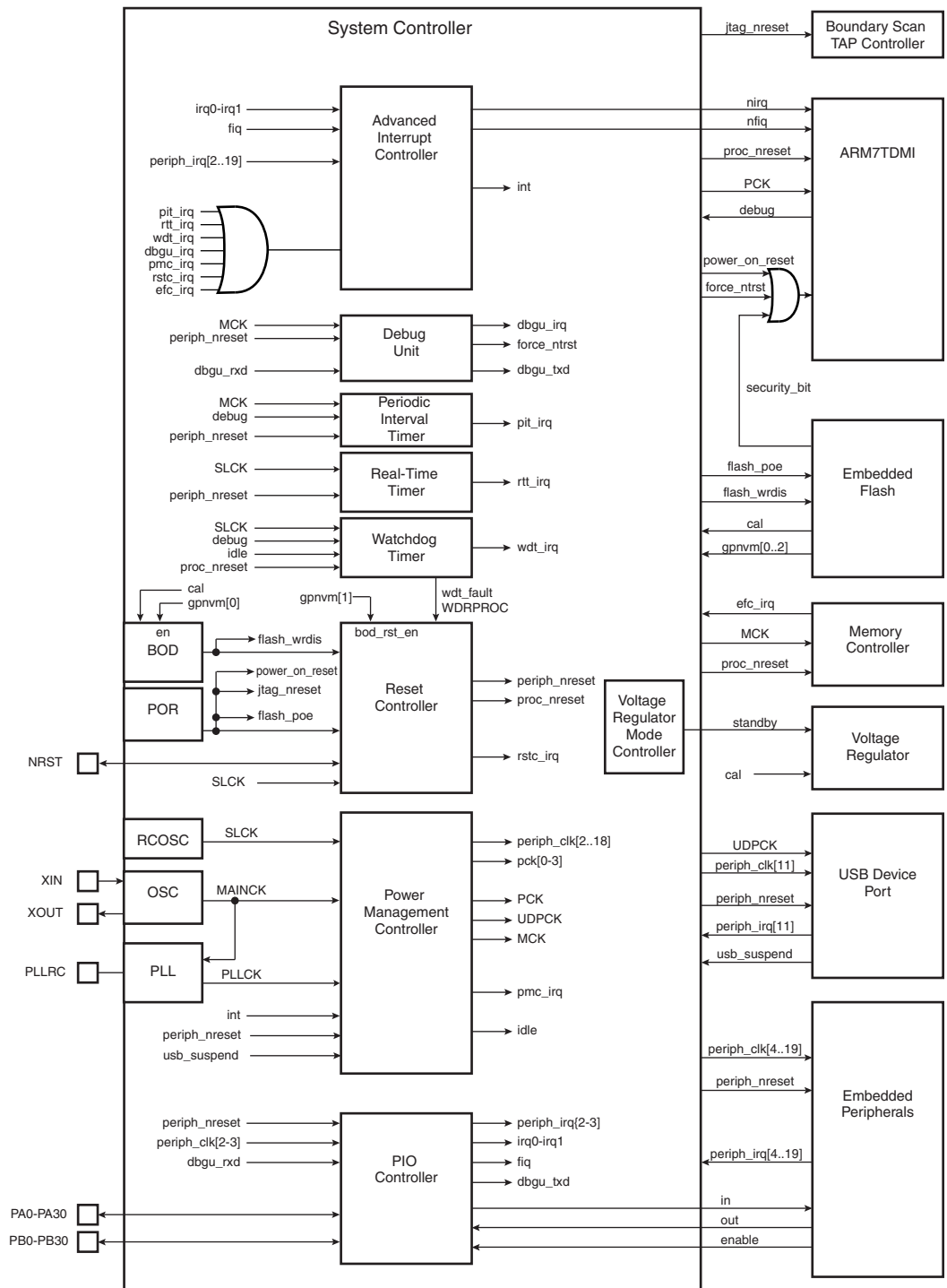
The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

The System Controller peripherals are all mapped to the highest 4 Kbytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF.

[Figure 9-1 on page 25](#) shows the System Controller Block Diagram.

[Figure 8-1 on page 18](#) shows the mapping of the User Interface of the System Controller peripherals. Note that the Memory Controller configuration user interface is also mapped within this address space.

Figure 9-1. System Controller Block Diagram



9.1 Reset Controller

- Based on one power-on reset cell and one brownout detector
- Status of the last reset, either Power-up Reset, Software Reset, User Reset, Watchdog Reset, Brownout Reset
- Controls the internal resets and the NRST pin output
- Allows to shape a signal on the NRST line, guaranteeing that the length of the pulse meets any requirement.

9.1.1 Brownout Detector and Power-on Reset

The AT91SAM7X512/256/128 embeds one brownout detection circuit and a power-on reset cell. The power-on reset is supplied with and monitors VDDCORE.

Both signals are provided to the Flash to prevent any code corruption during power-up or power-down sequences or if brownouts occur on the power supplies.

The power-on reset cell has a limited-accuracy threshold at around 1.5V. Its output remains low during power-up until VDDCORE goes over this voltage level. This signal goes to the reset controller and allows a full re-initialization of the device.

The brownout detector monitors the VDDCORE and VDDFLASH levels during operation by comparing them to a fixed trigger level. It secures system operations in the most difficult environments and prevents code corruption in case of brownout on the VDDCORE or VDDFLASH.

When the brownout detector is enabled and VDDCORE decreases to a value below the trigger level (V_{bot18-} , defined as $V_{bot18} - hyst/2$), the brownout output is immediately activated.

When VDDCORE increases above the trigger level (V_{bot18+} , defined as $V_{bot18} + hyst/2$), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1 μ s.

The VDDCORE threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 1.68V with an accuracy of $\pm 2\%$ and is factory calibrated.

When the brownout detector is enabled and VDDFLASH decreases to a value below the trigger level (V_{bot33-} , defined as $V_{bot33} - hyst/2$), the brownout output is immediately activated.

When VDDFLASH increases above the trigger level (V_{bot33+} , defined as $V_{bot33} + hyst/2$), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1 μ s.

The VDDFLASH threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 2.80V with an accuracy of $\pm 3.5\%$ and is factory calibrated.

The brownout detector is low-power, as it consumes less than 28 μ A static current. However, it can be deactivated to save its static current. In this case, it consumes less than 1 μ A. The deactivation is configured through the GPNVM bit 0 of the Flash.

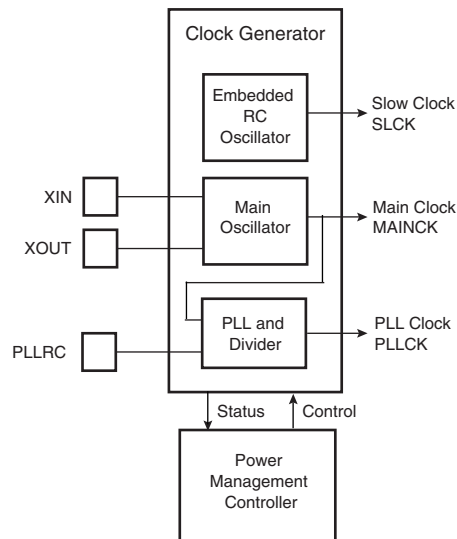
9.2 Clock Generator

The Clock Generator embeds one low-power RC Oscillator, one Main Oscillator and one PLL with the following characteristics:

- RC Oscillator ranges between 22 KHz and 42 KHz
- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 200 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 9-2. Clock Generator Block Diagram



9.3 Power Management Controller

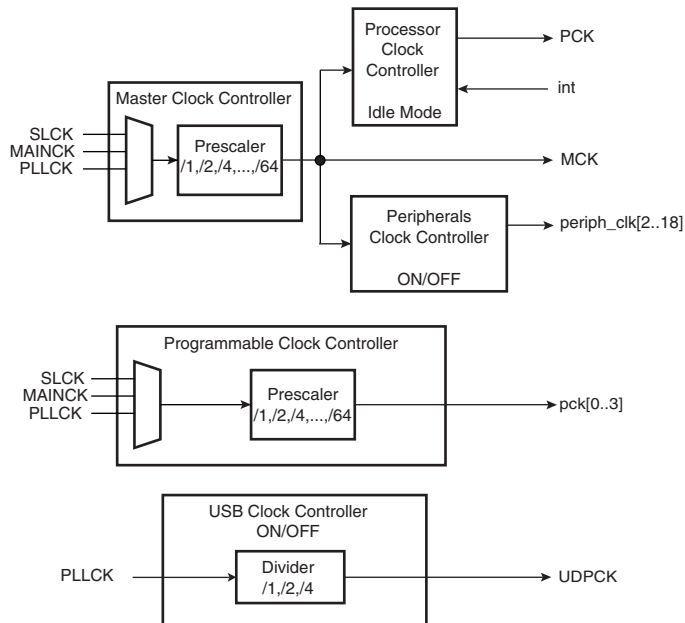
The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCCK
- all the peripheral clocks, independently controllable
- four programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

Figure 9-3. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
 - Source 0 is reserved for the Fast Interrupt Input (FIQ)
 - Source 1 is reserved for system peripherals (RTT, PIT, EFC, PMC, DBGU, etc.)
 - Other sources control the peripheral interrupts or external interrupts
 - Programmable edge-triggered or level-sensitive internal sources
 - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
 - Drives the normal interrupt nIRQ of the processor
 - Handles priority of the interrupt sources

- Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
 - Optimizes interrupt service routine branch and execution
 - One 32-bit vector register per interrupt source
 - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
 - Easy debugging by preventing automatic operations
- Fast Forcing
 - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
 - Provides processor synchronization on events without triggering an interrupt

9.5 Debug Unit

- Comprises:
 - One two-pin UART
 - One Interface for the Debug Communication Channel (DCC) support
 - One set of Chip ID Registers
 - One Interface providing ICE Access Prevention
- Two-pin UART
 - USART-compatible User Interface
 - Programmable Baud Rate Generator
 - Parity, Framing and Overrun Error
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
 - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
 - Identification of the device revision, sizes of the embedded memories, set of peripherals
 - Chip ID is 0x275C 0A40 (VERSION 0) for AT91SAM7X512
 - Chip ID is 0x275B 0940 (VERSION 0) for AT91SAM7X256
 - Chip ID is 0x275A 0740 (VERSION 0) for AT91SAM7X128

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SLCK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SLCK
- Programmable 16-bit prescaler for SLCK accuracy compensation

9.9 PIO Controllers

- Two PIO Controllers, each controlling 31 I/O lines
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
 - Input change interrupt
 - Half a clock period glitch filter
 - Multi-drive option enables driving in open drain
 - Programmable pull-up on each I/O line
 - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The purpose of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 Mbytes of address space between 0xF000 0000 and 0xFFFF EFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is provided in [Figure 8-1 on page 18](#).

10.2 Peripheral Identifiers

The AT91SAM7X512/256/128 embeds a wide range of peripherals. [Table 10-1](#) defines the Peripheral Identifiers of the AT91SAM7X512/256/128. Unique peripheral identifiers are defined for both the Advanced Interrupt Controller and the Power Management Controller.

Table 10-1. Peripheral Identifiers

| Peripheral ID | Peripheral Mnemonic | Peripheral Name | External Interrupt |
|---------------|---------------------|-----------------------------------|--------------------|
| 0 | AIC | Advanced Interrupt Controller | FIQ |
| 1 | SYSC ⁽¹⁾ | System Controller | |
| 2 | PIOA | Parallel I/O Controller A | |
| 3 | PIOB | Parallel I/O Controller B | |
| 4 | SPIO | Serial Peripheral Interface 0 | |
| 5 | SPI1 | Serial Peripheral Interface 1 | |
| 6 | US0 | USART 0 | |
| 7 | US1 | USART 1 | |
| 8 | SSC | Synchronous Serial Controller | |
| 9 | TWI | Two-wire Interface | |
| 10 | PWMC | Pulse Width Modulation Controller | |
| 11 | UDP | USB Device Port | |
| 12 | TC0 | Timer/Counter 0 | |
| 13 | TC1 | Timer/Counter 1 | |
| 14 | TC2 | Timer/Counter 2 | |
| 15 | CAN | CAN Controller | |
| 16 | EMAC | Ethernet MAC | |
| 17 | ADC ⁽¹⁾ | Analog-to Digital Converter | |
| 18 - 29 | Reserved | | |
| 30 | AIC | Advanced Interrupt Controller | IRQ0 |
| 31 | AIC | Advanced Interrupt Controller | IRQ1 |

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller and ADC are continuously clocked.

10.3 Peripheral Multiplexing on PIO Lines

The AT91SAM7X512/256/128 features two PIO controllers, PIOA and PIOB, that multiplex the I/O lines of the peripheral set.

Each PIO Controller controls 31 lines. Each line can be assigned to one of two peripheral functions, A or B. Some of them can also be multiplexed with the analog inputs of the ADC Controller.

[Table 10-2 on page 33](#) and [Table 10-3 on page 34](#) defines how the I/O lines of the peripherals A, B or the analog inputs are multiplexed on the PIO Controller A and PIO Controller B. The two columns “Function” and “Comments” have been inserted for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions that are output only, may be duplicated in the table.

At reset, all I/O lines are automatically configured as input with the programmable pull-up enabled, so that the device is maintained in a static state as soon as a reset is detected.

10.4 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

| PIO Controller A | | | | Application Usage | |
|------------------|--------------|--------------|------------|-------------------|----------|
| I/O Line | Peripheral A | Peripheral B | Comments | Function | Comments |
| PA0 | RXD0 | | High-Drive | | |
| PA1 | TXD0 | | High-Drive | | |
| PA2 | SCK0 | SPI1_NPCS1 | High-Drive | | |
| PA3 | RTS0 | SPI1_NPCS2 | High-Drive | | |
| PA4 | CTS0 | SPI1_NPCS3 | | | |
| PA5 | RXD1 | | | | |
| PA6 | TXD1 | | | | |
| PA7 | SCK1 | SPI0_NPCS1 | | | |
| PA8 | RTS1 | SPI0_NPCS2 | | | |
| PA9 | CTS1 | SPI0_NPCS3 | | | |
| PA10 | TWD | | | | |
| PA11 | TWCK | | | | |
| PA12 | SPI_NPCS0 | | | | |
| PA13 | SPI0_NPCS1 | PCK1 | | | |
| PA14 | SPI0_NPCS2 | IRQ1 | | | |
| PA15 | SPI0_NPCS3 | TCLK2 | | | |
| PA16 | SPI0_MISO | | | | |
| PA17 | SPI0_MOSI | | | | |
| PA18 | SPI0_SPCK | | | | |
| PA19 | CANRX | | | | |
| PA20 | CANTX | | | | |
| PA21 | TF | SPI1_NPCS0 | | | |
| PA22 | TK | SPI1_SPCK | | | |
| PA23 | TD | SPI1_MOSI | | | |
| PA24 | RD | SPI1_MISO | | | |
| PA25 | RK | SPI1_NPCS1 | | | |
| PA26 | RF | SPI1_NPCS2 | | | |
| PA27 | DRXD | PCK3 | | | |
| PA28 | DTXD | | | | |
| PA29 | FIQ | SPI1_NPCS3 | | | |
| PA30 | IRQ0 | PCK2 | | | |



10.5 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

| PIO Controller B | | | | Application Usage | |
|------------------|--------------|--------------|----------|-------------------|----------|
| I/O Line | Peripheral A | Peripheral B | Comments | Function | Comments |
| PB0 | ETXCK/EREFCK | PCK0 | | | |
| PB1 | ETXEN | | | | |
| PB2 | ETX0 | | | | |
| PB3 | ETX1 | | | | |
| PB4 | ECRS | | | | |
| PB5 | ERX0 | | | | |
| PB6 | ERX1 | | | | |
| PB7 | ERXER | | | | |
| PB8 | EMDC | | | | |
| PB9 | EMDIO | | | | |
| PB10 | ETX2 | SPI1_NPCS1 | | | |
| PB11 | ETX3 | SPI1_NPCS2 | | | |
| PB12 | ETXER | TCLK0 | | | |
| PB13 | ERX2 | SPI0_NPCS1 | | | |
| PB14 | ERX3 | SPI0_NPCS2 | | | |
| PB15 | ERXDV/ECRSDV | | | | |
| PB16 | ECOL | SPI1_NPCS3 | | | |
| PB17 | ERXCK | SPI0_NPCS3 | | | |
| PB18 | EF100 | ADTRG | | | |
| PB19 | PWM0 | TCLK1 | | | |
| PB20 | PWM1 | PCK0 | | | |
| PB21 | PWM2 | PCK1 | | | |
| PB22 | PWM3 | PCK2 | | | |
| PB23 | TIOA0 | DCD1 | | | |
| PB24 | TIOB0 | DSR1 | | | |
| PB25 | TIOA1 | DTR1 | | | |
| PB26 | TIOB1 | RI1 | | | |
| PB27 | TIOA2 | PWM0 | AD0 | | |
| PB28 | TIOB2 | PWM1 | AD1 | | |
| PB29 | PCK1 | PWM2 | AD2 | | |
| PB30 | PCK2 | PWM3 | AD3 | | |

10.6 Ethernet MAC

- DMA Master on Receive and Transmit Channels
- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s operation
- Full- and half-duplex operation
- Statistics Counter Registers
- MII/RMII interface to the physical layer
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit FIFO and 28-byte receive FIFO
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Support Promiscuous Mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- Physical layer management through MDIO interface
- Half-duplex flow control by forcing collisions on incoming frames
- Full-duplex flow control with recognition of incoming pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Jumbo frames up to 10240 bytes supported

10.7 Serial Peripheral Interface

- Supports communication with external serial devices
 - Four chip selects with external decoder allow communication with up to 15 peripherals
 - Serial memories, such as DataFlash® and 3-wire EEPROMs
 - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
 - External co-processors
- Master or slave serial peripheral bus interface
 - 8- to 16-bit programmable data length per chip select
 - Programmable phase and polarity per chip select
 - Programmable transfer delays per chip select, between consecutive transfers and between clock and data
 - Programmable delay between consecutive transfers
 - Selectable mode fault detection
 - Maximum frequency at up to Master Clock

10.8 Two-wire Interface

- Master Mode only
- Compatibility with I²C compatible devices (refer to the TWI section of the datasheet)

- One, two or three bytes internal address registers for easy Serial Memory access
- 7-bit or 10-bit slave addressing
- Sequential read/write operations

10.9 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
 - 1, 1.5 or 2 stop bits in Asynchronous Mode
 - 1 or 2 stop bits in Synchronous Mode
 - Parity generation and error detection
 - Framing error detection, overrun error detection
 - MSB or LSB first
 - Optional break generation and detection
 - By 8 or by 16 over-sampling receiver frequency
 - Hardware handshaking RTS - CTS
 - Modem Signals Management DTR-DSR-DCD-RI on USART1
 - Receiver time-out and transmitter timeguard
 - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
 - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
 - Communication at up to 115.2 Kbps
- Test Modes
 - Remote Loopback, Local Loopback, Automatic Echo

10.10 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.11 Timer Counter

- Three 16-bit Timer Counter Channels
 - Two output compare or one input capture per channel
- Wide range of functions including:
 - Frequency measurement
 - Event counting
 - Interval measurement

- Pulse generation
- Delay timing
- Pulse Width Modulation
- Up/down capabilities
- Each channel is user-configurable and contains:
 - Three external clock inputs
- Five internal clock inputs, as defined in [Table 10-4](#)

Table 10-4. Timer Counter Clocks Assignment

| TC Clock input | Clock |
|----------------|----------|
| TIMER_CLOCK1 | MCK/2 |
| TIMER_CLOCK2 | MCK/8 |
| TIMER_CLOCK3 | MCK/32 |
| TIMER_CLOCK4 | MCK/128 |
| TIMER_CLOCK5 | MCK/1024 |

- Two multi-purpose input/output signals
- Two global registers that act on all three TC channels

10.12 Pulse Width Modulation Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
 - One Modulo n counter providing eleven clocks
 - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
 - Independent enable/disable commands
 - Independent clock selection
 - Independent period and duty cycle, with double buffering
 - Programmable selection of the output waveform polarity
 - Programmable center or left aligned output waveform

10.13 USB Device Port

- USB V2.0 full-speed compliant, 12 Mbits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded 1352-byte dual-port RAM for endpoints
- Six endpoints
 - Endpoint 0: 8 bytes
 - Endpoint 1 and 2: 64 bytes ping-pong
 - Endpoint 3: 64 bytes
 - Endpoint 4 and 5: 256 bytes ping-pong
 - Ping-pong Mode (two memory banks) for bulk endpoints

- Suspend/resume logic

10.14 CAN Controller

- Fully compliant with CAN 2.0A and 2.0B
- Bit rates up to 1Mbit/s
- Eight object oriented mailboxes each with the following properties:
 - CAN Specification 2.0 Part A or 2.0 Part B Programmable for each Message
 - Object configurable to receive (with overwrite or not) or transmit
 - Local tag and mask filters up to 29-bit identifier/channel
 - 32-bit access to data registers for each mailbox data object
 - Uses a 16-bit time stamp on receive and transmit message
 - Hardware concatenation of ID unmasked bitfields to speedup family ID processing
 - 16-bit internal timer for time stamping and network synchronization
 - Programmable reception buffer length up to 8 mailbox objects
 - Priority management between transmission mailboxes
 - Autobaud and listening mode
 - Low power mode and programmable wake-up on bus activity or by the application
 - Data, remote, error and overload frame handling

10.15 Analog-to-Digital Converter

- 8-channel ADC
- 10-bit 384 K samples/sec. Successive Approximation Register ADC
- ± 2 LSB Integral Non Linearity, ± 1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
 - Hardware or software trigger
 - External trigger pin
 - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
 - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Four of eight analog inputs shared with digital signals

11. Package Drawings

Figure 11-1. LQFP Package Drawing

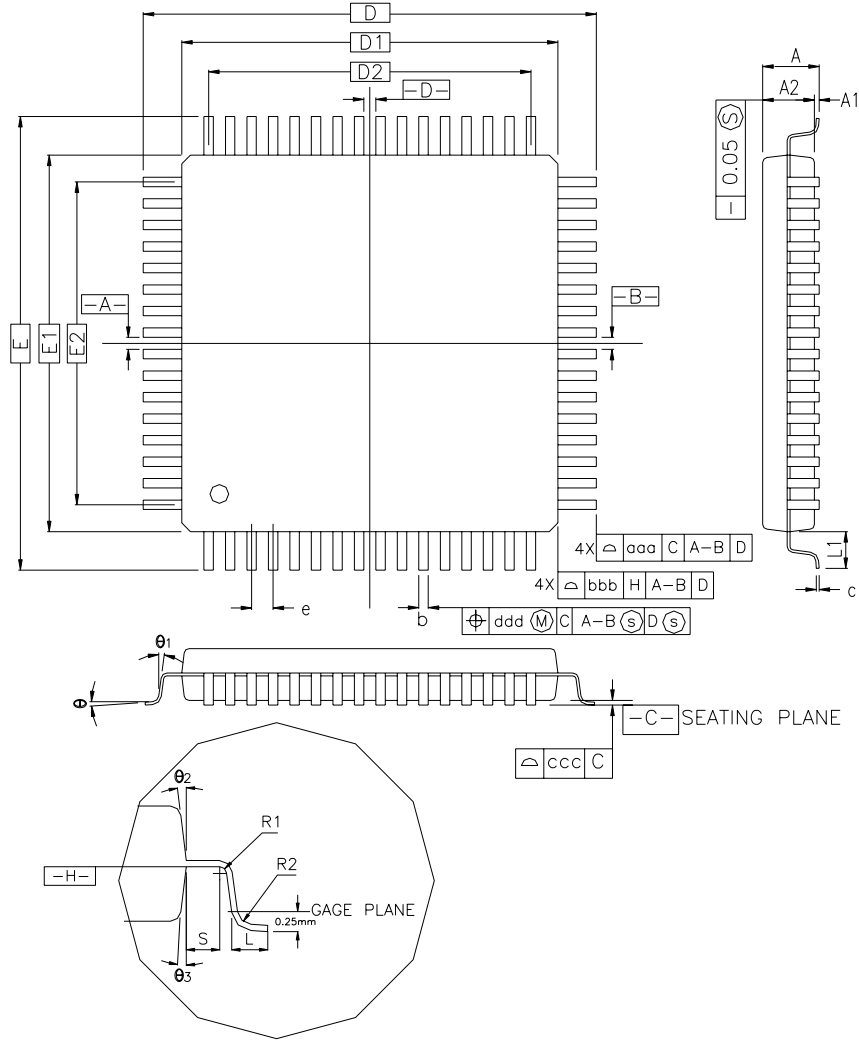
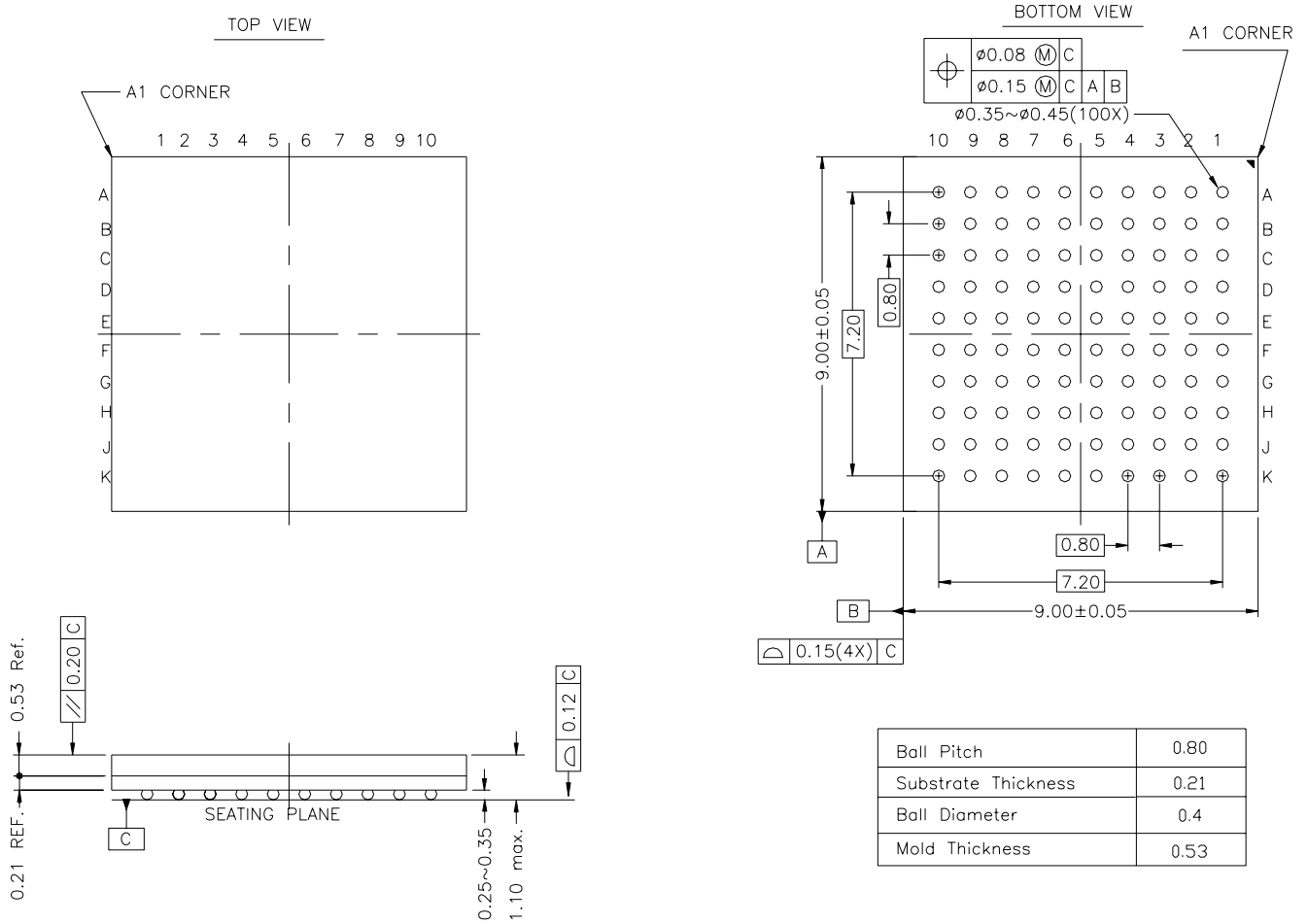




Table 11-1. 100-lead LQFP Package Dimensions

| Symbol | Millimeter | | | Inch | | |
|---------------------------------|------------|------|------|-----------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | | | 1.60 | | | 0.63 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 16.00 BSC | | | 0.630 BSC | | |
| D1 | 14.00 BSC | | | 0.551 BSC | | |
| E | 16.00 BSC | | | 0.630 BSC | | |
| E1 | 14.00 BSC | | | 0.551 BSC | | |
| R2 | 0.08 | | 0.20 | 0.003 | | 0.008 |
| R1 | 0.08 | | | 0.003 | | |
| Q | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | | | 0° | | |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | | 0.20 | 0.004 | | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | | | 0.008 | | |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC | | | 0.020 BSC | | |
| D2 | 12.00 | | | 0.472 | | |
| E2 | 12.00 | | | 0.472 | | |
| Tolerances of Form and Position | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

Figure 11-2. TFBGA Package Drawing



All dimensions are in mm

12. Ordering Information

Table 12-1. Ordering Information

| Ordering Code | Package | Package Type | Temperature Operating Range |
|------------------------------------|-----------------------|--------------|-------------------------------|
| AT91SAM7X512-AU AT91SAM7X512-CU | LQFP 100 TFBGA 100 | Green | Industrial (-40°C to 85°C) |
| AT91SAM7X256-AU AT91SAM7X256-CU | LQFP 100 TFBGA 100 | Green | Industrial (-40°C to 85°C) |
| AT91SAM7X128-AU AT91SAM7X128-CU | LQFP 100 TFBGA 100 | Green | Industrial (-40°C to 85°C) |

Revision History

Table 12-2. Revision History

| Doc. Rev | Comments | Change Request Ref. |
|----------|---|---------------------|
| 6120AS | First issue - Unqualified on Intranet Legal page updated. Qualified on Intranet | |
| 6120BS | <p>Corrections to maintain consistency with full datasheet:</p> <p>In "Features" on page 1, corrected Page Programming Time and Full Erase Time; corrected number of PDC channels, removed Wake-on-LAN support.</p> <p>In Figure 2-1 on page 4, corrected number of PDC channels.</p> <p>In Figure 2-1 on page 4, Table 3-1 on page 5, Table 10-2 on page 33 and Table 10-3 on page 34, changed all SPI pin names.</p> <p>In Section 5.2 "Power Consumption" on page 11, changed value of static current level and value of dynamic power consumption level on VDDCORE</p> <p>In Section 6.2 "Test Pin" on page 13, removed reference to SAM-BA boot recovery.</p> <p>In Section 6.6 "I/O Lines Current Drawing" on page 14, changed value of total current level.</p> <p>In Section 7.4 "Peripheral DMA Controller" on page 16, corrected number of PDC channels.</p> <p>In Section 8. "Memories" on page 17, corrected Page Programming Time and Full Erase Time.</p> <p>In Section 8.7 "SAM-BA Boot Assistant" on page 22, updated section.</p> <p>In Figure 9-1 on page 25, changed range of periph_irq and periph_clk on AIC and for Embedded Peripherals block.</p> <p>In Section 10.6 "Ethernet MAC" on page 35, updated features.</p> | CSR 05-388 |
| 6120CS | Update to product functionalities including changes to "Features" on page 1 , Figure 2-1 on page 4 , Section 9.5 "Debug Unit" on page 29 and to Peripheral mapping. | 05-457 05-462 |
| | Updated PLL output range max value in Section 9.2 "Clock Generator" on page 27 . | 05-491 |
| | Updated information in Section 5.1 "Power Supplies" on page 11 . | |
| | Updated ordering information in "Ordering Information" on page 42 . | 05-471 |
| 6120DS | <p>Added AT91SAM7X512 to product family. "Features" on page 1 and global Reformatted Memories Section 8. "Memories" on page 17.</p> <p>Reordered sub sections in Peripherals Section 10. "Peripherals" on page 31</p> <p>Consolidated Memory Mapping in Figure 8-1 on page 18.</p> <p>Added TFBGA information Section 4.3 "100-ball TFBGA Package Outline" on page 10. added LQFP and TFBGA package drawings Section 11. on page 39.</p> | 2723 2728 |
| | <p>System Controller block diagram Figure 9-1 on page 25, "ice_nreset" signals changed to "power_on_reset".</p> <p>Section 10.1 "User Interface" User Peripherals are mapped between 0xF000 0000 and 0xFFFF EFFF.</p> <p>Table 10-1 on page 31 SYSIRQ changed to SYSC in "Peripheral Identifiers"</p> | rfo review |

Table 12-2. Revision History

| Doc. Rev | Comments | Change Request Ref. |
|----------|---|---|
| 6120ES | <p>“Features”, TWI updated to include Atmel TWI compatibility with I2C Standard.</p> <p>Section 10.8 “Two-wire Interface”, updated.</p> <p>Section 7.4 “Peripheral DMA Controller”, added PDC priority list.</p> <p>Section 10.11 “Timer Counter”, The TC has Two output compare or one input capture per channel.</p> <p>Section 10.15 “Analog-to-Digital Converter”, INL and DNL updated.</p> | <p>4247</p> <p>4774</p> <p>4210</p> <p>4007</p> |



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