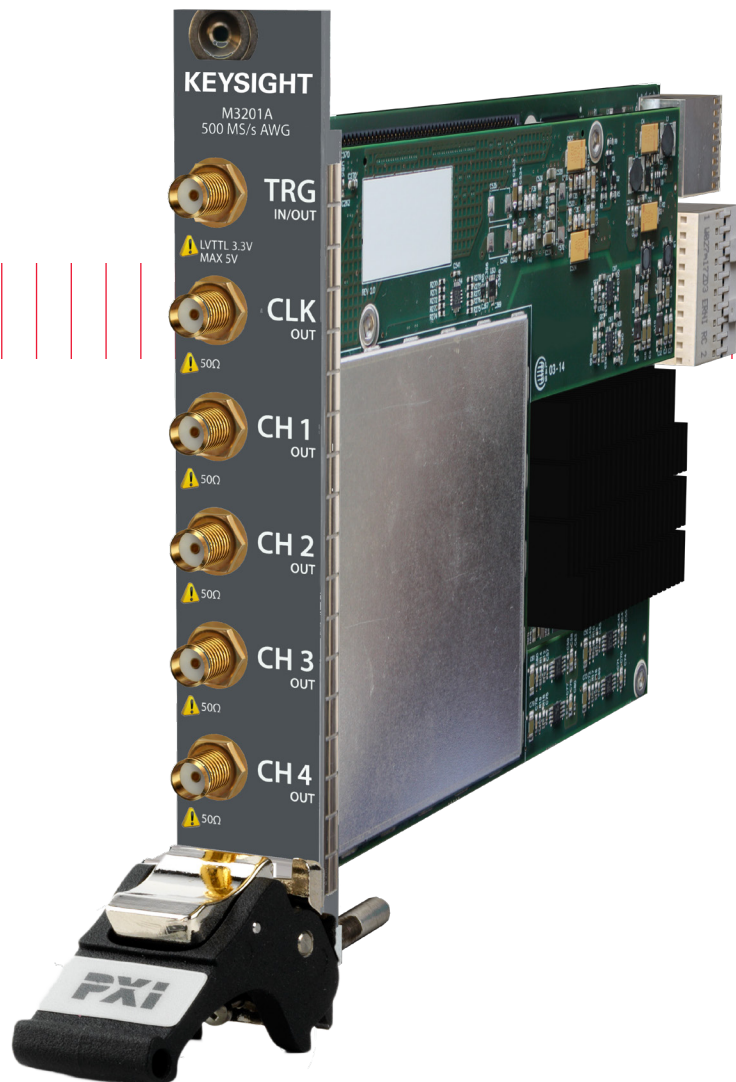


# Keysight M3201A

PXIe Arbitrary Waveform Generator  
with Optional Real-Time Sequencing  
and FPGA Programming

500 MSa/s, 16 Bits, 2/4 Channels

Data Sheet



## Generate High-Precision, Complex, Real-World Signals

The M3201A high-performance, high-bandwidth arbitrary waveform generator combines an advanced waveform generation system with embedded function generators and modulators (frequency/phase/amplitude) for broadband and IF signal generation. Performance meets simplicity thanks to easy-to-use programming libraries, real-time sequencing technology (Hard Virtual Instrumentation or HVI technology), and graphical FPGA programming technology.

### Features

**500 MSa/s, 16 bits, 2/4 channels, 200 MHz BW (400 MHz IQ)**

**Embedded advanced arbitrary waveform generators (AWGs)**

- Advanced triggering and marking (up to 8 reconfigurable I/Os)
- Waveform queue system with cycles, delays and prescalers

**Embedded high-precision function generators (FGs)**

- Sinusoidal, triangular, square, DC, and more
- 45-bit frequency resolution (up to  $\sim 5.68 \mu\text{Hz}$ )
- 24-bit phase resolution (up to  $\sim 21.5 \mu\text{deg}$ )

**Embedded ultra-flexible amplitude and angle modulators**

**High-quality output signal with low phase noise**

- SFDR: 64 dBc @80 MHz (typ.)
- Average noise density: down to  $-145 \text{ dBm/Hz}$  (typ.)

**Optional features**

- Simultaneous amplitude and angle modulations

**Optional HW programming for high-performance applications**

- Real-time sequencing (HVI technology)
- FPGA programming
  - Xilinx Kintex-7 325T or 410T FPGA

**Up to 2 GB of onboard RAM ( $\sim 1 \text{ Gsamples}$ )**

**Mechanical/interface**

- 1 slot 3U (PXIe)
- Up to 1.6 GB/s transfer BW with P2P capabilities (PCIe Gen 2)
- Independent direct memory access (DMA) channels for fast and efficient data transfer

### Applications

**MIMO, beam forming and other multi-channel coherent signal generation**

**Manufacturing in wireless devices, automated test equipment (ATE)**

**General purpose, RF/arbitrary waveform generation**

**R&D/scientific research equipment, aerospace & defense (A/D)**

## Programming Technology and Software Tools

### Software programming

- Easy-to-use native programming libraries for most common languages: C, C++, Visual Studio, LabVIEW, MATLAB, Python, and more

### Hardware programming (optional)

- Real-time sequencing (Hard Virtual Instrumentation or HVI technology)
  - Graphical flowchart-style M3601A design environment (-HV1 option required on HW)
  - Ultra-fast, fully-parallelized, hard real-time execution
  - Ultra-fast, time-deterministic decision-making
  - Off-the-shelf inter-module synchronization & data exchange
- FPGA programming
  - Graphical M3602A FPGA design environment (-FP1 option required on HW)
  - No FPGA know-how required
  - Include from high-level to low-level design elements: off-the-shelf DSP blocks, MATLAB/Simulink designs, Xilinx CORE Generator IP cores, Xilinx VIVADO/ISE projects, VHDL or Verilog code
  - Ultra-fast, one-click compiling and on-the-fly programming

### No programming

- Ready-to-use SD1 SPF (software front panels)

## PXIe Arbitrary Waveform Generators, Digitizers and Combination Modules

Product	Type	Outputs (AWGs)				Inputs (Digitizers)			
		Speed (MSa/s)	Bits	Ch	BW (MHz)	Speed (MSa/s)	Bits	Ch	BW (MHz)
M3202A	AWG	1000	14	2/4	DC-400				
M3201A	AWG	500	16	2/4	DC-200				
M3102A	Digitizer					500	14	2/4	DC-200
M3100A	Digitizer					100	14	4/8	DC-100
M3302A	Combo	500	16	2	DC-200	500	14	2	DC-200
M3300A	Combo	500	16	2/4	DC-200	100	14	4/8	DC-100

## Functional Block Diagram

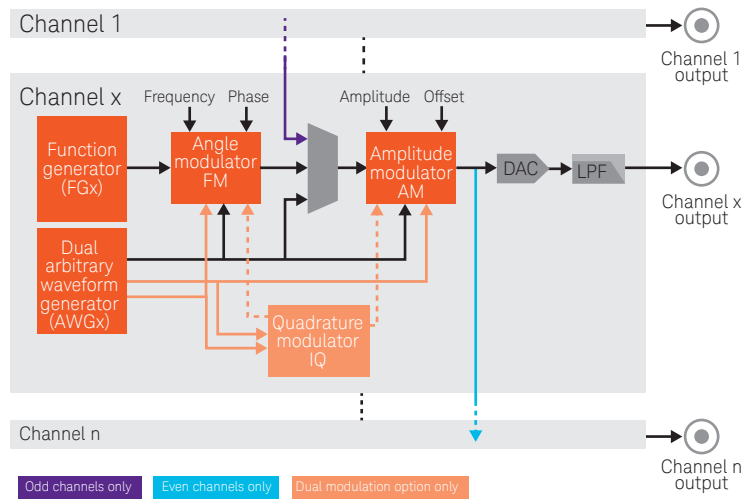


Figure 1. M3201A output functional block diagram, all channels have identical output structure

## Ordering Information <sup>1</sup>

Product	Description
M3201A	PXI arbitrary waveform generator: 500 MSa/s, 16 Bits
Options	Description
M3201A-CH2 / -CH4	Two channels <sup>2</sup> / four channels
M3201A-CLV / -CLF	Variable sampling clock <sup>2</sup> / fixed sampling clock, low jitter
M3201A-DM1	Dual modulation capability (amplitude and angle simultaneously)
M3201A-M01 / -M12 / -M20	Memory 16 MB, 8 MSamples <sup>2</sup> / 128 MB, 60 MSamples / 2 GB, 1 GSamples
HW programming options	Description
M3201A-HVI	Enabled HVI programming, requires an HVI design environment license (M3601A)
M3201A-FP1	Enabled FPGA programming, requires -K32 or -K41 option and an FPGA design environment license (M3602A)
M3201A-K32 / -K41	FPGA, Xilinx 7K325T / 7K410T, required for -FP1 option only (needs memory option -M20)
Related software	Description
M3601A	HVI design environment
M3602A	FPGA design environment

1. All options must be selected at time of purchase and are not upgradable
2. These options represent the standard configuration

## Technical Specifications and Characteristics

### General characteristics

Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>Inputs and outputs</b>								
Channels (single-ended mode)	2			4			Out	
Channels (differential mode)	1			2			Out	Differential uses 2 channels
Reference clock <sup>1</sup>	1			1			Out	
Reference clock <sup>2</sup>	1			1			In	
Triggers/markers <sup>1,3</sup>	1			1			In/out	Reconfigurable
Triggers/markers <sup>2,3</sup>	8			8			In/out	Reconfigurable
<b>Output channels overview</b>								
Sampling rate <sup>4</sup>	0.005		500	0.005		500	MSa/s	
Voltage resolution	16			16			Bits	
Output frequency	DC		200	DC		200	MHz	
Real-time BW	200			200			MHz	
Output voltage	-1.5		1.5	-1.5		1.5	Volts	
<b>Built-in functionality</b>								
Function generators	2			4				1 per channel
Dual AWGs	2			4				1 per channel
IQ modulators	2			4				1 per channel
Frequency modulators	2			4				1 per channel
Phase modulators	2			4				1 per channel
Amplitude modulators	2			4				1 per channel
DC offset modulators	2			4				1 per channel
<b>Onboard memory</b>								
RAM memory	16		2048	16		2048	MBytes	

1. At front panel
2. At backplane
3. Markers available from firmware version v3.0 or later
4. (-CLV) option: DC to 500 MSa/s; (-CLF) option: fixed 500 MSa/s

## I/O specifications

Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>Output channels</b>								
Sampling rate <sup>1</sup>	0.005		500	0.005		500	MSa/s	
Output frequency	DC		200	DC		200	MHz	Limited by a reconstruction filter
Output voltage	-1.5		1.5	-1.5		1.5	Volts	On a 50 $\Omega$ load
Source impedance		50			50		$\Omega$	
<b>Reference clock output</b>								
Frequency		10 or 100			10 or 100		MHz	Generated from the internal clock, user selectable
Voltage		800			800		mV <sub>pp</sub>	On a 50 $\Omega$ load
Power		2			2		dBm	On a 50 $\Omega$ load
Source impedance		50			50		$\Omega$	AC coupled
<b>External I/O trigger/marker</b>								
V <sub>IH</sub>	2		5	2		5	V	
V <sub>IL</sub>	0		0.8	0		0.8	V	
V <sub>OH</sub>	2.4		3.3	2.4		3.3	V	On a high Z load
V <sub>OL</sub>	0		0.5	0		0.5	V	On a high Z load
Input impedance		10			10		K $\Omega$	
Source impedance		TTL			TTL		–	
Speed		100			100		MHz	

1. (-CLV) option: DC to 500 MSa/s; (-CLF) option: fixed 500 MSa/s

## Function generators (FGs) specifications

Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>General specifications</b>								
Function generators	2			4			-	1 per channel
Waveform types	4			4			-	Sinusoidal, triangular, square and DC
Frequency range	0	200		0	200		MHz	
Frequency resolution	45			45			Bits	
Frequency resolution	5.7			5.7			μHz	
Phase range	0	360		0	360		Deg	
Phase resolution	24			24			Bits	
Phase resolution	21.5			21.5			μdeg	
<b>Speed performance</b>								
Frequency change rate	100			100			MChanges/s	With HVI technology
Frequency modulation rate	500			500			MSamples/s	With AWGs and angle modulators
Phase change rate	100			100			MChanges/s	With HVI technology
Phase modulation rate	500			500			MSamples/s	With AWGs and angle modulators

## Amplitude and offset specifications

Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>General specifications</b>								
Amplitude / offset range	-1.5	1.5		-1.5	1.5		Volts	Amplitude + offset values
Amplitude / offset resolution	16			16			Bits	
Amplitude / offset resolution	45.8			45.8			μV	
<b>Speed performance</b>								
Amplitude / offset change rate	500			500			MChanges/s	With HVI technology
Amplitude / offset modulation rate	500			500			MSamples/s	With AWGs and amplitude modulators

## Arbitrary waveform generators (AWGs) specifications

Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>General specifications</b>								
Dual AWGs	2			4				1 dual AWG per output channel
Aggregated speed (16 bits)	2000			4000			MSa/s	For all onboard waveforms combined
Aggregated speed (32 bits)	1000			2000			MSa/s	For all onboard waveforms combined
Waveform multiple	5			5			Samples	Waveform length must be a multiple of this value
16-bit waveform length	15		957M	15		957M	Samples	Maximum depends on onboard RAM
32-bit waveform length	10		478M	10		478M	Samples	Maximum depends on onboard RAM
Waveform length efficiency	93.5			93.5			%	Effic. = waveform size / waveform size in RAM
Trigger	Selec.			Selec.				External trigger (input connector, backplane triggers), software trigger
<b>AWG specifications (16-bit single waveform)</b>								
Speed	500			500			MSa/s	Per AWG
Resolution	16			16			Bits	
AWG destination	Selec.			Selec.				Amplitude, offset, frequency or phase
<b>AWG specifications (16-bit dual waveform)</b>								
Speed (waveform A)	500			500			MSa/s	Per AWG
Speed (waveform B)	500			500			MSa/s	Per AWG
Resolution (waveform A)	16			16			Bits	
Resolution (waveform B)	16			16			Bits	
AWG destination (waveform A)	Selec.			Selec.				Amplitude, offset or I
AWG destination (waveform B)	Selec.			Selec.				Frequency, phase or Q
<b>AWG specifications (32-bit single waveform)</b>								
Speed	100			100			MSa/s	Per AWG, minimum prescaler: 1
Resolution	32			32			Bits	
AWG destination	Selec.			Selec.				Amplitude, offset, frequency or phase
<b>AWG specifications (32-bit dual waveform)</b>								
Speed (waveform A)	100			100			MSa/s	Per AWG, minimum prescaler: 1
Speed (waveform B)	100			100			MSa/s	Per AWG, minimum prescaler: 1
Resolution (waveform A)	32			32			Bits	
Resolution (waveform B)	32			32			Bits	
AWG destination (waveform A)	Selec.			Selec.				Amplitude or offset
AWG destination (waveform B)	Selec.			Selec.				Frequency or phase



## Angle modulators specifications

Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>General specifications</b>								
Frequency modulators		2			4			1 per output channel
Phase modulators		2			4			1 per output channel
Carrier signal source		FGs			FGs			Table 3 on page 7
Modulating signal source		AWGs			AWGs			Table 5 on page 8
<b>Frequency modulators (16-bit modulating waveform)</b>								
Deviation	-Dev. gain		+Dev. gain	-Dev. gain		+Dev. gain	MHz	
Modulating signal resolution		16			16		Bits	AWG waveform
Modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit
Deviation gain	0		200	0		200	MHz	
Deviation gain resolution		16			16		Bits	
<b>Frequency modulators (32-bit modulating waveform)</b>								
Deviation	-Dev. gain		+Dev. gain	-Dev. gain		+Dev. gain	MHz	
Modulating signal resolution		32			32		Bits	AWG waveform
Modulating signal BW	0		50	0		50	MHz	AWG Nyquist limit
Deviation gain	0		200	0		200	MHz	
Deviation gain resolution		16			16		Bits	
<b>Phase modulators (16-bit modulating waveform)</b>								
Deviation	-Dev. gain		+Dev. gain	-Dev. gain		+Dev. gain	Deg	
Modulating signal resolution		16			16		Bits	AWG waveform
Modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit
Deviation gain	0		180	0		180	Deg	
Deviation gain resolution		16			16		Bits	~ 5.5 mdeg
<b>Phase modulators (32-bit modulating waveform)</b>								
Deviation	-Dev. gain		+Dev. gain	-Dev. gain		+Dev. gain	Deg	
Modulating signal resolution		16			16		Bits	AWG waveform is truncated
Modulating signal BW	0		50	0		50	MHz	AWG Nyquist limit
Deviation gain	0		180	0		180	Deg	
Deviation gain resolution		16			16		Bits	~ 5.5 mdeg

## Amplitude modulators specifications

Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>General specifications</b>								
Amplitude modulators	2			4				1 per output channel
Offset modulators	2			4				1 per output channel
Carrier signal source	FGs			FGs				Table 3 on page 7
Modulating signal source	AWGs			AWGs				Table 5 on page 8
<b>Amplitude &amp; offset modulators (16-bit modulating waveform)</b>								
Deviation	-Dev. gain	+Dev. gain		-Dev. gain	+Dev. gain		$V_p$	
Modulating signal resolution	16			16			Bits	AWG waveform
Modulating signal BW	0	250		0	250		MHz	AWG Nyquist limit
Deviation gain	0	1.5		0	1.5		$V_p$	
Deviation gain resolution	16			16			Bits	Limited by the output DAC
<b>Amplitude &amp; offset modulators (32-bit modulating waveform)</b>								
Deviation	-Dev. gain	+Dev. gain		-Dev. gain	+Dev. gain		$V_p$	
Modulating signal resolution	16			16			Bits	AWG waveform is truncated
Modulating signal BW	0	50		0	50		MHz	AWG Nyquist limit
Deviation gain	0	1.5		0	1.5		$V_p$	
Deviation gain resolution	16			16			Bits	Limited by the output DAC

## IQ modulators specifications

Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>General specifications</b>								
IQ modulators	2			4				1 per output channel
Carrier signal source	FGs			FGs				Table 3 on page 7
Modulating signal source	AWGs			AWGs				Table 5 on page 8
Amplitude deviation	-1.5		-1.5	-1.5		-1.5	V <sub>p</sub>	
Phase deviation	-180		180	-180		180	Deg	
I modulating signal resolution	16			16			Bits	AWG waveform
I modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit
Q modulating signal resolution	16			16			Bits	AWG waveform
Q modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit

## Clock system specifications

Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>General specifications</b>								
Clock frequency <sup>1</sup>	>100		500	>100		500	MHz	

1. (-CLV) option: 100 to 500 MSa/s; (-CLF) option: fixed 500 MSa/s

## AC performance

Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>General characteristics</b>								
Analog output jitter		<2			<2		ps	RMS (cycle-to-cycle)
AWG trigger to output jitter		<2			<2		ps	RMS (cycle-to-cycle) for any trigger referenced to the chassis clock; independent of input trigger jitter if input jitter < 4nS peak-to-peak
Trigger resolution		10			10		ns	
Channel-to-channel skew		<20			<20		ps	Between ch 0 & ch 1, and ch 2 & ch 3
		<50			<50		ps	Between any channel
		<150			<150		ps	Between modules, chassis dependent <sup>2</sup>
Clock output jitter		<2			<2		ps	RMS (cycle-to-cycle)
Clock accuracy and stability		100			100		ppm	PXIe, cPXIe versions; chassis dependent <sup>1</sup>
<b>AC characteristics</b>								
Spurious-free dynamic range (SFDR)								$P_{out} = 0$ dBm, measured from DC to max frequency
$f_{out} = 10$ MHz		68			68		dBc	
$f_{out} = 80$ MHz		64			64		dBc	
$f_{out} = 120$ MHz		57			57		dBc	
$f_{out} = 160$ MHz		54			54		dBc	
Crosstalk (adjacent channels)								
$f_{out} = 10$ MHz		<-105			<-105		dB	
$f_{out} = 80$ MHz		-75			-75		dB	
$f_{out} = 120$ MHz		-88			-88		dB	
$f_{out} = 160$ MHz		-73			-73		dB	
Crosstalk (non-adjacent channels)								
$f_{out} = 10$ MHz		<-105			<-105		dB	
$f_{out} = 80$ MHz		-78			-78		dB	
$f_{out} = 120$ MHz		<-105			<-105		dB	
$f_{out} = 160$ MHz		-92			-92		dB	
Phase noise (SSB)								
offset = 1 kHz		<-127			<-127		dBc/Hz	
offset = 10 kHz		<-133			<-133		dBc/Hz	
offset = 100 kHz		<-138			<-138		dBc/Hz	
Average noise power density		<-145			<-145		dBm/Hz	

1. This value corresponds to a chassis that fulfills the PXI Express specifications. This value can be improved with an external chassis clock or a System Timing Module.
2. This value corresponds to a M9005A PXIe chassis.

### AC performance, typical

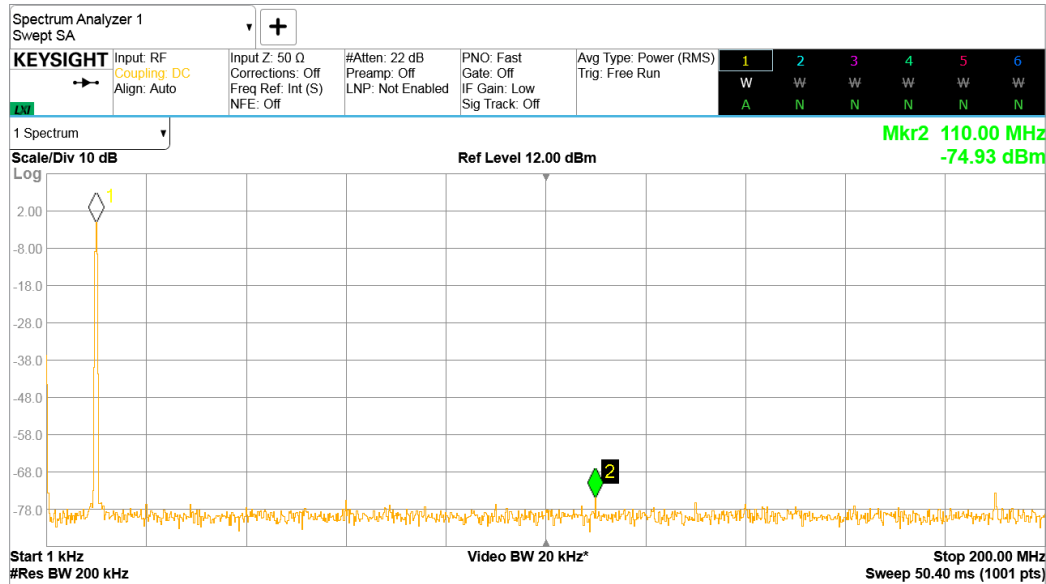


Figure 2. Single-tone spectrum @  $f_{out} = 10$  MHz

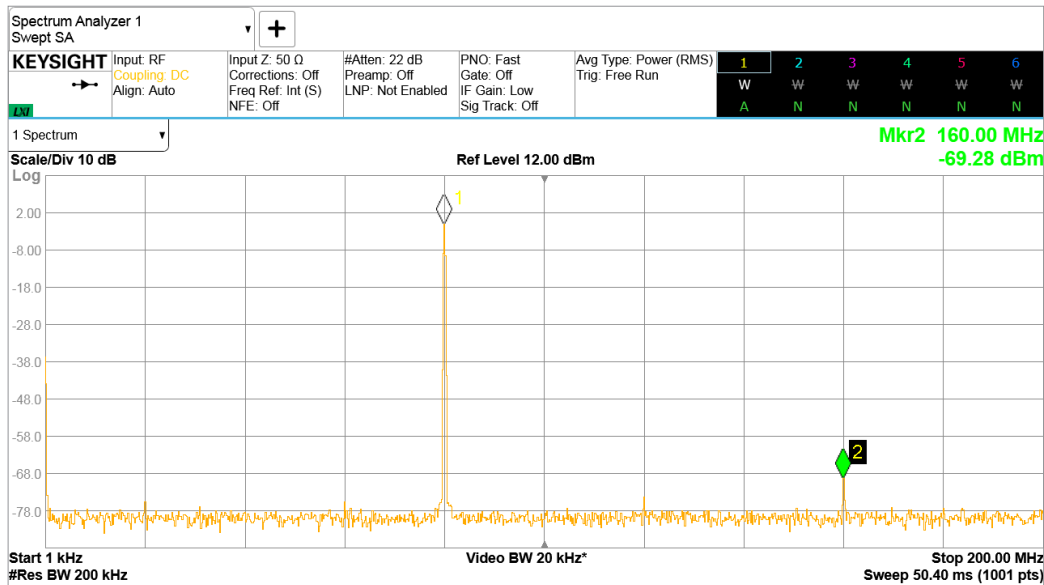


Figure 3. Single-tone spectrum @  $f_{out} = 80$  MHz

## AC performance, typical

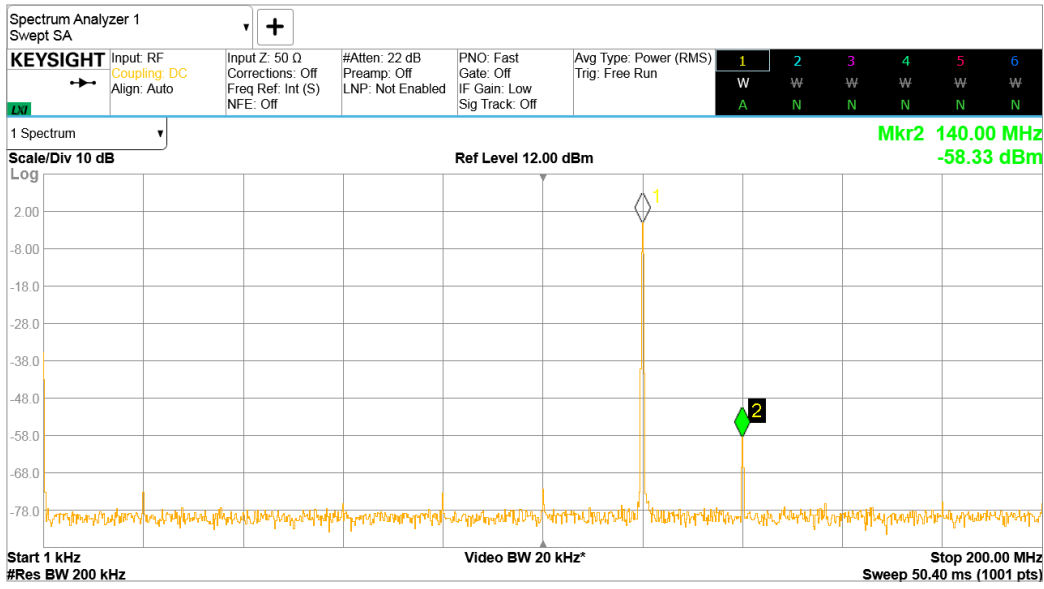


Figure 4. Single-tone spectrum @  $f_{out} = 120$  MHz

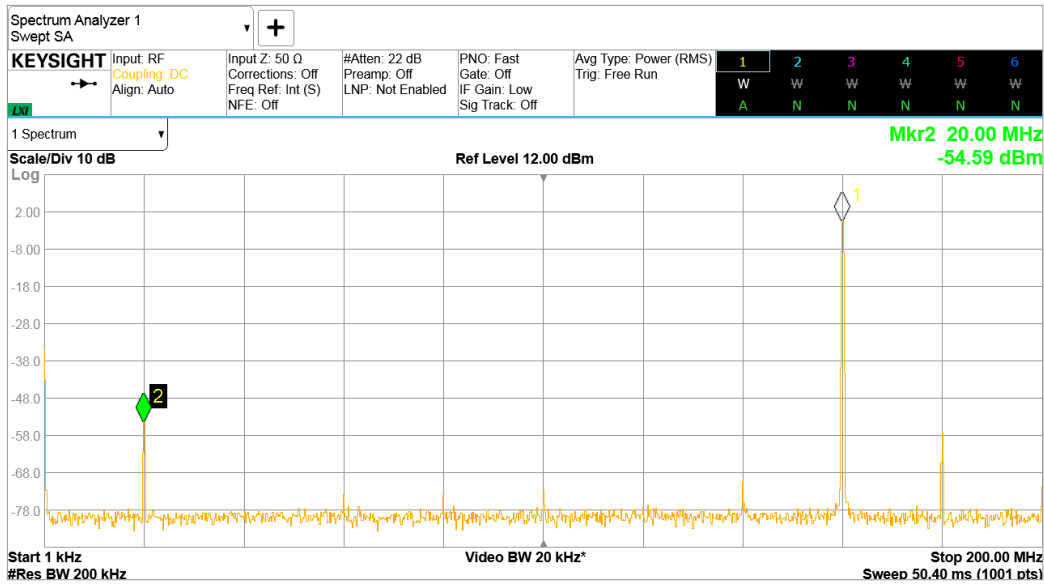


Figure 5. Single-tone spectrum @  $f_{out} = 160$  MHz

## System Specifications

### Environmental specifications (PXI Express)

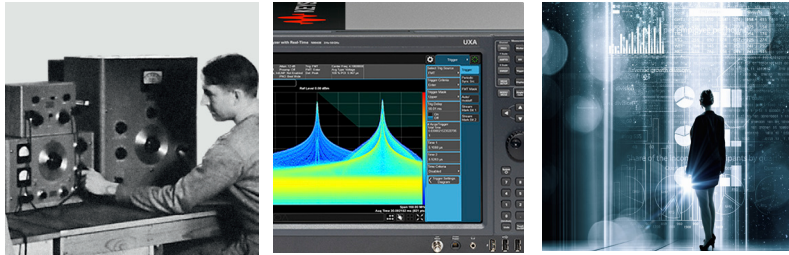
Parameter	M3201A-CH2			M3201A-CH4			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
<b>System bus</b>								
Slots	1			1			Slot	PXI Express (CompactPCI Express compatible)
PCI Express type	Gen 1		Gen 2	Gen 1		Gen 2	–	Automatic gen negotiation, chassis dependent
PCI Express link	1		4	1		4	Lanes	Automatic lane negotiation, chassis dependent
PCI Express speed	400		1600	400		1600	MBytes/s	Depends on # of lanes, chassis, congestion, and more
Sustainable throughput	200		800	200		800	MPoints/s	Depends on # of lanes, chassis, congestion, and more
<b>Power and temperature</b>								
3.3 V PXIe power supply	1.5			1.5			A	~ 5 W
12 V PXIe power supply	2			2			A	~ 24 W

<b>Environmental <sup>1</sup></b>	
Temperature range	Operating Non-operating
	0 to +55°C (10,000 feet) -40 to +70 °C (up to 15,000 feet)
Max operative altitude	4000 m (10,000 feet)
Operating Humidity range (%RH)	10 to 95% at 40 °C
Non-operating Humidity range (%RH): 5 to 95	5 to 95%
Calibration interval	1 year
EMC	Complies with European EMC Directive – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A This ISM device is in compliance with Canadian ICES-001 Cet appareil ISM est conforme à la norme NMB-001 du Canada. This ISM device is in compliance with Australian and New Zealand RCM This ISM device is in compliance with South Korea EMC KCC

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

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