32-Channel 14-Bit DAC with High-Speed 3-Wire Serial Interface

AD5532HS*

FEATURES

High Integration: 32-Channel DAC in 12 × 12 mm² LFBGA
Guaranteed Monotonic
DSP-/Microcontroller-Compatible Serial Interface
Channel Update Rate 1.1 MHz
Output Impedance 0.5 Ω
Selectable Output Voltage 0 V to 5 V or –2.5 V to +2.5 V
Asynchronous $\overline{\text{RESET}}$ Facility
Temperature Range –40°C to +85°C

APPLICATIONS

Optical Networks
Level Setting
Instrumentation
Automatic Test Equipment
Industrial Control Systems
Data Acquisition
Low Cost I/O

GENERAL DESCRIPTION

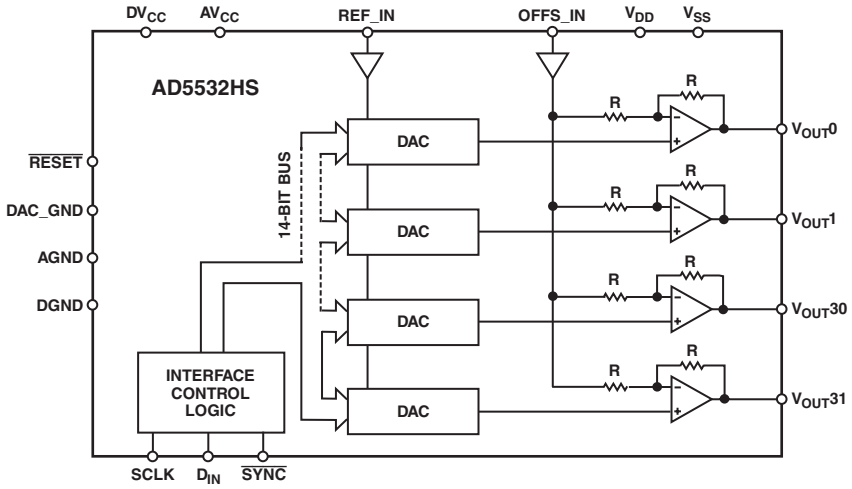
The AD5532HS is a 32-channel voltage-output 14-bit DAC with a high-speed serial interface. The selected DAC register is written to via the 3-wire interface. The serial interface operates at clock rates up to 30 MHz and is compatible with DSP and microcontroller interface standards. The output voltage range is 0 V to 5 V or –2.5 V to +2.5 V and is determined by the offset voltage at the OFFS_IN pin. It is restricted to a range from V_{SS} + 2 V to V_{DD} – 2 V because of the headroom of the output amplifier.

The device is operated with AV_{CC} = 5 V ± 5%, DV_{CC} = 2.7 V to 5.25 V, V_{SS} = –4.75 V to –12 V and V_{DD} = +4.75 V to +12 V and requires a stable 2.5 V reference on REF_IN.

PRODUCT HIGHLIGHTS

1. 32 14-bit DACs in one package, guaranteed monotonic.
2. The AD5532HS is available in a 74-ball LFBGA package with a body size of 12 mm by 12 mm.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No. 5,969,657; other patents pending.

REV. 0

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AD5532HS–SPECIFICATIONS

(V_{DD} = +4.75 V to +12 V, V_{SS} = –4.75 V to –12 V; AV_{CC} = 4.75 V to 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DAC_GND = 0 V; REF_IN = 2.5 V; OFFS_IN = 0 V; All outputs unloaded. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	A Version[2] Min	Typ	Max	Unit	Conditions/Comments
DAC DC PERFORMANCE					
Resolution		14		Bits	
Integral Nonlinearity (INL)	–0.39	±0.1	+0.39	% of FSR	See TPC 7
Differential Nonlinearity (DNL)	–1	±0.5	+1	LSB	Monotonic
Offset Error	–10	+15	+50	mV	See TPC 8
Full-Scale Error	–1	–0.3	+0.5	% of FSR	See TPC 9
VOLTAGE REFERENCE REF_IN					
Input Voltage Range[3]	2.375	2.5	2.625	V	
Input Current		±0.001	±1	µA	
ANALOG INPUT OFFS_IN					
Input Voltage Range[3, 4]	0		V_{DD} – 1.5	V	
Input Current		±0.1	±1	µA	
ANALOG OUTPUTS ($V_{OUT}0$–$V_{OUT}31$)					
Output Temperature Coefficient[3, 5]		20		ppm/°C	
DC Output Impedance[3]		0.5		Ω	
Output Range[4]					
OFFS_IN = 0		0 – 2REF_IN		V	
OFFS_IN = REF_IN		–REF_IN to +REF_IN		V	
Resistive Load[3]	5			kΩ	
Capacitive Load[3]			100	pF	
Short-Circuit Current[3]		7		mA	
DC Power-Supply Rejection Ratio[3]		–70		dB	V_{DD} = +10 V ± 5%
		–70		dB	V_{SS} = –10 V ± 5%
DC Crosstalk[3]			120	µV	
DIGITAL INPUTS[3]					
Input Current		±5	±10	µA	
Input Low Voltage			0.8	V	DV_{CC} = 5 V ± 5%
			0.4	V	DV_{CC} = 3 V ± 10%
Input High Voltage	2.4			V	DV_{CC} = 5 V ± 5%
	2.0			V	DV_{CC} = 3 V ± 10%
Input Hysteresis (SCLK and $\overline{SYNC}$ Only)		200		mV	
Input Capacitance			10	pF	
POWER SUPPLY VOLTAGES					
V_{DD}	+4.75		+12	V	
V_{SS}	–4.75		–12	V	
AV_{CC}	4.75		5.25	V	
DV_{CC}	2.7		5.25	V	
POWER SUPPLY CURRENTS[6]					
I_{DD}		9	12	mA	All Channels Full Scale
I_{SS}		9	12	mA	All Channels Full Scale
AI_{CC}		6.5	10	mA	
DI_{CC}		0.1	0.5	mA	V_{IH} = DV_{CC} and V_{IL} = DGND
POWER DISSIPATION[6]		123		mW	V_{DD} = +5 V, V_{SS} = –5 V

NOTES
[1]See Terminology
[2]A Version: Industrial temperature range –40°C to +85°C; typical at 25°C.
[3]Guaranteed by design and characterization, not production tested.
[4]Output range is restricted from V_{SS} + 2 V to V_{DD} – 2 V.
[5]AD780 as reference for the AD5532HS.
[6]Outputs unloaded.

Specifications subject to change without notice.

AC CHARACTERISTICS (V_{DD} = +4.75 V to +12 V, V_{SS} = –4.75 V to –12 V; AV_{CC} = 4.75 V to 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DAC_GND = 0 V; REF_IN = 2.5 V; All outputs unloaded. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1, 2]	A Version[3]	Unit	Conditions/Comments
Output Voltage Settling Time[4]	10	µs max	100 pF, 5 kΩ Load; Full-Scale Change
Slew Rate	0.85	V/µs typ	
Digital-to-Analog Glitch Impulse	1	nV-s typ	1 LSB Change around Major Carry
Digital Crosstalk	5	nV-s typ	
Analog Crosstalk	1	nV-s typ	
Digital Feedthrough	0.2	nV-s typ	
Output Noise Spectral Density @ 1 kHz	170	nV/√Hz typ	

NOTES
[1]See Terminology
[2]Guaranteed by design and characterization, not production tested
[3]B Version: Industrial temperature range –40°C to +85°C.
[4]Timed from the end of a write sequence.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = +4.75 V to +12 V, V_{SS} = –4.75 V to –12 V; AV_{CC} = 4.75 V to 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DAC_GND = 0 V; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX} (A Version)	Unit	Conditions/Comments
f_{UPDATE}	1.1	MHz max	Channel Update Rate
f_{CLKIN}	30	MHz max	SCLK Frequency
t_1	13	ns min	SCLK High Pulsewidth
t_2	13	ns min	SCLK Low Pulsewidth
t_3	15	ns min	$\overline{SYNC}$ Falling Edge to SCLK Falling Edge Setup Time
t_4	50	ns min	$\overline{SYNC}$ Low Time
t_5	10	ns min	$\overline{SYNC}$ High Time
t_6	10	ns min	D_{IN} Setup Time
t_7	5	ns min	D_{IN} Hold Time
t_8	280	ns min	19th SCLK Falling Edge to $\overline{SYNC}$ Falling Edge for Next Write
t_9	20	ns min	$\overline{RESET}$ Pulsewidth

NOTES
[1]See Timing Diagrams in Figure 1.
[2]Guaranteed by design and characterization, not production tested.
[3]All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

Specifications subject to change without notice.

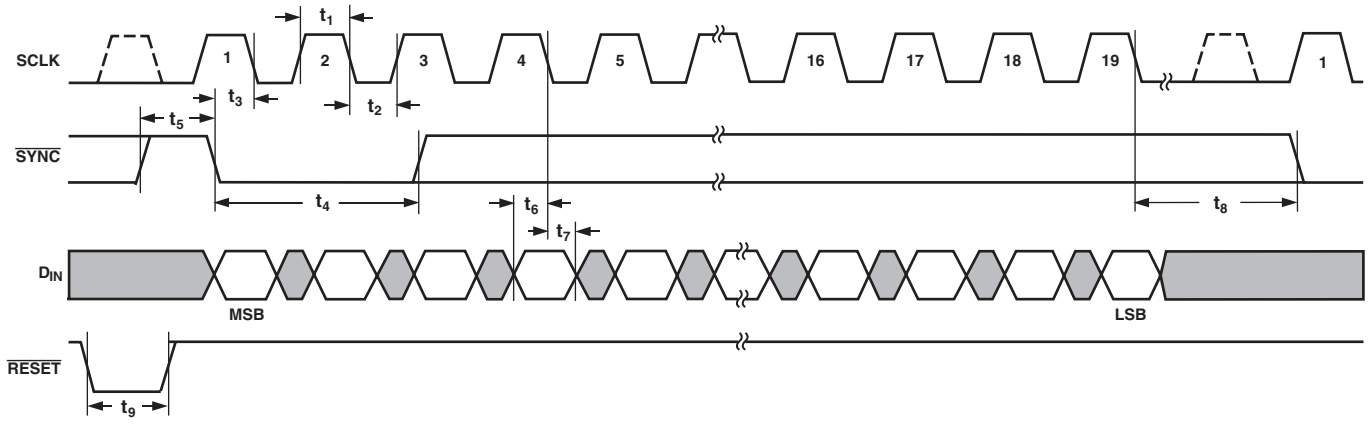


Figure 1. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]
(T_A = 25°C unless otherwise noted)

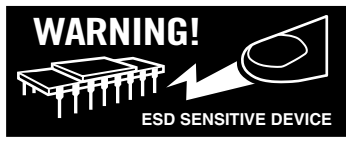
V_{DD} to AGND . . . . . –0.3 V to +17 V
V_{SS} to AGND . . . . . +0.3 V to –17 V
AV_{CC} to AGND, DAC_GND . . . . . –0.3 V to +7 V
DV_{CC} to DGND . . . . . –0.3 V to +7 V
Digital Inputs to DGND . . . . . –0.3 V to DV_{CC} + 0.3 V
REF_IN to AGND, DAC_GND . . . . . –0.3 V to +7 V
$V_{OUT}0$–$V_{OUT}31$ to AGND . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
$V_{OUT}0$–$V_{OUT}31$ to V_{SS} . . . . . –0.3 V to +24 V
OFFS_IN to AGND . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Operating Temperature Range
Industrial . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature (T_J max) . . . . . 150°C
74-Lead LFBGA Package, θ_{JA} Thermal Impedance . . . 41°C/W
Reflow Soldering
Peak Temperature . . . . . 220°C
Time at Peak Temperature . . . . . 10 sec to 40 sec
Max Power Dissipation at T_A = 70°C,
Outputs Loaded . . . . . 550 mW[3]
(for T_A > 70°C, derate at 26 mW for each °C over 70°C)

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Transient currents of up to 100 mA will not cause SCR latch-up.
[3] This limit includes load power and applies only when there is a resistive load on V_{OUT} outputs.

ORDERING GUIDE

Model	Function	Output Voltage Span	Package Description	Package Option
AD5532HSABC	32 DACs	5 V	74-Ball LFBGA	BC-74

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5532HS features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



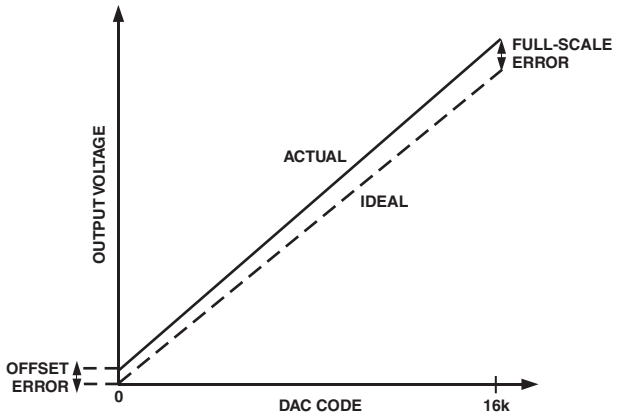
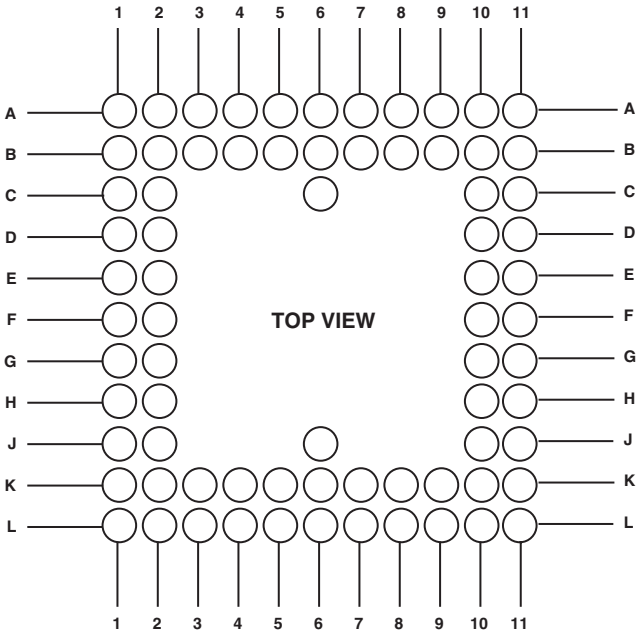


Figure 2. DAC Transfer Function (OFFS_IN = 0)

PIN CONFIGURATION



AD5532HS 74-Ball (LFBGA) Configuration

LFBGA Number	Ball Name	LFBGA Number	Ball Name	LFBGA Number	Ball Name
A1	N/C	C10	AVCC1	J10	VO9
A2	N/C	C11	N/C	J11	VO11
A3	N/C	D1	VO20	K1	VO17
A4	N/C	D2	DAC_GND2	K2	VO15
A5	$\overline{\text{SYNC}}$	D10	AVCC2	K3	VO27
A6	DVCC	D11	N/C	K4	VSS3
A7	SCLK	E1	VO26	K5	VSS1
A8	N/C	E2	VO14	K6	VSS4
A9	N/C	E10	AGND1	K7	VDD2
A10	$\overline{\text{RESET}}$	E11	OFFS_IN	K8	VO2
A11	N/C	F1	VO25	K9	VO10
B1	VO16	F2	VO21	K10	VO13
B2	N/C	F10	AGND2	K11	VO12
B3	N/C	F11	VO6	L1	N/C
B4	N/C	G1	VO24	L2	VO28
B5	N/C	G2	VO8	L3	VO29
B6	DGND	G10	VO5	L4	VO30
B7	DIN	G11	VO3	L5	VDD3
B8	DGND	H1	VO23	L6	VDD1
B9	N/C	H2	N/C	L7	VDD4
B10	N/C	H10	VO4	L8	VO31
B11	REF_IN	H11	VO7	L9	VO0
C1	VO18	J1	VO22	L10	VO1
C2	DAC_GND1	J2	VO19	L11	N/C
C6	N/C	J6	VSS2		

PIN FUNCTION DESCRIPTIONS

Pin	Function
AGND (1–2)	Analog GND Pins.
AV_{CC} (1–2)	Analog Supply Pins. Voltage range from 4.75 V to 5.25 V.
V_{DD} (1–4)	V_{DD} Supply Pins. Voltage range from 8 V to 12 V.
V_{SS} (1–4)	V_{SS} Supply Pins. Voltage range from –4.75 V to –12 V.
DGND	Digital GND Pins.
DV_{CC}	Digital Supply Pins. Voltage range from 2.7 V to 5.25 V.
DAC_GND (1–2)	Reference GND Supply for All the DACs.
REF_IN	Reference Voltage for Channels 0–31.
$V_{OUT}0$–$V_{OUT}31$	Analog Output Voltages from the 32 Channels.
$\overline{SYNC}$	Active Low Input. This is the Frame Synchronization signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred in on the falling edge of SCLK.
SCLK*	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 30 MHz.
D_{IN}*	Serial Data Input. Data must be valid on the falling edge of SCLK.
OFFS_IN	Offset Input. The user can connect this to GND or REF_IN to determine the output span.
$\overline{RESET}$*	Active Low Input. This pin can also be used to reset the complete device to its power-on-reset conditions.

*Internal pull-up device on this logic input. Therefore, it can be left floating and will default to a logic high condition.

TERMINOLOGY

Integral Nonlinearity (INL)
A measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is expressed as a percentage of full-scale range.

Differential Nonlinearity (DNL)
The difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity.

Offset Error
A measure of the error present at the device output with all 0s loaded to the DAC. It includes the offset of the DAC and the output amplifier. It is expressed in mV.

Full-Scale Error
A measure of the output error with all 1s loaded to the DAC. Ideally the output should be 2 REF_IN if OFFS_IN = 0. It is expressed as a percentage of full-scale range.

DC Power-Supply Rejection Ratio (PSRR)
A measure of the change in analog output for a change in supply voltage (V_{DD} and V_{SS}). It is expressed in dB. V_{DD} and V_{SS} are varied ±5%.

DC Crosstalk
The dc change in the output level of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) and output change of all other DACs. It is expressed in µV.

Output Temperature Coefficient
A measure of the change in analog output with changes in temperature. It is expressed in ppm/°C.

Output Voltage Settling Time
The time taken from when the last data bit is clocked into the DAC until the output has settled to within ±0.5 LSB of its final value.

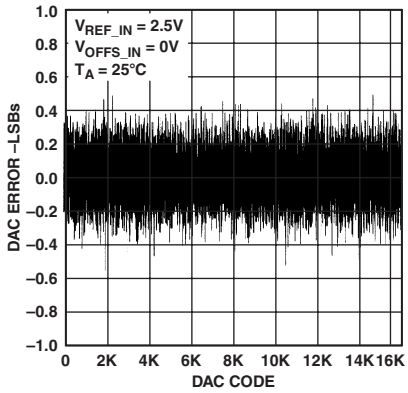
Digital-to-Analog Glitch Impulse
The area of the glitch injected into the analog output when the code in the DAC register changes state. It is specified as the area of the glitch in nV-secs when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

Digital Crosstalk
The glitch impulse transferred to the output of one DAC at midscale while a full-scale code change (all 1s to all 0s and vice versa) is being written to another DAC. It is expressed in nV-secs.

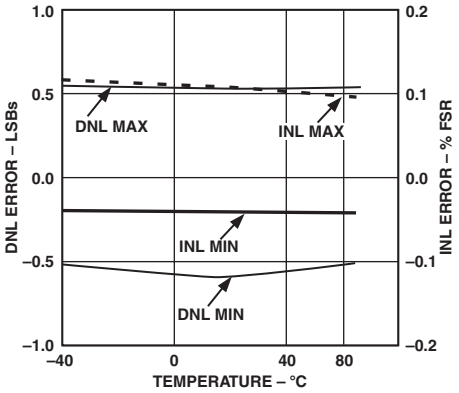
Analog Crosstalk
The area of the glitch transferred to the output (V_{OUT}) of one DAC due to a full-scale change in the output (V_{OUT}) of another DAC. The area of the glitch is expressed in nV-secs.

Digital Feedthrough
A measure of the impulse injected into the analog outputs from the digital control inputs when the part is not being written to, i.e., $\overline{SYNC}$ is high. It is specified in nV-secs and measured with a worst-case change on the digital input pins, e.g., from all 0s to all 1s and vice versa.

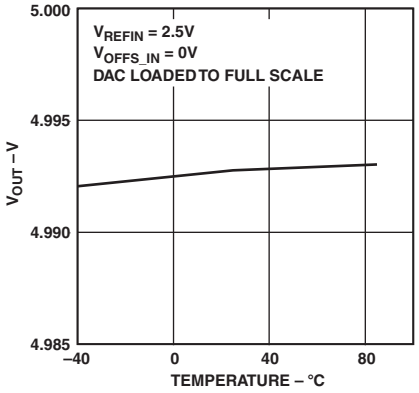
Output Noise Spectral Density
A measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per root Hertz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in nV/$\sqrt{Hz}$.



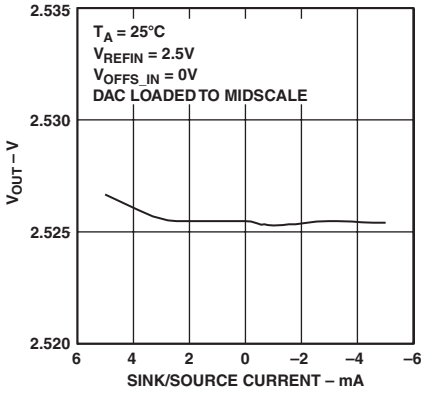
TPC 1. Typical DNL Plot



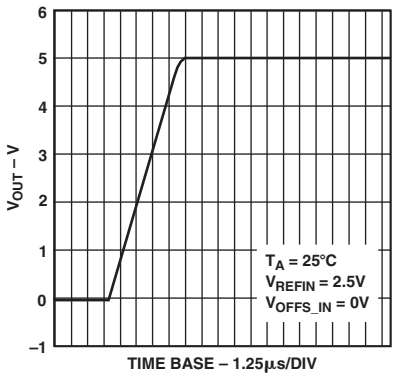
TPC 2. INL Error and DNL Error vs. Temperature



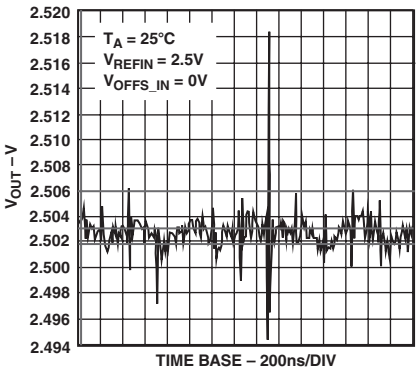
TPC 3. V_{OUT} vs. Temperature



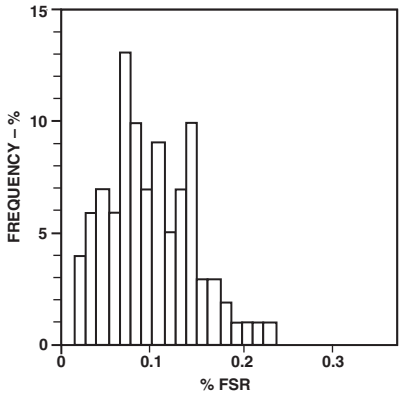
TPC 4. V_{OUT} Source and Sink Capability



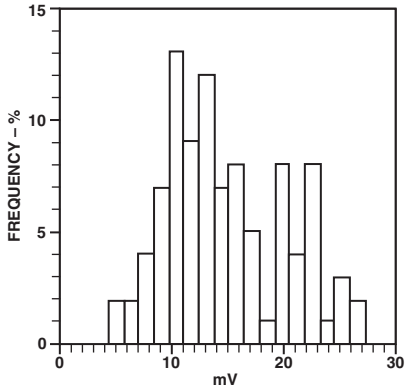
TPC 5. Full-Scale Settling Time



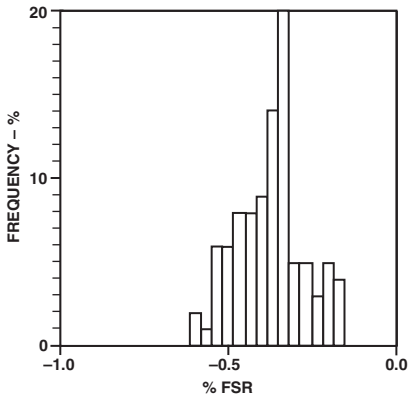
TPC 6. Major Code Transition Glitch Impulse



TPC 7. INL Error Distribution at 25°C



TPC 8. Offset Error Distribution at 25°C



TPC 9. Full-Scale Error Distribution at 25°C

FUNCTIONAL DESCRIPTION

The AD5532HS consists of 32 DACs in a single package. A 14-bit digital word is loaded into one of the 32 DAC registers via the serial interface. This is then converted (with gain and offset) into an analog output voltage ($V_{OUT}0$–$V_{OUT}31$).

To update a DAC's output voltage, the required DAC is addressed via the serial port. When the 5-bit DAC address and 14-bit DAC data have been loaded the selected DAC converts the code.

On power-on, all the DACs are loaded with zeros.

Digital-to-Analog Section

The architecture of each DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the REF_IN pin provides the reference voltage for the corresponding DAC. Since the input coding to the DAC is straight binary, the ideal DAC output voltage is given by:

$$V_{DAC} = \frac{V_{REF_IN} \times D}{2^{14}}$$

where D = decimal equivalent of the binary code that is loaded to the DAC register i.e., 0–16,383.

Output Buffer Stage—Gain and Offset

The function of the output buffer stage is to translate the 0 V–2.5 V output of the DAC to a wider range. This is done by gaining up the DAC output by two and offsetting the voltage by the voltage on OFFS_IN pin.

$$V_{OUT} = (2 \times V_{DAC}) - V_{OFFS_IN}$$

V_{DAC} is the output of the DAC.
V_{OFFS_IN} is the voltage at the OFFS_IN pin.

Table I shows how the output range of V_{OUT} relates to the offset voltage supplied by the user.

Table I. Sample Output Voltage Ranges

V_{OFFS_IN} (V)	V_{DAC} (V)	V_{OUT} (V)
0	0 to 2.5	0 to 5
2.5	0 to 2.5	–2.5 to +2.5

V_{OUT} is limited only by the headroom of the output amplifiers. V_{OUT} must be within maximum ratings.

Reset Function

The reset function on the AD5532HS can be used to reset all nodes on the device to their power-on-reset condition. All the DACs are loaded with 0s and all registers are cleared. The reset function is implemented by taking the $\overline{\text{RESET}}$ pin low.

SERIAL INTERFACE

The serial interface is controlled by three pins as follows:

$\overline{\text{SYNC}}$: This pin is the Frame Synchronization pin for the serial interface.

SCLK: This pin is the Serial Clock Input. It operates at clock speeds up to 30 MHz.

D_{IN}: This pin is the Serial Data Input. Data must be valid on the falling edge of SCLK.

To update a single DAC channel a 19-bit data-word is written into the AD5532HS. See Table II.

Table II. Serial Data Format

MSB					LSB
A4	A3	A2	A1	A0	DB13–DB0

A4–A0 Bits

Used to address any one of the 32 channels (A4 = MSB of address, A0 = LSB).

DB13–DB0 Bits

These are used to write a 14-bit word into the addressed DAC register.

Figure 1 shows the timing diagram for a serial write to the AD5532HS. The serial interface works with both a continuous and a noncontinuous serial clock. The first falling edge of $\overline{\text{SYNC}}$ resets a counter that counts the number of serial clocks to ensure the correct number of bits are shifted in and out of the serial shift registers. Any further edges on $\overline{\text{SYNC}}$ are ignored until the correct number of bits are shifted in or out. Once 19 bits have been shifted in or out, the SCLK is ignored. In order for another serial transfer to take place, the counter must be reset by the falling edge of $\overline{\text{SYNC}}$. The user must allow 280 ns (min) between successive writes (refer to Timing Specifications).

MICROPROCESSOR INTERFACING

AD5532HS-to-ADSP-21xx Interface

The ADSP-21xx family of DSPs are easily interfaced to the AD5532HS without the need for extra logic.

A data transfer is initiated by writing a word to the Tx register after the SPORT has been enabled. In a write sequence, data is clocked out on each rising edge of the DSP's serial clock and clocked into the AD5532HS on the falling edge of its SCLK. The easiest way to provide the 19-bit data-word required by the AD5532HS, is to transmit two 10-bit data-words from the ADSP-21xx. Ensure that the data is positioned correctly in the TX register so that the first 19 bits transmitted contain valid data. The SPORT control register should be set up as follows:

TFSW = 1, Alternate Framing
INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
ISCLK = 1, Internal Serial Clock
TFSR = 1, Frame Every Word
ITFS = 1, Internal Framing Signal
SLEN = 1001, 10-Bit Data Word

Figure 3 shows the connection diagram.

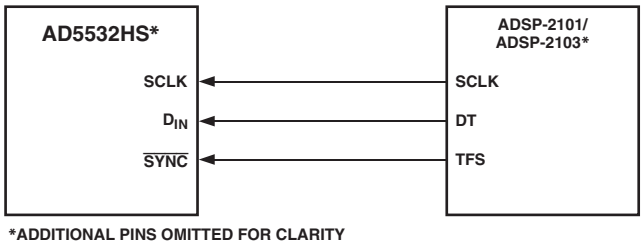


Figure 3. AD5532HS-to-ADSP-2101/ADSP-2103 Interface

AD5532HS-to-MC68HC11 Interface

The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 0 and the Clock Phase Bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see *68HC11 User Manual*. SCK of the 68HC11 drives the SCLK of the AD5532HS and the MOSI output drives the serial data line (D_{IN}) of the AD5532HS. The $\overline{SYNC}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5532HS, the $\overline{SYNC}$ line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. The 68HC11 transfers only eight bits of data during each serial transfer operation; therefore, three consecutive write operations are necessary to transmit 19 bits of data. Data is transmitted MSB first. It is important to left-justify the data in the SPDR register so that the first 19 bits transmitted contain valid data. PC7 must be pulled low to start a transfer. It is taken high and pulled low again before any further write cycles can take place. See Figure 4.

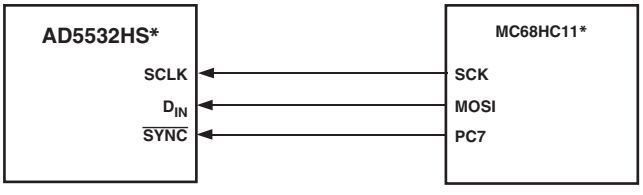


Figure 4. AD5532HS-to-MC68HC11 Interface

AD5532HS-to-PIC16C6x/7x Interface

The PIC16C6x/7x Synchronous Serial Port (SSP) is configured as an SPI Master with the Clock Polarity bit = 0. This is done by writing to the Synchronous Serial Port Control Register (SSPCON). See user *PIC16/17 Microcontroller User Manual*. In this example I/O port RA1 is being used to pulse $\overline{SYNC}$ and enable the serial port of the AD5532HS. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, three consecutive write operations are necessary to transmit 19 bits of data. Data is transmitted MSB first. It is important to left-justify the data in the SPDR register so that the first 19 bits transmitted contain valid data. RA1 must be pulled low to start a transfer. It is taken high and pulled low again before any further write cycles can take place. Figure 5 shows the connection diagram.

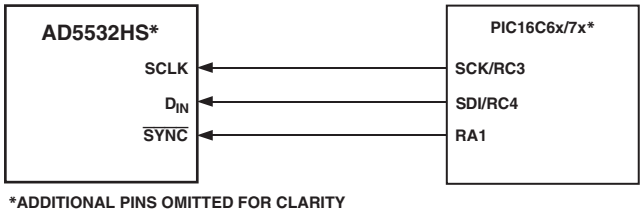


Figure 5. AD5532HS-to-PIC16C6x/7x Interface

AD5532HS-to-8051 Interface

The AD5532HS requires a clock synchronized to the serial data. The 8051 serial interface must therefore be operated in Mode 0. In this mode serial data exits the 8051 through RxD and a shift clock is output on TxD. The $\overline{SYNC}$ signal is derived from a port line (P1.1). Figure 6 shows how the 8051 is connected to the AD5532HS. Because the AD5532HS shifts data out on the rising edge of the shift clock and latches data in on the falling edge, the shift clock must be inverted. Note also that the AD5532HS requires its data with the MSB first. Since the 8051 outputs the LSB first, the transmit routine must take this into account.

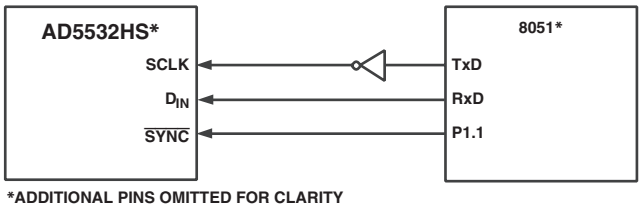


Figure 6. AD5532HS-to-8051 Interface

APPLICATION CIRCUITS

AD5532HS in an Optical Network Control Loop

The AD5532HS can be used in optical network applications that require a large number of DACs to perform a control and measurement function. In the circuit shown in Figure 7, the 0 V–5 V outputs of the AD5532HS are amplified to a range of 0 V–180 V and then used to control actuators that determine the position of MEMS mirrors in an optical switch. The exact position of each mirror is measured using sensors. The sensor readings are muxed using four dual 4-channel matrix switches (ADG739) and fed back to an 8-channel 14-bit ADC (AD7856).

The control loop is driven by an ADSP-21065L, a 32-bit SHARC® DSP with an SPI-compatible SPORT interface. It writes data to the DAC, controls the multiplexor, and reads data from the ADC via a 3-wire serial interface.

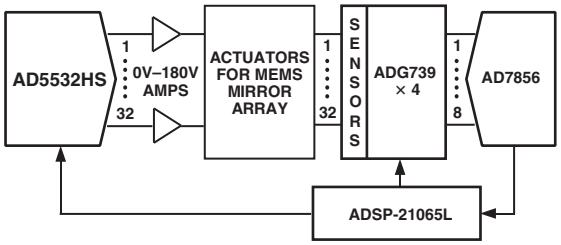


Figure 7. AD5532HS and DSP Control an Optical Switch

Alternatively, the AD5532HS can be driven by an ADMC401 Motor-Controller as shown in the control-loop in Figure 8. The DAC outputs are fed into eight AD8534 quad transconductance amps to generate currents for voice-coil actuators that determine the position of the mirrors. The exact position of each mirror is measured and the readings are muxed into the on-chip 8-channel ADC of the ADMC401.

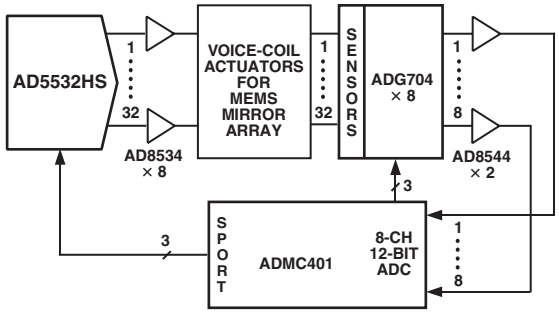


Figure 8. AD5532HS and ADMC401 Control an Optical Switch

AD5532HS in a Typical ATE System

The AD5532HS is ideally suited for use in Automatic Test Equipment. Several DACs are required to control pin drivers, comparators, active loads, and signal timing. Traditionally, sample-and-hold devices were used in this application.

The AD5532HS has several advantages: no refreshing is required, there is no droop, pedestal error is eliminated, and there is no need for extra filtering to remove glitches. A higher level of integration is achieved in a smaller area (see Figure 9).

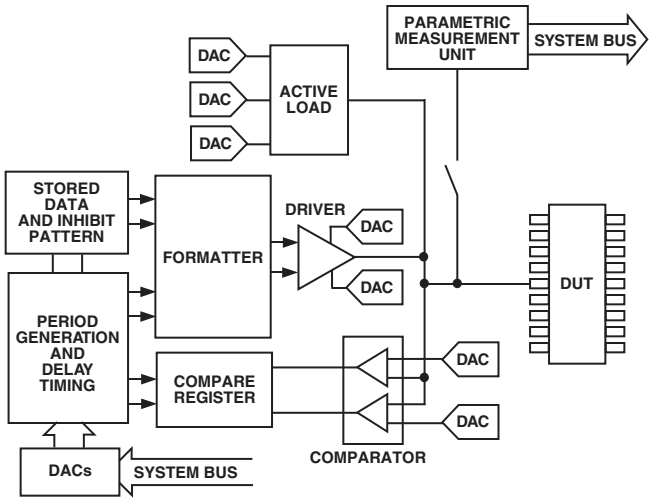


Figure 9. AD5532HS in an ATE System

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5532HS is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the AD5532HS is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins (V_{SS}, V_{DD}, AV_{CC}), it is recommended to tie those pins together. The AD5532HS should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

The power supply lines of the AD5532HS should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the D_{IN} and SCLK lines will help reduce crosstalk between them (not required on a multilayer board as there will be a separate ground plane, but separating the lines will help). It is essential to minimize noise on REF_IN.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

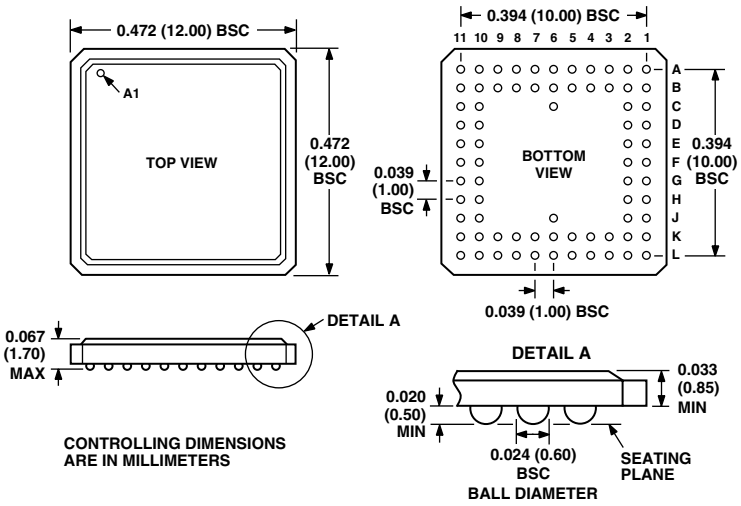
As is the case for all thin packages, care must be taken to avoid flexing the package and to avoid a point load on the surface of the package during the assembly process.

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OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

74-Ball LFBGA
(BC-74)



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