TMS320F280049, TMS320F280049C
TMS320F280048, TMS320F280048C, TMS320F280045
TMS320F280041, TMS320F280041C, TMS320F280040, TMS320F280040C
SPRS945D – JANUARY 2017 – REVISED OCTOBER 2018

# TMS320F28004x Piccolo™ Microcontrollers

## 1 Device Overview

### 1.1 Features

- TMS320C28x 32-Bit CPU
  - 100 MHz
  - IEEE 754 Single-Precision Floating-Point Unit (FPU)
  - Trigonometric Math Unit (TMU)
    - 3×-Cycle to 4×-Cycle Improvement for Common Trigonometric Functions Versus Software Libraries
    - 13-Cycle Park Transform
  - Viterbi/Complex Math Unit (VCU-I)
  - Ten Hardware Breakpoints
- Programmable Control Law Accelerator (CLA)
  - 100 MHz
  - IEEE 754 Single-Precision Floating-Point Instructions
  - Executes Code Independently of Main CPU
- On-Chip Memory
  - 256KB (128KW) of Flash (ECC-Protected) Across Two Independent Banks
  - 100KB (50KW) of RAM (ECC-Protected or Parity-Protected)
  - Dual-Zone Security Supporting Third-Party Development
  - Unique Identification Number
- Clock and System Control
  - Two Internal Zero-Pin 10-MHz Oscillators
  - On-Chip Crystal Oscillator and External Clock Input
  - Windowed Watchdog Timer Module
  - Missing Clock Detection Circuitry
- 1.2-V Core, 3.3-V I/O Design
  - Internal VREG or DC-DC for 1.2-V Generation Allows for Single-Supply Designs
  - Brownout Reset (BOR) Circuit
- System Peripherals
  - 6-Channel Direct Memory Access (DMA) Controller
  - 40 Individually Programmable Multiplexed General-Purpose Input/Output (GPIO) Pins
  - 21 Digital Inputs on Analog Pins
  - Enhanced Peripheral Interrupt Expansion (ePIE) Module
  - Multiple Low-Power Mode (LPM) Support With External Wakeup
  - Embedded Real-Time Analysis and Diagnostic (ERAD)
- Communications Peripherals
  - One Power Management Bus (PMBus) Interface
  - One Inter-Integrated Circuit (I2C) Interface (Pin-Bootable)
  - Two Controller Area Network (CAN) Bus Ports (Pin-Bootable)
  - Two Serial Peripheral Interface (SPI) Ports (Pin-Bootable)
  - Two Serial Communication Interfaces (SCIs) (Pin-Bootable)
  - One Local Interconnect Network (LIN)
  - One Fast Serial Interface (FSI) With a Transmitter and Receiver
- Analog System
  - Three 3.45-MSPS, 12-Bit Analog-to-Digital Converters (ADCs)
    - Up to 21 External Channels
    - Four Integrated Post-Processing Blocks (PPBs) per ADC
  - Seven Windowed Comparators (CMPSS) With 12-Bit Reference Digital-to-Analog Converters (DACs)
    - Digital Glitch Filters
  - Two 12-Bit Buffered DAC Outputs
  - Seven Programmable Gain Amplifiers (PGAs)
    - Programmable Gain Settings: 3, 6, 12, 24
    - Programmable Output Filtering
- Enhanced Control Peripherals
  - 16 ePWM Channels With High-Resolution Capability (150-ps Resolution)
    - Integrated Dead-Band Support With High Resolution
    - Integrated Hardware Trip Zones (TZs)
  - Seven Enhanced Capture (eCAP) Modules
    - High-Resolution Capture (HRCAP) Available on Two Modules
  - Two Enhanced Quadrature Encoder Pulse (eQEP) Modules With Support for CW/CCW Operation Modes
  - Four Sigma-Delta Filter Module (SDFM) Input Channels (Two Parallel Filters per Channel)
    - Standard SDFM Data Filtering
    - Comparator Filter for Fast Action for Overvalue or Undervalue Condition
- Configurable Logic Block (CLB)
  - Augments Existing Peripheral Capability
  - Supports Position Manager Solutions

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

- InstaSPIN-FOC™
  - Sensorless Field-oriented Control (FOC) With FAST™ Software Encoder
  - Library in On-chip ROM Memory
- Package Options:
  - 100-Pin Low-Profile Quad Flatpack (LQFP) [PZ Suffix]
  - 64-Pin LQFP [PM Suffix]
  - 56-Pin Very Thin Quad Flatpack No-Lead (VQFN) [RSH Suffix]
- Temperature Options:
  - S: –40°C to 125°C Junction
  - Q: –40ºC to 125ºC Free-Air (AEC Q100 Qualification for Automotive Applications)

## 1.2 Applications

- Appliances
- Building Automation
- Electric Vehicle/Hybrid Electric Vehicle (EV/HEV) Powertrain
- Factory Automation
- Grid Infrastructure
- Industrial Transport
- Medical, Healthcare, and Fitness
- Motor Drives
- Power Delivery
- Telecom Infrastructure
- Test and Measurement


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## 1.3 Description

C2000™ 32-bit microcontrollers are optimized for processing, sensing, and actuation to improve closed-loop performance in real-time control applications such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; motor control; and sensing and signal processing. The C2000 line includes the Delfino™ Premium Performance family and the Piccolo™ Entry Performance family.

The Piccolo™ TMS320F28004x (F28004x) is a powerful 32-bit floating-point microcontroller unit (MCU) that lets designers incorporate crucial control peripherals, differentiated analog, and nonvolatile memory on a single device.

The real-time control subsystem is based on TI's 32-bit C28x CPU, which provides 100 MHz of signal processing performance. The C28x CPU is further boosted by the new TMU extended instruction set, which enables fast execution of algorithms with trigonometric operations commonly found in transforms and torque loop calculations; and the VCU-I extended instruction set, which reduces the latency for complex math operations commonly found in encoded applications.

The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has its own dedicated memory resources and it can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching.

The F28004x supports up to 256KB (128KW) of flash memory divided into two 128KB (64KW) banks, which enables programming and execution in parallel. Up to 100KB (50KW) of on-chip SRAM is also available in blocks of 4KB (2KW) and 16KB (8KW) for efficient system partitioning. Flash ECC, SRAM ECC/parity, and dual-zone security are also supported.

High-performance analog blocks are integrated on the F28004x MCU to further enable system consolidation. Three separate 12-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. Seven PGAs on the analog front end enable on-chip voltage scaling before conversion. Seven analog comparator modules provide continuous monitoring of input voltage levels for trip conditions.

The TMS320C2000™ devices contain industry-leading control peripherals with frequency-independent ePWM/HRPWM and eCAP allow for a best-in-class level of control to the system. The built-in 4-channel SDFM allows for seamless integration of an oversampling sigma-delta modulator across an isolation barrier.

Connectivity is supported through various industry-standard communication ports (such as SPI, SCI, I2C, LIN, and CAN) and offers multiple muxing options for optimal signal placement in a variety of applications. New to the C2000™ platform is the fully compliant PMBus. Additionally, in an industry first, the FSI enables high-speed, robust communication to complement the rich set of peripherals that are embedded in the device.

A specially enabled device variant, TMS320F28004xC, allows access to the Configurable Logic Block (CLB) for additional interfacing features and allows access to the secure ROM, which includes a library to enable InstaSPIN-FOC™. See Device Comparison for more information.

The Embedded Real-Time Analysis and Diagnostic (ERAD) module enhances the debug and system analysis capabilities of the device by providing additional hardware breakpoints and counters for profiling.

To learn more about the C2000 MCUs, visit the C2000 Overview at www.ti.com/c2000.

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**Device Information**(1)

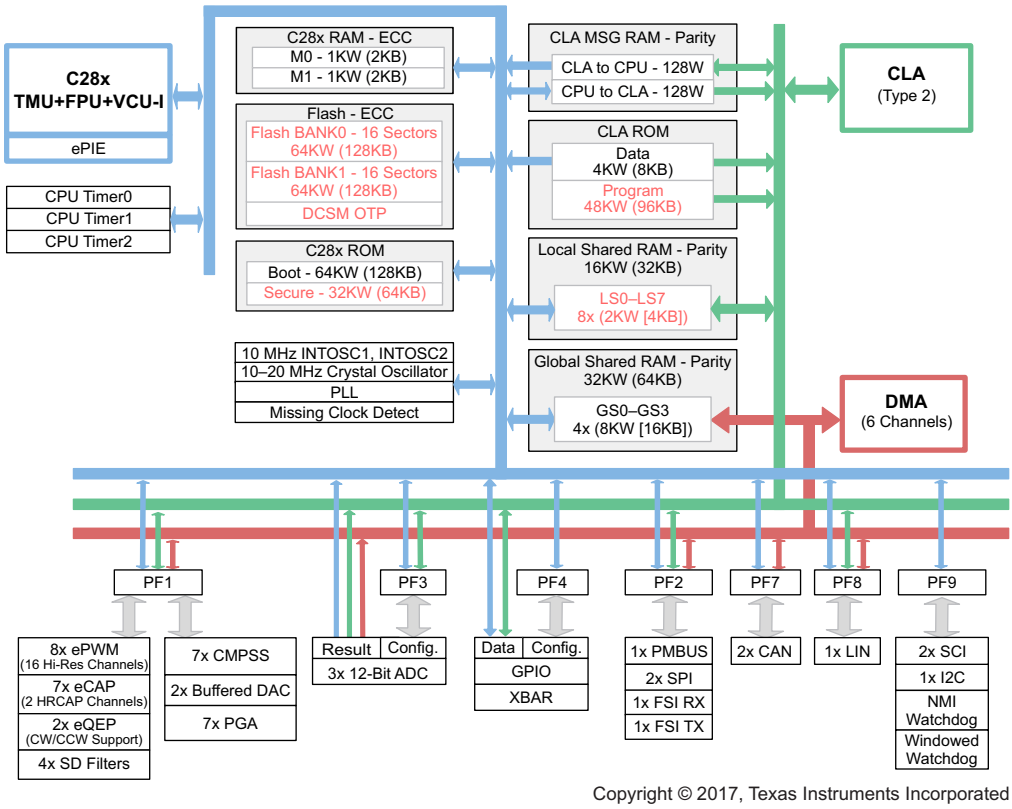
| PART NUMBER | PACKAGE | BODY SIZE |
|---|---|---|
| TMS320F280049PZ | LQFP (100) | 14.0 mm × 14.0 mm |
| TMS320F280049CPZ | LQFP (100) | 14.0 mm × 14.0 mm |
| TMS320F280045PZ | LQFP (100) | 14.0 mm × 14.0 mm |
| TMS320F280041PZ | LQFP (100) | 14.0 mm × 14.0 mm |
| TMS320F280041CPZ | LQFP (100) | 14.0 mm × 14.0 mm |
| TMS320F280049PM | LQFP (64) | 10.0 mm × 10.0 mm |
| TMS320F280049CPM | LQFP (64) | 10.0 mm × 10.0 mm |
| TMS320F280048PM | LQFP (64) | 10.0 mm × 10.0 mm |
| TMS320F280048CPM | LQFP (64) | 10.0 mm × 10.0 mm |
| TMS320F280045PM | LQFP (64) | 10.0 mm × 10.0 mm |
| TMS320F280041PM | LQFP (64) | 10.0 mm × 10.0 mm |
| TMS320F280041CPM | LQFP (64) | 10.0 mm × 10.0 mm |
| TMS320F280040PM | LQFP (64) | 10.0 mm × 10.0 mm |
| TMS320F280040CPM | LQFP (64) | 10.0 mm × 10.0 mm |
| TMS320F280049RSH | VQFN (56) | 7.0 mm × 7.0 mm |
| TMS320F280049CRSH | VQFN (56) | 7.0 mm × 7.0 mm |
| TMS320F280045RSH | VQFN (56) | 7.0 mm × 7.0 mm |
| TMS320F280041RSH | VQFN (56) | 7.0 mm × 7.0 mm |
| TMS320F280041CRSH | VQFN (56) | 7.0 mm × 7.0 mm |

(1) For more information on these devices, see Mechanical, Packaging, and Orderable Information.


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## 1.4 Functional Block Diagram

Figure 1-1 shows the CPU system and associated peripherals.




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**Figure 1-1. Functional Block Diagram**

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## 2 Revision History

**Changes from December 15, 2017 to October 23, 2018 (from C Revision (December 2017) to D Revision)** **Page**

- **Global:** Replaced references to *TMS320C28x Floating Point Unit and Instruction Set Reference Guide* with references to *TMS320C28x Extended Instruction Sets Technical Reference Manual*. ..... 1
- Section 1.3 (Description): Added "C2000™ 32-bit microcontrollers are optimized for processing, sensing, and actuation ..." paragraph and "To learn more about the C2000 MCUs ..." paragraph. ..... 3
- Section 3.1 (Related Products): Updated section. ..... 10
- Table 4-1 (Pin Attributes): Updated DESCRIPTION of GPIO22_VFBSW, GPIO23_VSW, X1, XRSn, and VDDIO_SW. ..... 15
- Table 4-3 (Digital Signals): Updated DESCRIPTION of GPIO22_VFBSW and GPIO23_VSW. ..... 28
- Table 4-4 (Power and Ground): Updated DESCRIPTION of VDDIO_SW. ..... 28
- Table 4-5 (Test, JTAG, Voltage Regulator, and Reset): Updated DESCRIPTION of XRSn. ..... 28
- Table 4-10 (Connections for Unused Pins): Updated ACCEPTABLE PRACTICE for VREFHIx. ..... 51
- Section 5.8 (Thermal Design Considerations): Added section. ..... 63
- Section 5.9.1.3 (Power Sequencing): Updated section. ..... 66
- Section 5.9.5 (Emulation/JTAG): Added description of cJTAG. ..... 80
- Figure 5-54 (eCAP Block Diagram): Updated footnote. ..... 127
- Figure 5-55 (HRCAP Block Diagram): Updated footnote. ..... 130
- Figure 5-58 (ePWM Submodules and Critical Internal Signal Interconnects): Updated figure. ..... 134
- Section 5.11.6 (Sigma-Delta Filter Module (SDFM)): Added NOTE about avoiding noise on the SDx_Cy input. ..... 142
- Section 5.11.6.1 (SDFM Electrical Data and Timing): Changed table title of Table 5-65 from "SDFM Timing Requirements" to "SDFM Timing Requirements When Using Asynchronous GPIO (ASYNC) Option". ..... 144
- Section 5.11.6.1: Added WARNING about SDFM clock inputs. ..... 144
- Section 5.11.6.2 (SDFM Electrical Data and Timing (Synchronized GPIO)): Added section. ..... 146
- Section 6.3.2 (Control Law Accelerator (CLA) ROM Memory Map): Added section. ..... 182
- Table 6-9 (Bus Master Peripheral Access): Added FSI to COMMUNICATIONS PERIPHERALS group. ..... 190
- Section 6.9.1 (Configuring Alternate Boot Mode Select Pins): Changed section title from "Configuring Alternate Boot Mode Pins" to "Configuring Alternate Boot Mode **Select** Pins". ..... 198
- Table 6-15 (BOOTPIN_CONFIG Bit Fields): Updated DESCRIPTION of BMSP2 and BMSP1. ..... 198
- Table 6-17 (BOOTDEF Bit Fields): Updated table. ..... 199
- Section 6.9.3 (GPIO Assignments): Updated section. ..... 199
- Table 6-18 (SCI Boot Options): Updated OPTION column. ..... 199
- Table 6-19 (CAN Boot Options): Updated OPTION column. ..... 200
- Table 6-20 (Flash Boot Options): Updated OPTION column. ..... 200
- Table 6-21 (Wait Boot Options): Updated OPTION column. ..... 200
- Table 6-23 (I2C Boot Options): Updated OPTION and BOOTDEFx VALUE columns. ..... 201
- Table 6-24 (Parallel Boot Options): Updated OPTION column. ..... 201
- Table 6-25 (RAM Boot Options): Added table. ..... 201
- Section 6.10 (Dual Code Security Module): Added section. ..... 202
- Figure 6-4 (Windowed Watchdog): Updated figure. ..... 203
- Section 8.2 (Tools and Software): Added F280049C controlCARD Evaluation Module and UniFlash Standalone Flash Tool. ..... 206

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# 3 Device Comparison

Table 3-1 lists the features of the TMS320F28004x devices.

**Table 3-1. Device Comparison**

| FEATURE[1] | | F280049<br>F280049C | F280048<br>F280048C | F280045 | F280041<br>F280041C | F280040<br>F280040C |
|---|---|---|---|---|---|---|
| **PROCESSOR AND ACCELERATORS** | | | | | | |
| C28x | Frequency (MHz) | 100 | | | | |
| | FPU | Yes | | | | |
| | VCU-I | Yes | | | | |
| | TMU – Type 0 | Yes | | | | |
| CLA – Type 2 | Available | Yes | | No | | |
| | Frequency (MHz) | 100 | | – | | |
| 6-Channel DMA – Type 0 | | Yes | | | | |
| **MEMORY** | | | | | | |
| Flash | | 256KB (128KW) | | | 128KB (64KW) | |
| RAM | Dedicated and Local Shared RAM | 36KB (18KW) | | | | |
| | Global Shared RAM | 64KB (32KW) | | | | |
| | **TOTAL RAM** | **100KB (50KW)** | | | | |
| Code security for on-chip flash, RAM, and OTP blocks | | Yes | | | | |
| Boot ROM | | Yes | | | | |
| User-configurable DCSM OTP | | 4KB (2KW) | | | | |
| **SYSTEM**[2] | | | | | | |
| Configurable Logic Block (CLB) | | F280049C | F280048C | – | F280041C | F280040C |
| InstaSPIN-FOC™ | | F280049C | F280048C | – | F280041C | F280040C |
| 32-bit CPU timers | | 3 | | | | |
| Watchdog timers | | 1 | | | | |
| Nonmaskable Interrupt Watchdog (NMIWD) timers | | 1 | | | | |
| Crystal oscillator/External clock input | | 1 | | | | |
| 0-pin internal oscillator | | 2 | | | | |
| GPIO pins | 100-pin PZ | 40 | – | 40 | 40 | – |
| | 64-pin PM | 26 | 24 | 26 | 26 | 24 |
| | 56-pin RSH | 25 | – | 25 | 25 | – |
| AIO inputs | 100-pin PZ | 21 | | | | |
| | 64-pin PM | 14 | | | | |
| | 56-pin RSH | 12 | | | | |
| External interrupts | | 5 | | | | |


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**Table 3-1. Device Comparison (continued)**

| FEATURE[1] | | F280049<br>F280049C | F280048<br>F280048C | F280045 | F280041<br>F280041C | F280040<br>F280040C |
|---|---|---|---|---|---|---|
| **ANALOG PERIPHERALS** | | | | | | |
| ADC 12-bit | Number of ADCs | 3 | | | | |
| | MSPS | 3.45 | | | | |
| | Conversion Time (ns)[3] | 300 | | | | |
| ADC channels (single-ended) | 100-pin PZ | 21 | | | | |
| | 64-pin PM | 14 | | | | |
| | 56-pin RSH | 12 | | | | |
| Temperature sensor | | 1 | | | | |
| Buffered DAC | | 2 | | | | |
| CMPSS (each CMPSS has two comparators and two internal DACs) | 100-pin PZ | 7 | | | | |
| | 64-pin PM | 6 | | | | |
| | 56-pin RSH | 5 | | | | |
| PGAs (Gain Settings: 3, 6, 12, 24) | 100-pin PZ | 7 | | | | |
| | 64-pin PM | 5 | | | | |
| | 56-pin RSH | 4 | | | | |
| **CONTROL PERIPHERALS[4]** | | | | | | |
| eCAP/HRCAP modules – Type 1 | | 7 (2 with HRCAP capability) | | | | |
| ePWM/HRPWM channels – Type 4 | | 16 | | | | |
| eQEP modules – Type 1 | 100-pin PZ | 2 | | | | |
| | 64-pin PM | 1 | | | | |
| | 56-pin RSH | 1 | | | | |
| SDFM channels – Type 1 | 100-pin PZ | 4 | | | | |
| | 64-pin PM | 3 | | | | |
| | 56-pin RSH | 3 | | | | |
| **COMMUNICATION PERIPHERALS[4]** | | | | | | |
| CAN – Type 0 | | 2 | | | | |
| I2C – Type 1 | | 1 | | | | |
| SCI – Type 0 | | 2 | | | | |
| SPI – Type 2 | | 2 | | | | |
| LIN – Type 1 | | 1 | | | | |
| PMBus – Type 0 | | 1 | | | | |
| FSI – Type 0 | | 1 | | | | |
| **PACKAGE OPTIONS, TEMPERATURE, AND QUALIFICATION** | | | | | | |
| Junction Temperature ($T_J$) | S: –40°C to 125°C | 100-pin PZ | – | 100-pin PZ | 100-pin PZ | – |
| | | 64-pin PM | – | 64-pin PM | 64-pin PM | – |
| | | 56-pin RSH | – | 56-pin RSH | 56-pin RSH | – |
| Free-Air Temperature ($T_A$) | Q: –40°C to 125°C[5] | 100-pin PZ | 64-pin PM | – | 100-pin PZ | 64-pin PM |

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. For more information, see the *C2000 Real-Time Control Peripherals Reference Guide*.

(2) For more information about InstaSPIN-FOC™ devices, see Section 8.3 for a list of InstaSPIN Technical Reference Manuals.

(3) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.

(4) For devices that are available in more than one package, the peripheral count listed in the smaller package is reduced because the smaller package has less device pins available. The number of peripherals internally present on the device is not reduced compared to the largest package offered within a part number. See Section 4 to identify which peripheral instances are accessible on pins in the smaller package.

(5) The letter Q refers to AEC Q100 qualification for automotive applications.

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## 3.1 Related Products

For information about other devices in the Piccolo family of products, see the following links:

**Original Piccolo™ series:**

TMS320F2802x Piccolo™ Microcontrollers
The F2802x series is the original Piccolo and offers the lowest pin-count and Flash memory size options. InstaSPIN-FOC™ versions are available.

TMS320F2803x Piccolo™ Microcontrollers
The F2803x series increases the pin-count and memory size options. The F2803x series also introduces the parallel control law accelerator (CLA) option.

TMS320F2805x Piccolo™ Microcontrollers
The F2805x series is similar to the F2803x series but adds on-chip programmable gain amplifiers (PGAs). InstaSPIN-FOC and InstaSPIN-MOTION™ versions are available.

TMS320F2806x Piccolo™ Microcontrollers
The F2806x series is the first to include a floating-point unit (FPU). The F2806x series also increases the pin-count, memory size options, and the quantity of peripherals. InstaSPIN-FOC™ and InstaSPIN-MOTION™ versions are available.

**Newest Piccolo™ series:**

TMS320F2807x Piccolo™ Microcontrollers
The F2807x series is the highest-end Piccolo with the most performance, largest pin counts, flash memory sizes, and peripheral options. The F2807x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

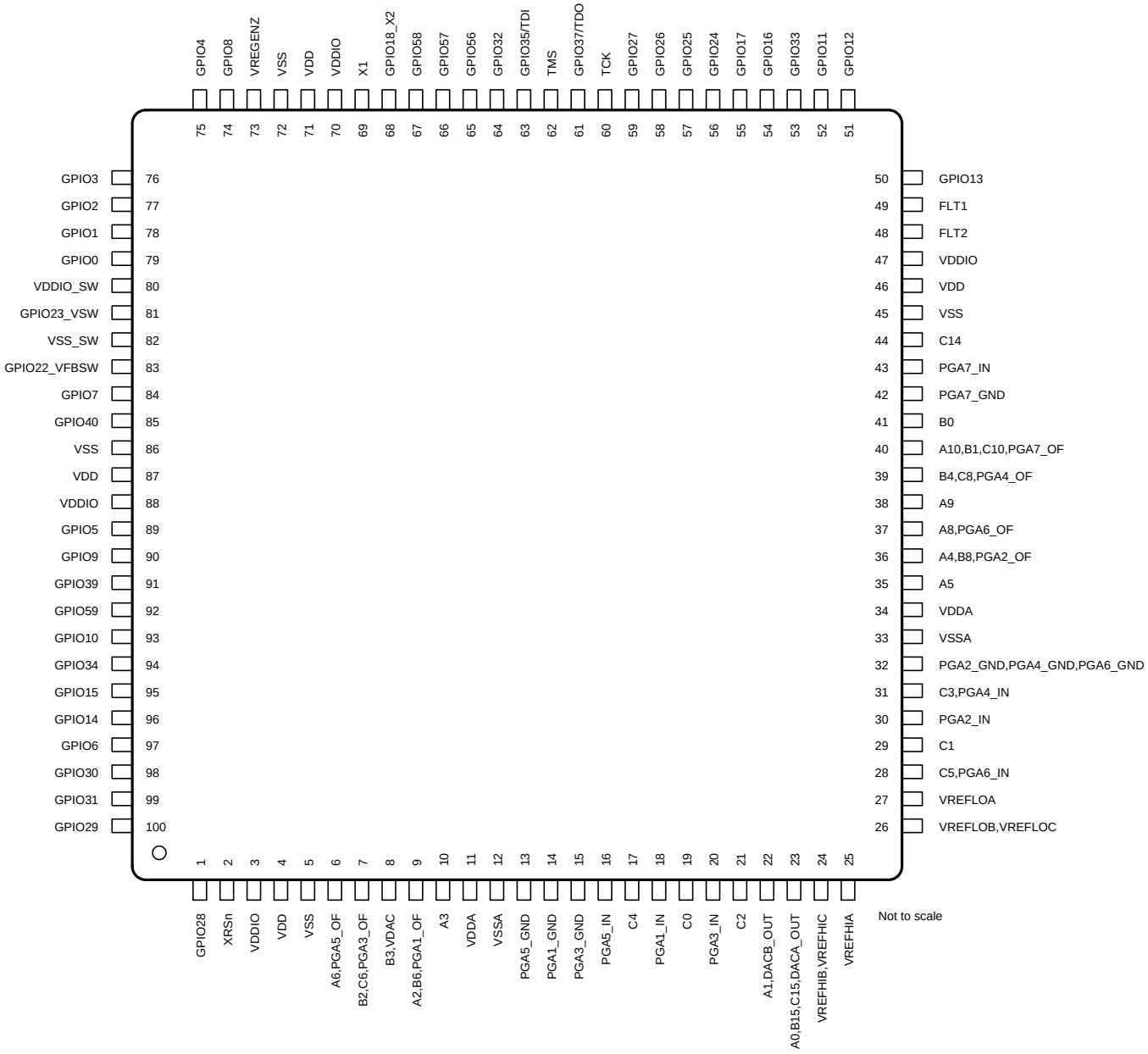
TMS320F28004x Piccolo™ Microcontrollers
The F28004x series is a reduced version of the F2807x series with the latest generational enhancements. The F28004x series is the best roadmap option for those using the F2806x series. InstaSPIN-FOC and configurable logic block (CLB) versions are available.


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# 4 Terminal Configuration and Functions

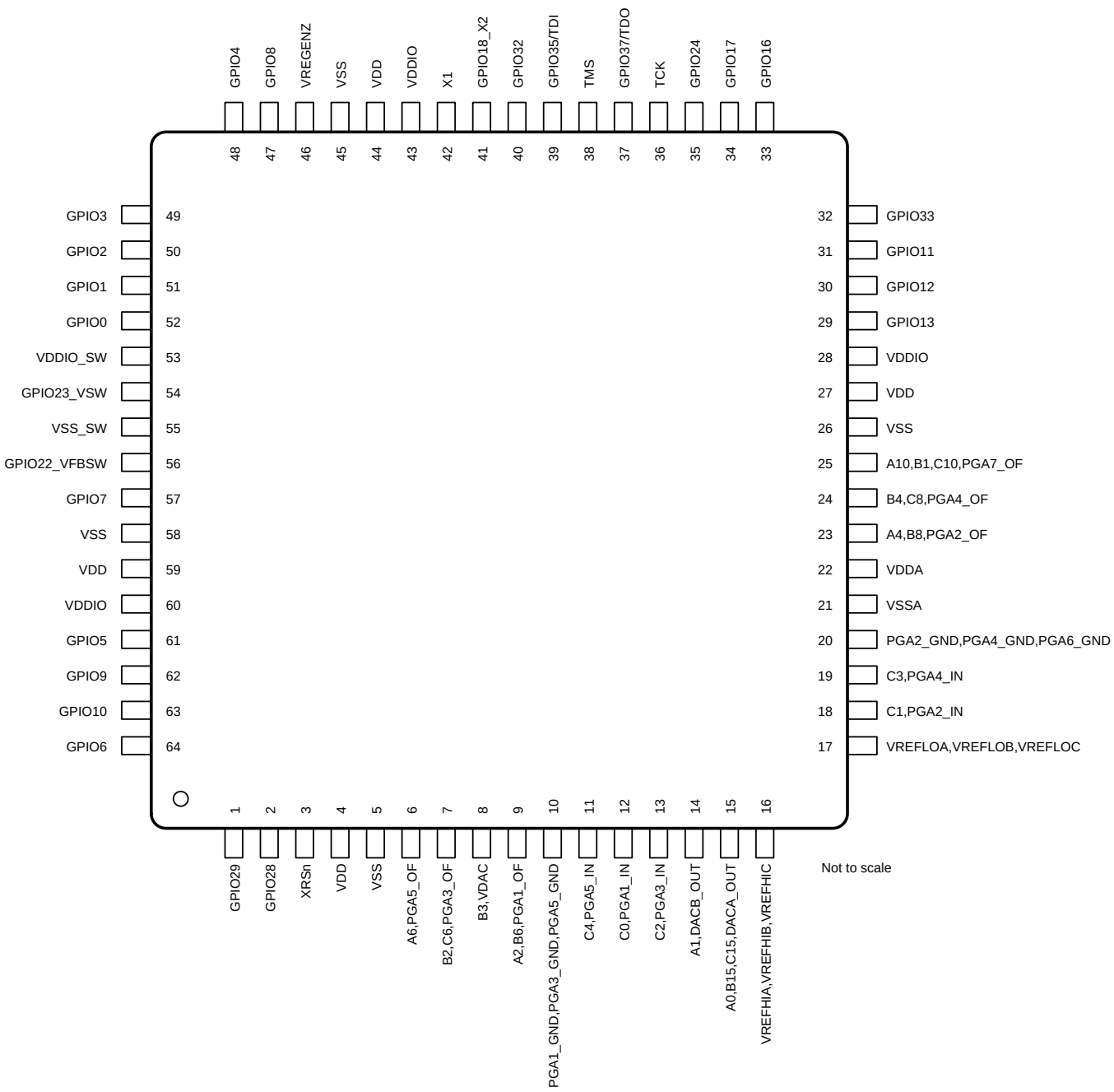
## 4.1 Pin Diagrams

Figure 4-1 shows the pin assignments on the 100-pin PZ Low-Profile Quad Flatpack. Figure 4-2 shows the pin assignments on the 64-Pin PM Low-Profile Quad Flatpack. Figure 4-3 shows the pin assignments on the 64-Pin PM Low-Profile Quad Flatpack for the Q-temperature device. Figure 4-4 shows the pin assignments on the 56-Pin RSH Very Thin Quad Flatpack No-Lead.




A. Only the GPIO function is shown on GPIO terminals. See Section 4.3 for the complete, muxed signal name.

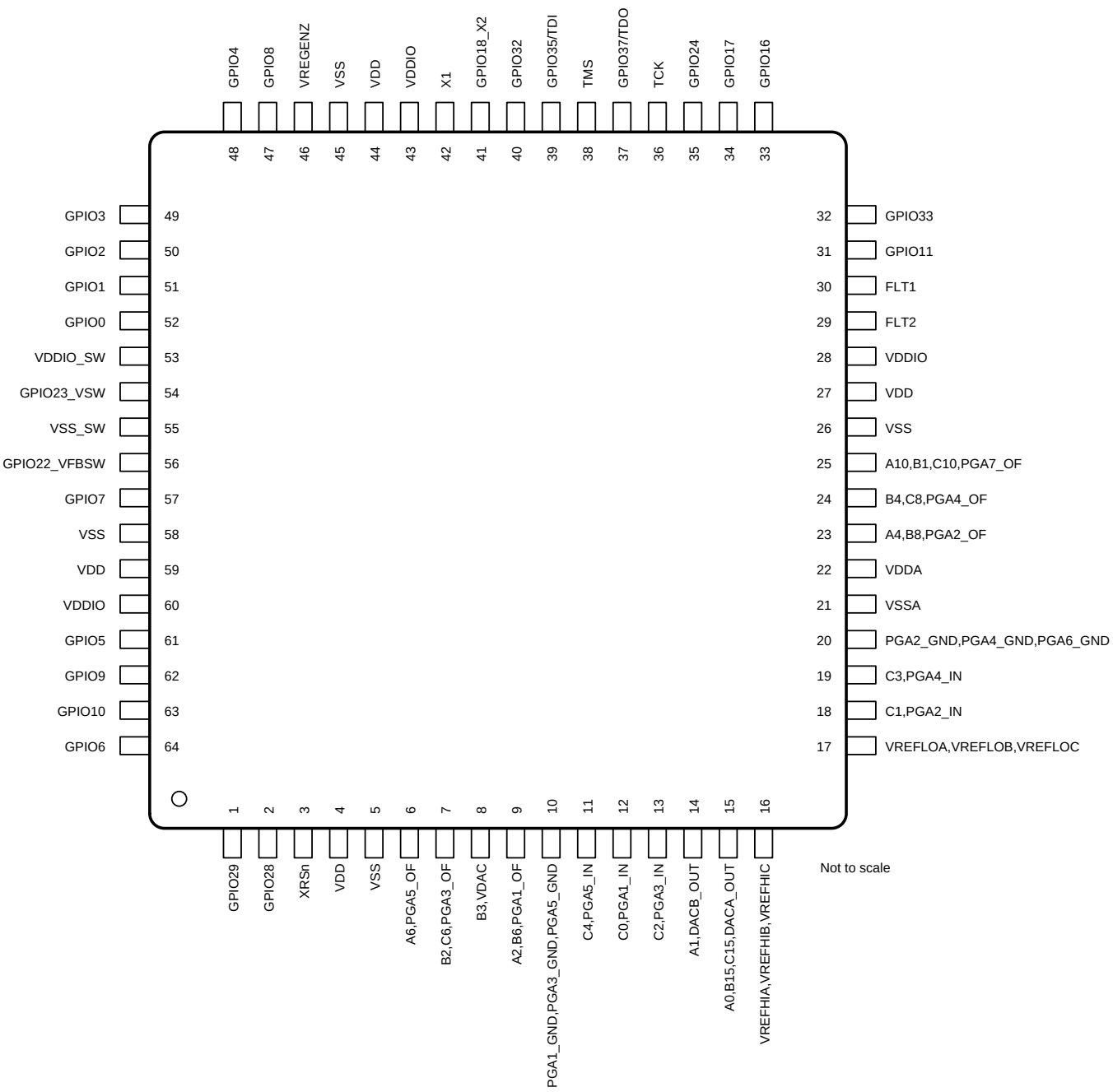
**Figure 4-1. 100-Pin PZ Low-Profile Quad Flatpack (Top View)**




A. Only the GPIO function is shown on GPIO terminals. See Section 4.3 for the complete, muxed signal name.

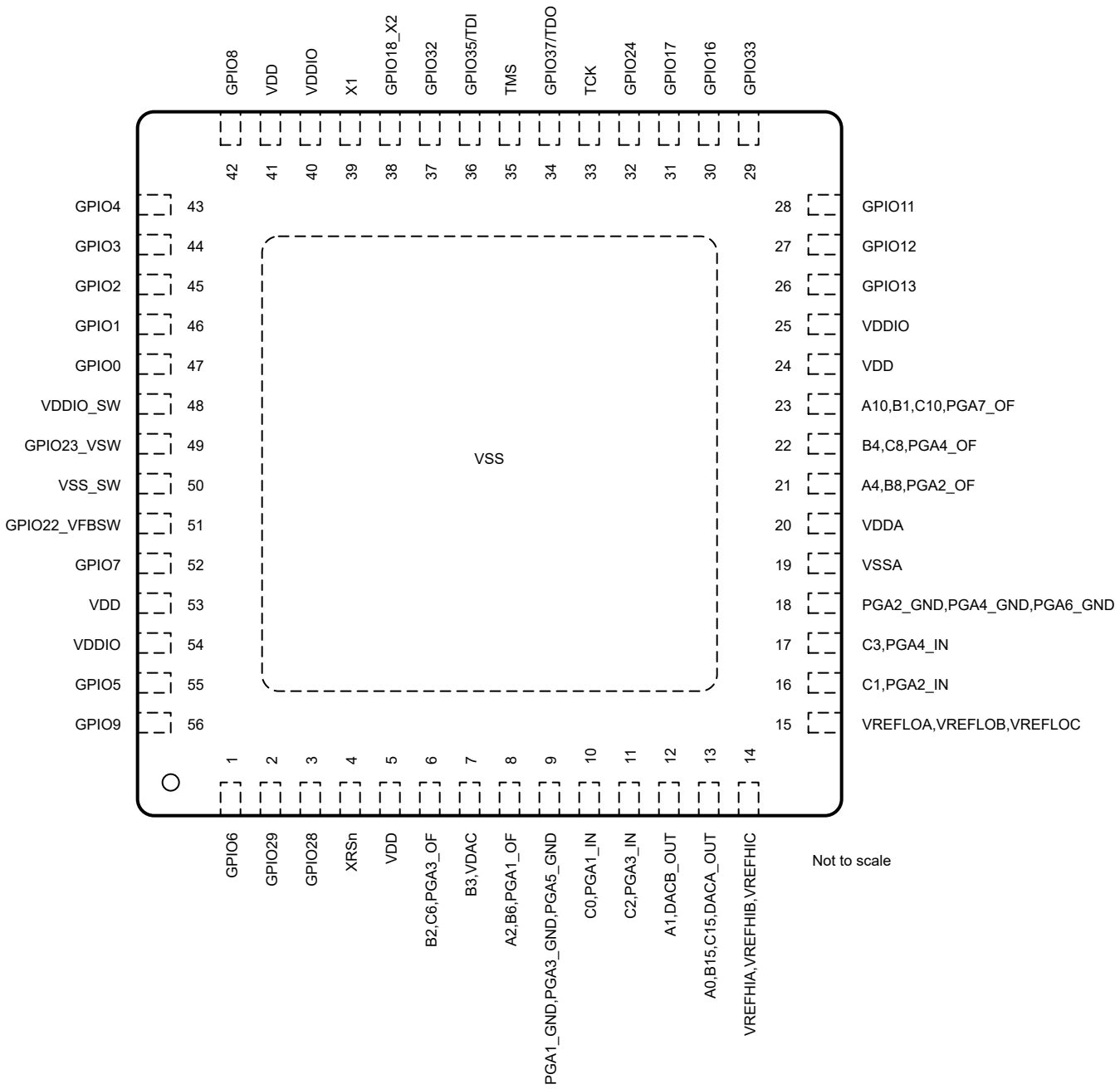
**Figure 4-2. F280049/C/M, F280045, F280041/C 64-Pin PM Low-Profile Quad Flatpack (Top View)**


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A. Only the GPIO function is shown on GPIO terminals. See Section 4.3 for the complete, muxed signal name.

**Figure 4-3. F280048/C, F280040/C 64-Pin PM Low-Profile Quad Flatpack — Q-Temperature (Top View)**




A. Only the GPIO function is shown on GPIO terminals. See Section 4.3 for the complete, muxed signal name.

B. This figure shows the top view of the 56-pin RSH package. The terminals are actually on the bottom side of the package. See Section 9 for the 56-pin RSH mechanical drawing.

**Figure 4-4. 56-Pin RSH Very Thin Quad Flatpack No-Lead (Top View)**


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## 4.2 Pin Attributes

**Table 4-1. Pin Attributes**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| **ANALOG** | | | | | | | |
| A0 | | | | | | I | ADC-A Input 0 |
| B15 | | | | | | I | ADC-B Input 15 |
| C15 | | 23 | 15 | 15 | 13 | I | ADC-C Input 15 |
| DACA_OUT | | | | | | O | Buffered DAC-A Output |
| AIO231 | | | | | | I | Digital Input-231 on ADC Pin |
| A1 | | | | | | I | ADC-A Input 1 |
| DACB_OUT | | 22 | 14 | 14 | 12 | O | Buffered DAC-B Output |
| AIO232 | | | | | | I | Digital Input-232 on ADC Pin |
| A10 | | | | | | I | ADC-A Input 10 |
| B1 | | | | | | I | ADC-B Input 1 |
| C10 | | | | | | I | ADC-C Input 10 |
| PGA7_OF | | 40 | 25 | 25 | 23 | O | PGA-7 Output Filter (Optional) |
| CMP7_HP0 | | | | | | I | CMPSS-7 High Comparator Positive Input 0 |
| CMP7_LP0 | | | | | | I | CMPSS-7 Low Comparator Positive Input 0 |
| AIO230 | | | | | | I | Digital Input-230 on ADC Pin |
| A2 | | | | | | I | ADC-A Input 2 |
| B6 | | | | | | I | ADC-B Input 6 |
| PGA1_OF | | 9 | 9 | 9 | 8 | O | PGA-1 Output Filter (Optional) |
| CMP1_HP0 | | | | | | I | CMPSS-1 High Comparator Positive Input 0 |
| CMP1_LP0 | | | | | | I | CMPSS-1 Low Comparator Positive Input 0 |
| AIO224 | | | | | | I | Digital Input-224 on ADC Pin |
| A3 | | | | | | I | ADC-A Input 3 |
| CMP1_HP3 | | | | | | I | CMPSS-1 High Comparator Positive Input 3 |
| CMP1_HN0 | | 10 | | | | I | CMPSS-1 High Comparator Negative Input 0 |
| CMP1_LP3 | | | | | | I | CMPSS-1 Low Comparator Positive Input 3 |
| CMP1_LN0 | | | | | | I | CMPSS-1 Low Comparator Negative Input 0 |
| AIO233 | | | | | | I | Digital Input-233 on ADC Pin |
| A4 | | | | | | I | ADC-A Input 4 |
| B8 | | | | | | I | ADC-B Input 8 |
| PGA2_OF | | 36 | 23 | 23 | 21 | O | PGA-2 Output Filter (Optional) |
| CMP2_HP0 | | | | | | I | CMPSS-2 High Comparator Positive Input 0 |
| CMP2_LP0 | | | | | | I | CMPSS-2 Low Comparator Positive Input 0 |
| AIO225 | | | | | | I | Digital Input-225 on ADC Pin |
| A5 | | | | | | I | ADC-A Input 5 |
| CMP2_HP3 | | | | | | I | CMPSS-2 High Comparator Positive Input 3 |
| CMP2_HN0 | | 35 | | | | I | CMPSS-2 High Comparator Negative Input 0 |
| CMP2_LP3 | | | | | | I | CMPSS-2 Low Comparator Positive Input 3 |
| CMP2_LN0 | | | | | | I | CMPSS-2 Low Comparator Negative Input 0 |
| AIO234 | | | | | | I | Digital Input-234 on ADC Pin |
| A6 | | | | | | I | ADC-A Input 6 |
| PGA5_OF | | | | | | O | PGA-5 Output Filter (Optional) |
| CMP5_HP0 | | 6 | 6 | 6 | | I | CMPSS-5 High Comparator Positive Input 0 |
| CMP5_LP0 | | | | | | I | CMPSS-5 Low Comparator Positive Input 0 |
| AIO228 | | | | | | I | Digital Input-228 on ADC Pin |

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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| A8 | | 37 | | | | I | ADC-A Input 8 |
| PGA6_OF | | | | | | O | PGA-6 Output Filter (Optional) |
| CMP6_HP0 | | | | | | I | CMPSS-6 High Comparator Positive Input 0 |
| CMP6_LP0 | | | | | | I | CMPSS-6 Low Comparator Positive Input 0 |
| AIO229 | | | | | | I | Digital Input-229 on ADC Pin |
| A9 | | 38 | | | | I | ADC-A Input 9 |
| CMP6_HP3 | | | | | | I | CMPSS-6 High Comparator Positive Input 3 |
| CMP6_HN0 | | | | | | I | CMPSS-6 High Comparator Negative Input 0 |
| CMP6_LP3 | | | | | | I | CMPSS-6 Low Comparator Positive Input 3 |
| CMP6_LN0 | | | | | | I | CMPSS-6 Low Comparator Negative Input 0 |
| AIO236 | | | | | | I | Digital Input-236 on ADC Pin |
| B0 | | 41 | | | | I | ADC-B Input 0 |
| CMP7_HP3 | | | | | | I | CMPSS-7 High Comparator Positive Input 3 |
| CMP7_HN0 | | | | | | I | CMPSS-7 High Comparator Negative Input 0 |
| CMP7_LP3 | | | | | | I | CMPSS-7 Low Comparator Positive Input 3 |
| CMP7_LN0 | | | | | | I | CMPSS-7 Low Comparator Negative Input 0 |
| AIO241 | | | | | | I | Digital Input-241 on ADC Pin |
| B2 | | 7 | 7 | 7 | 6 | I | ADC-B Input 2 |
| C6 | | | | | | I | ADC-C Input 6 |
| PGA3_OF | | | | | | O | PGA-3 Output Filter (Optional) |
| CMP3_HP0 | | | | | | I | CMPSS-3 High Comparator Positive Input 0 |
| CMP3_LP0 | | | | | | I | CMPSS-3 Low Comparator Positive Input 0 |
| AIO226 | | | | | | I | Digital Input-226 on ADC Pin |
| B3 | | 8 | 8 | 8 | 7 | I | ADC-B Input 3 |
| VDAC | | | | | | I | Optional external reference voltage for on-chip DACs. There is a 100-pF capacitor to VSSA on this pin whether used for ADC input or DAC reference which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-µF capacitor on this pin. |
| CMP3_HP3 | | | | | | I | CMPSS-3 High Comparator Positive Input 3 |
| CMP3_HN0 | | | | | | I | CMPSS-3 High Comparator Negative Input 0 |
| CMP3_LP3 | | | | | | I | CMPSS-3 Low Comparator Positive Input 3 |
| CMP3_LN0 | | | | | | I | CMPSS-3 Low Comparator Negative Input 0 |
| AIO242 | | | | | | I | Digital Input-242 on ADC Pin |
| B4 | | 39 | 24 | 24 | 22 | I | ADC-B Input 4 |
| C8 | | | | | | I | ADC-C Input 8 |
| PGA4_OF | | | | | | O | PGA-4 Output Filter (Optional) |
| CMP4_HP0 | | | | | | I | CMPSS-4 High Comparator Positive Input 0 |
| CMP4_LP0 | | | | | | I | CMPSS-4 Low Comparator Positive Input 0 |
| AIO227 | | | | | | I | Digital Input-227 on ADC Pin |
| C0 | | 19 | 12 | 12 | 10 | I | ADC-C Input 0 |
| CMP1_HP1 | | | | | | I | CMPSS-1 High Comparator Positive Input 1 |
| CMP1_HN1 | | | | | | I | CMPSS-1 High Comparator Negative Input 1 |
| CMP1_LP1 | | | | | | I | CMPSS-1 Low Comparator Positive Input 1 |
| CMP1_LN1 | | | | | | I | CMPSS-1 Low Comparator Negative Input 1 |
| AIO237 | | | | | | I | Digital Input-237 on ADC Pin |


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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| C1 | | 29 | 18 | 18 | 16 | I | ADC-C Input 1 |
| CMP2_HP1 | | | | | | I | CMPSS-2 High Comparator Positive Input 1 |
| CMP2_HN1 | | | | | | I | CMPSS-2 High Comparator Negative Input 1 |
| CMP2_LP1 | | | | | | I | CMPSS-2 Low Comparator Positive Input 1 |
| CMP2_LN1 | | | | | | I | CMPSS-2 Low Comparator Negative Input 1 |
| AIO238 | | | | | | I | Digital Input-238 on ADC Pin |
| C14 | | 44 | | | | I | ADC-C Input 14 |
| CMP7_HP1 | | | | | | I | CMPSS-7 High Comparator Positive Input 1 |
| CMP7_HN1 | | | | | | I | CMPSS-7 High Comparator Negative Input 1 |
| CMP7_LP1 | | | | | | I | CMPSS-7 Low Comparator Positive Input 1 |
| CMP7_LN1 | | | | | | I | CMPSS-7 Low Comparator Negative Input 1 |
| AIO246 | | | | | | I | Digital Input-246 on ADC Pin |
| C2 | | 21 | 13 | 13 | 11 | I | ADC-C Input 2 |
| CMP3_HP1 | | | | | | I | CMPSS-3 High Comparator Positive Input 1 |
| CMP3_HN1 | | | | | | I | CMPSS-3 High Comparator Negative Input 1 |
| CMP3_LP1 | | | | | | I | CMPSS-3 Low Comparator Positive Input 1 |
| CMP3_LN1 | | | | | | I | CMPSS-3 Low Comparator Negative Input 1 |
| AIO244 | | | | | | I | Digital Input-244 on ADC Pin |
| C3 | | 31 | 19 | 19 | 17 | I | ADC-C Input 3 |
| CMP4_HP1 | | | | | | I | CMPSS-4 High Comparator Positive Input 1 |
| CMP4_HN1 | | | | | | I | CMPSS-4 High Comparator Negative Input 1 |
| CMP4_LP1 | | | | | | I | CMPSS-4 Low Comparator Positive Input 1 |
| CMP4_LN1 | | | | | | I | CMPSS-4 Low Comparator Negative Input 1 |
| AIO245 | | | | | | I | Digital Input-245 on ADC Pin |
| C4 | | 17 | 11 | 11 | | I | ADC-C Input 4 |
| CMP5_HP1 | | | | | | I | CMPSS-5 High Comparator Positive Input 1 |
| CMP5_HN1 | | | | | | I | CMPSS-5 High Comparator Negative Input 1 |
| CMP5_LP1 | | | | | | I | CMPSS-5 Low Comparator Positive Input 1 |
| CMP5_LN1 | | | | | | I | CMPSS-5 Low Comparator Negative Input 1 |
| AIO239 | | | | | | I | Digital Input-239 on ADC Pin |
| C5 | | 28 | | | | I | ADC-C Input 5 |
| CMP6_HP1 | | | | | | I | CMPSS-6 High Comparator Positive Input 1 |
| CMP6_HN1 | | | | | | I | CMPSS-6 High Comparator Negative Input 1 |
| CMP6_LP1 | | | | | | I | CMPSS-6 Low Comparator Positive Input 1 |
| CMP6_LN1 | | | | | | I | CMPSS-6 Low Comparator Negative Input 1 |
| AIO240 | | | | | | I | Digital Input-240 on ADC Pin |
| PGA1_GND | | 14 | 10 | 10 | 9 | I | PGA-1 Ground |
| PGA1_IN | | 18 | 12 | 12 | 10 | I | PGA-1 Input |
| CMP1_HP2 | | | | | | I | CMPSS-1 High Comparator Positive Input 2 |
| CMP1_LP2 | | | | | | I | CMPSS-1 Low Comparator Positive Input 2 |
| PGA2_GND | | 32 | 20 | 20 | 18 | I | PGA-2 Ground |
| PGA2_IN | | 30 | 18 | 18 | 16 | I | PGA-2 Input |
| CMP2_HP2 | | | | | | I | CMPSS-2 High Comparator Positive Input 2 |
| CMP2_LP2 | | | | | | I | CMPSS-2 Low Comparator Positive Input 2 |
| PGA3_GND | | 15 | 10 | 10 | 9 | I | PGA-3 Ground |

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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| PGA3_IN | | | | | | I | PGA-3 Input |
| CMP3_HP2 | | 20 | 13 | 13 | 11 | I | CMPSS-3 High Comparator Positive Input 2 |
| CMP3_LP2 | | | | | | I | CMPSS-3 Low Comparator Positive Input 2 |
| PGA4_GND | | 32 | 20 | 20 | 18 | I | PGA-4 Ground |
| PGA4_IN | | | | | | I | PGA-4 Input |
| CMP4_HP2 | | 31 | 19 | 19 | 17 | I | CMPSS-4 High Comparator Positive Input 2 |
| CMP4_LP2 | | | | | | I | CMPSS-4 Low Comparator Positive Input 2 |
| PGA5_GND | | 13 | 10 | 10 | 9 | I | PGA-5 Ground |
| PGA5_IN | | | | | | I | PGA-5 Input |
| CMP5_HP2 | | 16 | 11 | 11 | | I | CMPSS-5 High Comparator Positive Input 2 |
| CMP5_LP2 | | | | | | I | CMPSS-5 Low Comparator Positive Input 2 |
| PGA6_GND | | 32 | 20 | 20 | 18 | I | PGA-6 Ground |
| PGA6_IN | | | | | | I | PGA-6 Input |
| CMP6_HP2 | | 28 | | | | I | CMPSS-6 High Comparator Positive Input 2 |
| CMP6_LP2 | | | | | | I | CMPSS-6 Low Comparator Positive Input 2 |
| PGA7_GND | | 42 | | | | I | PGA-7 Ground |
| PGA7_IN | | | | | | I | PGA-7 Input |
| CMP7_HP2 | | 43 | | | | I | CMPSS-7 High Comparator Positive Input 2 |
| CMP7_LP2 | | | | | | I | CMPSS-7 Low Comparator Positive Input 2 |
| VREFHIA | | 25 | 16 | 16 | 14 | I/O | ADC-A High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHIA and VREFLOA pins. Do not load this pin externally in either internal or external reference mode. |
| VREFHIB | | 24 | 16 | 16 | 14 | I/O | ADC-B High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHIB and VREFLOB pins. Do not load this pin externally in either internal or external reference mode. |
| VREFHIC | | 24 | 16 | 16 | 14 | I/O | ADC-C High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHIC and VREFLOC pins. Do not load this pin externally in either internal or external reference mode. |
| VREFLOA | | 27 | 17 | 17 | 15 | I | ADC-A Low Reference |
| VREFLOB | | 26 | 17 | 17 | 15 | I | ADC-B Low Reference |
| VREFLOC | | 26 | 17 | 17 | 15 | I | ADC-C Low Reference |
| **GPIO** | | | | | | | |
| GPIO0 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 0 |
| EPWM1_A | 1 | 79 | 52 | 52 | 47 | O | ePWM-1 Output A |
| I2CA_SDA | 6 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| GPIO1 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 1 |
| EPWM1_B | 1 | 78 | 51 | 51 | 46 | O | ePWM-1 Output B |
| I2CA_SCL | 6 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |


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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| GPIO2 | 0, 4, 8, 12 | 77 | 50 | 50 | 45 | I/O | General-Purpose Input Output 2 |
| EPWM2_A | 1 | | | | | O | ePWM-2 Output A |
| OUTPUTXBAR1 | 5 | | | | | O | Output X-BAR Output 1 |
| PMBUSA_SDA | 6 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SCIA_TX | 9 | | | | | O | SCI-A Transmit Data |
| FSIRXA_D1 | 10 | | | | | I | FSIRX-A Optional Additional Data Input |
| GPIO3 | 0, 4, 8, 12 | 76 | 49 | 49 | 44 | I/O | General-Purpose Input Output 3 |
| EPWM2_B | 1 | | | | | O | ePWM-2 Output B |
| OUTPUTXBAR2 | 2, 5 | | | | | O | Output X-BAR Output 2 |
| PMBUSA_SCL | 6 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SPIA_CLK | 7 | | | | | I/O | SPI-A Clock |
| SCIA_RX | 9 | | | | | I | SCI-A Receive Data |
| FSIRXA_D0 | 10 | | | | | I | FSIRX-A Primary Data Input |
| GPIO4 | 0, 4, 8, 12 | 75 | 48 | 48 | 43 | I/O | General-Purpose Input Output 4 |
| EPWM3_A | 1 | | | | | O | ePWM-3 Output A |
| OUTPUTXBAR3 | 5 | | | | | O | Output X-BAR Output 3 |
| CANA_TX | 6 | | | | | O | CAN-A Transmit |
| FSIRXA_CLK | 10 | | | | | I | FSIRX-A Input Clock |
| GPIO5 | 0, 4, 8, 12 | 89 | 61 | 61 | 55 | I/O | General-Purpose Input Output 5 |
| EPWM3_B | 1 | | | | | O | ePWM-3 Output B |
| OUTPUTXBAR3 | 3 | | | | | O | Output X-BAR Output 3 |
| CANA_RX | 6 | | | | | I | CAN-A Receive |
| SPIA_STE | 7 | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| FSITXA_D1 | 9 | | | | | O | FSITX-A Optional Additional Data Output |
| GPIO6 | 0, 4, 8, 12 | 97 | 64 | 64 | 1 | I/O | General-Purpose Input Output 6 |
| EPWM4_A | 1 | | | | | O | ePWM-4 Output A |
| OUTPUTXBAR4 | 2 | | | | | O | Output X-BAR Output 4 |
| SYNCOUT | 3 | | | | | O | External ePWM Synchronization Pulse |
| EQEP1_A | 5 | | | | | I | eQEP-1 Input A |
| CANB_TX | 6 | | | | | O | CAN-B Transmit |
| SPIB_SOMI | 7 | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| FSITXA_D0 | 9 | | | | | O | FSITX-A Primary Data Output |
| GPIO7 | 0, 4, 8, 12 | 84 | 57 | 57 | 52 | I/O | General-Purpose Input Output 7 |
| EPWM4_B | 1 | | | | | O | ePWM-4 Output B |
| OUTPUTXBAR5 | 3 | | | | | O | Output X-BAR Output 5 |
| EQEP1_B | 5 | | | | | I | eQEP-1 Input B |
| CANB_RX | 6 | | | | | I | CAN-B Receive |
| SPIB_SIMO | 7 | | | | | I/O | SPI-B Slave In, Master Out (SIMO) |
| FSITXA_CLK | 9 | | | | | O | FSITX-A Output Clock |

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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| GPIO8 | 0, 4, 8, 12 | 74 | 47 | 47 | 42 | I/O | General-Purpose Input Output 8 |
| EPWM5_A | 1 | | | | | O | ePWM-5 Output A |
| CANB_TX | 2 | | | | | O | CAN-B Transmit |
| ADCSOCAO | 3 | | | | | O | ADC Start of Conversion A Output for External ADC (from ePWM modules) |
| EQEP1_STROBE | 5 | | | | | I/O | eQEP-1 Strobe |
| SCIA_TX | 6 | | | | | O | SCI-A Transmit Data |
| SPIA_SIMO | 7 | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| I2CA_SCL | 9 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| FSITXA_D1 | 10 | | | | | O | FSITX-A Optional Additional Data Output |
| GPIO9 | 0, 4, 8, 12 | 90 | 62 | 62 | 56 | I/O | General-Purpose Input Output 9 |
| EPWM5_B | 1 | | | | | O | ePWM-5 Output B |
| SCIB_TX | 2 | | | | | O | SCI-B Transmit Data |
| OUTPUTXBAR6 | 3 | | | | | O | Output X-BAR Output 6 |
| EQEP1_INDEX | 5 | | | | | I/O | eQEP-1 Index |
| SCIA_RX | 6 | | | | | I | SCI-A Receive Data |
| SPIA_CLK | 7 | | | | | I/O | SPI-A Clock |
| FSITXA_D0 | 10 | | | | | O | FSITX-A Primary Data Output |
| GPIO10 | 0, 4, 8, 12 | 93 | 63 | 63 | | I/O | General-Purpose Input Output 10 |
| EPWM6_A | 1 | | | | | O | ePWM-6 Output A |
| CANB_RX | 2 | | | | | I | CAN-B Receive |
| ADCSOCBO | 3 | | | | | O | ADC Start of Conversion B Output for External ADC (from ePWM modules) |
| EQEP1_A | 5 | | | | | I | eQEP-1 Input A |
| SCIB_TX | 6 | | | | | O | SCI-B Transmit Data |
| SPIA_SOMI | 7 | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| I2CA_SDA | 9 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| FSITXA_CLK | 10 | | | | | O | FSITX-A Output Clock |
| GPIO11 | 0, 4, 8, 12 | 52 | 31 | 31 | 28 | I/O | General-Purpose Input Output 11 |
| EPWM6_B | 1 | | | | | O | ePWM-6 Output B |
| SCIB_RX | 2, 6 | | | | | I | SCI-B Receive Data |
| OUTPUTXBAR7 | 3 | | | | | O | Output X-BAR Output 7 |
| EQEP1_B | 5 | | | | | I | eQEP-1 Input B |
| SPIA_STE | 7 | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| FSIRXA_D1 | 9 | | | | | I | FSIRX-A Optional Additional Data Input |
| GPIO12 | 0, 4, 8, 12 | 51 | | 30 | 27 | I/O | General-Purpose Input Output 12 |
| EPWM7_A | 1 | | | | | O | ePWM-7 Output A |
| CANB_TX | 2 | | | | | O | CAN-B Transmit |
| EQEP1_STROBE | 5 | | | | | I/O | eQEP-1 Strobe |
| SCIB_TX | 6 | | | | | O | SCI-B Transmit Data |
| PMBUSA_CTL | 7 | | | | | I | PMBus-A Control Signal |
| FSIRXA_D0 | 9 | | | | | I | FSIRX-A Primary Data Input |


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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| GPIO13 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 13 |
| EPWM7_B | 1 | | | | | O | ePWM-7 Output B |
| CANB_RX | 2 | | | | | I | CAN-B Receive |
| EQEP1_INDEX | 5 | 50 | | 29 | 26 | I/O | eQEP-1 Index |
| SCIB_RX | 6 | | | | | I | SCI-B Receive Data |
| PMBUSA_ALERT | 7 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| FSIRXA_CLK | 9 | | | | | I | FSIRX-A Input Clock |
| GPIO14 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 14 |
| EPWM8_A | 1 | | | | | O | ePWM-8 Output A |
| SCIB_TX | 2 | | | | | O | SCI-B Transmit Data |
| OUTPUTXBAR3 | 6 | 96 | | | | O | Output X-BAR Output 3 |
| PMBUSA_SDA | 7 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SPIB_CLK | 9 | | | | | I/O | SPI-B Clock |
| EQEP2_A | 10 | | | | | I | eQEP-2 Input A |
| GPIO15 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 15 |
| EPWM8_B | 1 | | | | | O | ePWM-8 Output B |
| SCIB_RX | 2 | | | | | I | SCI-B Receive Data |
| OUTPUTXBAR4 | 6 | 95 | | | | O | Output X-BAR Output 4 |
| PMBUSA_SCL | 7 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SPIB_STE | 9 | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| EQEP2_B | 10 | | | | | I | eQEP-2 Input B |
| GPIO16 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 16 |
| SPIA_SIMO | 1 | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| CANB_TX | 2 | | | | | O | CAN-B Transmit |
| OUTPUTXBAR7 | 3 | | | | | O | Output X-BAR Output 7 |
| EPWM5_A | 5 | | | | | O | ePWM-5 Output A |
| SCIA_TX | 6 | 54 | 33 | 33 | 30 | O | SCI-A Transmit Data |
| SD1_D1 | 7 | | | | | I | SDFM-1 Channel 1 Data Input |
| EQEP1_STROBE | 9 | | | | | I/O | eQEP-1 Strobe |
| PMBUSA_SCL | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| XCLKOUT | 11 | | | | | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. |
| GPIO17 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 17 |
| SPIA_SOMI | 1 | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| CANB_RX | 2 | | | | | I | CAN-B Receive |
| OUTPUTXBAR8 | 3 | | | | | O | Output X-BAR Output 8 |
| EPWM5_B | 5 | 55 | 34 | 34 | 31 | O | ePWM-5 Output B |
| SCIA_RX | 6 | | | | | I | SCI-A Receive Data |
| SD1_C1 | 7 | | | | | I | SDFM-1 Channel 1 Clock Input |
| EQEP1_INDEX | 9 | | | | | I/O | eQEP-1 Index |
| PMBUSA_SDA | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |

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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| GPIO18_X2 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 18. This pin and its digital mux options can only be used when the system is clocked by INTOSC and X1 has an external pulldown resistor (recommended 1 kΩ). |
| SPIA_CLK | 1 | | | | | I/O | SPI-A Clock |
| SCIB_TX | 2 | | | | | O | SCI-B Transmit Data |
| CANA_RX | 3 | | | | | I | CAN-A Receive |
| EPWM6_A | 5 | 68 | 41 | 41 | 38 | O | ePWM-6 Output A |
| I2CA_SCL | 6 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SD1_D2 | 7 | | | | | I | SDFM-1 Channel 2 Data Input |
| EQEP2_A | 9 | | | | | I | eQEP-2 Input A |
| PMBUSA_CTL | 10 | | | | | I | PMBus-A Control Signal |
| XCLKOUT | 11 | | | | | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. |
| X2 | ALT | | | | | I/O | Crystal oscillator output |
| GPIO20 | 0 | | | | | I/O | General-Purpose Input Output 20 |
| GPIO21 | 0 | | | | | I/O | General-Purpose Input Output 21 |
| GPIO22_VFBSW | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 22. This pin is configured for DC-DC mode by default. If the internal DC-DC regulator is not used, this can be configured as General-Purpose Input Output 22 by disabling DC-DC and clearing their bits in GPAAMSEL register. |
| EQEP1_STROBE | 1 | | | | | I/O | eQEP-1 Strobe |
| SCIB_TX | 3 | 83 | 56 | 56 | 51 | O | SCI-B Transmit Data |
| SPIB_CLK | 6 | | | | | I/O | SPI-B Clock |
| SD1_D4 | 7 | | | | | I | SDFM-1 Channel 4 Data Input |
| LINA_TX | 9 | | | | | O | LIN-A Transmit |
| VFBSW | ALT | | | | | - | Internal DC-DC regulator feedback signal. If the internal DC-DC regulator is used, tie this pin to the node where L(VSW) connects to the VDD rail (as close as possible to the device). |
| GPIO23_VSW | 0 | 81 | 54 | 54 | 49 | I/O | General-Purpose Input Output 23. This pin is configured for DC-DC mode by default. If the internal DC-DC regulator is not used, this can be configured as General-Purpose Input Output 23 by disabling DC-DC and clearing their bits in GPAAMSEL register. This pin has an internal capacitance of approximately 100 pF. TI Recommends using an alternate GPIO, or using this pin only for applications which do not require a fast switching response. |
| VSW | ALT | | | | | - | Switching output of the internal DC-DC regulator |
| GPIO24 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 24 |
| OUTPUTXBAR1 | 1 | | | | | O | Output X-BAR Output 1 |
| EQEP2_A | 2 | | | | | I | eQEP-2 Input A |
| EPWM8_A | 5 | | | | | O | ePWM-8 Output A |
| SPIB_SIMO | 6 | 56 | 35 | 35 | 32 | I/O | SPI-B Slave In, Master Out (SIMO) |
| SD1_D1 | 7 | | | | | I | SDFM-1 Channel 1 Data Input |
| PMBUSA_SCL | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SCIA_TX | 11 | | | | | O | SCI-A Transmit Data |
| ERRORSTS | 13 | | | | | O | Error Status Output. This signal requires an external pullup. |


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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| GPIO25 | 0, 4, 8, 12 | 57 | | | | I/O | General-Purpose Input Output 25 |
| OUTPUTXBAR2 | 1 | | | | | O | Output X-BAR Output 2 |
| EQEP2_B | 2 | | | | | I | eQEP-2 Input B |
| SPIB_SOMI | 6 | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| SD1_C1 | 7 | | | | | I | SDFM-1 Channel 1 Clock Input |
| FSITXA_D1 | 9 | | | | | O | FSITX-A Optional Additional Data Output |
| PMBUSA_SDA | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SCIA_RX | 11 | | | | | I | SCI-A Receive Data |
| GPIO26 | 0, 4, 8, 12 | 58 | | | | I/O | General-Purpose Input Output 26 |
| OUTPUTXBAR3 | 1, 5 | | | | | O | Output X-BAR Output 3 |
| EQEP2_INDEX | 2 | | | | | I/O | eQEP-2 Index |
| SPIB_CLK | 6 | | | | | I/O | SPI-B Clock |
| SD1_D2 | 7 | | | | | I | SDFM-1 Channel 2 Data Input |
| FSITXA_D0 | 9 | | | | | O | FSITX-A Primary Data Output |
| PMBUSA_CTL | 10 | | | | | I | PMBus-A Control Signal |
| I2CA_SDA | 11 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| GPIO27 | 0, 4, 8, 12 | 59 | | | | I/O | General-Purpose Input Output 27 |
| OUTPUTXBAR4 | 1, 5 | | | | | O | Output X-BAR Output 4 |
| EQEP2_STROBE | 2 | | | | | I/O | eQEP-2 Strobe |
| SPIB_STE | 6 | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| SD1_C2 | 7 | | | | | I | SDFM-1 Channel 2 Clock Input |
| FSITXA_CLK | 9 | | | | | O | FSITX-A Output Clock |
| PMBUSA_ALERT | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| I2CA_SCL | 11 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| GPIO28 | 0, 4, 8, 12 | 1 | 2 | 2 | 3 | I/O | General-Purpose Input Output 28 |
| SCIA_RX | 1 | | | | | I | SCI-A Receive Data |
| EPWM7_A | 3 | | | | | O | ePWM-7 Output A |
| OUTPUTXBAR5 | 5 | | | | | O | Output X-BAR Output 5 |
| EQEP1_A | 6 | | | | | I | eQEP-1 Input A |
| SD1_D3 | 7 | | | | | I | SDFM-1 Channel 3 Data Input |
| EQEP2_STROBE | 9 | | | | | I/O | eQEP-2 Strobe |
| LINA_TX | 10 | | | | | O | LIN-A Transmit |
| SPIB_CLK | 11 | | | | | I/O | SPI-B Clock |
| ERRORSTS | 13 | | | | | O | Error Status Output. This signal requires an external pullup. |
| GPIO29 | 0, 4, 8, 12 | 100 | 1 | 1 | 2 | I/O | General-Purpose Input Output 29 |
| SCIA_TX | 1 | | | | | O | SCI-A Transmit Data |
| EPWM7_B | 3 | | | | | O | ePWM-7 Output B |
| OUTPUTXBAR6 | 5 | | | | | O | Output X-BAR Output 6 |
| EQEP1_B | 6 | | | | | I | eQEP-1 Input B |
| SD1_C3 | 7 | | | | | I | SDFM-1 Channel 3 Clock Input |
| EQEP2_INDEX | 9 | | | | | I/O | eQEP-2 Index |
| LINA_RX | 10 | | | | | I | LIN-A Receive |
| SPIB_STE | 11 | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| ERRORSTS | 13 | | | | | O | Error Status Output. This signal requires an external pullup. |

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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| GPIO30 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 30 |
| CANA_RX | 1 | | | | | I | CAN-A Receive |
| SPIB_SIMO | 3 | 98 | | | | I/O | SPI-B Slave In, Master Out (SIMO) |
| OUTPUTXBAR7 | 5 | | | | | O | Output X-BAR Output 7 |
| EQEP1_STROBE | 6 | | | | | I/O | eQEP-1 Strobe |
| SD1_D4 | 7 | | | | | I | SDFM-1 Channel 4 Data Input |
| GPIO31 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 31 |
| CANA_TX | 1 | | | | | O | CAN-A Transmit |
| SPIB_SOMI | 3 | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| OUTPUTXBAR8 | 5 | 99 | | | | O | Output X-BAR Output 8 |
| EQEP1_INDEX | 6 | | | | | I/O | eQEP-1 Index |
| SD1_C4 | 7 | | | | | I | SDFM-1 Channel 4 Clock Input |
| FSIRXA_D1 | 9 | | | | | I | FSIRX-A Optional Additional Data Input |
| GPIO32 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 32 |
| I2CA_SDA | 1 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| SPIB_CLK | 3 | | | | | I/O | SPI-B Clock |
| EPWM8_B | 5 | 64 | 40 | 40 | 37 | O | ePWM-8 Output B |
| LINA_TX | 6 | | | | | O | LIN-A Transmit |
| SD1_D3 | 7 | | | | | I | SDFM-1 Channel 3 Data Input |
| FSIRXA_D0 | 9 | | | | | I | FSIRX-A Primary Data Input |
| CANA_TX | 10 | | | | | O | CAN-A Transmit |
| GPIO33 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 33 |
| I2CA_SCL | 1 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SPIB_STE | 3 | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| OUTPUTXBAR4 | 5 | 53 | 32 | 32 | 29 | O | Output X-BAR Output 4 |
| LINA_RX | 6 | | | | | I | LIN-A Receive |
| SD1_C3 | 7 | | | | | I | SDFM-1 Channel 3 Clock Input |
| FSIRXA_CLK | 9 | | | | | I | FSIRX-A Input Clock |
| CANA_RX | 10 | | | | | I | CAN-A Receive |
| GPIO34 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 34 |
| OUTPUTXBAR1 | 1 | 94 | | | | O | Output X-BAR Output 1 |
| PMBUSA_SDA | 6 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| GPIO35 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 35 |
| SCIA_RX | 1 | | | | | I | SCI-A Receive Data |
| I2CA_SDA | 3 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| CANA_RX | 5 | | | | | I | CAN-A Receive |
| PMBUSA_SCL | 6 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| LINA_RX | 7 | 63 | 39 | 39 | 36 | I | LIN-A Receive |
| EQEP1_A | 9 | | | | | I | eQEP-1 Input A |
| PMBUSA_CTL | 10 | | | | | I | PMBus-A Control Signal |
| TDI | 15 | | | | | I | JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input. |


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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| GPIO37 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 37 |
| OUTPUTXBAR2 | 1 | | | | | O | Output X-BAR Output 2 |
| I2CA_SCL | 3 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SCIA_TX | 5 | | | | | O | SCI-A Transmit Data |
| CANA_TX | 6 | | | | | O | CAN-A Transmit |
| LINA_TX | 7 | | | | | O | LIN-A Transmit |
| EQEP1_B | 9 | 61 | 37 | 37 | 34 | I | eQEP-1 Input B |
| PMBUSA_ALERT | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| TDO | 15 | | | | | O | JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. |
| GPIO39 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 39 |
| CANB_RX | 6 | 91 | | | | I | CAN-B Receive |
| FSIRXA_CLK | 7 | | | | | I | FSIRX-A Input Clock |
| GPIO40 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 40 |
| PMBUSA_SDA | 6 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| FSIRXA_D0 | 7 | 85 | | | | I | FSIRX-A Primary Data Input |
| SCIB_TX | 9 | | | | | O | SCI-B Transmit Data |
| EQEP1_A | 10 | | | | | I | eQEP-1 Input A |
| GPIO41 | 0 | | | | | I/O | General-Purpose Input Output 41 |
| GPIO42 | 0 | | | | | I/O | General-Purpose Input Output 42 |
| GPIO43 | 0 | | | | | I/O | General-Purpose Input Output 43 |
| GPIO44 | 0 | | | | | I/O | General-Purpose Input Output 44 |
| GPIO45 | 0 | | | | | I/O | General-Purpose Input Output 45 |
| GPIO46 | 0 | | | | | I/O | General-Purpose Input Output 46 |
| GPIO47 | 0 | | | | | I/O | General-Purpose Input Output 47 |
| GPIO48 | 0 | | | | | I/O | General-Purpose Input Output 48 |
| GPIO49 | 0 | | | | | I/O | General-Purpose Input Output 49 |
| GPIO50 | 0 | | | | | I/O | General-Purpose Input Output 50 |
| GPIO51 | 0 | | | | | I/O | General-Purpose Input Output 51 |
| GPIO52 | 0 | | | | | I/O | General-Purpose Input Output 52 |
| GPIO53 | 0 | | | | | I/O | General-Purpose Input Output 53 |
| GPIO54 | 0 | | | | | I/O | General-Purpose Input Output 54 |
| GPIO55 | 0 | | | | | I/O | General-Purpose Input Output 55 |
| GPIO56 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 56 |
| SPIA_CLK | 1 | | | | | I/O | SPI-A Clock |
| EQEP2_STROBE | 5 | | | | | I/O | eQEP-2 Strobe |
| SCIB_TX | 6 | 65 | | | | O | SCI-B Transmit Data |
| SD1_D3 | 7 | | | | | I | SDFM-1 Channel 3 Data Input |
| SPIB_SIMO | 9 | | | | | I/O | SPI-B Slave In, Master Out (SIMO) |
| EQEP1_A | 11 | | | | | I | eQEP-1 Input A |

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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| GPIO57 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 57 |
| SPIA_STE | 1 | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| EQEP2_INDEX | 5 | | | | | I/O | eQEP-2 Index |
| SCIB_RX | 6 | 66 | | | | I | SCI-B Receive Data |
| SD1_C3 | 7 | | | | | I | SDFM-1 Channel 3 Clock Input |
| SPIB_SOMI | 9 | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| EQEP1_B | 11 | | | | | I | eQEP-1 Input B |
| GPIO58 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 58 |
| OUTPUTXBAR1 | 5 | | | | | O | Output X-BAR Output 1 |
| SPIB_CLK | 6 | | | | | I/O | SPI-B Clock |
| SD1_D4 | 7 | 67 | | | | I | SDFM-1 Channel 4 Data Input |
| LINA_TX | 9 | | | | | O | LIN-A Transmit |
| CANB_TX | 10 | | | | | O | CAN-B Transmit |
| EQEP1_STROBE | 11 | | | | | I/O | eQEP-1 Strobe |
| GPIO59 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 59 |
| OUTPUTXBAR2 | 5 | | | | | O | Output X-BAR Output 2 |
| SPIB_STE | 6 | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| SD1_C4 | 7 | 92 | | | | I | SDFM-1 Channel 4 Clock Input |
| LINA_RX | 9 | | | | | I | LIN-A Receive |
| CANB_RX | 10 | | | | | I | CAN-B Receive |
| EQEP1_INDEX | 11 | | | | | I/O | eQEP-1 Index |
| **TEST, JTAG, VOLTAGE REGULATOR, AND RESET** | | | | | | | |
| FLT1 | | 49 | 30 | | | I/O | Flash test pin 1. Reserved for TI. Must be left unconnected. |
| FLT2 | | 48 | 29 | | | I/O | Flash test pin 2. Reserved for TI. Must be left unconnected. |
| TCK | | 60 | 36 | 36 | 33 | I | JTAG test clock with internal pullup. |
| TMS | | 62 | 38 | 38 | 35 | I | JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation. |
| VREGENZ | | 73 | 46 | 46 | | I | Internal voltage regulator enable with internal pulldown. Tie directly to VSS (low) to enable the internal VREG. Tie directly to VDDIO (high) to use an external supply. |
| X1 | | 69 | 42 | 42 | 39 | I/O | Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock. GPIO19 is not supported. Internally GPIO19 is connected to the X1 function, therefore the GPIO19 should be kept in Input Mode with the Pullup disabled to avoid interference with the X1 clock function. |


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**Table 4-1. Pin Attributes (continued)**

| SIGNAL NAME | MUX POSITION | 100 PZ | 64 PMQ | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| XRSn | | 2 | 3 | 3 | 4 | I/OD | Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. The output buffer of this pin is an open-drain with an internal pullup. If this pin is driven by an external device, It should be done using an open-drain device. |
| **POWER AND GROUND** | | | | | | | |
| VDD | | 4, 46, 71, 87 | 4, 27, 44, 59 | 4, 27, 44, 59 | 5, 24, 41, 53 | | 1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 20 µF. When not using the internal voltage regulator, the exact value of the decoupling capacitance should be determined by your system voltage regulation solution. |
| VDDA | | 11, 34 | 22 | 22 | 20 | | 3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor to VSSA on each pin. |
| VDDIO | | 3, 47, 70, 88 | 28, 43, 60 | 28, 43, 60 | 25, 40, 54 | | 3.3-V Digital I/O Power Pins. Place a minimum 0.1-µF decoupling capacitor on each pin. |
| VDDIO_SW | | 80 | 53 | 53 | 48 | | 3.3-V Supply pin for the internal DC-DC regulator. If the internal DC-DC regulator is used, a bulk input capacitance of 20-µF should be placed on this pin. If the internal DC-DC regulator is not used, this pin should be treated as a VDDIO pin. |
| VSS | | 5, 45, 72, 86 | 5, 26, 45, 58 | 5, 26, 45, 58 | PAD | | Digital Ground |
| VSSA | | 12, 33 | 21 | 21 | 19 | | Analog Ground |
| VSS_SW | | 82 | 55 | 55 | 50 | | Internal DC-DC regulator ground. If the internal DC-DC regulator is not used, this pin must be treated as a VSS pin. |

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## 4.3 Signal Descriptions

### 4.3.1 Analog Signals

**Table 4-2. Analog Signals**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| A0 | ADC-A Input 0 | I | | 23 | 15 | 15 | 13 |
| A1 | ADC-A Input 1 | I | | 22 | 14 | 14 | 12 |
| A2 | ADC-A Input 2 | I | | 9 | 9 | 9 | 8 |
| A3 | ADC-A Input 3 | I | | 10 | | | |
| A4 | ADC-A Input 4 | I | | 36 | 23 | 23 | 21 |
| A5 | ADC-A Input 5 | I | | 35 | | | |
| A6 | ADC-A Input 6 | I | | 6 | 6 | 6 | |
| A8 | ADC-A Input 8 | I | | 37 | | | |
| A9 | ADC-A Input 9 | I | | 38 | | | |
| A10 | ADC-A Input 10 | I | | 40 | 25 | 25 | 23 |
| AIO224 | Digital Input-224 on ADC Pin | I | | 9 | 9 | 9 | 8 |
| AIO225 | Digital Input-225 on ADC Pin | I | | 36 | 23 | 23 | 21 |
| AIO226 | Digital Input-226 on ADC Pin | I | | 7 | 7 | 7 | 6 |
| AIO227 | Digital Input-227 on ADC Pin | I | | 39 | 24 | 24 | 22 |
| AIO228 | Digital Input-228 on ADC Pin | I | | 6 | 6 | 6 | |
| AIO229 | Digital Input-229 on ADC Pin | I | | 37 | | | |
| AIO230 | Digital Input-230 on ADC Pin | I | | 40 | 25 | 25 | 23 |
| AIO231 | Digital Input-231 on ADC Pin | I | | 23 | 15 | 15 | 13 |
| AIO232 | Digital Input-232 on ADC Pin | I | | 22 | 14 | 14 | 12 |
| AIO233 | Digital Input-233 on ADC Pin | I | | 10 | | | |
| AIO234 | Digital Input-234 on ADC Pin | I | | 35 | | | |
| AIO236 | Digital Input-236 on ADC Pin | I | | 38 | | | |
| AIO237 | Digital Input-237 on ADC Pin | I | | 19 | 12 | 12 | 10 |
| AIO238 | Digital Input-238 on ADC Pin | I | | 29 | 18 | 18 | 16 |
| AIO239 | Digital Input-239 on ADC Pin | I | | 17 | 11 | 11 | |
| AIO240 | Digital Input-240 on ADC Pin | I | | 28 | | | |
| AIO241 | Digital Input-241 on ADC Pin | I | | 41 | | | |
| AIO242 | Digital Input-242 on ADC Pin | I | | 8 | 8 | 8 | 7 |
| AIO244 | Digital Input-244 on ADC Pin | I | | 21 | 13 | 13 | 11 |
| AIO245 | Digital Input-245 on ADC Pin | I | | 31 | 19 | 19 | 17 |
| AIO246 | Digital Input-246 on ADC Pin | I | | 44 | | | |
| B0 | ADC-B Input 0 | I | | 41 | | | |
| B1 | ADC-B Input 1 | I | | 40 | 25 | 25 | 23 |
| B2 | ADC-B Input 2 | I | | 7 | 7 | 7 | 6 |
| B3 | ADC-B Input 3 | I | | 8 | 8 | 8 | 7 |
| B4 | ADC-B Input 4 | I | | 39 | 24 | 24 | 22 |
| B6 | ADC-B Input 6 | I | | 9 | 9 | 9 | 8 |
| B8 | ADC-B Input 8 | I | | 36 | 23 | 23 | 21 |
| B15 | ADC-B Input 15 | I | | 23 | 15 | 15 | 13 |
| C0 | ADC-C Input 0 | I | | 19 | 12 | 12 | 10 |
| C1 | ADC-C Input 1 | I | | 29 | 18 | 18 | 16 |
| C2 | ADC-C Input 2 | I | | 21 | 13 | 13 | 11 |
| C3 | ADC-C Input 3 | I | | 31 | 19 | 19 | 17 |


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**Table 4-2. Analog Signals (continued)**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| C4 | ADC-C Input 4 | I | | 17 | 11 | 11 | |
| C5 | ADC-C Input 5 | I | | 28 | | | |
| C6 | ADC-C Input 6 | I | | 7 | 7 | 7 | 6 |
| C8 | ADC-C Input 8 | I | | 39 | 24 | 24 | 22 |
| C10 | ADC-C Input 10 | I | | 40 | 25 | 25 | 23 |
| C14 | ADC-C Input 14 | I | | 44 | | | |
| C15 | ADC-C Input 15 | I | | 23 | 15 | 15 | 13 |
| CMP1_HN0 | CMPSS-1 High Comparator Negative Input 0 | I | | 10 | | | |
| CMP1_HN1 | CMPSS-1 High Comparator Negative Input 1 | I | | 19 | 12 | 12 | 10 |
| CMP1_HP0 | CMPSS-1 High Comparator Positive Input 0 | I | | 9 | 9 | 9 | 8 |
| CMP1_HP1 | CMPSS-1 High Comparator Positive Input 1 | I | | 19 | 12 | 12 | 10 |
| CMP1_HP2 | CMPSS-1 High Comparator Positive Input 2 | I | | 18 | 12 | 12 | 10 |
| CMP1_HP3 | CMPSS-1 High Comparator Positive Input 3 | I | | 10 | | | |
| CMP1_LN0 | CMPSS-1 Low Comparator Negative Input 0 | I | | 10 | | | |
| CMP1_LN1 | CMPSS-1 Low Comparator Negative Input 1 | I | | 19 | 12 | 12 | 10 |
| CMP1_LP0 | CMPSS-1 Low Comparator Positive Input 0 | I | | 9 | 9 | 9 | 8 |
| CMP1_LP1 | CMPSS-1 Low Comparator Positive Input 1 | I | | 19 | 12 | 12 | 10 |
| CMP1_LP2 | CMPSS-1 Low Comparator Positive Input 2 | I | | 18 | 12 | 12 | 10 |
| CMP1_LP3 | CMPSS-1 Low Comparator Positive Input 3 | I | | 10 | | | |
| CMP2_HN0 | CMPSS-2 High Comparator Negative Input 0 | I | | 35 | | | |
| CMP2_HN1 | CMPSS-2 High Comparator Negative Input 1 | I | | 29 | 18 | 18 | 16 |
| CMP2_HP0 | CMPSS-2 High Comparator Positive Input 0 | I | | 36 | 23 | 23 | 21 |
| CMP2_HP1 | CMPSS-2 High Comparator Positive Input 1 | I | | 29 | 18 | 18 | 16 |
| CMP2_HP2 | CMPSS-2 High Comparator Positive Input 2 | I | | 30 | 18 | 18 | 16 |
| CMP2_HP3 | CMPSS-2 High Comparator Positive Input 3 | I | | 35 | | | |
| CMP2_LN0 | CMPSS-2 Low Comparator Negative Input 0 | I | | 35 | | | |
| CMP2_LN1 | CMPSS-2 Low Comparator Negative Input 1 | I | | 29 | 18 | 18 | 16 |
| CMP2_LP0 | CMPSS-2 Low Comparator Positive Input 0 | I | | 36 | 23 | 23 | 21 |
| CMP2_LP1 | CMPSS-2 Low Comparator Positive Input 1 | I | | 29 | 18 | 18 | 16 |
| CMP2_LP2 | CMPSS-2 Low Comparator Positive Input 2 | I | | 30 | 18 | 18 | 16 |
| CMP2_LP3 | CMPSS-2 Low Comparator Positive Input 3 | I | | 35 | | | |
| CMP3_HN0 | CMPSS-3 High Comparator Negative Input 0 | I | | 8 | 8 | 8 | 7 |
| CMP3_HN1 | CMPSS-3 High Comparator Negative Input 1 | I | | 21 | 13 | 13 | 11 |
| CMP3_HP0 | CMPSS-3 High Comparator Positive Input 0 | I | | 7 | 7 | 7 | 6 |
| CMP3_HP1 | CMPSS-3 High Comparator Positive Input 1 | I | | 21 | 13 | 13 | 11 |
| CMP3_HP2 | CMPSS-3 High Comparator Positive Input 2 | I | | 20 | 13 | 13 | 11 |
| CMP3_HP3 | CMPSS-3 High Comparator Positive Input 3 | I | | 8 | 8 | 8 | 7 |
| CMP3_LN0 | CMPSS-3 Low Comparator Negative Input 0 | I | | 8 | 8 | 8 | 7 |
| CMP3_LN1 | CMPSS-3 Low Comparator Negative Input 1 | I | | 21 | 13 | 13 | 11 |
| CMP3_LP0 | CMPSS-3 Low Comparator Positive Input 0 | I | | 7 | 7 | 7 | 6 |
| CMP3_LP1 | CMPSS-3 Low Comparator Positive Input 1 | I | | 21 | 13 | 13 | 11 |
| CMP3_LP2 | CMPSS-3 Low Comparator Positive Input 2 | I | | 20 | 13 | 13 | 11 |
| CMP3_LP3 | CMPSS-3 Low Comparator Positive Input 3 | I | | 8 | 8 | 8 | 7 |
| CMP4_HN1 | CMPSS-4 High Comparator Negative Input 1 | I | | 31 | 19 | 19 | 17 |
| CMP4_HP0 | CMPSS-4 High Comparator Positive Input 0 | I | | 39 | 24 | 24 | 22 |
| CMP4_HP1 | CMPSS-4 High Comparator Positive Input 1 | I | | 31 | 19 | 19 | 17 |
| CMP4_HP2 | CMPSS-4 High Comparator Positive Input 2 | I | | 31 | 19 | 19 | 17 |

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**Table 4-2. Analog Signals (continued)**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| CMP4_LN1 | CMPSS-4 Low Comparator Negative Input 1 | I | | 31 | 19 | 19 | 17 |
| CMP4_LP0 | CMPSS-4 Low Comparator Positive Input 0 | I | | 39 | 24 | 24 | 22 |
| CMP4_LP1 | CMPSS-4 Low Comparator Positive Input 1 | I | | 31 | 19 | 19 | 17 |
| CMP4_LP2 | CMPSS-4 Low Comparator Positive Input 2 | I | | 31 | 19 | 19 | 17 |
| CMP5_HN1 | CMPSS-5 High Comparator Negative Input 1 | I | | 17 | 11 | 11 | |
| CMP5_HP0 | CMPSS-5 High Comparator Positive Input 0 | I | | 6 | 6 | 6 | |
| CMP5_HP1 | CMPSS-5 High Comparator Positive Input 1 | I | | 17 | 11 | 11 | |
| CMP5_HP2 | CMPSS-5 High Comparator Positive Input 2 | I | | 16 | 11 | 11 | |
| CMP5_LN1 | CMPSS-5 Low Comparator Negative Input 1 | I | | 17 | 11 | 11 | |
| CMP5_LP0 | CMPSS-5 Low Comparator Positive Input 0 | I | | 6 | 6 | 6 | |
| CMP5_LP1 | CMPSS-5 Low Comparator Positive Input 1 | I | | 17 | 11 | 11 | |
| CMP5_LP2 | CMPSS-5 Low Comparator Positive Input 2 | I | | 16 | 11 | 11 | |
| CMP6_HN0 | CMPSS-6 High Comparator Negative Input 0 | I | | 38 | | | |
| CMP6_HN1 | CMPSS-6 High Comparator Negative Input 1 | I | | 28 | | | |
| CMP6_HP0 | CMPSS-6 High Comparator Positive Input 0 | I | | 37 | | | |
| CMP6_HP1 | CMPSS-6 High Comparator Positive Input 1 | I | | 28 | | | |
| CMP6_HP2 | CMPSS-6 High Comparator Positive Input 2 | I | | 28 | | | |
| CMP6_HP3 | CMPSS-6 High Comparator Positive Input 3 | I | | 38 | | | |
| CMP6_LN0 | CMPSS-6 Low Comparator Negative Input 0 | I | | 38 | | | |
| CMP6_LN1 | CMPSS-6 Low Comparator Negative Input 1 | I | | 28 | | | |
| CMP6_LP0 | CMPSS-6 Low Comparator Positive Input 0 | I | | 37 | | | |
| CMP6_LP1 | CMPSS-6 Low Comparator Positive Input 1 | I | | 28 | | | |
| CMP6_LP2 | CMPSS-6 Low Comparator Positive Input 2 | I | | 28 | | | |
| CMP6_LP3 | CMPSS-6 Low Comparator Positive Input 3 | I | | 38 | | | |
| CMP7_HN0 | CMPSS-7 High Comparator Negative Input 0 | I | | 41 | | | |
| CMP7_HN1 | CMPSS-7 High Comparator Negative Input 1 | I | | 44 | | | |
| CMP7_HP0 | CMPSS-7 High Comparator Positive Input 0 | I | | 40 | 25 | 25 | 23 |
| CMP7_HP1 | CMPSS-7 High Comparator Positive Input 1 | I | | 44 | | | |
| CMP7_HP2 | CMPSS-7 High Comparator Positive Input 2 | I | | 43 | | | |
| CMP7_HP3 | CMPSS-7 High Comparator Positive Input 3 | I | | 41 | | | |
| CMP7_LN0 | CMPSS-7 Low Comparator Negative Input 0 | I | | 41 | | | |
| CMP7_LN1 | CMPSS-7 Low Comparator Negative Input 1 | I | | 44 | | | |
| CMP7_LP0 | CMPSS-7 Low Comparator Positive Input 0 | I | | 40 | 25 | 25 | 23 |
| CMP7_LP1 | CMPSS-7 Low Comparator Positive Input 1 | I | | 44 | | | |
| CMP7_LP2 | CMPSS-7 Low Comparator Positive Input 2 | I | | 43 | | | |
| CMP7_LP3 | CMPSS-7 Low Comparator Positive Input 3 | I | | 41 | | | |
| DACA_OUT | Buffered DAC-A Output | O | | 23 | 15 | 15 | 13 |
| DACB_OUT | Buffered DAC-B Output | O | | 22 | 14 | 14 | 12 |
| PGA1_GND | PGA-1 Ground | I | | 14 | 10 | 10 | 9 |
| PGA1_IN | PGA-1 Input | I | | 18 | 12 | 12 | 10 |
| PGA1_OF | PGA-1 Output Filter (Optional) | O | | 9 | 9 | 9 | 8 |
| PGA2_GND | PGA-2 Ground | I | | 32 | 20 | 20 | 18 |
| PGA2_IN | PGA-2 Input | I | | 30 | 18 | 18 | 16 |
| PGA2_OF | PGA-2 Output Filter (Optional) | O | | 36 | 23 | 23 | 21 |
| PGA3_GND | PGA-3 Ground | I | | 15 | 10 | 10 | 9 |
| PGA3_IN | PGA-3 Input | I | | 20 | 13 | 13 | 11 |
| PGA3_OF | PGA-3 Output Filter (Optional) | O | | 7 | 7 | 7 | 6 |


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**Table 4-2. Analog Signals (continued)**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| PGA4_GND | PGA-4 Ground | I | | 32 | 20 | 20 | 18 |
| PGA4_IN | PGA-4 Input | I | | 31 | 19 | 19 | 17 |
| PGA4_OF | PGA-4 Output Filter (Optional) | O | | 39 | 24 | 24 | 22 |
| PGA5_GND | PGA-5 Ground | I | | 13 | 10 | 10 | 9 |
| PGA5_IN | PGA-5 Input | I | | 16 | 11 | 11 | |
| PGA5_OF | PGA-5 Output Filter (Optional) | O | | 6 | 6 | 6 | |
| PGA6_GND | PGA-6 Ground | I | | 32 | 20 | 20 | 18 |
| PGA6_IN | PGA-6 Input | I | | 28 | | | |
| PGA6_OF | PGA-6 Output Filter (Optional) | O | | 37 | | | |
| PGA7_GND | PGA-7 Ground | I | | 42 | | | |
| PGA7_IN | PGA-7 Input | I | | 43 | | | |
| PGA7_OF | PGA-7 Output Filter (Optional) | O | | 40 | 25 | 25 | 23 |
| VDAC | Optional external reference voltage for on-chip DACs. There is a 100-pF capacitor to VSSA on this pin whether used for ADC input or DAC reference which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-µF capacitor on this pin. | I | | 8 | 8 | 8 | 7 |
| VREFHIA | ADC-A High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHIA and VREFLOA pins. Do not load this pin externally in either internal or external reference mode. | I/O | | 25 | 16 | 16 | 14 |
| VREFHIB | ADC-B High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHIB and VREFLOB pins. Do not load this pin externally in either internal or external reference mode. | I/O | | 24 | 16 | 16 | 14 |
| VREFHIC | ADC-C High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHIC and VREFLOC pins. Do not load this pin externally in either internal or external reference mode. | I/O | | 24 | 16 | 16 | 14 |
| VREFLOA | ADC-A Low Reference | I | | 27 | 17 | 17 | 15 |
| VREFLOB | ADC-B Low Reference | I | | 26 | 17 | 17 | 15 |
| VREFLOC | ADC-C Low Reference | I | | 26 | 17 | 17 | 15 |

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### 4.3.2 Digital Signals

**Table 4-3. Digital Signals**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| ADCSOCAO | ADC Start of Conversion A Output for External ADC (from ePWM modules) | O | 8 | 74 | 47 | 47 | 42 |
| ADCSOCBO | ADC Start of Conversion B Output for External ADC (from ePWM modules) | O | 10 | 93 | 63 | 63 | |
| CANA_RX | CAN-A Receive | I | 18, 30, 33, 35, 5 | 53, 63, 68, 89, 98 | 32, 39, 41, 61 | 32, 39, 41, 61 | 29, 36, 38, 55 |
| CANA_TX | CAN-A Transmit | O | 31, 32, 37, 4 | 61, 64, 75, 99 | 37, 40, 48 | 37, 40, 48 | 34, 37, 43 |
| CANB_RX | CAN-B Receive | I | 10, 13, 17, 39, 59, 7 | 50, 55, 84, 91, 92, 93 | 34, 57, 63 | 29, 34, 57, 63 | 26, 31, 52 |
| CANB_TX | CAN-B Transmit | O | 12, 16, 58, 6, 8 | 51, 54, 67, 74, 97 | 33, 47, 64 | 30, 33, 47, 64 | 1, 27, 30, 42 |
| EPWM1_A | ePWM-1 Output A | O | 0 | 79 | 52 | 52 | 47 |
| EPWM1_B | ePWM-1 Output B | O | 1 | 78 | 51 | 51 | 46 |
| EPWM2_A | ePWM-2 Output A | O | 2 | 77 | 50 | 50 | 45 |
| EPWM2_B | ePWM-2 Output B | O | 3 | 76 | 49 | 49 | 44 |
| EPWM3_A | ePWM-3 Output A | O | 4 | 75 | 48 | 48 | 43 |
| EPWM3_B | ePWM-3 Output B | O | 5 | 89 | 61 | 61 | 55 |
| EPWM4_A | ePWM-4 Output A | O | 6 | 97 | 64 | 64 | 1 |
| EPWM4_B | ePWM-4 Output B | O | 7 | 84 | 57 | 57 | 52 |
| EPWM5_A | ePWM-5 Output A | O | 16, 8 | 54, 74 | 33, 47 | 33, 47 | 30, 42 |
| EPWM5_B | ePWM-5 Output B | O | 17, 9 | 55, 90 | 34, 62 | 34, 62 | 31, 56 |
| EPWM6_A | ePWM-6 Output A | O | 10, 18 | 68, 93 | 41, 63 | 41, 63 | 38 |
| EPWM6_B | ePWM-6 Output B | O | 11 | 52 | 31 | 31 | 28 |
| EPWM7_A | ePWM-7 Output A | O | 12, 28 | 1, 51 | 2 | 2, 30 | 27, 3 |
| EPWM7_B | ePWM-7 Output B | O | 13, 29 | 100, 50 | 1 | 1, 29 | 2, 26 |
| EPWM8_A | ePWM-8 Output A | O | 14, 24 | 56, 96 | 35 | 35 | 32 |
| EPWM8_B | ePWM-8 Output B | O | 15, 32 | 64, 95 | 40 | 40 | 37 |
| EQEP1_A | eQEP-1 Input A | I | 10, 28, 35, 40, 56, 6 | 1, 63, 65, 85, 93, 97 | 2, 39, 63, 64 | 2, 39, 63, 64 | 1, 3, 36 |
| EQEP1_B | eQEP-1 Input B | I | 11, 29, 37, 57, 7 | 100, 52, 61, 66, 84 | 1, 31, 37, 57 | 1, 31, 37, 57 | 2, 28, 34, 52 |
| EQEP1_INDEX | eQEP-1 Index | I/O | 13, 17, 31, 59, 9 | 50, 55, 90, 92, 99 | 34, 62 | 29, 34, 62 | 26, 31, 56 |
| EQEP1_STROBE | eQEP-1 Strobe | I/O | 12, 16, 22, 30, 58, 8 | 51, 54, 67, 74, 83, 98 | 33, 47, 56 | 30, 33, 47, 56 | 27, 30, 42, 51 |
| EQEP2_A | eQEP-2 Input A | I | 14, 18, 24 | 56, 68, 96 | 35, 41 | 35, 41 | 32, 38 |
| EQEP2_B | eQEP-2 Input B | I | 15, 25 | 57, 95 | | | |
| EQEP2_INDEX | eQEP-2 Index | I/O | 26, 29, 57 | 100, 58, 66 | 1 | 1 | 2 |
| EQEP2_STROBE | eQEP-2 Strobe | I/O | 27, 28, 56 | 1, 59, 65 | 2 | 2 | 3 |


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**Table 4-3. Digital Signals (continued)**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| ERRORSTS | Error Status Output. This signal requires an external pullup. | O | 24, 28, 29 | 1, 100, 56 | 1, 2, 35 | 1, 2, 35 | 2, 3, 32 |
| FSIRXA_CLK | FSIRX-A Input Clock | I | 13, 33, 39, 4 | 50, 53, 75, 91 | 32, 48 | 29, 32, 48 | 26, 29, 43 |
| FSIRXA_D0 | FSIRX-A Primary Data Input | I | 12, 3, 32, 40 | 51, 64, 76, 85 | 40, 49 | 30, 40, 49 | 27, 37, 44 |
| FSIRXA_D1 | FSIRX-A Optional Additional Data Input | I | 11, 2, 31 | 52, 77, 99 | 31, 50 | 31, 50 | 28, 45 |
| FSITXA_CLK | FSITX-A Output Clock | O | 10, 27, 7 | 59, 84, 93 | 57, 63 | 57, 63 | 52 |
| FSITXA_D0 | FSITX-A Primary Data Output | O | 26, 6, 9 | 58, 90, 97 | 62, 64 | 62, 64 | 1, 56 |
| FSITXA_D1 | FSITX-A Optional Additional Data Output | O | 25, 5, 8 | 57, 74, 89 | 47, 61 | 47, 61 | 42, 55 |
| GPIO0 | General-Purpose Input Output 0 | I/O | 0 | 79 | 52 | 52 | 47 |
| GPIO1 | General-Purpose Input Output 1 | I/O | 1 | 78 | 51 | 51 | 46 |
| GPIO2 | General-Purpose Input Output 2 | I/O | 2 | 77 | 50 | 50 | 45 |
| GPIO3 | General-Purpose Input Output 3 | I/O | 3 | 76 | 49 | 49 | 44 |
| GPIO4 | General-Purpose Input Output 4 | I/O | 4 | 75 | 48 | 48 | 43 |
| GPIO5 | General-Purpose Input Output 5 | I/O | 5 | 89 | 61 | 61 | 55 |
| GPIO6 | General-Purpose Input Output 6 | I/O | 6 | 97 | 64 | 64 | 1 |
| GPIO7 | General-Purpose Input Output 7 | I/O | 7 | 84 | 57 | 57 | 52 |
| GPIO8 | General-Purpose Input Output 8 | I/O | 8 | 74 | 47 | 47 | 42 |
| GPIO9 | General-Purpose Input Output 9 | I/O | 9 | 90 | 62 | 62 | 56 |
| GPIO10 | General-Purpose Input Output 10 | I/O | 10 | 93 | 63 | 63 | |
| GPIO11 | General-Purpose Input Output 11 | I/O | 11 | 52 | 31 | 31 | 28 |
| GPIO12 | General-Purpose Input Output 12 | I/O | 12 | 51 | | 30 | 27 |
| GPIO13 | General-Purpose Input Output 13 | I/O | 13 | 50 | | 29 | 26 |
| GPIO14 | General-Purpose Input Output 14 | I/O | 14 | 96 | | | |
| GPIO15 | General-Purpose Input Output 15 | I/O | 15 | 95 | | | |
| GPIO16 | General-Purpose Input Output 16 | I/O | 16 | 54 | 33 | 33 | 30 |
| GPIO17 | General-Purpose Input Output 17 | I/O | 17 | 55 | 34 | 34 | 31 |
| GPIO18_X2 | General-Purpose Input Output 18. This pin and its digital mux options can only be used when the system is clocked by INTOSC and X1 has an external pulldown resistor (recommended 1 kΩ). | I/O | 18 | 68 | 41 | 41 | 38 |
| GPIO20 | General-Purpose Input Output 20 | I/O | 20 | | | | |
| GPIO21 | General-Purpose Input Output 21 | I/O | 21 | | | | |
| GPIO22_VFBSW | General-Purpose Input Output 22. This pin is configured for DC-DC mode by default. If the internal DC-DC regulator is not used, this can be configured as General-Purpose Input Output 22 by disabling DC-DC and clearing their bits in GPAAMSEL register. | I/O | 22 | 83 | 56 | 56 | 51 |

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**Table 4-3. Digital Signals (continued)**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| GPIO23_VSW | General-Purpose Input Output 23. This pin is configured for DC-DC mode by default. If the internal DC-DC regulator is not used, this can be configured as General-Purpose Input Output 23 by disabling DC-DC and clearing their bits in GPAAMSEL register. This pin has an internal capacitance of approximately 100 pF. TI Recommends using an alternate GPIO, or using this pin only for applications which do not require a fast switching response. | I/O | 23 | 81 | 54 | 54 | 49 |
| GPIO24 | General-Purpose Input Output 24 | I/O | 24 | 56 | 35 | 35 | 32 |
| GPIO25 | General-Purpose Input Output 25 | I/O | 25 | 57 | | | |
| GPIO26 | General-Purpose Input Output 26 | I/O | 26 | 58 | | | |
| GPIO27 | General-Purpose Input Output 27 | I/O | 27 | 59 | | | |
| GPIO28 | General-Purpose Input Output 28 | I/O | 28 | 1 | 2 | 2 | 3 |
| GPIO29 | General-Purpose Input Output 29 | I/O | 29 | 100 | 1 | 1 | 2 |
| GPIO30 | General-Purpose Input Output 30 | I/O | 30 | 98 | | | |
| GPIO31 | General-Purpose Input Output 31 | I/O | 31 | 99 | | | |
| GPIO32 | General-Purpose Input Output 32 | I/O | 32 | 64 | 40 | 40 | 37 |
| GPIO33 | General-Purpose Input Output 33 | I/O | 33 | 53 | 32 | 32 | 29 |
| GPIO34 | General-Purpose Input Output 34 | I/O | 34 | 94 | | | |
| GPIO35 | General-Purpose Input Output 35 | I/O | 35 | 63 | 39 | 39 | 36 |
| GPIO37 | General-Purpose Input Output 37 | I/O | 37 | 61 | 37 | 37 | 34 |
| GPIO39 | General-Purpose Input Output 39 | I/O | 39 | 91 | | | |
| GPIO40 | General-Purpose Input Output 40 | I/O | 40 | 85 | | | |
| GPIO41 | General-Purpose Input Output 41 | I/O | 41 | | | | |
| GPIO42 | General-Purpose Input Output 42 | I/O | 42 | | | | |
| GPIO43 | General-Purpose Input Output 43 | I/O | 43 | | | | |
| GPIO44 | General-Purpose Input Output 44 | I/O | 44 | | | | |
| GPIO45 | General-Purpose Input Output 45 | I/O | 45 | | | | |
| GPIO46 | General-Purpose Input Output 46 | I/O | 46 | | | | |
| GPIO47 | General-Purpose Input Output 47 | I/O | 47 | | | | |
| GPIO48 | General-Purpose Input Output 48 | I/O | 48 | | | | |
| GPIO49 | General-Purpose Input Output 49 | I/O | 49 | | | | |
| GPIO50 | General-Purpose Input Output 50 | I/O | 50 | | | | |
| GPIO51 | General-Purpose Input Output 51 | I/O | 51 | | | | |
| GPIO52 | General-Purpose Input Output 52 | I/O | 52 | | | | |
| GPIO53 | General-Purpose Input Output 53 | I/O | 53 | | | | |
| GPIO54 | General-Purpose Input Output 54 | I/O | 54 | | | | |
| GPIO55 | General-Purpose Input Output 55 | I/O | 55 | | | | |
| GPIO56 | General-Purpose Input Output 56 | I/O | 56 | 65 | | | |
| GPIO57 | General-Purpose Input Output 57 | I/O | 57 | 66 | | | |
| GPIO58 | General-Purpose Input Output 58 | I/O | 58 | 67 | | | |
| GPIO59 | General-Purpose Input Output 59 | I/O | 59 | 92 | | | |
| I2CA_SCL | I2C-A Open-Drain Bidirectional Clock | I/OD | 1, 18, 27, 33, 37, 8 | 53, 59, 61, 68, 74, 78 | 32, 37, 41, 47, 51 | 32, 37, 41, 47, 51 | 29, 34, 38, 42, 46 |
| I2CA_SDA | I2C-A Open-Drain Bidirectional Data | I/OD | 0, 10, 26, 32, 35 | 58, 63, 64, 79, 93 | 39, 40, 52, 63 | 39, 40, 52, 63 | 36, 37, 47 |


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**Table 4-3. Digital Signals (continued)**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| LINA_RX | LIN-A Receive | I | 29, 33, 35, 59 | 100, 53, 63, 92 | 1, 32, 39 | 1, 32, 39 | 2, 29, 36 |
| LINA_TX | LIN-A Transmit | O | 22, 28, 32, 37, 58 | 1, 61, 64, 67, 83 | 2, 37, 40, 56 | 2, 37, 40, 56 | 3, 34, 37, 51 |
| OUTPUTXBAR1 | Output X-BAR Output 1 | O | 2, 24, 34, 58 | 56, 67, 77, 94 | 35, 50 | 35, 50 | 32, 45 |
| OUTPUTXBAR2 | Output X-BAR Output 2 | O | 25, 3, 37, 59 | 57, 61, 76, 92 | 37, 49 | 37, 49 | 34, 44 |
| OUTPUTXBAR3 | Output X-BAR Output 3 | O | 14, 26, 4, 5 | 58, 75, 89, 96 | 48, 61 | 48, 61 | 43, 55 |
| OUTPUTXBAR4 | Output X-BAR Output 4 | O | 15, 27, 33, 6 | 53, 59, 95, 97 | 32, 64 | 32, 64 | 1, 29 |
| OUTPUTXBAR5 | Output X-BAR Output 5 | O | 28, 7 | 1, 84 | 2, 57 | 2, 57 | 3, 52 |
| OUTPUTXBAR6 | Output X-BAR Output 6 | O | 29, 9 | 100, 90 | 1, 62 | 1, 62 | 2, 56 |
| OUTPUTXBAR7 | Output X-BAR Output 7 | O | 11, 16, 30 | 52, 54, 98 | 31, 33 | 31, 33 | 28, 30 |
| OUTPUTXBAR8 | Output X-BAR Output 8 | O | 17, 31 | 55, 99 | 34 | 34 | 31 |
| PMBUSA_ALERT | PMBus-A Open-Drain Bidirectional Alert Signal | I/OD | 13, 27, 37 | 50, 59, 61 | 37 | 29, 37 | 26, 34 |
| PMBUSA_CTL | PMBus-A Control Signal | I | 12, 18, 26, 35 | 51, 58, 63, 68 | 39, 41 | 30, 39, 41 | 27, 36, 38 |
| PMBUSA_SCL | PMBus-A Open-Drain Bidirectional Clock | I/OD | 15, 16, 24, 3, 35 | 54, 56, 63, 76, 95 | 33, 35, 39, 49 | 33, 35, 39, 49 | 30, 32, 36, 44 |
| PMBUSA_SDA | PMBus-A Open-Drain Bidirectional Data | I/OD | 14, 17, 2, 25, 34, 40 | 55, 57, 77, 85, 94, 96 | 34, 50 | 34, 50 | 31, 45 |
| SCIA_RX | SCI-A Receive Data | I | 17, 25, 28, 3, 35, 9 | 1, 55, 57, 63, 76, 90 | 2, 34, 39, 49, 62 | 2, 34, 39, 49, 62 | 3, 31, 36, 44, 56 |
| SCIA_TX | SCI-A Transmit Data | O | 16, 2, 24, 29, 37, 8 | 100, 54, 56, 61, 74, 77 | 1, 33, 35, 37, 47, 50 | 1, 33, 35, 37, 47, 50 | 2, 30, 32, 34, 42, 45 |
| SCIB_RX | SCI-B Receive Data | I | 11, 13, 15, 57 | 50, 52, 66, 95 | 31 | 29, 31 | 26, 28 |
| SCIB_TX | SCI-B Transmit Data | O | 10, 12, 14, 18, 22, 40, 56, 9 | 51, 65, 68, 83, 85, 90, 93, 96 | 41, 56, 62, 63 | 30, 41, 56, 62, 63 | 27, 38, 51, 56 |
| SD1_C1 | SDFM-1 Channel 1 Clock Input | I | 17, 25 | 55, 57 | 34 | 34 | 31 |
| SD1_C2 | SDFM-1 Channel 2 Clock Input | I | 27 | 59 | | | |
| SD1_C3 | SDFM-1 Channel 3 Clock Input | I | 29, 33, 57 | 100, 53, 66 | 1, 32 | 1, 32 | 2, 29 |
| SD1_C4 | SDFM-1 Channel 4 Clock Input | I | 31, 59 | 92, 99 | | | |
| SD1_D1 | SDFM-1 Channel 1 Data Input | I | 16, 24 | 54, 56 | 33, 35 | 33, 35 | 30, 32 |
| SD1_D2 | SDFM-1 Channel 2 Data Input | I | 18, 26 | 58, 68 | 41 | 41 | 38 |
| SD1_D3 | SDFM-1 Channel 3 Data Input | I | 28, 32, 56 | 1, 64, 65 | 2, 40 | 2, 40 | 3, 37 |
| SD1_D4 | SDFM-1 Channel 4 Data Input | I | 22, 30, 58 | 67, 83, 98 | 56 | 56 | 51 |
| SPIA_CLK | SPI-A Clock | I/O | 18, 3, 56, 9 | 65, 68, 76, 90 | 41, 49, 62 | 41, 49, 62 | 38, 44, 56 |
| SPIA_SIMO | SPI-A Slave In, Master Out (SIMO) | I/O | 16, 8 | 54, 74 | 33, 47 | 33, 47 | 30, 42 |
| SPIA_SOMI | SPI-A Slave Out, Master In (SOMI) | I/O | 10, 17 | 55, 93 | 34, 63 | 34, 63 | 31 |

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**Table 4-3. Digital Signals (continued)**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| SPIA_STE | SPI-A Slave Transmit Enable (STE) | I/O | 11, 5, 57 | 52, 66, 89 | 31, 61 | 31, 61 | 28, 55 |
| SPIB_CLK | SPI-B Clock | I/O | 14, 22, 26, 28, 32, 58 | 1, 58, 64, 67, 83, 96 | 2, 40, 56 | 2, 40, 56 | 3, 37, 51 |
| SPIB_SIMO | SPI-B Slave In, Master Out (SIMO) | I/O | 24, 30, 56, 7 | 56, 65, 84, 98 | 35, 57 | 35, 57 | 32, 52 |
| SPIB_SOMI | SPI-B Slave Out, Master In (SOMI) | I/O | 25, 31, 57, 6 | 57, 66, 97, 99 | 64 | 64 | 1 |
| SPIB_STE | SPI-B Slave Transmit Enable (STE) | I/O | 15, 27, 29, 33, 59 | 100, 53, 59, 92, 95 | 1, 32 | 1, 32 | 2, 29 |
| SYNCOUT | External ePWM Synchronization Pulse | O | 6 | 97 | 64 | 64 | 1 |
| TDI | JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input. | I | 35 | 63 | 39 | 39 | 36 |
| TDO | JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. | O | 37 | 61 | 37 | 37 | 34 |
| VFBSW | Internal DC-DC regulator feedback signal. If the internal DC-DC regulator is used, tie this pin to the node where L(VSW) connects to the VDD rail (as close as possible to the device). | - | 22 | 83 | 56 | 56 | 51 |
| VSW | Switching output of the internal DC-DC regulator | - | 23 | 81 | 54 | 54 | 49 |
| X2 | Crystal oscillator output | I/O | 18 | 68 | 41 | 41 | 38 |
| XCLKOUT | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. | O | 16, 18 | 54, 68 | 33, 41 | 33, 41 | 30, 38 |


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### 4.3.3 Power and Ground

**Table 4-4. Power and Ground**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| VDD | 1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 20 µF. When not using the internal voltage regulator, the exact value of the decoupling capacitance should be determined by your system voltage regulation solution. | | | 4, 46, 71, 87 | 27, 4, 44, 59 | 27, 4, 44, 59 | 24, 41, 5, 53 |
| VDDA | 3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor to VSSA on each pin. | | | 11, 34 | 22 | 22 | 20 |
| VDDIO | 3.3-V Digital I/O Power Pins. Place a minimum 0.1-µF decoupling capacitor on each pin. | | | 3, 47, 70, 88 | 28, 43, 60 | 28, 43, 60 | 25, 40, 54 |
| VDDIO_SW | 3.3-V Supply pin for the internal DC-DC regulator. If the internal DC-DC regulator is used, a bulk input capacitance of 20-µF should be placed on this pin. If the internal DC-DC regulator is not used, this pin should be treated as a VDDIO pin. | | | 80 | 53 | 53 | 48 |
| VSS | Digital Ground | | | 45, 5, 72, 86 | 26, 45, 5, 58 | 26, 45, 5, 58 | PAD |
| VSSA | Analog Ground | | | 12, 33 | 21 | 21 | 19 |
| VSS_SW | Internal DC-DC regulator ground. If the internal DC-DC regulator is not used, this pin must be treated as a VSS pin. | | | 82 | 55 | 55 | 50 |

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### 4.3.4 Test, JTAG, Voltage Regulator, and Reset

**Table 4-5. Test, JTAG, Voltage Regulator, and Reset**

| SIGNAL NAME | DESCRIPTION | PIN TYPE | GPIO | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|---|
| FLT1 | Flash test pin 1. Reserved for TI. Must be left unconnected. | I/O | | 49 | 30 | | |
| FLT2 | Flash test pin 2. Reserved for TI. Must be left unconnected. | I/O | | 48 | 29 | | |
| TCK | JTAG test clock with internal pullup. | I | | 60 | 36 | 36 | 33 |
| TMS | JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation. | I | | 62 | 38 | 38 | 35 |
| VREGENZ | Internal voltage regulator enable with internal pulldown. Tie directly to VSS (low) to enable the internal VREG. Tie directly to VDDIO (high) to use an external supply. | I | | 73 | 46 | 46 | |
| X1 | Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock. GPIO19 is not supported. Internally GPIO19 is connected to the X1 function, therefore the GPIO19 should be kept in Input Mode with the Pullup disabled to avoid interference with the X1 clock function. | I/O | | 69 | 42 | 42 | 39 |
| XRSn | Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. The output buffer of this pin is an open-drain with an internal pullup. If this pin is driven by an external device, It should be done using an open-drain device. | I/OD | | 2 | 3 | 3 | 4 |


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## 4.4 Pin Multiplexing

### 4.4.1 GPIO Muxed Pins

Table 4-6 lists the GPIO muxed pins. The default mode for each GPIO pin is the GPIO function, except GPIO35 and GPIO37, which default to TDI and TDO, respectively. Secondary functions can be selected by setting both the GPyGMUXn.GPIOz and GPyMUXn.GPIOz register bits. The GPyGMUXn register should be configured before the GPyMUXn to avoid transient pulses on GPIOs from alternate mux selections. Columns that are not shown and blank cells are reserved GPIO Mux settings.

**NOTE**

GPIO20, GPIO21, and GPIO41 to GPIO55 are not available on any packages. Boot ROM enables pullups on these pins. For more details, see Section 4.5.

## Table 4-6. GPIO Muxed Pins

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GPIO0 | EPWM1_A | | | | I2CA_SDA | | | | | | | |
| GPIO1 | EPWM1_B | | | | I2CA_SCL | | | | | | | |
| GPIO2 | EPWM2_A | | | OUTPUTXBAR1 | PMBUSA_SDA | | SCIA_TX | FSIRXA_D1 | | | | |
| GPIO3 | EPWM2_B | OUTPUTXBAR2 | | OUTPUTXBAR2 | PMBUSA_SCL | SPIA_CLK | SCIA_RX | FSIRXA_D0 | | | | |
| GPIO4 | EPWM3_A | | | OUTPUTXBAR3 | CANA_TX | | | FSIRXA_CLK | | | | |
| GPIO5 | EPWM3_B | | OUTPUTXBAR3 | | CANA_RX | SPIA_STE | FSITXA_D1 | | | | | |
| GPIO6 | EPWM4_A | OUTPUTXBAR4 | SYNCOUT | EQEP1_A | CANB_TX | SPIB_SOMI | FSITXA_D0 | | | | | |
| GPIO7 | EPWM4_B | | OUTPUTXBAR5 | EQEP1_B | CANB_RX | SPIB_SIMO | FSITXA_CLK | | | | | |
| GPIO8 | EPWM5_A | CANB_TX | ADCSOCAO | EQEP1_STROBE | SCIA_TX | SPIA_SIMO | I2CA_SCL | FSITXA_D1 | | | | |
| GPIO9 | EPWM5_B | SCIB_TX | OUTPUTXBAR6 | EQEP1_INDEX | SCIA_RX | SPIA_CLK | | FSITXA_D0 | | | | |
| GPIO10 | EPWM6_A | CANB_RX | ADCSOCBO | EQEP1_A | SCIB_TX | SPIA_SOMI | I2CA_SDA | FSITXA_CLK | | | | |
| GPIO11 | EPWM6_B | SCIB_RX | OUTPUTXBAR7 | EQEP1_B | SCIB_RX | SPIA_STE | FSIRXA_D1 | | | | | |
| GPIO12 | EPWM7_A | CANB_TX | | EQEP1_STROBE | SCIB_TX | PMBUSA_CTL | FSIRXA_D0 | | | | | |
| GPIO13 | EPWM7_B | CANB_RX | | EQEP1_INDEX | SCIB_RX | PMBUSA_ALERT | FSIRXA_CLK | | | | | |
| GPIO14 | EPWM8_A | SCIB_TX | | | OUTPUTXBAR3 | PMBUSA_SDA | SPIB_CLK | EQEP2_A | | | | |
| GPIO15 | EPWM8_B | SCIB_RX | | | OUTPUTXBAR4 | PMBUSA_SCL | SPIB_STE | EQEP2_B | | | | |
| GPIO16 | SPIA_SIMO | CANB_TX | OUTPUTXBAR7 | EPWM5_A | SCIA_TX | SD1_D1 | EQEP1_STROBE | PMBUSA_SCL | XCLKOUT | | | |
| GPIO17 | SPIA_SOMI | CANB_RX | OUTPUTXBAR8 | EPWM5_B | SCIA_RX | SD1_C1 | EQEP1_INDEX | PMBUSA_SDA | | | | |
| GPIO18_X2 | SPIA_CLK | SCIB_TX | CANA_RX | EPWM6_A | I2CA_SCL | SD1_D2 | EQEP2_A | PMBUSA_CTL | XCLKOUT | | | |
| GPIO20 | | | | | | | | | | | | |
| GPIO21 | | | | | | | | | | | | |
| GPIO22_VFBSW | EQEP1_STROBE | | SCIB_TX | | SPIB_CLK | SD1_D4 | LINA_TX | | | | | |
| GPIO23_VSW | | | | | | | | | | | | |
| GPIO24 | OUTPUTXBAR1 | EQEP2_A | | EPWM8_A | SPIB_SIMO | SD1_D1 | | PMBUSA_SCL | SCIA_TX | ERRORSTS | | |
| GPIO25 | OUTPUTXBAR2 | EQEP2_B | | | SPIB_SOMI | SD1_C1 | FSITXA_D1 | PMBUSA_SDA | SCIA_RX | | | |
| GPIO26 | OUTPUTXBAR3 | EQEP2_INDEX | | OUTPUTXBAR3 | SPIB_CLK | SD1_D2 | FSITXA_D0 | PMBUSA_CTL | I2CA_SDA | | | |
| GPIO27 | OUTPUTXBAR4 | EQEP2_STROBE | | OUTPUTXBAR4 | SPIB_STE | SD1_C2 | FSITXA_CLK | PMBUSA_ALERT | I2CA_SCL | | | |
| GPIO28 | SCIA_RX | | EPWM7_A | OUTPUTXBAR5 | EQEP1_A | SD1_D3 | EQEP2_STROBE | LINA_TX | SPIB_CLK | ERRORSTS | | |
| GPIO29 | SCIA_TX | | EPWM7_B | OUTPUTXBAR6 | EQEP1_B | SD1_C3 | EQEP2_INDEX | LINA_RX | SPIB_STE | ERRORSTS | | |
| GPIO30 | CANA_RX | | SPIB_SIMO | OUTPUTXBAR7 | EQEP1_STROBE | SD1_D4 | | | | | | |
| GPIO31 | CANA_TX | | SPIB_SOMI | OUTPUTXBAR8 | EQEP1_INDEX | SD1_C4 | FSIRXA_D1 | | | | | |
| GPIO32 | I2CA_SDA | | SPIB_CLK | EPWM8_B | LINA_TX | SD1_D3 | FSIRXA_D0 | CANA_TX | | | | |
| GPIO33 | I2CA_SCL | | SPIB_STE | OUTPUTXBAR4 | LINA_RX | SD1_C3 | FSIRXA_CLK | CANA_RX | | | | |
| GPIO34 | OUTPUTXBAR1 | | | | PMBUSA_SDA | | | | | | | |
| GPIO35 | SCIA_RX | | I2CA_SDA | CANA_RX | PMBUSA_SCL | LINA_RX | EQEP1_A | PMBUSA_CTL | | | | TDI |
| GPIO37 | OUTPUTXBAR2 | | I2CA_SCL | SCIA_TX | CANA_TX | LINA_TX | EQEP1_B | PMBUSA_ALERT | | | | TDO |
| GPIO39 | | | | | CANB_RX | FSIRXA_CLK | | | | | | |
| GPIO40 | | | | | PMBUSA_SDA | FSIRXA_D0 | SCIB_TX | EQEP1_A | | | | |
| GPIO41 | | | | | | | | | | | | |


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**Table 4-6. GPIO Muxed Pins (continued)**

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GPIO42 | | | | | | | | | | | | |
| GPIO43 | | | | | | | | | | | | |
| GPIO44 | | | | | | | | | | | | |
| GPIO45 | | | | | | | | | | | | |
| GPIO46 | | | | | | | | | | | | |
| GPIO47 | | | | | | | | | | | | |
| GPIO48 | | | | | | | | | | | | |
| GPIO49 | | | | | | | | | | | | |
| GPIO50 | | | | | | | | | | | | |
| GPIO51 | | | | | | | | | | | | |
| GPIO52 | | | | | | | | | | | | |
| GPIO53 | | | | | | | | | | | | |
| GPIO54 | | | | | | | | | | | | |
| GPIO55 | | | | | | | | | | | | |
| GPIO56 | SPIA_CLK | | | EQEP2_STROBE | SCIB_TX | SD1_D3 | SPIB_SIMO | | EQEP1_A | | | |
| GPIO57 | SPIA_STE | | | EQEP2_INDEX | SCIB_RX | SD1_C3 | SPIB_SOMI | | EQEP1_B | | | |
| GPIO58 | | | | OUTPUTXBAR1 | SPIB_CLK | SD1_D4 | LINA_TX | CANB_TX | EQEP1_STROBE | | | |
| GPIO59 | | | | OUTPUTXBAR2 | SPIB_STE | SD1_C4 | LINA_RX | CANB_RX | EQEP1_INDEX | | | |

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Table 4-7 lists all muxed signals available and the respective GPIO within each package.

**Table 4-7. Digital Signals by GPIO**

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|
| ADCSOCAO | O | ADC Start of Conversion A Output for External ADC (from ePWM modules) | GPIO8 | GPIO8 | GPIO8 | GPIO8 |
| ADCSOCBO | O | ADC Start of Conversion B Output for External ADC (from ePWM modules) | GPIO10 | GPIO10 | GPIO10 | |
| CANA_RX | I | CAN-A Receive | GPIO5<br>GPIO18_X2<br>GPIO30<br>GPIO33<br>GPIO35/TDI | GPIO5<br>GPIO18_X2<br>GPIO33<br>GPIO35/TDI | GPIO5<br>GPIO18_X2<br>GPIO33<br>GPIO35/TDI | GPIO5<br>GPIO18_X2<br>GPIO33<br>GPIO35/TDI |
| CANA_TX | O | CAN-A Transmit | GPIO4<br>GPIO31<br>GPIO32<br>GPIO37/TDO | GPIO4<br>GPIO32<br>GPIO37/TDO | GPIO4<br>GPIO32<br>GPIO37/TDO | GPIO4<br>GPIO32<br>GPIO37/TDO |
| CANB_RX | I | CAN-B Receive | GPIO7<br>GPIO10<br>GPIO13<br>GPIO17<br>GPIO39<br>GPIO59 | GPIO7<br>GPIO10<br>GPIO17 | GPIO7<br>GPIO10<br>GPIO13<br>GPIO17 | GPIO7<br>GPIO13<br>GPIO17 |
| CANB_TX | O | CAN-B Transmit | GPIO6<br>GPIO8<br>GPIO12<br>GPIO16<br>GPIO58 | GPIO6<br>GPIO8<br>GPIO16 | GPIO6<br>GPIO8<br>GPIO12<br>GPIO16 | GPIO6<br>GPIO8<br>GPIO12<br>GPIO16 |
| EPWM1_A | O | ePWM-1 Output A | GPIO0 | GPIO0 | GPIO0 | GPIO0 |
| EPWM1_B | O | ePWM-1 Output B | GPIO1 | GPIO1 | GPIO1 | GPIO1 |
| EPWM2_A | O | ePWM-2 Output A | GPIO2 | GPIO2 | GPIO2 | GPIO2 |
| EPWM2_B | O | ePWM-2 Output B | GPIO3 | GPIO3 | GPIO3 | GPIO3 |
| EPWM3_A | O | ePWM-3 Output A | GPIO4 | GPIO4 | GPIO4 | GPIO4 |
| EPWM3_B | O | ePWM-3 Output B | GPIO5 | GPIO5 | GPIO5 | GPIO5 |
| EPWM4_A | O | ePWM-4 Output A | GPIO6 | GPIO6 | GPIO6 | GPIO6 |
| EPWM4_B | O | ePWM-4 Output B | GPIO7 | GPIO7 | GPIO7 | GPIO7 |
| EPWM5_A | O | ePWM-5 Output A | GPIO8<br>GPIO16 | GPIO8<br>GPIO16 | GPIO8<br>GPIO16 | GPIO8<br>GPIO16 |
| EPWM5_B | O | ePWM-5 Output B | GPIO9<br>GPIO17 | GPIO9<br>GPIO17 | GPIO9<br>GPIO17 | GPIO9<br>GPIO17 |
| EPWM6_A | O | ePWM-6 Output A | GPIO10<br>GPIO18_X2 | GPIO10<br>GPIO18_X2 | GPIO10<br>GPIO18_X2 | GPIO18_X2 |
| EPWM6_B | O | ePWM-6 Output B | GPIO11 | GPIO11 | GPIO11 | GPIO11 |
| EPWM7_A | O | ePWM-7 Output A | GPIO12<br>GPIO28 | GPIO28 | GPIO12<br>GPIO28 | GPIO12<br>GPIO28 |
| EPWM7_B | O | ePWM-7 Output B | GPIO13<br>GPIO29 | GPIO29 | GPIO13<br>GPIO29 | GPIO13<br>GPIO29 |
| EPWM8_A | O | ePWM-8 Output A | GPIO14<br>GPIO24 | GPIO24 | GPIO24 | GPIO24 |
| EPWM8_B | O | ePWM-8 Output B | GPIO15<br>GPIO32 | GPIO32 | GPIO32 | GPIO32 |


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**Table 4-7. Digital Signals by GPIO (continued)**

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|
| EQEP1_A | I | eQEP-1 Input A | GPIO6<br>GPIO10<br>GPIO28<br>GPIO35/TDI<br>GPIO40<br>GPIO56 | GPIO6<br>GPIO10<br>GPIO28<br>GPIO35/TDI | GPIO6<br>GPIO10<br>GPIO28<br>GPIO35/TDI | GPIO6<br>GPIO28<br>GPIO35/TDI |
| EQEP1_B | I | eQEP-1 Input B | GPIO7<br>GPIO11<br>GPIO29<br>GPIO37/TDO<br>GPIO57 | GPIO7<br>GPIO11<br>GPIO29<br>GPIO37/TDO | GPIO7<br>GPIO11<br>GPIO29<br>GPIO37/TDO | GPIO7<br>GPIO11<br>GPIO29<br>GPIO37/TDO |
| EQEP1_INDEX | I/O | eQEP-1 Index | GPIO9<br>GPIO13<br>GPIO17<br>GPIO31<br>GPIO59 | GPIO9<br>GPIO17 | GPIO9<br>GPIO13<br>GPIO17 | GPIO9<br>GPIO13<br>GPIO17 |
| EQEP1_STROBE | I/O | eQEP-1 Strobe | GPIO8<br>GPIO12<br>GPIO16<br>GPIO22_VFBSW<br>GPIO30<br>GPIO58 | GPIO8<br>GPIO16<br>GPIO22_VFBSW | GPIO8<br>GPIO12<br>GPIO16<br>GPIO22_VFBSW | GPIO8<br>GPIO12<br>GPIO16<br>GPIO22_VFBSW |
| EQEP2_A | I | eQEP-2 Input A | GPIO14<br>GPIO18_X2<br>GPIO24 | GPIO18_X2<br>GPIO24 | GPIO18_X2<br>GPIO24 | GPIO18_X2<br>GPIO24 |
| EQEP2_B | I | eQEP-2 Input B | GPIO15<br>GPIO25 | | | |
| EQEP2_INDEX | I/O | eQEP-2 Index | GPIO26<br>GPIO29<br>GPIO57 | GPIO29 | GPIO29 | GPIO29 |
| EQEP2_STROBE | I/O | eQEP-2 Strobe | GPIO27<br>GPIO28<br>GPIO56 | GPIO28 | GPIO28 | GPIO28 |
| ERRORSTS | O | Error Status Output. This signal requires an external pullup. | GPIO24<br>GPIO28<br>GPIO29 | GPIO24<br>GPIO28<br>GPIO29 | GPIO24<br>GPIO28<br>GPIO29 | GPIO24<br>GPIO28<br>GPIO29 |
| FSIRXA_CLK | I | FSIRX-A Input Clock | GPIO4<br>GPIO13<br>GPIO33<br>GPIO39 | GPIO4<br>GPIO33 | GPIO4<br>GPIO13<br>GPIO33 | GPIO4<br>GPIO13<br>GPIO33 |
| FSIRXA_D0 | I | FSIRX-A Primary Data Input | GPIO3<br>GPIO12<br>GPIO32<br>GPIO40 | GPIO3<br>GPIO32 | GPIO3<br>GPIO12<br>GPIO32 | GPIO3<br>GPIO12<br>GPIO32 |
| FSIRXA_D1 | I | FSIRX-A Optional Additional Data Input | GPIO2<br>GPIO11<br>GPIO31 | GPIO2<br>GPIO11 | GPIO2<br>GPIO11 | GPIO2<br>GPIO11 |
| FSITXA_CLK | O | FSITX-A Output Clock | GPIO7<br>GPIO10<br>GPIO27 | GPIO7<br>GPIO10 | GPIO7<br>GPIO10 | GPIO7 |
| FSITXA_D0 | O | FSITX-A Primary Data Output | GPIO6<br>GPIO9<br>GPIO26 | GPIO6<br>GPIO9 | GPIO6<br>GPIO9 | GPIO6<br>GPIO9 |
| FSITXA_D1 | O | FSITX-A Optional Additional Data Output | GPIO5<br>GPIO8<br>GPIO25 | GPIO5<br>GPIO8 | GPIO5<br>GPIO8 | GPIO5<br>GPIO8 |

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**Table 4-7. Digital Signals by GPIO (continued)**

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|
| I2CA_SCL | I/OD | I2C-A Open-Drain Bidirectional Clock | GPIO1 GPIO8 GPIO18_X2 GPIO27 GPIO33 GPIO37/TDO | GPIO1 GPIO8 GPIO18_X2 GPIO33 GPIO37/TDO | GPIO1 GPIO8 GPIO18_X2 GPIO33 GPIO37/TDO | GPIO1 GPIO8 GPIO18_X2 GPIO33 GPIO37/TDO |
| I2CA_SDA | I/OD | I2C-A Open-Drain Bidirectional Data | GPIO0 GPIO10 GPIO26 GPIO32 GPIO35/TDI | GPIO0 GPIO10 GPIO32 GPIO35/TDI | GPIO0 GPIO10 GPIO32 GPIO35/TDI | GPIO0 GPIO32 GPIO35/TDI |
| LINA_RX | I | LIN-A Receive | GPIO29 GPIO33 GPIO35/TDI GPIO59 | GPIO29 GPIO33 GPIO35/TDI | GPIO29 GPIO33 GPIO35/TDI | GPIO29 GPIO33 GPIO35/TDI |
| LINA_TX | O | LIN-A Transmit | GPIO22_VFBSW GPIO28 GPIO32 GPIO37/TDO GPIO58 | GPIO22_VFBSW GPIO28 GPIO32 GPIO37/TDO | GPIO22_VFBSW GPIO28 GPIO32 GPIO37/TDO | GPIO22_VFBSW GPIO28 GPIO32 GPIO37/TDO |
| OUTPUTXBAR1 | O | Output X-BAR Output 1 | GPIO2 GPIO24 GPIO34 GPIO58 | GPIO2 GPIO24 | GPIO2 GPIO24 | GPIO2 GPIO24 |
| OUTPUTXBAR2 | O | Output X-BAR Output 2 | GPIO3 GPIO25 GPIO37/TDO GPIO59 | GPIO3 GPIO37/TDO | GPIO3 GPIO37/TDO | GPIO3 GPIO37/TDO |
| OUTPUTXBAR3 | O | Output X-BAR Output 3 | GPIO4 GPIO5 GPIO14 GPIO26 | GPIO4 GPIO5 | GPIO4 GPIO5 | GPIO4 GPIO5 |
| OUTPUTXBAR4 | O | Output X-BAR Output 4 | GPIO6 GPIO15 GPIO27 GPIO33 | GPIO6 GPIO33 | GPIO6 GPIO33 | GPIO6 GPIO33 |
| OUTPUTXBAR5 | O | Output X-BAR Output 5 | GPIO7 GPIO28 | GPIO7 GPIO28 | GPIO7 GPIO28 | GPIO7 GPIO28 |
| OUTPUTXBAR6 | O | Output X-BAR Output 6 | GPIO9 GPIO29 | GPIO9 GPIO29 | GPIO9 GPIO29 | GPIO9 GPIO29 |
| OUTPUTXBAR7 | O | Output X-BAR Output 7 | GPIO11 GPIO16 GPIO30 | GPIO11 GPIO16 | GPIO11 GPIO16 | GPIO11 GPIO16 |
| OUTPUTXBAR8 | O | Output X-BAR Output 8 | GPIO17 GPIO31 | GPIO17 | GPIO17 | GPIO17 |
| PMBUSA_ALERT | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal | GPIO13 GPIO27 GPIO37/TDO | GPIO37/TDO | GPIO13 GPIO37/TDO | GPIO13 GPIO37/TDO |
| PMBUSA_CTL | I | PMBus-A Control Signal | GPIO12 GPIO18_X2 GPIO26 GPIO35/TDI | GPIO18_X2 GPIO35/TDI | GPIO12 GPIO18_X2 GPIO35/TDI | GPIO12 GPIO18_X2 GPIO35/TDI |


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**Table 4-7. Digital Signals by GPIO (continued)**

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|
| PMBUSA_SCL | I/OD | PMBus-A Open-Drain Bidirectional Clock | GPIO3 GPIO15 GPIO16 GPIO24 GPIO35/TDI | GPIO3 GPIO16 GPIO24 GPIO35/TDI | GPIO3 GPIO16 GPIO24 GPIO35/TDI | GPIO3 GPIO16 GPIO24 GPIO35/TDI |
| PMBUSA_SDA | I/OD | PMBus-A Open-Drain Bidirectional Data | GPIO2 GPIO14 GPIO17 GPIO25 GPIO34 GPIO40 | GPIO2 GPIO17 | GPIO2 GPIO17 | GPIO2 GPIO17 |
| SCIA_RX | I | SCI-A Receive Data | GPIO3 GPIO9 GPIO17 GPIO25 GPIO28 GPIO35/TDI | GPIO3 GPIO9 GPIO17 GPIO28 GPIO35/TDI | GPIO3 GPIO9 GPIO17 GPIO28 GPIO35/TDI | GPIO3 GPIO9 GPIO17 GPIO28 GPIO35/TDI |
| SCIA_TX | O | SCI-A Transmit Data | GPIO2 GPIO8 GPIO16 GPIO24 GPIO29 GPIO37/TDO | GPIO2 GPIO8 GPIO16 GPIO24 GPIO29 GPIO37/TDO | GPIO2 GPIO8 GPIO16 GPIO24 GPIO29 GPIO37/TDO | GPIO2 GPIO8 GPIO16 GPIO24 GPIO29 GPIO37/TDO |
| SCIB_RX | I | SCI-B Receive Data | GPIO11 GPIO13 GPIO15 GPIO57 | GPIO11 | GPIO11 GPIO13 | GPIO11 GPIO13 |
| SCIB_TX | O | SCI-B Transmit Data | GPIO9 GPIO10 GPIO12 GPIO14 GPIO18_X2 GPIO22_VFBSW GPIO40 GPIO56 | GPIO9 GPIO10 GPIO18_X2 GPIO22_VFBSW | GPIO9 GPIO10 GPIO12 GPIO18_X2 GPIO22_VFBSW | GPIO9 GPIO12 GPIO18_X2 GPIO22_VFBSW |
| SD1_C1 | I | SDFM-1 Channel 1 Clock Input | GPIO17 GPIO25 | GPIO17 | GPIO17 | GPIO17 |
| SD1_C2 | I | SDFM-1 Channel 2 Clock Input | GPIO27 | | | |
| SD1_C3 | I | SDFM-1 Channel 3 Clock Input | GPIO29 GPIO33 GPIO57 | GPIO29 GPIO33 | GPIO29 GPIO33 | GPIO29 GPIO33 |
| SD1_C4 | I | SDFM-1 Channel 4 Clock Input | GPIO31 GPIO59 | | | |
| SD1_D1 | I | SDFM-1 Channel 1 Data Input | GPIO16 GPIO24 | GPIO16 GPIO24 | GPIO16 GPIO24 | GPIO16 GPIO24 |
| SD1_D2 | I | SDFM-1 Channel 2 Data Input | GPIO18_X2 GPIO26 | GPIO18_X2 | GPIO18_X2 | GPIO18_X2 |
| SD1_D3 | I | SDFM-1 Channel 3 Data Input | GPIO28 GPIO32 GPIO56 | GPIO28 GPIO32 | GPIO28 GPIO32 | GPIO28 GPIO32 |
| SD1_D4 | I | SDFM-1 Channel 4 Data Input | GPIO22_VFBSW GPIO30 GPIO58 | GPIO22_VFBSW | GPIO22_VFBSW | GPIO22_VFBSW |

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**Table 4-7. Digital Signals by GPIO (continued)**

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 64 PMQ | 64 PM | 56 RSH |
|---|---|---|---|---|---|---|
| SPIA_CLK | I/O | SPI-A Clock | GPIO3 GPIO9 GPIO18_X2 GPIO56 | GPIO3 GPIO9 GPIO18_X2 | GPIO3 GPIO9 GPIO18_X2 | GPIO3 GPIO9 GPIO18_X2 |
| SPIA_SIMO | I/O | SPI-A Slave In, Master Out (SIMO) | GPIO8 GPIO16 | GPIO8 GPIO16 | GPIO8 GPIO16 | GPIO8 GPIO16 |
| SPIA_SOMI | I/O | SPI-A Slave Out, Master In (SOMI) | GPIO10 GPIO17 | GPIO10 GPIO17 | GPIO10 GPIO17 | GPIO17 |
| SPIA_STE | I/O | SPI-A Slave Transmit Enable (STE) | GPIO5 GPIO11 GPIO57 | GPIO5 GPIO11 | GPIO5 GPIO11 | GPIO5 GPIO11 |
| SPIB_CLK | I/O | SPI-B Clock | GPIO14 GPIO22_VFBSW GPIO26 GPIO28 GPIO32 GPIO58 | GPIO22_VFBSW GPIO28 GPIO32 | GPIO22_VFBSW GPIO28 GPIO32 | GPIO22_VFBSW GPIO28 GPIO32 |
| SPIB_SIMO | I/O | SPI-B Slave In, Master Out (SIMO) | GPIO7 GPIO24 GPIO30 GPIO56 | GPIO7 GPIO24 | GPIO7 GPIO24 | GPIO7 GPIO24 |
| SPIB_SOMI | I/O | SPI-B Slave Out, Master In (SOMI) | GPIO6 GPIO25 GPIO31 GPIO57 | GPIO6 | GPIO6 | GPIO6 |
| SPIB_STE | I/O | SPI-B Slave Transmit Enable (STE) | GPIO15 GPIO27 GPIO29 GPIO33 GPIO59 | GPIO29 GPIO33 | GPIO29 GPIO33 | GPIO29 GPIO33 |
| SYNCOUT | O | External ePWM Synchronization Pulse | GPIO6 | GPIO6 | GPIO6 | GPIO6 |
| TDI | I | JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input. | GPIO35/TDI | GPIO35/TDI | GPIO35/TDI | GPIO35/TDI |
| TDO | O | JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. | GPIO37/TDO | GPIO37/TDO | GPIO37/TDO | GPIO37/TDO |
| VFBSW | - | Internal DC-DC regulator feedback signal. If the internal DC-DC regulator is used, tie this pin to the node where L(VSW) connects to the VDD rail (as close as possible to the device). | GPIO22_VFBSW | GPIO22_VFBSW | GPIO22_VFBSW | GPIO22_VFBSW |
| VSW | - | Switching output of the internal DC-DC regulator | GPIO23_VSW | GPIO23_VSW | GPIO23_VSW | GPIO23_VSW |
| X2 | I/O | Crystal oscillator output | GPIO18_X2 | GPIO18_X2 | GPIO18_X2 | GPIO18_X2 |
| XCLKOUT | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. | GPIO16 GPIO18_X2 | GPIO16 GPIO18_X2 | GPIO16 GPIO18_X2 | GPIO16 GPIO18_X2 |


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### 4.4.2 Digital Inputs on ADC Pins (AIOs)

GPIOs on port H (GPIO224–GPIO255) are multiplexed with analog pins. These are also referred to as AIOs. These pins can only function in input mode. By default, these pins will function as analog pins and the GPIOs are in a high-Z state. The GPHAMSEL register is used to configure these pins for digital or analog operation.

**NOTE**

If digital signals with sharp edges (high dv/dt) are connected to the AIOs, cross-talk can occur with adjacent analog signals. The user should therefore limit the edge rate of signals connected to AIOs if adjacent channels are being used for analog functions.

### 4.4.3 GPIO Input X-BAR

The Input X-BAR is used to route signals from a GPIO to many different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts (see Figure 4-5). Table 4-8 lists the input X-BAR destinations. For details on configuring the Input X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

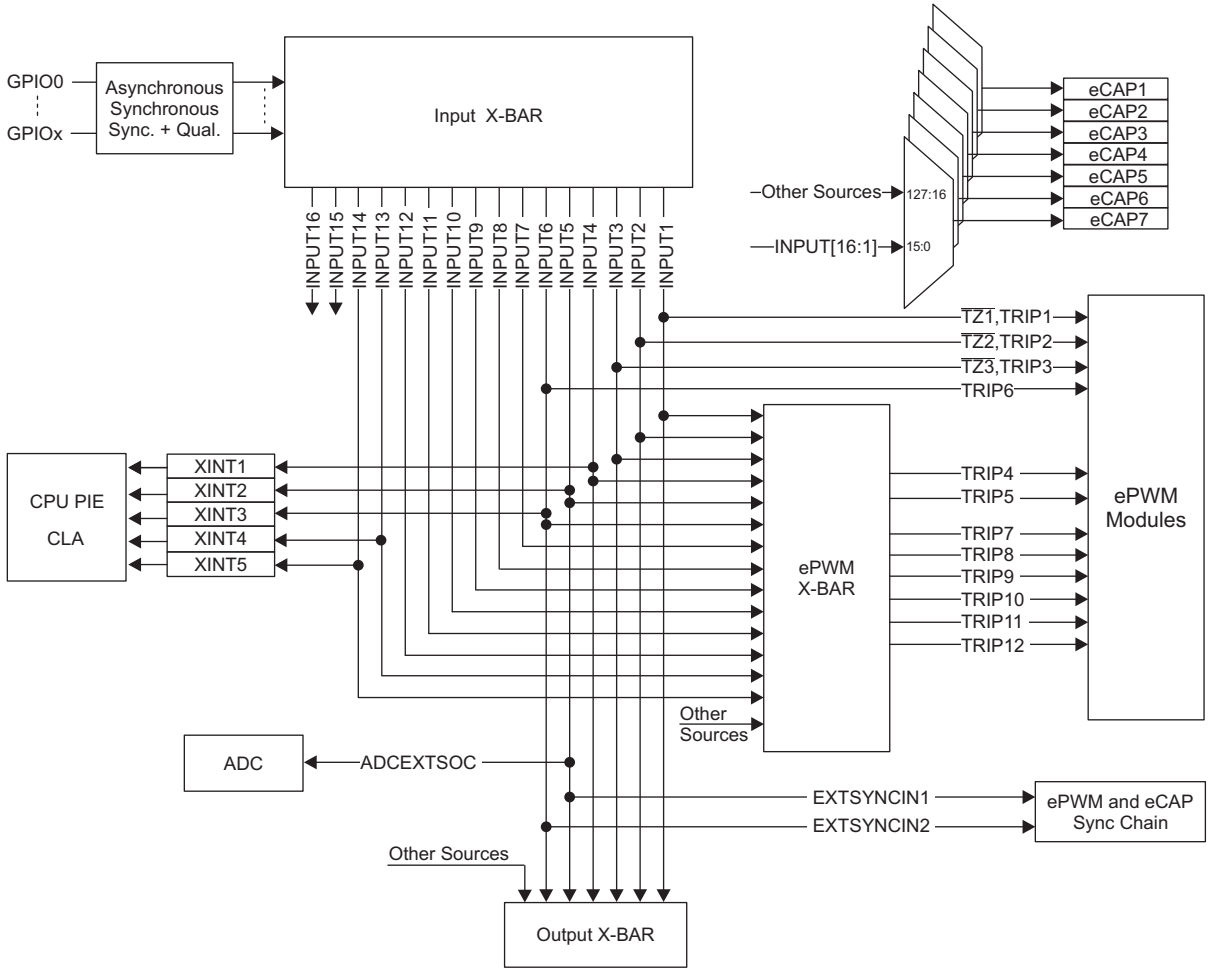



**Figure 4-5. Input X-BAR**

**Table 4-8. Input X-BAR Destinations**

| INPUT | DESTINATIONS |
|---|---|
| INPUT1 | eCAPx, ePWM X-BAR, ePWM[TZ1,TRIP1], Output X-BAR |
| INPUT2 | eCAPx, ePWM X-BAR, ePWM[TZ2,TRIP2], Output X-BAR |
| INPUT3 | eCAPx, ePWM X-BAR, ePWM[TZ3,TRIP3], Output X-BAR |
| INPUT4 | eCAPx, ePWM X-BAR, XINT1, Output X-BAR |
| INPUT5 | eCAPx, ePWM X-BAR, XINT2, ADCEXTSOC, EXTSYNCIN1, Output X-BAR |
| INPUT6 | eCAPx, ePWM X-BAR, XINT3, ePWM[TRIP6], EXTSYNCIN2, Output X-BAR |
| INPUT7 | eCAPx, ePWM X-BAR |
| INPUT8 | eCAPx, ePWM X-BAR |
| INPUT9 | eCAPx, ePWM X-BAR |
| INPUT10 | eCAPx, ePWM X-BAR |
| INPUT11 | eCAPx, ePWM X-BAR |
| INPUT12 | eCAPx, ePWM X-BAR |
| INPUT13 | eCAPx, ePWM X-BAR, XINT4 |
| INPUT14 | eCAPx, ePWM X-BAR, XINT5 |
| INPUT15 | eCAPx |
| INPUT16 | eCAPx |


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### 4.4.4 GPIO Output X-BAR and ePWM X-BAR

The Output X-BAR has eight outputs which are routed to the GPIO module. The ePWM X-BAR has eight outputs which are routed to each ePWM module. Figure 4-6 shows the sources for both the Output X-BAR and ePWM X-BAR. For details on the Output X-BAR and ePWM X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

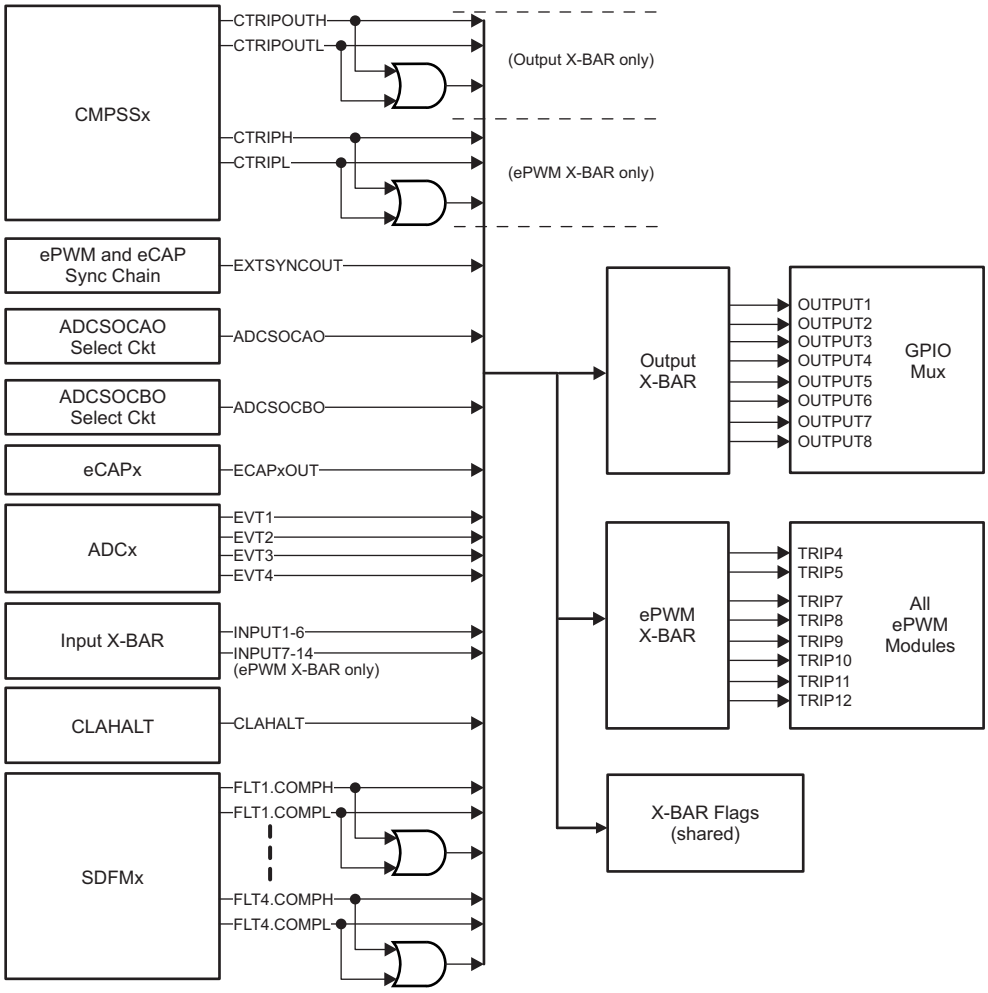



**Figure 4-6. Output X-BAR and ePWM X-BAR Sources**

## 4.5 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. Table 4-9 lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. To avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in Table 4-9 with pullups and pulldowns are always on and cannot be disabled.

**Table 4-9. Pins With Internal Pullup and Pulldown**

| PIN | RESET (XRSn = 0) | DEVICE BOOT | APPLICATION |
|---|---|---|---|
| GPIOx (including AIOs) | Pullup disabled | Pullup disabled(1) | Application defined |
| GPIO35/TDI | Pullup disabled | | Application defined |
| GPIO37/TDO | Pullup disabled | | Application defined |
| TCK | Pullup active | | |
| TMS | Pullup active | | |
| VREGENZ | Pulldown active | | |
| XRSn | Pullup active | | |
| Other pins | No pullup or pulldown present | | |

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.


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## 4.6 Connections for Unused Pins

For applications that do not need to use all functions of the device, Table 4-10 lists acceptable conditioning for any unused pins. When multiple options are listed in Table 4-10, any option is acceptable. Pins not listed in Table 4-10 must be connected according to Section 4.

**Table 4-10. Connections for Unused Pins**

| SIGNAL NAME | ACCEPTABLE PRACTICE |
|---|---|
| **ANALOG** | |
| Analog input pins with DACx_OUT | • No Connect<br>• Tie to VSSA through 4.7-kΩ or larger resistor |
| Analog input pins with PGAx_OUTF | • No Connect<br>• Tie to VSSA through 4.7-kΩ or larger resistor |
| Analog input pins (except for DACx_OUT and PGAx_OUTF) | • No Connect<br>• Tie to VSSA<br>• Tie to VSSA through resistor |
| PGAx_GND | Tie to VSSA |
| VREFHIx | Tie to VDDA (applies only if ADC or DAC are not used in the application) |
| VREFLOx | Tie to VSSA |
| **DIGITAL** | |
| FLT1 (Flash Test pin 1) | • No Connect<br>• Tie to VSS through 4.7-kΩ or larger resistor |
| FLT2 (Flash Test pin 2) | • No Connect<br>• Tie to VSS through 4.7-kΩ or larger resistor |
| GPIOx | • Input mode with internal pullup enabled<br>• Input mode with external pullup or pulldown resistor<br>• Output mode with internal pullup disabled |
| GPIO35/TDI | When TDI mux option is selected (default), the GPIO is in Input mode.<br>• Internal pullup enabled<br>• External pullup resistor |
| GPIO37/TDO | When TDO mux option is selected (default), the GPIO is in Output mode only during JTAG activity; otherwise, it is in a tri-state condition. The pin must be biased to avoid extra current on the input buffer.<br>• Internal pullup enabled<br>• External pullup resistor |
| TCK | • No Connect<br>• Pullup resistor |
| TMS | Pullup resistor |
| VREGENZ | Tie to VDDIO if internal regulator is not used |
| X1 | Tie to VSS |
| X2 | No Connect |
| **POWER AND GROUND** | |
| VDD | All VDD pins must be connected per Section 4.3. |
| VDDA | If a dedicated analog supply is not used, tie to VDDIO. |
| VDDIO | All VDDIO pins must be connected per Section 4.3. |
| VDDIO_SW | Must always be tied to VDDIO |
| VSS | All VSS pins must be connected to board ground. |
| VSS_SW | Tie to VSS |
| VSSA | If an analog ground is not used, tie to VSS. |

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# 5 Specifications

## 5.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | VDDIO with respect to VSS | –0.3 | 4.6 | V |
| | VDDA with respect to VSSA | –0.3 | 4.6 | |
| | VDD with respect to VSS | –0.3 | 1.5 | |
| Voltage difference between VDDIO and VDDIO_SW pins | | | ±0.3 | V |
| Input voltage | $V_{IN}$ (3.3 V) | –0.3 | 4.6 | V |
| Output voltage | $V_O$ | –0.3 | 4.6 | V |
| Input clamp current | Digital input (per pin), $I_{IK}$ ($V_{IN}$ < VSS or $V_{IN}$ > VDDIO) | –20 | 20 | mA |
| | Analog input (per pin), $I_{IKANALOG}$ ($V_{IN}$ < VSSA or $V_{IN}$ > VDDA) | –20 | 20 | |
| | Total for all inputs, $I_{IKTOTAL}$ ($V_{IN}$ < VSS/VSSA or $V_{IN}$ > VDDIO/VDDA) | –20 | 20 | |
| Output current | Digital output (per pin), $I_{OUT}$ | –20 | 20 | mA |
| Free-Air temperature | $T_A$ | –40 | 125 | °C |
| Operating junction temperature | $T_J$ | –40 | 150 | °C |
| Storage temperature[3] | $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.4 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *IC Package Thermal Metrics Application Report* (SPRA953).


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## 5.2 ESD Ratings – Commercial

| | | | VALUE | UNIT |
|---|---|---|---|---|
| F28004x in 100-pin PZ package (S temperature range) | | | | |
| $V_{(ESD)}$ | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±500 | |
| F28004x in 64-pin PM package (S temperature range) | | | | |
| $V_{(ESD)}$ | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±500 | |
| F28004x in 56-pin RSH package (S temperature range) | | | | |
| $V_{(ESD)}$ | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 ESD Ratings – Automotive

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| F28004x in 100-pin PZ package (Q temperature range) | | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002[1] | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 100-pin PZ: 1, 25, 26, 50, 51, 75, 76, 100 | ±750 | |
| F28004x in 64-pin PM package (Q temperature range) | | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002[1] | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64 | ±750 | |

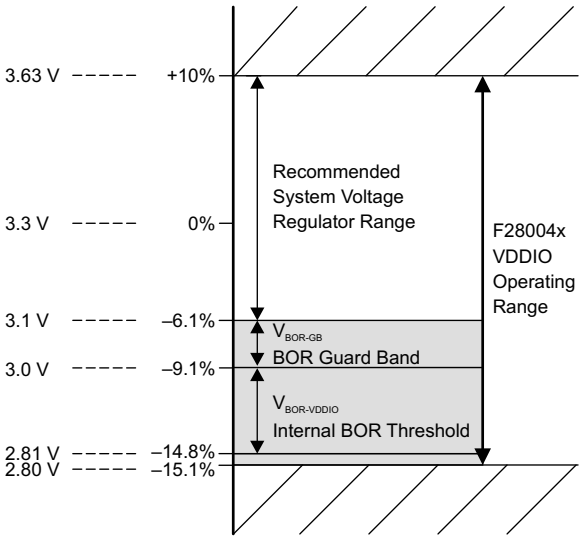
(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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## 5.4 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Device supply voltage, VDDIO and VDDA | Internal BOR enabled(1) | $V_{BOR-VDDIO}$(MAX) + $V_{BOR-GB}$ (2) | 3.3 | 3.63 | V |
| | Internal BOR disabled | 2.8 | 3.3 | 3.63 | |
| Device supply voltage, VDD | | 1.14 | 1.2 | 1.32 | V |
| Device ground, VSS | | | 0 | | V |
| Analog ground, VSSA | | | 0 | | V |
| $SR_{SUPPLY}$ | Supply ramp rate of VDDIO, VDD, VDDA with respect to VSS.(3) | | | $10^5$ | V/s |
| $t_{VDDIO-RAMP}$ | VDDIO supply ramp time from 1 V to $V_{BOR-VDDIO}$(MAX) | | | 10 | ms |
| $V_{BOR-GB}$ | VDDIO BOR guard band(4) | | 0.1 | | V |
| Junction temperature, $T_J$ | S version(5) | –40 | | 125 | °C |
| Free-Air temperature, $T_A$ | Q version(5) (AEC Q100 qualification) | –40 | | 125 | °C |

(1) Internal BOR is enabled by default.
(2) The VDDIO BOR voltage ($V_{BOR-VDDIO}$[MAX]) in Electrical Characteristics determines the lower voltage bound for device operation. TI recommends that system designers budget an additional guard band ($V_{BOR-GB}$) as shown in Figure 5-1.
(3) Supply ramp rate faster than this can trigger the on-chip ESD protection.
(4) TI recommends $V_{BOR-GB}$ to avoid BOR resets due to normal supply noise or load-transient events on the 3.3-V VDDIO system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR during normal device operation. The value of $V_{BOR-GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.
(5) Operation above $T_J$ = 105°C for extended duration will reduce the lifetime of the device. See Calculating Useful Lifetimes of Embedded Processors for more information.



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**Figure 5-1. Supply Voltages**


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## 5.5 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations. Table 5-1 lists the system current consumption values for an external supply. Table 5-2 lists the system current consumption values for the internal VREG. Table 5-3 lists the system current consumption values for the DCDC. See Section 5.5.1 for a detailed description of the test case run while measuring the current consumption in operating mode.

**Table 5-1. System Current Consumption (External Supply)**

over operating free-air temperature range (unless otherwise noted).
TYP : $V_{nom}$, 30℃

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPERATING MODE** | | | | | | |
| $I_{DD}$ | VDD current consumption during operational usage | See Section 5.5.1. | | 61 | 90 | mA |
| $I_{DDIO}$ | VDDIO current consumption during operational usage | | | 26 | 45 | mA |
| $I_{DDA}$ | VDDA current consumption during operational usage | | | 12 | 30 | mA |
| **IDLE MODE** | | | | | | |
| $I_{DD}$ | VDD current consumption while device is in Idle mode | • CPU is in IDLE mode<br>• Flash is powered down<br>• XCLKOUT is turned off | | 18 | 40 | mA |
| $I_{DDIO}$ | VDDIO current consumption while device is in Idle mode | | | 1.2 | 4 | mA |
| $I_{DDA}$ | VDDA current consumption while device is in Idle mode | | | 0.9 | 1.2 | mA |
| **HALT MODE** | | | | | | |
| $I_{DD}$ | VDD current consumption while device is in Halt mode | • CPU is in HALT mode<br>• Flash is powered down<br>• XCLKOUT is turned off | | 0.9 | 20 | mA |
| $I_{DDIO}$ | VDDIO current consumption while device is in Halt mode | | | 0.8 | 4 | mA |
| $I_{DDA}$ | VDDA current consumption while device is in Halt mode | | | 0.2 | 0.5 | mA |
| **FLASH ERASE/PROGRAM** | | | | | | |
| $I_{DD}$ | VDD Current consumption during Erase/Program cycle(1) | • CPU is running from Flash, performing Erase and Program on the unused sector.<br>• VREG is disabled.<br>• SYSCLK is running at 100 MHz.<br>• I/Os are inputs with pullups enabled.<br>• Peripheral clocks are turned OFF. | | 40 | 70 | mA |
| $I_{DDIO}$ | VDDIO Current consumption during Erase/Program cycle(1) | | | 33 | 75 | mA |
| $I_{DDA}$ | VDDA Current consumption during Erase/Program cycle | | | 0.1 | 2.5 | mA |

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.

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### Table 5-2. System Current Consumption (Internal VREG)

over operating free-air temperature range (unless otherwise noted).
TYP : $V_{nom}$, 30℃

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPERATING MODE** | | | | | | |
| $I_{DDIO}$ | VDDIO current consumption during operational usage | See Section 5.5.1. | | 86 | 113 | mA |
| $I_{DDA}$ | VDDA current consumption during operational usage | | | 12 | 30 | mA |
| **IDLE MODE** | | | | | | |
| $I_{DDIO}$ | VDDIO current consumption while device is in Idle mode | • CPU is in IDLE mode<br>• Flash is powered down<br>• XCLKOUT is turned off | | 19.2 | 36 | mA |
| $I_{DDA}$ | VDDA current consumption while device is in Idle mode | | | 0.9 | 1.2 | mA |
| **HALT MODE** | | | | | | |
| $I_{DDIO}$ | VDDIO current consumption while device is in Halt mode | • CPU is in HALT mode<br>• Flash is powered down<br>• XCLKOUT is turned off | | 1.7 | 18 | mA |
| $I_{DDA}$ | VDDA current consumption while device is in Halt mode | | | 0.2 | 0.5 | mA |
| **FLASH ERASE/PROGRAM** | | | | | | |
| $I_{DDIO}$ | VDDIO current consumption during Erase/Program cycle(1) | • CPU is running from Flash, performing Erase and Program on the unused sector.<br>• Internal VREG is enabled.<br>• SYSCLK is running at 100 MHz.<br>• I/Os are inputs with pullups enabled.<br>• Peripheral clocks are turned OFF. | | 72 | 106 | mA |
| $I_{DDA}$ | VDDA current consumption during Erase/Program cycle | | | 0.1 | 2.5 | mA |

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.


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**Table 5-3. System Current Consumption (DCDC)**

over operating free-air temperature range (unless otherwise noted).
TYP : $V_{nom}$, 30℃

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPERATING MODE** | | | | | | |
| $I_{DDIO}$ | VDDIO current consumption during operational usage | See Section 5.5.1. | | 52 | 70 | mA |
| $I_{DDA}$ | VDDA current consumption during operational usage | | | 12 | 25 | mA |
| **IDLE MODE** | | | | | | |
| $I_{DDIO}$ | VDDIO current consumption while device is in Idle mode | • CPU is in IDLE mode<br>• Flash is powered down<br>• XCLKOUT is turned off | | 9.2 | 28 | mA |
| $I_{DDA}$ | VDDA current consumption while device is in Idle mode | | | 0.9 | 1.5 | mA |
| **HALT MODE** | | | | | | |
| $I_{DDIO}$ | VDDIO current consumption while device is in Halt mode | • CPU is in HALT mode<br>• Flash is powered down<br>• XCLKOUT is turned off | | 1.7 | 17 | mA |
| $I_{DDA}$ | VDDA current consumption while device is in Halt mode | | | 0.2 | 1.5 | mA |
| **FLASH ERASE/PROGRAM** | | | | | | |
| $I_{DDIO}$ | VDDIO current consumption during Erase/Program cycle(1) | • CPU is running from Flash, performing Erase and Program on the unused sector.<br>• DCDC is enabled.<br>• SYSCLK is running at 100 MHz.<br>• I/Os are inputs with pullups enabled.<br>• Peripheral clocks are turned OFF. | | 60 | 85 | mA |
| $I_{DDA}$ | VDDA current consumption during Erase/Program cycle | | | 0.25 | 2.5 | mA |

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.

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### 5.5.1 Operating Mode Test Description

Table 5-1, Table 5-2, and Table 5-3 list the current consumption values for the operational mode of the device. The operational mode provides an estimation of what an application might encounter. The test case run to achieve the values shown does the following in a loop. Peripherals that are not on the following list have had their clocks disabled.

- Code is executing from RAM.
- FLASH is read and kept in active state.
- No external components are driven by I/O pins.
- All of the communication peripherals are exercised: SPI-A to SPI-C; SCI-A to SCI-C; I2C-A; CAN-A to CAN-C; LIN-A; PMBUS-A; and FSI-A.
- ePWM-1 to ePWM-3 generate a 5-MHz output on 6 pins.
- ePWM-4 to ePWM-7 are in HRPWM mode and generating 25 MHz on 6 pins.
- CPU timers are active.
- CPU does FIR16 calculations.
- DMA does continuous 32-bit transfers.
- CLA-1 is executing a 1024-point DFT in a background task.
- All ADCs perform continuous conversions.
- All DACs vary voltage at the loop frequency ~11 kHz.
- All PGAs are enabled.
- All CMPSSs generate a square wave with a 100-kHz frequency.
- SDFM peripheral clock is enabled.
- eCAP-1 to eCAP-7 are in APWM mode, toggling at 250 kHz.
- All eQEP watchdogs are enabled and counting.
- System watchdog is enabled and counting.


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### 5.5.2 Current Consumption Graphs

Figure 5-2, Figure 5-3, and Figure 5-4 show a typical representation of the relationship between frequency and current consumption on the device. The operational test from Table 5-1 was run across frequency at $V_{NOM}$ and room temperature. Actual results will vary based on the system implementation and conditions.

Leakage current on the VDD core supply will increase with operating temperature in an exponential manner as seen in Figure 5-5. The current consumption in HALT mode is primarily leakage current as there is no active switching if the internal oscillator has been powered down.

Figure 5-5 shows the typical leakage current across temperature. The device was placed into HALT mode under nominal voltage conditions.

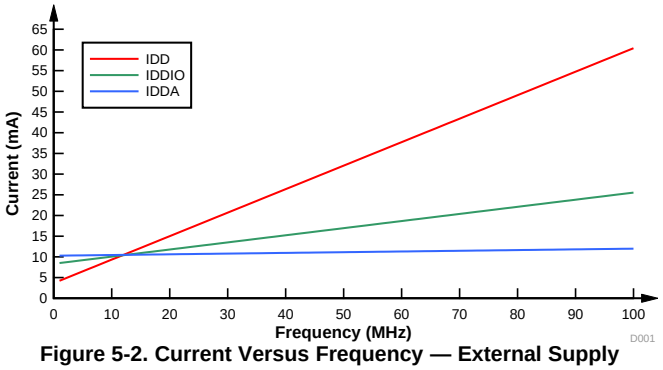



Figure 5-2. Current Versus Frequency — External Supply

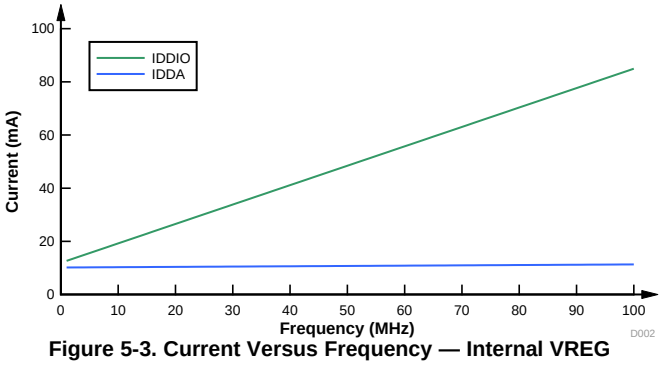



Figure 5-3. Current Versus Frequency — Internal VREG

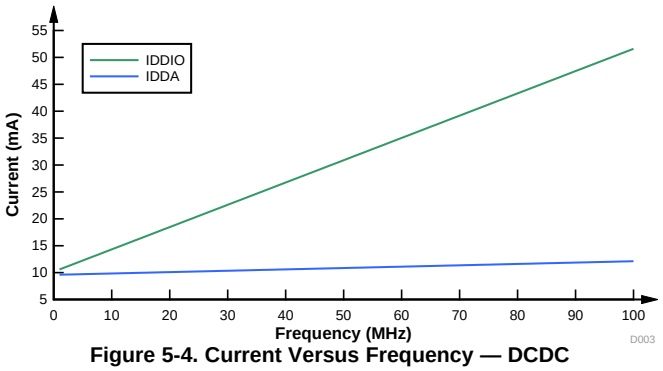



Figure 5-4. Current Versus Frequency — DCDC

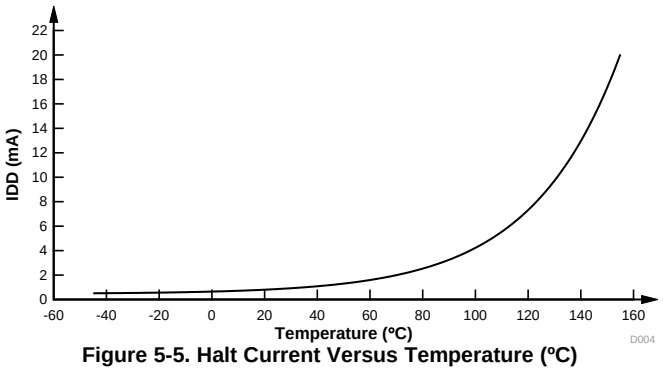



Figure 5-5. Halt Current Versus Temperature (ºC)

### 5.5.3 Reducing Current Consumption

All C2000™ microcontrollers provide some methods to reduce the device current consumption:

- Either of the two low-power modes—IDLE and HALT—could be entered to reduce the current consumption even further during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. Table 5-4 lists the typical current consumption value per peripheral at 100-MHz SYSCLK.

**Table 5-4. Typical $I_{DD}$ Current Reduction per Disabled Peripheral (at 100-MHz SYSCLK)(1)**

| PERIPHERAL | $I_{DD}$ CURRENT REDUCTION (mA) |
|---|---|
| ADC(2) | 0.8 |
| CAN | 1.1 |
| CLA | 0.4 |
| CLB | 1.1 |
| CMPSS(2) | 0.4 |
| CPU TIMER | 0.1 |
| DAC(2) | 0.2 |
| DMA | 0.5 |
| eCAP1 to eCAP5 | 0.1 |
| eCAP6 to eCAP7(3) | 0.4 |
| ePWM | 0.7 |
| eQEP | 0.1 |
| FSI | 0.7 |
| HRPWM | 0.8 |
| I2C | 0.3 |
| LIN | 0.4 |
| PGA(2) | 0.2 |
| PMBUS | 0.3 |
| SCI | 0.2 |
| SDFM | 0.9 |
| SPI | 0.2 |
| DCC | 0.1 |
| PLL at 100 MHz | 22.9 |

(1) All peripherals are disabled upon reset. Use the PCLKCRx register to individually enable peripherals. For peripherals with multiple instances, the current quoted is for a single module.
(2) This current represents the current drawn by the digital portion of the each module.
(3) eCAP6 and eCAP7 can also be configured as HRCAP.


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## 5.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Digital and Analog IO** | | | | | | | |
| $V_{OH}$ | High-level output voltage | | $I_{OH} = I_{OH}$ MIN | VDDIO * 0.8 | | | V |
| | | | $I_{OH}$ = –100 µA | VDDIO – 0.2 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL} = I_{OL}$ MAX | | | 0.4 | V |
| | | | $I_{OL}$ = 100 µA | | | 0.2 | |
| $I_{OH}$ | High-level output source current for all output pins | | | –4 | | | mA |
| $I_{OL}$ | Low-level output sink current for all output pins | | | | | 4 | mA |
| $R_{OH}$ | High-level output impedance for all output pins | | | | 70 | | Ω |
| $R_{OL}$ | Low-level output impedance for all output pins | | | | 70 | | Ω |
| $V_{IH}$ | High-level input voltage (3.3 V) | | | 2.0 | | VDDIO + 0.3 | V |
| $V_{IL}$ | Low-level input voltage (3.3 V) | | | VSS – 0.3 | | 0.8 | V |
| $V_{HYSTERESIS}$ | Input hysteresis | | | | 150 | | mV |
| $I_{PULLDOWN}$ | Input current | Inputs with pulldown (1) | VDDIO = 3.3 V<br>$V_{IN}$ = VDDIO | | 100 | | µA |
| $I_{PULLUP}$ | Input current | Digital inputs with pullup enabled (1) | VDDIO = 3.3 V<br>$V_{IN}$ = 0 V | | 160 | | µA |
| | | Analog inputs with pullup enabled (1) | VDDA = 3.3 V<br>$V_{IN}$ = 0 V | | 160 | | |
| $I_{LEAK}$ | Pin leakage | All GPIOs except GPIO23_VSW | Pullups and outputs disabled<br>0 V ≤ $V_{IN}$ ≤ VDDIO | | | 2 | µA |
| | | GPIO23_VSW | | | | 45 | |
| | | Analog pins (except ADCINB3/VDAC and PGAx_OF) | Analog drivers disabled<br>0 V ≤ $V_{IN}$ ≤ VDDA | | | 0.1 | |
| | | ADCINB3/VDAC | | | 2 | 11 | |
| | | PGAx_OF | | | | 0.25 | |
| $C_I$ | Input capacitance | All digital GPIOs except GPIO23_VSW | | | 2 | | pF |
| | | GPIO23_VSW | | | 100 | | |
| | | Analog pins (2) | | | | | |
| **VREG, DC-DC, and BOR** | | | | | | | |
| $V_{BOR-VDDIO}$ | VDDIO brownout reset voltage | | | 2.81 | | 3.0 | V |
| $V_{VREG}$ | Internal voltage regulator output | | Internal VREG On | | 1.2 | | V |
| $V_{DC-DC}$ | Internal switching regulator output | | Internal DC-DC On | | 1.2 | | V |
| Efficiency | Power efficiency of internal DC-DC switching regulator | | | 80% | | | |

(1) See Table 4-9 for a list of pins with a pullup or pulldown.
(2) The analog pins are specified separately; see Table 5-45.

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## 5.7 Thermal Resistance Characteristics

### 5.7.1 PZ Package

| | | °C/W(1) | AIR FLOW (lfm)(2) |
|---|---|---|---|
| $R\Theta_{JC}$ | Junction-to-case thermal resistance | 7.6 | N/A |
| $R\Theta_{JB}$ | Junction-to-board thermal resistance | 24.2 | N/A |
| $R\Theta_{JA}$ (High k PCB) | Junction-to-free air thermal resistance | 46.1 | 0 |
| $R\Theta_{JMA}$ | Junction-to-moving air thermal resistance | 37.3 | 150 |
| | | 34.8 | 250 |
| | | 32.6 | 500 |
| $Psi_{JT}$ | Junction-to-package top | 0.2 | 0 |
| | | 0.4 | 150 |
| | | 0.4 | 250 |
| | | 0.6 | 500 |
| $Psi_{JB}$ | Junction-to-board | 23.8 | 0 |
| | | 22.8 | 150 |
| | | 22.4 | 250 |
| | | 21.9 | 500 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

### 5.7.2 PM Package

| | | °C/W(1) | AIR FLOW (lfm)(2) |
|---|---|---|---|
| $R\Theta_{JC}$ | Junction-to-case thermal resistance | 12.4 | N/A |
| $R\Theta_{JB}$ | Junction-to-board thermal resistance | 25.6 | N/A |
| $R\Theta_{JA}$ (High k PCB) | Junction-to-free air thermal resistance | 51.8 | 0 |
| $R\Theta_{JMA}$ | Junction-to-moving air thermal resistance | 42.2 | 150 |
| | | 39.4 | 250 |
| | | 36.5 | 500 |
| $Psi_{JT}$ | Junction-to-package top | 0.5 | 0 |
| | | 0.9 | 150 |
| | | 1.1 | 250 |
| | | 1.4 | 500 |
| $Psi_{JB}$ | Junction-to-board | 25.1 | 0 |
| | | 23.8 | 150 |
| | | 23.4 | 250 |
| | | 22.7 | 500 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute


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### 5.7.3 RSH Package

| | | °C/W(1) | AIR FLOW (lfm)(2) |
|---|---|---|---|
| $R\Theta_{JC}$ | Junction-to-case thermal resistance | 11.9 | N/A |
| $R\Theta_{JB}$ | Junction-to-board thermal resistance | 3.3 | N/A |
| $R\Theta_{JA}$ (High k PCB) | Junction-to-free air thermal resistance | 25.8 | 0 |
| $R\Theta_{JMA}$ | Junction-to-moving air thermal resistance | 17.4 | 150 |
| | | 15.1 | 250 |
| | | 13.4 | 500 |
| $Psi_{JT}$ | Junction-to-package top | 0.2 | 0 |
| | | 0.3 | 150 |
| | | 0.4 | 250 |
| | | 0.4 | 500 |
| $Psi_{JB}$ | Junction-to-board | 3.3 | 0 |
| | | 3.2 | 150 |
| | | 3.2 | 250 |
| | | 3.2 | 500 |
| $R\Theta_{JC}$, bottom | Junction-to-bottom case thermal resistance | 0.7 | 0 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

## 5.8 Thermal Design Considerations

Based on the end application design and operational profile, the $I_{DD}$ and $I_{DDIO}$ currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature ($T_A$) varies with the end application and product design. The critical factor that affects reliability and functionality is $T_J$, the junction temperature, not the ambient temperature. Hence, care should be taken to keep $T_J$ within the specified limits. $T_{case}$ should be measured to estimate the operating junction temperature $T_J$. $T_{case}$ is normally measured at the center of the package top-side surface. The thermal application report *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

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## 5.9 System

### 5.9.1 Power Management

TMS320F28004x MCUs can be configured to operate with one of three options to supply the required 1.2 V to the core (VDD):

- An external supply (not available for 56-pin RSH package configurations)
- Internal 1.2-V LDO Voltage Regulator (VREG)
- Internal 1.2-V Switching Regulator (DC-DC)

The system requirements will dictate which supply option best suits the application.

**NOTE**

The same system voltage regulator must be used to drive both VDDIO and VDDIO_SW.

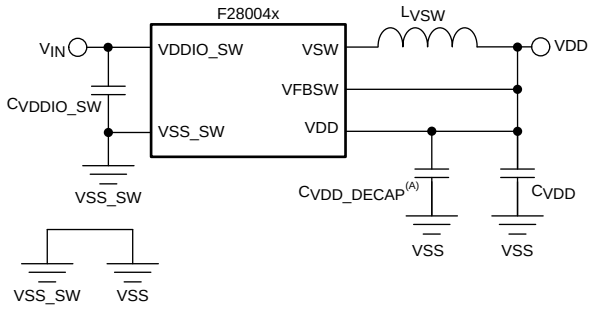
#### 5.9.1.1 Internal 1.2-V LDO Voltage Regulator (VREG)

The internal VREG is supplied by VDDIO and generates the 1.2 V required to power the VDD pins. Enable this functionality by pulling the VREGENZ pin low to VSS. The smaller pin-count packages may not include the VREGENZ pin; therefore, the internal VREG is always enabled and, as such, is the required supply source for the VDD pins. Review the description of VREGENZ in Table 4-5 to determine package configuration. Although the internal VREG eliminates the need to use an external power supply for VDD, decoupling capacitors are required on each VDD pin for VREG stability. There are two recommended capacitor configurations (described in the list that follows) for the VDD rail when using the internal VREG. The signal description for VDD can be found in Table 4-4.

- Configuration 1: Place a small decoupling capacitor to VSS on each pin as close to the device as possible. In addition, a bulk capacitance must be placed on the VDD node to VSS (one 20-µF capacitor or two parallel 10-µF capacitors).
- Configuration 2: Distribute the total capacitance to VSS evenly across all VDD pins (total capacitance divided by four VDD pins).

#### 5.9.1.2 Internal 1.2-V Switching Regulator (DC-DC)

The internal DC-DC regulator offers increased efficiency over the LDO for converting 3.3 V to 1.2 V. The internal DC-DC regulator is supplied by the VDDIO_SW pin and generates the 1.2 V required to power the VDD pins. To use the internal switching regulator, the core domain must power up initially using the internal LDO VREG supply (tie the VREGENZ pin low to VSS) and then transition to the DC-DC regulator through application software by setting the DCDCEN bit in the DCDCCTL register. The DC-DC regulator also requires external components (inductor, input capacitance, and output capacitance). The output of internal DC-DC regulator is not internally fed to the VDD rail and requires an external connection. Figure 5-6 shows the schematic implementation.




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A. One decoupling capacitor per each of the four VDD pins

**Figure 5-6. DC-DC Circuit Schematic**


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The VDDIO_SW supply pin ($V_{IN}$) requires a 3.3-V level voltage. A total input capacitance ($C_{VDDIO_SW}$) of 20 µF is required on VDDIO_SW. Due to the capacitor specification requirements detailed in Table 5-6, two parallel 10-µF capacitors in parallel is the recommended configuration. Decoupling capacitors of 100 nF should also be placed on each VDD pin as close to the device as possible.

**Table 5-5. DC-DC Inductor ($L_{VSW}$) Specifications Requirements**

| VALUE AND VARIATION | VALUE AT SATURATION | DCR | RATED CURRENT | SATURATION CURRENT | TEMPERATURE |
|---|---|---|---|---|---|
| 2.2 µH ± 20% | 1.54 µH ± 20% | 80 mΩ ± 25% | >1000 mA | >600 mA | –40°C to 125°C |

**Table 5-6. DC-DC Capacitor ($C_{VDDIO_SW}$ and $C_{VDD}$) Specifications Requirements**

| VALUE AND VARIATION AT 0 V | VALUE AT 1.2 V | VALUE AT 125°C | ESR | RATED VOLTAGE | TEMPERATURE |
|---|---|---|---|---|---|
| 10 µF ± 20% | 10 µF ± 20% | 8 µF ± 20% | <10 mΩ | 4 V or 6.3 V | –40°C to 125°C |

**Table 5-7. DC-DC Circuit Component Values**

| COMPONENT | MIN | NOM | MAX | UNIT | NOTES |
|---|---|---|---|---|---|
| Inductor | 1.76 | 2.2 | 2.64 | µH | 20% variance |
| Input capacitor | 8 | 10 | 12 | µF | 20% varaince, two such capacitors in parallel |
| Output capacitor | 8 | 10 | 12 | µF | 20% varaince, two such capacitors in parallel |

#### *5.9.1.2.1 PCB Layout and Component Guidelines*

For optimal performance the application board layout and component selection is important. The list that follows is a high-level guideline for laying out the DC-DC circuit.

- TI recommends star-connecting VDDIO_SW and VDDIO to the same 3.3-V supply.
- All external components should be placed as close to the pins as possible.
- The loop formed by the VDDIO_SW, input capacitor ($C_{VDDIO_SW}$), and VSS_SW must be as short as possible.
- The feedback trace must be as short as possible and kept away from any noise source such as the switching output (VSW).
- It is necessary to have a separate island or surgical cut in the ground plane for the input cap ($C_{VDDIO_SW}$) and VSS_SW.
- A VDD plane is recommended for connecting the VDD node to the $L_{VSW}$-$C_{VDD}$ point to minimize parasitic resistance and inductance.

**Table 5-8. Recommended External Components**

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{VDDIO}$ | Bulk capacitance on VDDIO | Based on External Supply IC Requirements (1) | | 0.1 | | µF |
| $C_{VDDIO_DECAP}$ | Decoupling capacitor on each VDDIO pin | | | 0.1 | | µF |
| $C_{VDDA}$ | Capacitor on VDDA pins | | | 2.2 | | µF |
| $C_{VDDIO_SW}$ | Capacitor on VDDIO_SW pin | For DC-DC operation (2) | | 20 | | µF |
| | | For LDO-only operation | | 0.1 | | |
| $C_{VDD}$ | Bulk capacitance on VDD | For DC-DC operation (2) | | 20 | | µF |
| | | For LDO-only operation (3) | 12 | 20 | 27 | |
| $C_{VDD_DECAP}$ | Decoupling capacitor on each VDD pin | For DC-DC operation (2) | | 0.1 | | µF |
| | | For LDO-only operation (3) | 0.1 | | 6.75 | |

(1) Bulk capacitance on this supply should be based on supply IC requirements.
(2) See Section 5.9.1.2 for details.
(3) See Section 5.9.1.1 for details.

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**Table 5-8. Recommended External Components (continued)**

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $L_{VSW}$ | Inductor between VSW pin and VDD node for DC-DC | | | 2.2 | | µH |
| $R_{LVSW-DCR}$ | Allowed DCR for $L_{VSW}$ | | | 80 | | mΩ |
| $I_{SAT-LVSW}$ | $L_{VSW}$ saturation current | | 600 | | | mA |

#### 5.9.1.3 Power Sequencing

**Signal Pin Requirements:** Before powering the device, no voltage larger than 0.3 V above VDDIO can be applied to any digital pin, and no voltage larger than 0.3 V above VDDA can be applied to any analog pin (including VREFHI).

**VDDIO, VDDIO_SW, and VDDA Requirements:** The 3.3-V supplies VDDIO, VDDIO_SW, and VDDA should be powered up together and kept within 0.3 V of each other during functional operation.

**VDD Requirements:** When VREGENZ is tied to VSS, the VDD sequencing requirements are handled by the device.

When using an external source for VDD (VREGENZ tied to VDDIO), VDDIO and VDD must be powered on and off at the same time. VDDIO should not be powered on when VDD is off. During the ramp, VDD should be kept no more than 0.3 V above VDDIO.

For applications not tying VREGENZ to VSS and not powering VDDIO and VDD at the same time, see the "INTOSC: VDDIO Powered Without VDD Can Cause INTOSC Frequency Drift" advisory in the *TMS320F28004x Piccolo™ Microcontrollers Silicon Errata*.

#### 5.9.1.4 Power-On Reset (POR)

An internal power-on reset (POR) circuit holds the device in reset and keeps the I/Os in a high-impedance state during power up. The POR is in control and forces XRSn low internally until the voltage on VDDIO crosses the POR threshold. When the voltage crosses the POR threshold, the internal brownout-reset (BOR) circuit takes control and holds the device in reset until the voltage crosses the BOR threshold (for internal BOR details, see Section 5.9.1.5).

#### 5.9.1.5 Brownout Reset (BOR)

An internal BOR circuit monitors the VDDIO rail for dips in voltage which result in the supply voltage dropping out of operational range. When the VDDIO voltage drops below the BOR threshold, the device is forced into reset, and XRSn is pulled low. XRSn will remain in reset until the voltage returns to the operational range. The BOR is enabled by default. To disable the BOR, set the BORLVMONDIS bit in the VMONCTL register. The internal BOR circuit monitors only the VDDIO rail. See Section 5.6 for BOR characteristics. External supply voltage supervisor (SVS) devices can be used to monitor the voltage on the 3.3-V and 1.2-V rails and to drive XRSn low if supplies fall outside operational specifications.


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### 5.9.2 Reset Timing

XRSn is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR). During power up, the POR circuit drives the XRSn pin low. A watchdog or NMI watchdog reset will also drive the pin low. An external circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and VDDIO. A capacitor should be placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to $V_{OL}$ within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 5-7 shows the recommended reset circuit.

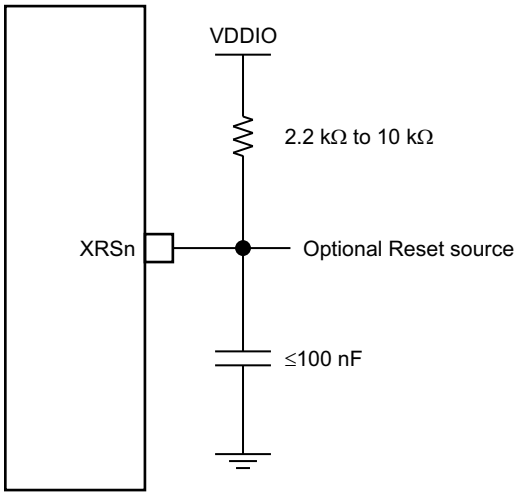



**Figure 5-7. Reset Circuit**

#### 5.9.2.1 Reset Sources

Table 5-9 summarizes the various reset signals and their effect on the device.

**Table 5-9. Reset Signals**

| RESET SOURCE | CPU CORE RESET (C28x, FPU, VCU) | PERIPHERALS RESET | JTAG/ DEBUG LOGIC RESET | I/Os | XRSn OUTPUT |
|---|---|---|---|---|---|
| POR | Yes | Yes | Yes | Hi-Z | Yes |
| XRSn Pin | Yes | Yes | Yes | Hi-Z | – |
| WDRS | Yes | Yes | Yes | Hi-Z | Yes |
| NMIWDRS | Yes | Yes | Yes | Hi-Z | Yes |
| SYSRS (Debugger Reset) | Yes | Yes | No | Hi-Z | No |
| SCCRESET | Yes | Yes | Yes | Hi-Z | No |

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The parameter $t_{h(boot-mode)}$ must account for a reset initiated from any of these sources.

See the Resets section of the System Control chapter in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

**CAUTION**

Some reset sources are internally driven by the device. Some of these sources will drive XRSn low, use this to disable any other devices driving the boot pins. The SCCRESET and debugger reset sources do not drive XRSn; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP; for more details, see the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.


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### 5.9.2.2 Reset Electrical Data and Timing

Table 5-10 lists the reset (XRSn) timing requirements. Table 5-11 lists the reset (XRSn) switching characteristics. Figure 5-8 shows the power-on reset. Figure 5-9 shows the warm reset.

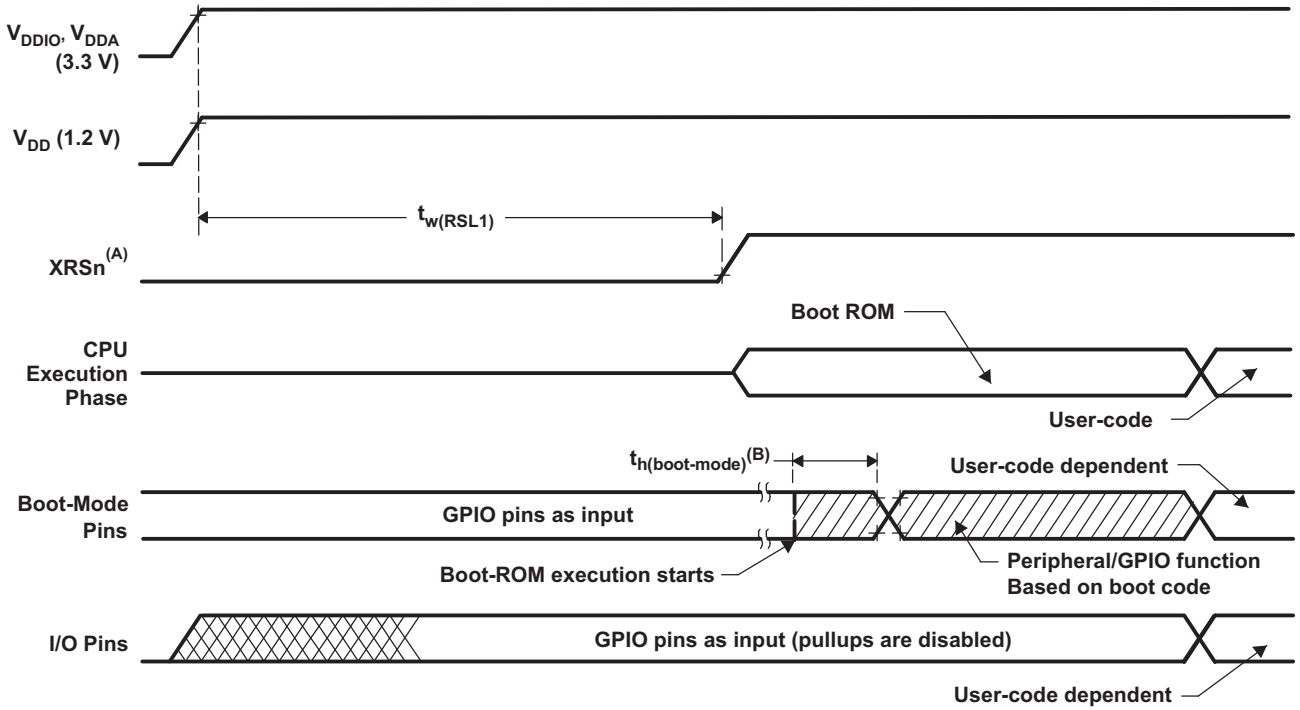
**Table 5-10. Reset (XRSn) Timing Requirements**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{h(boot\text{-}mode)}$ | Hold time for boot-mode pins | 1.5 | | ms |
| $t_{w(RSL2)}$ | Pulse duration, XRSn low on warm reset | 3.2 | | µs |

**Table 5-11. Reset (XRSn) Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(RSL1)}$ | Pulse duration, XRSn driven low by device after supplies are stable | | 100 | | µs |
| $t_{w(WDRS)}$ | Pulse duration, reset pulse generated by watchdog | | $512t_{c(OSCCLK)}$ | | cycles |

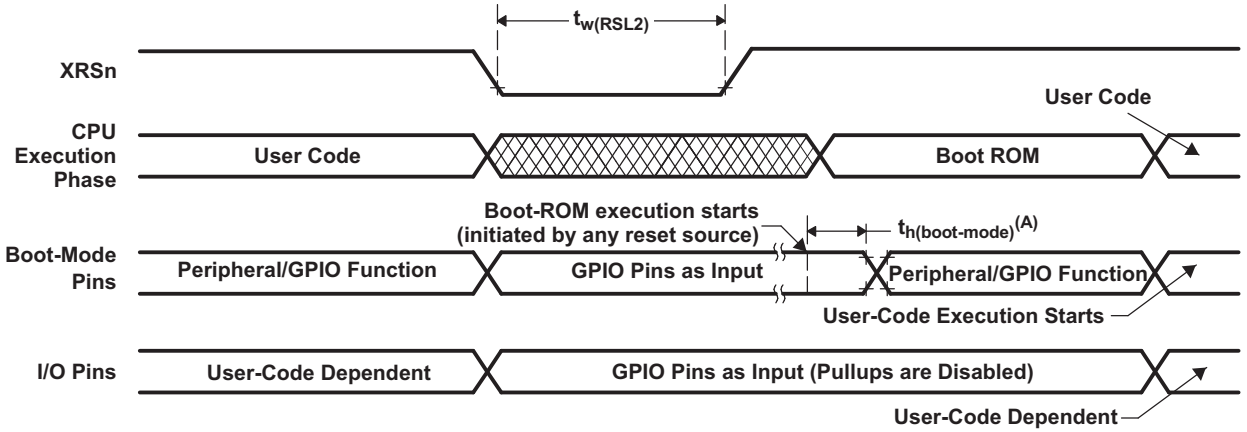



A. The XRSn pin can be driven externally by a supervisor or an external pullup resistor, see Table 4-1. On-chip POR logic will hold this pin low until the supplies are in a valid range.

B. After reset from any source (see Section 5.9.2.1), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

**Figure 5-8. Power-on Reset**

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A. After reset from any source (see Section 5.9.2.1), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

**Figure 5-9. Warm Reset**

## *5.9.3 Clock Specifications*

### 5.9.3.1 Clock Sources

Table 5-12 lists three possible clock sources. Figure 5-10 shows the clocking system. Figure 5-11 shows the system PLL.

**Table 5-12. Possible Reference Clock Sources**

| CLOCK SOURCE | MODULES CLOCKED | COMMENTS |
|---|---|---|
| INTOSC1 | Can be used to provide clock for:<br>• Watchdog block<br>• Main PLL<br>• CPU-Timer 2 | Internal oscillator 1.<br>Zero-pin overhead 10-MHz internal oscillator. |
| INTOSC2(1) | Can be used to provide clock for:<br>• Main PLL<br>• CPU-Timer 2 | Internal oscillator 2.<br>Zero-pin overhead 10-MHz internal oscillator. |
| X1 (XTAL) | Can be used to provide clock for:<br>• Main PLL<br>• CPU-Timer 2 | External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin. |

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for the system PLL (OSCCLK).


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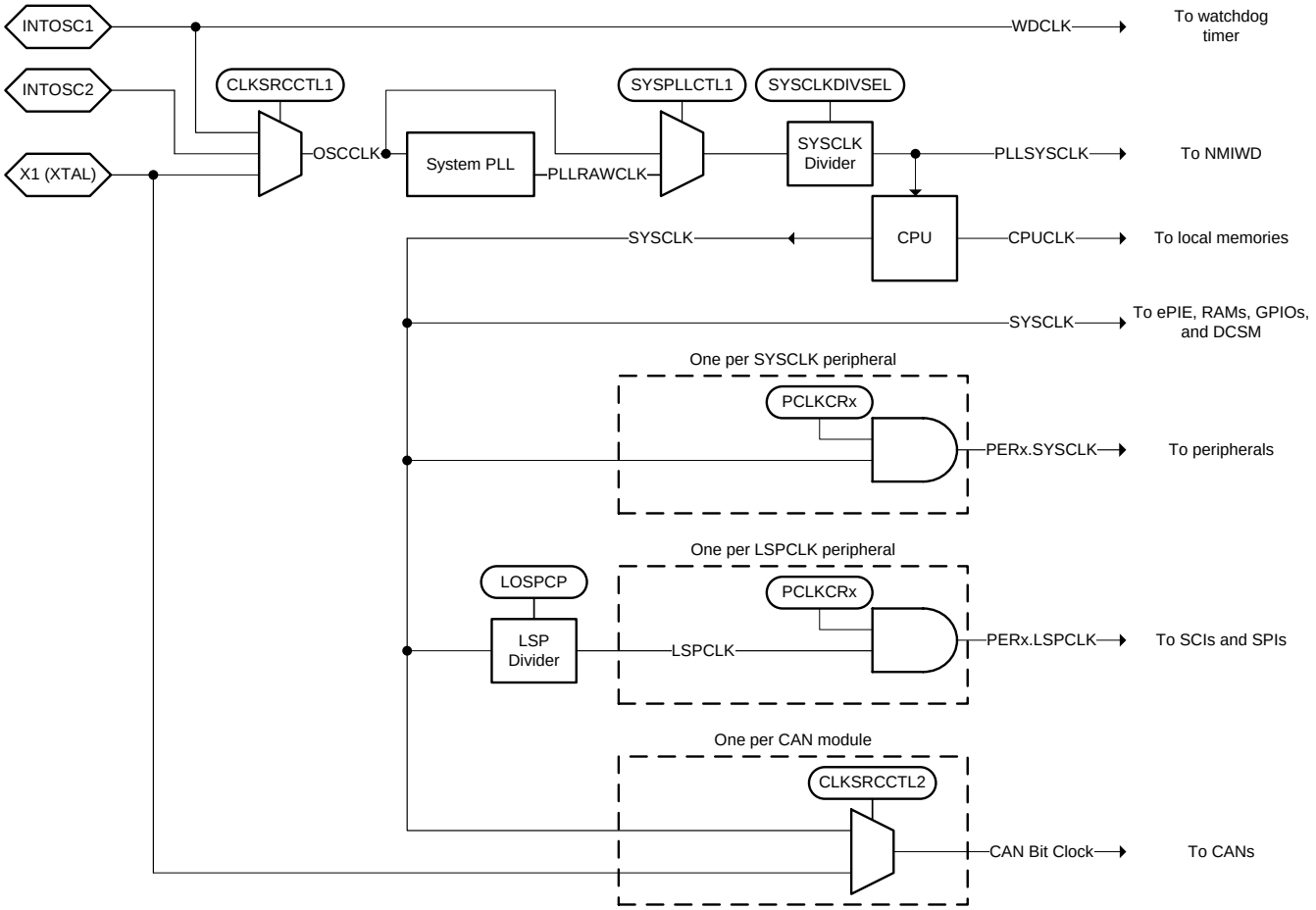



**Figure 5-10. Clocking System**

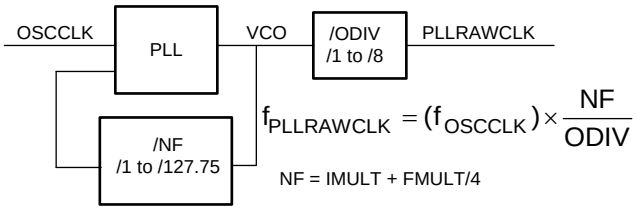



**Figure 5-11. System PLL**

#### 5.9.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

##### *5.9.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times*

Table 5-13 lists the frequency requirements for the input clocks. Table 5-14 lists the X1 input level characteristics when using an external clock source. Table 5-15 lists the XTAL oscillator characteristics. Table 5-16 lists the X1 timing requirements. Table 5-17 lists the PLL lock times for the Main PLL.

**Table 5-13. Input Clock Frequency**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{(XTAL)}$ | Frequency, X1/X2, from external crystal or resonator | 10 | 20 | MHz |
| $f_{(X1)}$ | Frequency, X1, from external oscillator ***(PLL enabled)*** | 2 | 20 | MHz |
| | Frequency, X1, from external oscillator ***(PLL disabled)*** | 2 | 100 | |

**Table 5-14. X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| X1 $V_{IL}$ | Valid low-level input voltage | –0.3 | 0.3 * VDDIO | V |
| X1 $V_{IH}$ | Valid high-level input voltage | 0.7 * VDDIO | VDDIO + 0.3 | V |

**Table 5-15. XTAL Oscillator Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| X1 $V_{IL}$ | Valid low-level input voltage | –0.3 | | 0.3 * VDDIO | V |
| X1 $V_{IH}$ | Valid high-level input voltage | 0.7 * VDDIO | | VDDIO + 0.3 | V |

**Table 5-16. X1 Timing Requirements**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{f(X1)}$ | Fall time, X1 | | 6 | ns |
| $t_{r(X1)}$ | Rise time, X1 | | 6 | ns |
| $t_{w(X1L)}$ | Pulse duration, X1 low as a percentage of $t_{c(X1)}$ | 45% | 55% | |
| $t_{w(X1H)}$ | Pulse duration, X1 high as a percentage of $t_{c(X1)}$ | 45% | 55% | |

**Table 5-17. PLL Lock Times**

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{(PLL)}$ | Lock time, Main PLL | | 25.5 µs + 1024 * $t_{c(OSCCLK)}$ | | µs |


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#### 5.9.3.2.2 Internal Clock Frequencies

Table 5-18 provides the clock frequencies for the internal clocks.

**Table 5-18. Internal Clock Frequencies**

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{(SYSCLK)}$ | Frequency, device (system) clock | 2 | | 100 | MHz |
| $t_{c(SYSCLK)}$ | Period, device (system) clock | 10 | | 500 | ns |
| $f_{(VCO)}$ | Frequency, PLL VCO (before output divider) | 120 | | 400 | MHz |
| $f_{(PLLRAWCLK)}$ | Frequency, system PLL output (before SYSCLK divider) | 15 | | 200 | MHz |
| $f_{(PLL)}$ | Frequency, PLLSYSCLK | 2 | | 100 | MHz |
| $f_{(LSP)}$ | Frequency, LSPCLK(1) | 2 | | 100 | MHz |
| $t_{c(LSPCLK)}$ | Period, LSPCLK | 10 | | 500 | ns |
| $f_{(OSCCLK)}$ | Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1) | | See respective clock | | MHz |
| $f_{(HRPWM)}$ | Frequency, HRPWMCLK | 60 | | 100 | MHz |

(1) Lower LSPCLK will reduce device power consumption. The default at reset is SYSCLK/4.

#### 5.9.3.2.3 Output Clock Frequency and Switching Characteristics

Table 5-19 lists the switching characteristics of the output clock, XCLKOUT.

**Table 5-19. XCLKOUT Switching Characteristics(1)(2)**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{f(XCO)}$ | Fall time, XCLKOUT | | 5 | ns |
| $t_{r(XCO)}$ | Rise time, XCLKOUT | | 5 | ns |
| $t_{w(XCOL)}$ | Pulse duration, XCLKOUT low | H – 2 | H + 2 | ns |
| $t_{w(XCOH)}$ | Pulse duration, XCLKOUT high | H – 2 | H + 2 | ns |
| $f_{(XCO)}$ | Frequency, XCLKOUT | | 50 | MHz |

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$

#### 5.9.3.3 Input Clocks and PLLs

**NOTE**

GPIO18* and its mux options can be used only when the system is clocked by INTOSC and X1 has an external pulldown resistor.

In addition to the internal 0-pin oscillators, three types of external clock sources are supported:

- A single-ended 3.3-V external clock. The clock signal should be connected to X1, as shown in Figure 5-12, with the XTALCR.SE bit set to 1.

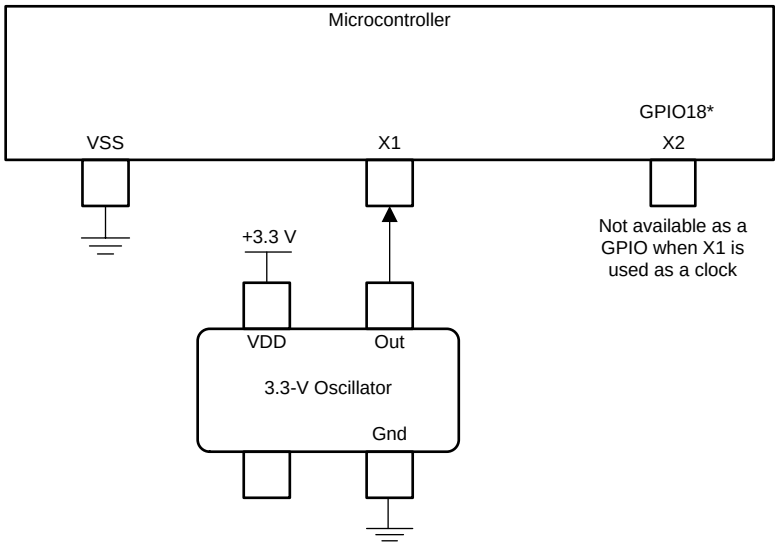



**Figure 5-12. Single-ended 3.3-V External Clock**

- An external crystal. The crystal should be connected across X1 and X2 with its load capacitors connected to VSS as shown in Figure 5-13.

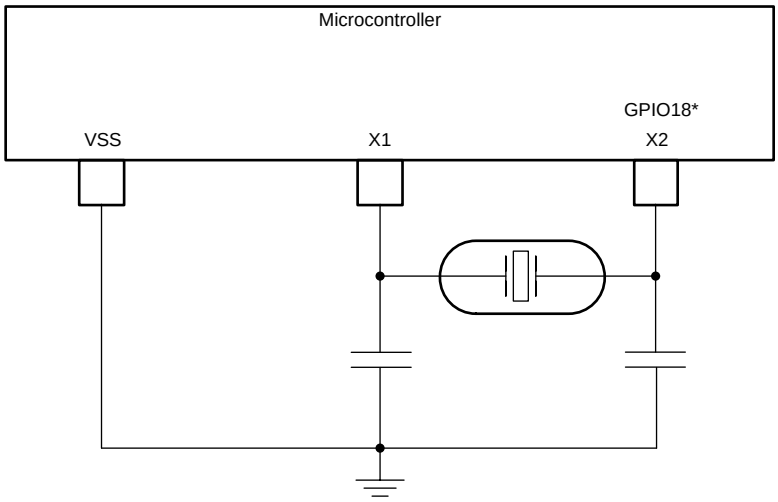



**Figure 5-13. External Crystal**

- An external resonator. The resonator should be connected across X1 and X2 with its ground connected to VSS as shown in Figure 5-14.


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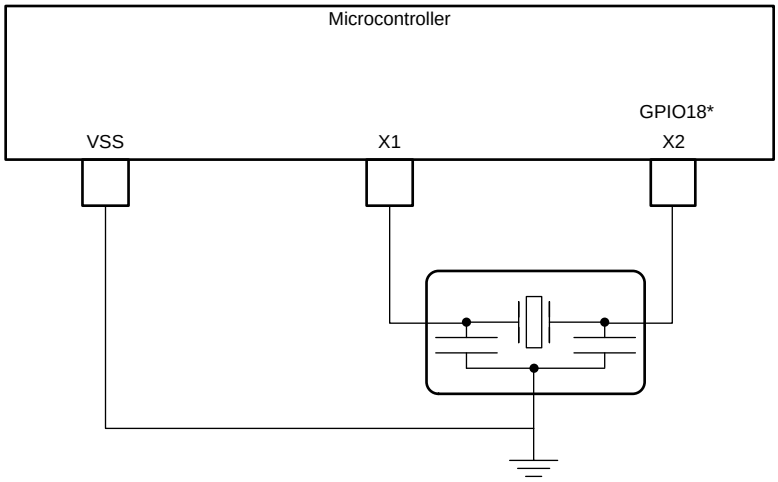



**Figure 5-14. External Resonator**

#### 5.9.3.4 Crystal Oscillator

When using a quartz crystal, it may be necessary to include a damping resistor ($R_D$) in the crystal circuit to prevent overdriving the crystal (drive level can be found in the crystal data sheet). In higher-frequency applications (10 MHz or greater), $R_D$ is generally not required. If a damping resistor is required, $R_D$ should be as small as possible because the size of the resistance affects start-up time (smaller $R_D$ = faster start-up time). TI recommends that the crystal manufacturer characterize the crystal with the application board. Table 5-20 lists the crystal oscillator parameters. Table 5-21 lists the crystal equivalent series resistance (ESR) requirements. Table 5-22 lists the crystal oscillator electrical characteristics.

**Table 5-20. Crystal Oscillator Parameters**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| CL1, CL2 | Load capacitance | 12 | 24 | pF |
| C0 | Crystal shunt capacitance | | 7 | pF |

**Table 5-21. Crystal Equivalent Series Resistance (ESR) Requirements(1)(2)**

| CRYSTAL FREQUENCY (MHz) | MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF) | MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF) |
|---|---|---|
| 10 | 55 | 110 |
| 12 | 50 | 95 |
| 14 | 50 | 90 |
| 16 | 45 | 75 |
| 18 | 45 | 65 |
| 20 | 45 | 50 |

(1) Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
(2) ESR = Negative Resistance/3

**Table 5-22. Crystal Oscillator Electrical Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Start-up time(1) | f = 20 MHz<br>ESR MAX = 50 Ω<br>CL1 = CL2 = 24 pF<br>C0 = 7 pF | | 2 | | ms |
| Crystal drive level (DL) | | | | 1 | mW |

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.


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#### 5.9.3.5 Internal Oscillators

To reduce production board costs and application development time, all F28004x devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, both oscillators are enabled at power up. INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source. INTOSC1 can also be manually configured as the system reference clock (OSCCLK). Table 5-23 provides the electrical characteristics of the internal oscillators to determine if this module meets the clocking requirements of the application.

**Table 5-23. INTOSC Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{INTOSC}$ | Frequency, INTOSC1 and INTOSC2 | | 9.7 | 10 | 10.3 | MHz |
| $f_{INTOSC-STABILITY}$ | Frequency stability at room temperature | 30°C, Nominal VDD | | ±0.1% | | |
| | Frequency stability over VDD | 30°C | | ±0.2% | | |
| | Frequency stability | | –3% | | 3% | |
| $t_{INT0SC-ST}$ | Start-up and settling time | | | | 20 | µs |

### 5.9.4 Flash Parameters

Table 5-24 lists the minimum required Flash wait states with different clock sources and frequencies.

**Table 5-24. Minimum Required Flash Wait States with Different Clock Sources and Frequencies(1)**

| CPUCLK (MHz) | EXTERNAL OSCILLATOR OR CRYSTAL | | INTOSC1 OR INTOSC2 | |
|---|---|---|---|---|
| | FLASH READ OR EXECUTE | PROGRAM, ERASE, BANK SLEEP, OR PUMP SLEEP | FLASH READ OR EXECUTE | PROGRAM, ERASE, BANK SLEEP, OR PUMP SLEEP (2) |
| 97 < CPUCLK ≤ 100 | 4 | | 4 | 5 |
| 80 < CPUCLK ≤ 97 | | | | 4 |
| 77 < CPUCLK ≤ 80 | 3 | | 3 | 4 |
| 60 < CPUCLK ≤ 77 | | | | 3 |
| 58 < CPUCLK ≤ 60 | 2 | | 2 | 3 |
| 40 < CPUCLK ≤ 58 | | | | 2 |
| 38 < CPUCLK ≤ 40 | 1 | | 1 | 2 |
| 20 < CPUCLK ≤ 38 | | | | 1 |
| 19 < CPUCLK ≤ 20 | 0 | | 0 | 1 |
| CPUCLK ≤ 19 | | | | 0 |

(1) Minimum required FRDCNTL[RWAIT].
(2) PROGRAM, ERASE, or SLEEP operations require an extra wait state when using INTOSC as the clock source for the frequency ranges indicated. Any wait state FRDCNTL[RWAIT] change must be made before beginning a PROGRAM, ERASE, or SLEEP mode operation. This setting impacts both flash banks. Applications which perform simultaneous READ of one bank and PROGRAM or ERASE of the other bank must use the higher RWAIT setting during the PROGRAM or ERASE operation or use a clock source or frequency with a common wait state setting.

The F28004x devices have an improved 128-bit prefetch buffer that provides high flash code execution efficiency across wait states. Figure 5-15 and Figure 5-16 illustrate typical efficiency across wait-state settings compared to previous-generation devices with a 64-bit prefetch buffer. Wait-state execution efficiency with a prefetch buffer will depend on how many branches are present in application software. Two examples of linear code and if-then-else code are provided.

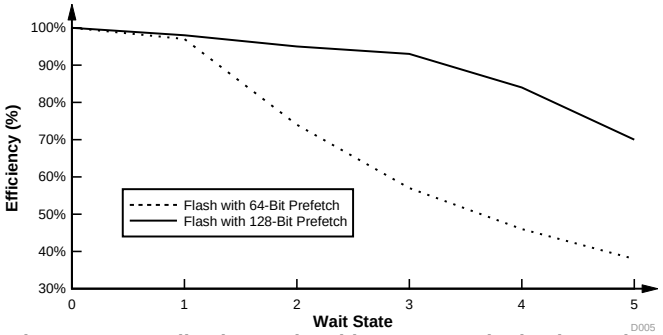



**Figure 5-15. Application Code With Heavy 32-Bit Floating-Point Math Instructions**

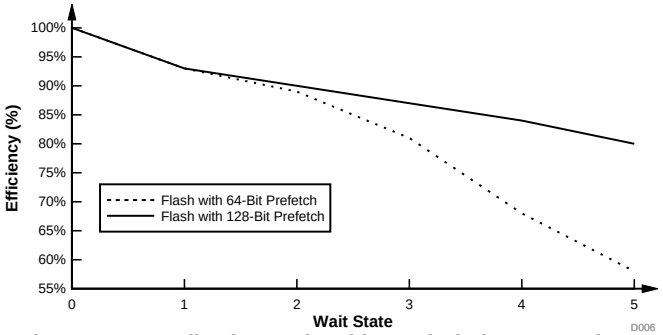



**Figure 5-16. Application Code With 16-Bit If-Else Instructions**


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Table 5-25 lists the Flash parameters.

**Table 5-25. Flash Parameters**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Program Time(1) | 128 data bits + 16 ECC bits | | 150 | 300 | µs |
| | 8KB sector | | 50 | 100 | ms |
| EraseTime(2) at < 25 cycles | 8KB sector | | 15 | 100 | ms |
| EraseTime(2) at 20K cycles | 8KB sector | | 120 | 4000 | ms |
| $N_{wec}$ Write/Erase Cycles | | | | 20000 | cycles |
| $t_{retention}$ Data retention duration at $T_J$ = 85°C | | 20 | | | years |

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the emulator used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Erase time includes Erase verify by the CPU.

**NOTE**

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle.

The DCSM OTP programming must be aligned to 128-bit address boundaries and each 128-bit word may only be programmed once. The exceptions are:

1. The DCSM Zx-LINKPOINTER1 and Zx-LINKPOINTER2 values in the DCSM OTP should be programmed together, and may be programmed 1 bit at a time as required by the DCSM operation.
2. The DCSM Zx-LINKPOINTER3 values in the DCSM OTP may be programmed 1 bit at a time on a 64-bit boundary to separate it from Zx-PSWDLOCK, which must only be programmed once.

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### 5.9.5 Emulation/JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. The cJTAG (IEEE Standard 1149.7-2009 for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture) port is a compact JTAG interface requiring only two pins (TMS and TCK), which allows other device functionality to be muxed to the traditional GPIO35 (TDI) and GPIO37 (TDO) pins.

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most emulator operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22-Ω resistors should be placed in series on each JTAG signal.

The PD (Power Detect) terminal of the emulator header should be connected to the board's 3.3-V supply. Header GND terminals should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output terminal back to the RTCK input terminal of the header (to sense clock continuity by the emulator). This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

Header terminal $\overline{\text{RESET}}$ is an open-drain output from the emulator header that enables board components to be reset through emulator commands (available only through the 20-pin header). Figure 5-17 shows how the 14-pin JTAG header connects to the MCU's JTAG port signals. Figure 5-18 shows how to connect to the 20-pin JTAG header. The 20-pin JTAG header terminals EMU2, EMU3, and EMU4 are not used and should be grounded.

For more information about hardware breakpoints and watchpoints, see Hardware Breakpoints and Watchpoints for C28x in CCS.

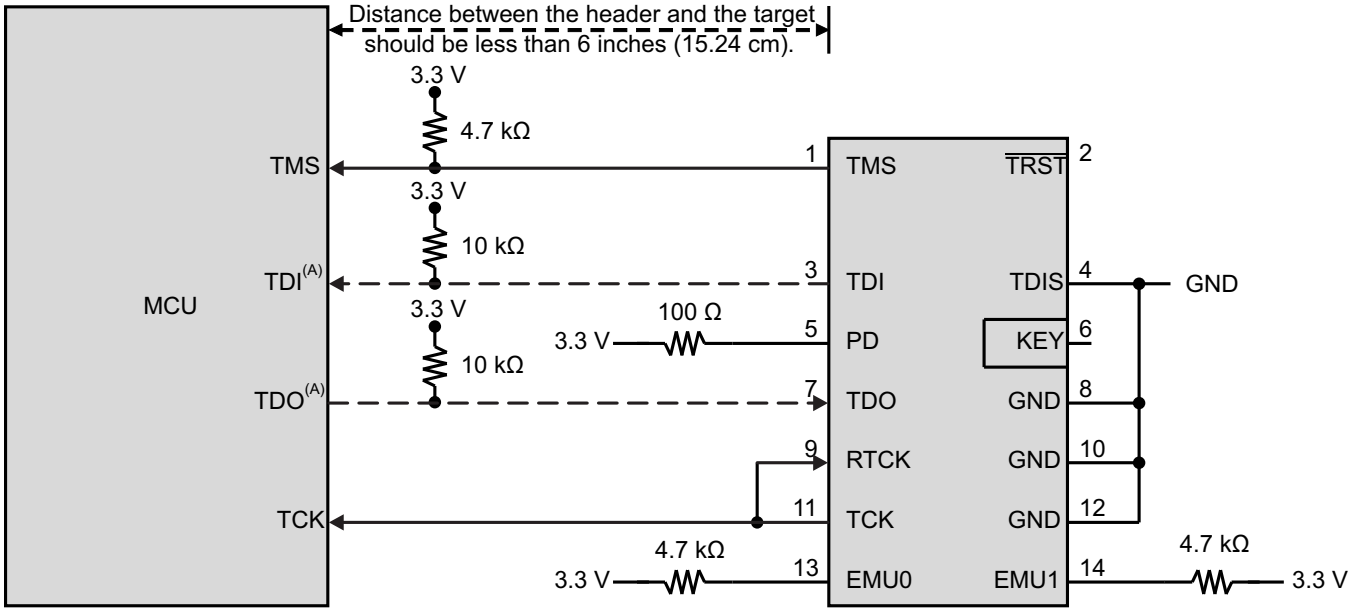
For more information about JTAG emulation, see the *XDS Target Connection Guide*.

**NOTE**

JTAG Test Data Input (TDI) is the default mux selection for the pin. The internal pullup is disabled by default. If this pin is used as JTAG TDI, the internal pullup should be enabled or an external pullup added on the board to avoid a floating input. In the cJTAG option, this pin can be used as GPIO.

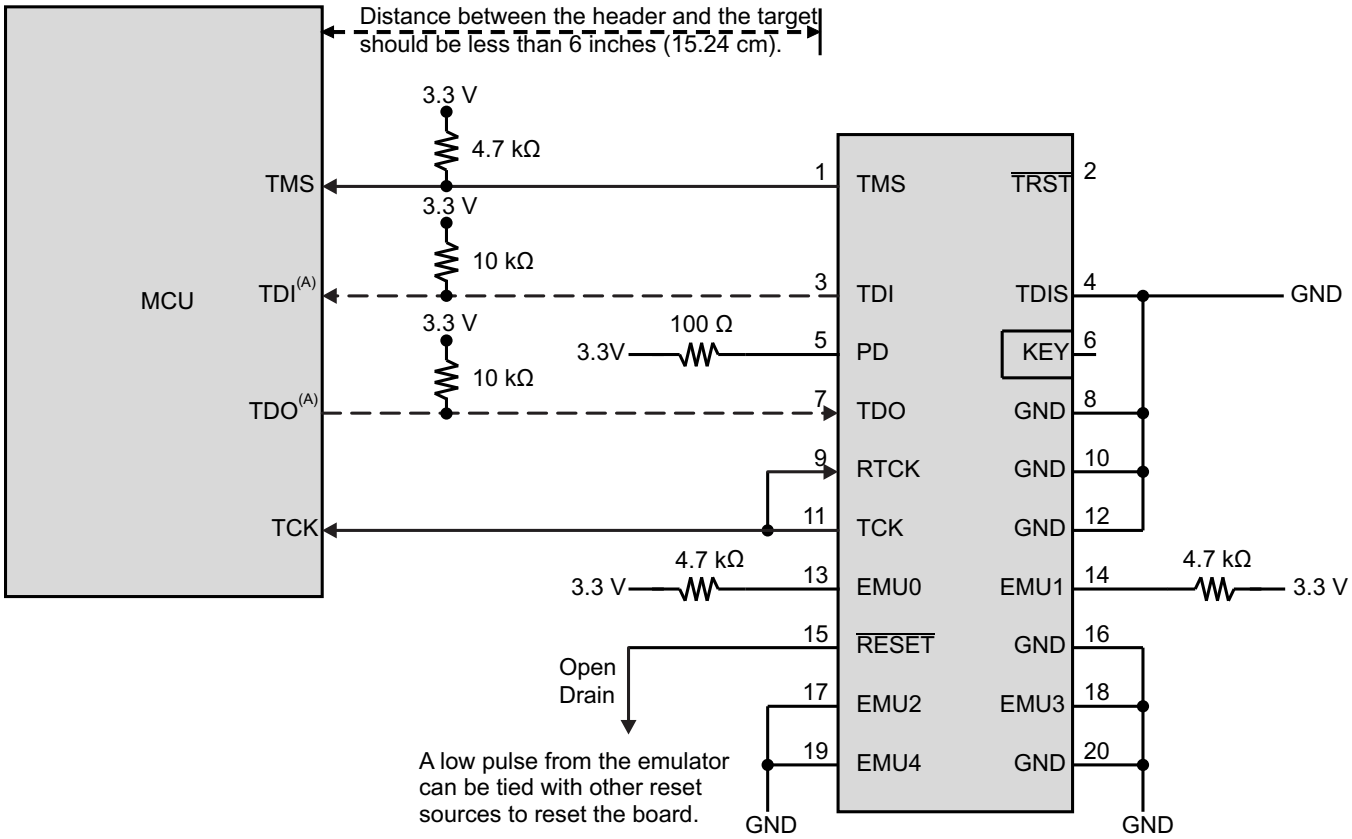
JTAG Test Data Output (TDO) is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating. The internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. In the cJTAG option, this pin can be used as GPIO.


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A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

**Figure 5-17. Connecting to the 14-Pin JTAG Header**




A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

**Figure 5-18. Connecting to the 20-Pin JTAG Header**

#### 5.9.5.1 JTAG Electrical Data and Timing

Table 5-26 lists the JTAG timing requirements. Table 5-27 lists the JTAG switching characteristics. Figure 5-19 shows the JTAG timing.

**Table 5-26. JTAG Timing Requirements**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 66.66 | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration, TCK high (40% of $t_c$) | 26.66 | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration, TCK low (40% of $t_c$) | 26.66 | | ns |
| 3 | $t_{su(TDI-TCKH)}$ | Input setup time, TDI valid to TCK high | 13 | | ns |
| | $t_{su(TMS-TCKH)}$ | Input setup time, TMS valid to TCK high | 13 | | |
| 4 | $t_{h(TCKH-TDI)}$ | Input hold time, TDI valid from TCK high | 7 | | ns |
| | $t_{h(TCKH-TMS)}$ | Input hold time, TMS valid from TCK high | 7 | | |

**Table 5-27. JTAG Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 2 | $t_{d(TCKL-TDO)}$ | Delay time, TCK low to TDO valid | 6 | 25 | ns |

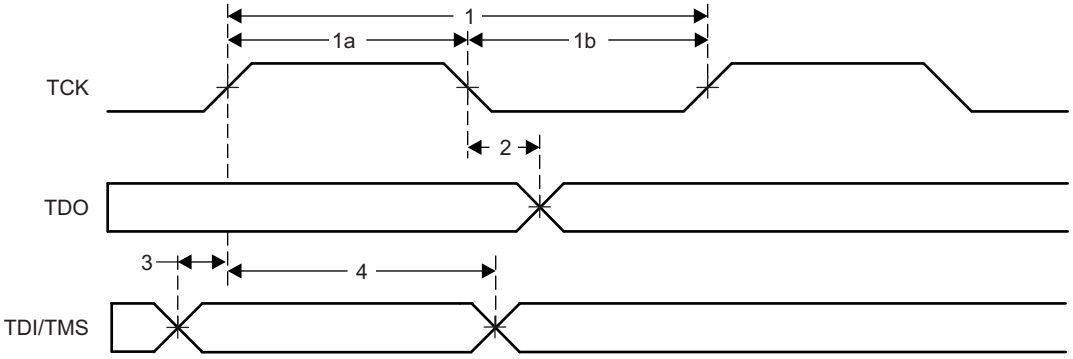



**Figure 5-19. JTAG Timing**


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### 5.9.5.2 cJTAG Electrical Data and Timing

Table 5-28 lists the cJTAG timing requirements. Table 5-29 lists the cJTAG switching characteristics. Figure 5-20 shows the cJTAG timing.

**Table 5-28. cJTAG Timing Requirements**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 100 | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration, TCK high (40% of $t_c$) | 40 | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration, TCK low (40% of $t_c$) | 40 | | ns |
| 3 | $t_{su(TMS-TCKH)}$ | Input setup time, TMS valid to TCK high | 15 | | ns |
| | $t_{su(TMS-TCKL)}$ | Input setup time, TMS valid to TCK low | 15 | | ns |
| 4 | $t_{h(TCKH-TMS)}$ | Input hold time, TMS valid from TCK high | 2 | | ns |
| | $t_{h(TCKL-TMS)}$ | Input hold time, TMS valid from TCK low | 2 | | ns |

**Table 5-29. cJTAG Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 2 | $t_{d(TCKL-TMS)}$ | Delay time, TCK low to TMS valid | 6 | 20 | ns |
| 5 | $t_{dis(TCKH-TMS)}$ | Delay time, TCK high to TMS disable | | 20 | ns |

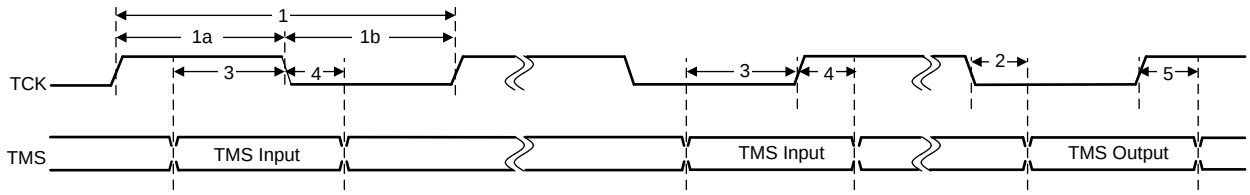



**Figure 5-20. cJTAG Timing**

### 5.9.6 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts. For more details, see the X-BAR chapter in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

#### 5.9.6.1 GPIO – Output Timing

Table 5-30 lists the general-purpose output switching characteristics. Figure 5-21 shows the general-purpose output timing.

**Table 5-30. General-Purpose Output Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{r(GPIO)}$ | Rise time, GPIO switching low to high | All GPIOs except GPIO23_VSW | | 8(1) | ns |
| $t_{f(GPIO)}$ | Fall time, GPIO switching high to low | All GPIOs except GPIO23_VSW | | 8(1) | ns |
| $f_{GPIO}$ | Toggling frequency, all GPIOs except GPIO23_VSW | | | 25 | MHz |

(1) Rise time and fall time vary with load. These values assume a 40-pF load.

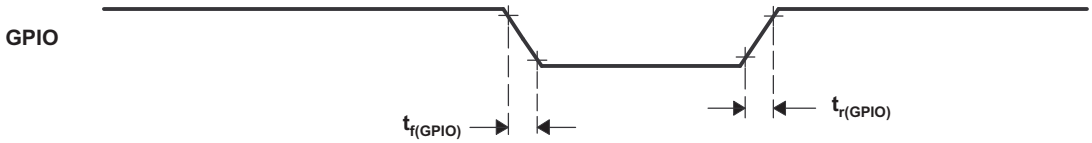



**Figure 5-21. General-Purpose Output Timing**


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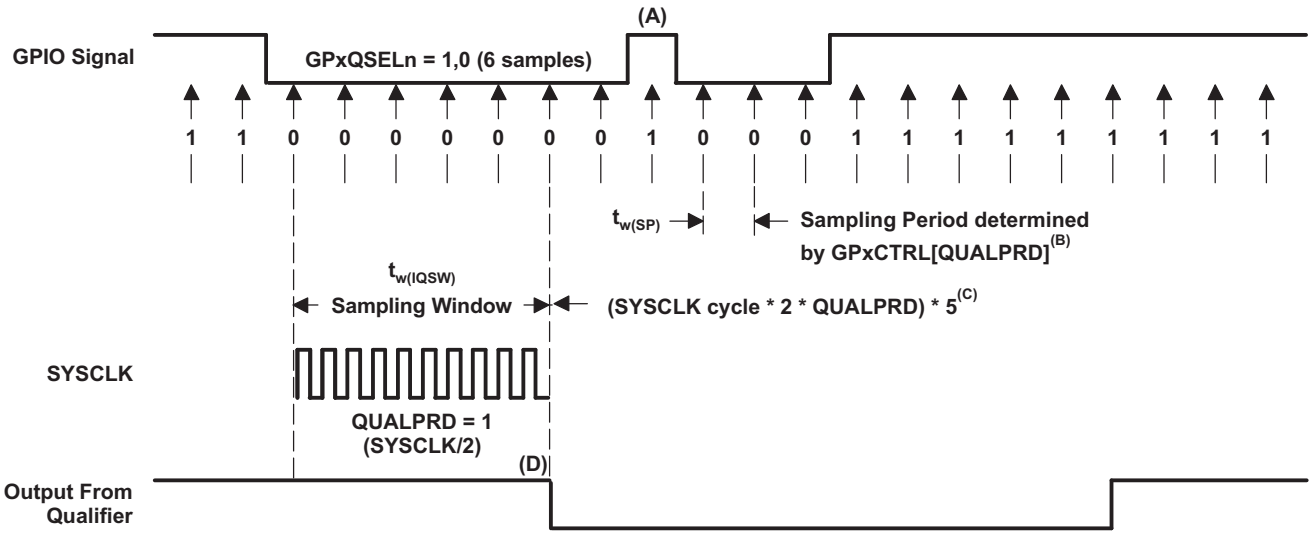
### 5.9.6.2 GPIO – Input Timing

Table 5-31 lists the general-purpose input timing requirements. Figure 5-22 shows the sampling mode.

**Table 5-31. General-Purpose Input Timing Requirements**

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(SP)}$ | Sampling period | QUALPRD = 0 | $1t_{c(SYSCLK)}$ | | cycles |
| | | QUALPRD ≠ 0 | $2t_{c(SYSCLK)}$ * QUALPRD | | |
| $t_{w(IQSW)}$ | Input qualifier sampling window | | $t_{w(SP)}$ * ($n^{(1)}$ – 1) | | cycles |
| $t_{w(GPI)}$ (2) | Pulse duration, GPIO low/high | Synchronous mode | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $t_{w(IQSW)}$ + $t_{w(SP)}$ + $1t_{c(SYSCLK)}$ | | |

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from $V_{IL}$ to $V_{IL}$ for an active low signal and $V_{IH}$ to $V_{IH}$ for an active high signal.




A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period in 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).

B. The qualification period selected through the GPxCTRL register applies to groups of eight GPIO pins.

C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.

D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for (5 × QUALPRD × 2) SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLK-wide pulse ensures reliable recognition.

**Figure 5-22. Sampling Mode**

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#### 5.9.6.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = SYSCLK/(2 × QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLK, if QUALPRD = 0

Sampling period = SYSCLK cycle × 2 × QUALPRD, if QUALPRD ≠ 0

In the previous equations, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

**Case 1:**

Qualification using 3 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 2, if QUALPRD = 0

**Case 2:**

Qualification using 6 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 5, if QUALPRD = 0

Figure 5-23 shows the general-purpose input timing.

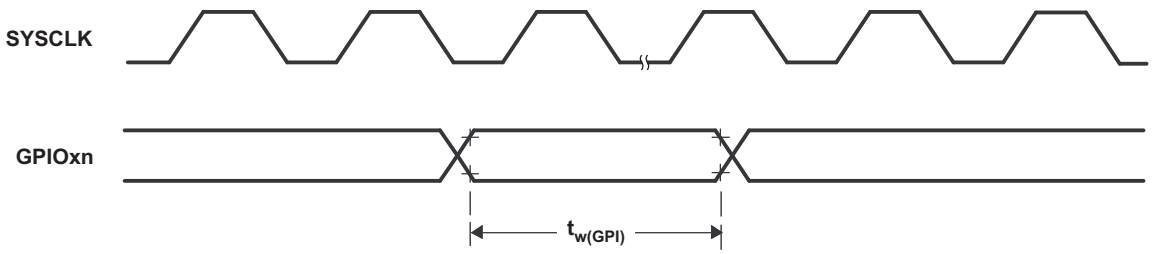



**Figure 5-23. General-Purpose Input Timing**


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### 5.9.7 Interrupts

The C28x CPU has fourteen peripheral interrupt lines. Two of them (INT13 and INT14) are connected directly to CPU timers 1 and 2, respectively. The remaining twelve are connected to peripheral interrupt signals through the enhanced Peripheral Interrupt Expansion (ePIE) module. The ePIE multiplexes up to sixteen peripheral interrupts into each CPU interrupt line. It also expands the vector table to allow each interrupt to have its own ISR. This allows the CPU to support a large number of peripherals.

An interrupt path is divided into three stages—the peripheral, the ePIE, and the CPU. Each stage has its own enable and flag registers. This system allows the CPU to handle one interrupt while others are pending, implement and prioritize nested interrupts in software, and disable interrupts during certain critical tasks.

Figure 5-24 shows the interrupt architecture for this device.

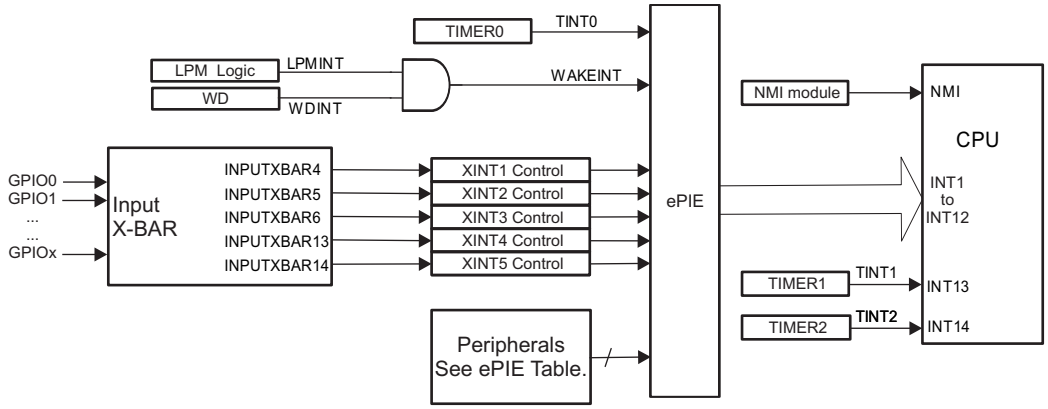



**Figure 5-24. Device Interrupt Architecture**

### 5.9.7.1 External Interrupt (XINT) Electrical Data and Timing

Table 5-32 lists the external interrupt timing requirements. Table 5-33 lists the external interrupt switching characteristics. Figure 5-25 shows the external interrupt timing.

**Table 5-32. External Interrupt Timing Requirements(1)**

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(INT)}$ | Pulse duration, INT input low/high | Synchronous | $2t_{c(SYSCLK)}$ | | cycles |
| | | With qualifier | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$ | | |

(1) For an explanation of the input qualifier parameters, see Table 5-31.

**Table 5-33. External Interrupt Switching Characteristics(1)**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(INT)}$ | Delay time, INT low/high to interrupt-vector fetch(2) | $t_{w(IQSW)} + 14t_{c(SYSCLK)}$ | $t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCLK)}$ | cycles |

(1) For an explanation of the input qualifier parameters, see Table 5-31.
(2) This assumes that the ISR is in a single-cycle memory.

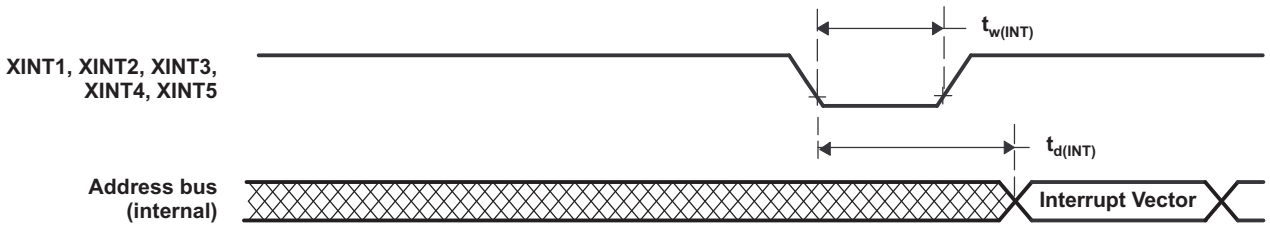



**Figure 5-25. External Interrupt Timing**


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### 5.9.8 Low-Power Modes

This device has HALT and IDLE as two clock-gating low-power modes. STANDBY mode is not supported on this device. See the *TMS320F28004x Piccolo™ Microcontrollers Silicon Errata* for more details.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the Low Power Modes section of the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

#### 5.9.8.1 Clock-Gating Low-Power Modes

IDLE and HALT modes on this device are similar to those on other C28x devices. Table 5-34 describes the effect on the system when any of the clock-gating low-power modes are entered.

**Table 5-34. Effect of Clock-Gating Low-Power Modes on the Device**

| MODULES/ CLOCK DOMAIN | IDLE | HALT |
|---|---|---|
| SYSCLK | Active | Gated |
| CPUCLK | Gated | Gated |
| Clock to modules connected to PERx.SYSCLK | Active | Gated |
| WDCLK | Active | Gated if CLKSRCCTL1.WDHALTI = 0 |
| PLL | Powered | Software must power down PLL before entering HALT. |
| INTOSC1 | Powered | Powered down if CLKSRCCTL1.WDHALTI = 0 |
| INTOSC2 | Powered | Powered down if CLKSRCCTL1.WDHALTI = 0 |
| Flash (1) | Powered | Powered |
| XTAL (2) | Powered | Powered |

(1) The Flash module is not powered down by hardware in any LPM. It may be powered down using software if required by the application. For more information, see the Flash and OTP Memory section of the System Control chapter in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

(2) The XTAL is not powered down by hardware in any LPM. It may be powered down by software setting the XTALCR.OSCOFF bit to 1. This can be done at any time during the application if the XTAL is not required.

### 5.9.8.2 Low-Power Mode Wake-up Timing

Table 5-35 lists the IDLE mode timing requirements, Table 5-36 lists the switching characteristics, and Figure 5-26 shows the timing diagram for IDLE mode.

**Table 5-35. IDLE Mode Timing Requirements(1)**

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(WAKE)}$ | Pulse duration, external wake-up signal | Without input qualifier | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |

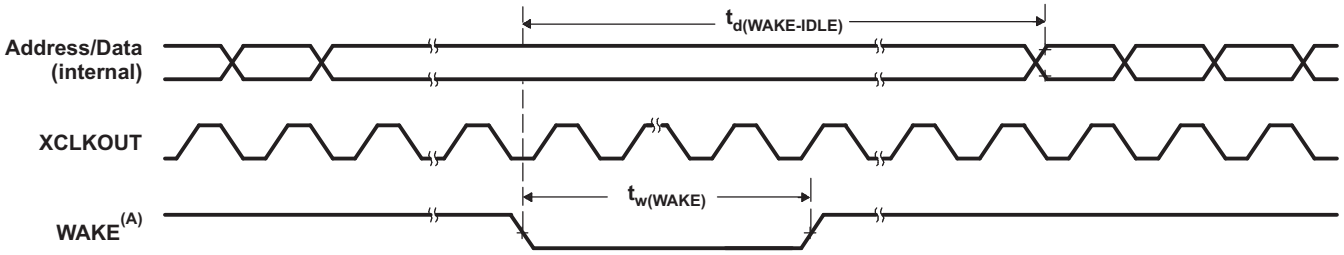
(1) For an explanation of the input qualifier parameters, see Table 5-31.

**Table 5-36. IDLE Mode Switching Characteristics(1)**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(WAKE-IDLE)}$ | Delay time, external wake signal to program execution resume (2) | | | | cycles |
| | • Wake up from flash<br>– Flash module in active state | Without input qualifier | | $40t_{c(SYSCLK)}$ | |
| | | With input qualifier | | $40t_{c(SYSCLK)} + t_{w(WAKE)}$ | |
| | • Wake up from flash<br>– Flash module in sleep state | Without input qualifier | | $6700t_{c(SYSCLK)}$ (3) | |
| | | With input qualifier | | $6700t_{c(SYSCLK)}$ (3) $+ t_{w(WAKE)}$ | |
| | • Wake up from RAM | Without input qualifier | | $25t_{c(SYSCLK)}$ | |
| | | With input qualifier | | $25t_{c(SYSCLK)} + t_{w(WAKE)}$ | |

(1) For an explanation of the input qualifier parameters, see Table 5-31.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(3) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash/OTP and Pump Power Modes and Wakeup section of the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.




A. WAKE can be any enabled interrupt, $\overline{\text{WDINT}}$ or XRSn. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

**Figure 5-26. IDLE Entry and Exit Timing Diagram**


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Table 5-37 lists the HALT mode timing requirements, Table 5-38 lists the switching characteristics, and Figure 5-27 shows the timing diagram for HALT mode.

**Table 5-37. HALT Mode Timing Requirements**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{w(WAKE-GPIO)}$ | Pulse duration, GPIO wake-up signal(1) | $t_{oscst} + 2t_{c(OSCCLK)}$ | | cycles |
| $t_{w(WAKE-XRS)}$ | Pulse duration, XRSn wake-up signal(1) | $t_{oscst} + 8t_{c(OSCCLK)}$ | | cycles |

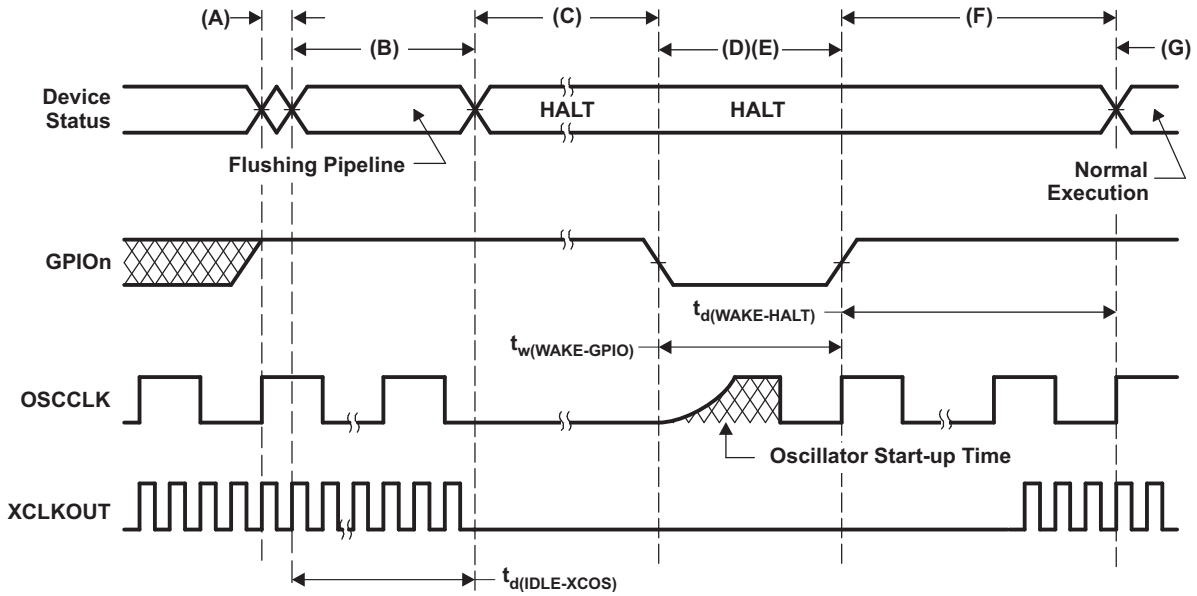
(1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See Table 5-22 for more information. For applications using INTOSC1 or INTOSC2 for OSCCLK, see Section 5.9.3.5 for $t_{oscst}$. Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

**Table 5-38. HALT Mode Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(IDLE-XCOS)}$ | Delay time, IDLE instruction executed to XCLKOUT stop | | $16t_{c(INTOSC1)}$ | cycles |
| $t_{d(WAKE-HALT)}$ | Delay time, external wake signal end to CPU program execution resume | | | cycles |
| | • Wake up from flash<br>– Flash module in active state | | $75t_{c(OSCCLK)}$ | |
| | • Wake up from flash<br>– Flash module in sleep state | | $17500t_{c(OSCCLK)}$ (1) | |
| | • Wake up from RAM | | $75t_{c(OSCCLK)}$ | |

(1) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash/OTP and Pump Power Modes and Wakeup section of the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.




A. IDLE instruction is executed to put the device into HALT mode.

B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wake-up procedure, care should be taken to maintain a low noise environment before entering and during HALT mode.

E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.

F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.

G. Normal operation resumes.

H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

**Figure 5-27. HALT Entry and Exit Timing Diagram**


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## 5.10 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device include the ADC, PGA, temperature sensor, buffered DAC, and CMPSS.

The analog subsystem has the following features:

- Flexible voltage references
  - The ADCs are referenced to VREFHIx and VREFLOx pins.
    - VREFHIx pin voltage can be driven in externally or can be generated by an internal bandgap voltage reference.
    - The internal voltage reference range can be selected to be 0 V to 3.3 V or 0 V to 2.5 V.
- The buffered DACs are referenced to VREFHIx and VREFLOx.
  - Alternately, these DACs can be referenced to the VDAC pin and VSSA.
- The comparator DACs are referenced to VDDA and VSSA.
  - Alternately, these DACs can be referenced to the VDAC pin and VSSA.
- Flexible pin usage
  - Buffered DAC outputs, comparator subsystem inputs, PGA functions, and digital inputs are multiplexed with ADC inputs
  - Internal connection to VREFLO on all ADCs for offset self-calibration

Figure 5-28 shows the Analog Subsystem Block Diagram for the 100-pin PZ LQFP.

Figure 5-29 shows the Analog Subsystem Block Diagram for the 64-pin PM LQFP.

Figure 5-30 shows the Analog Subsystem Block Diagram for the 56-pin RSH VQFN.

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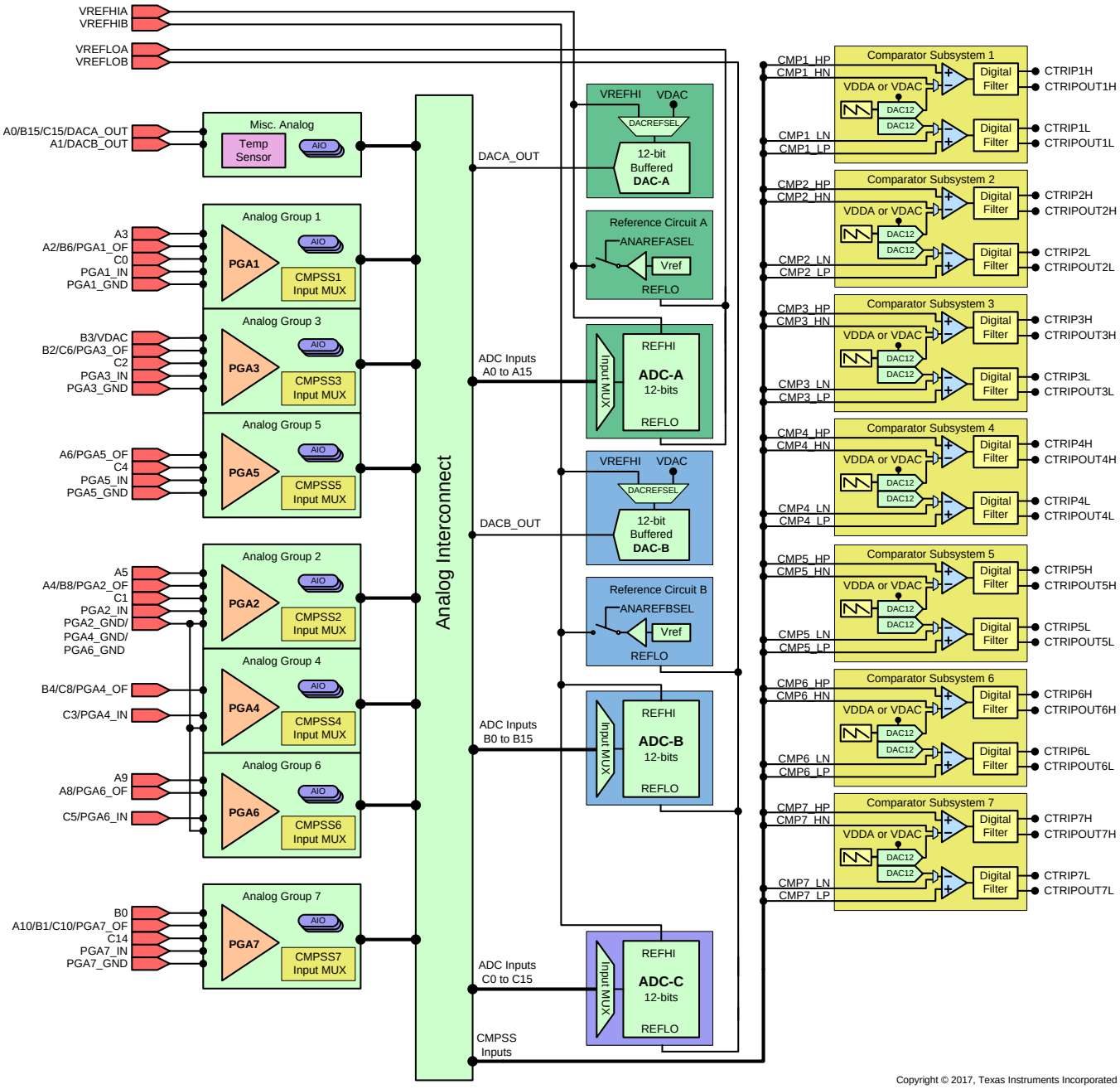
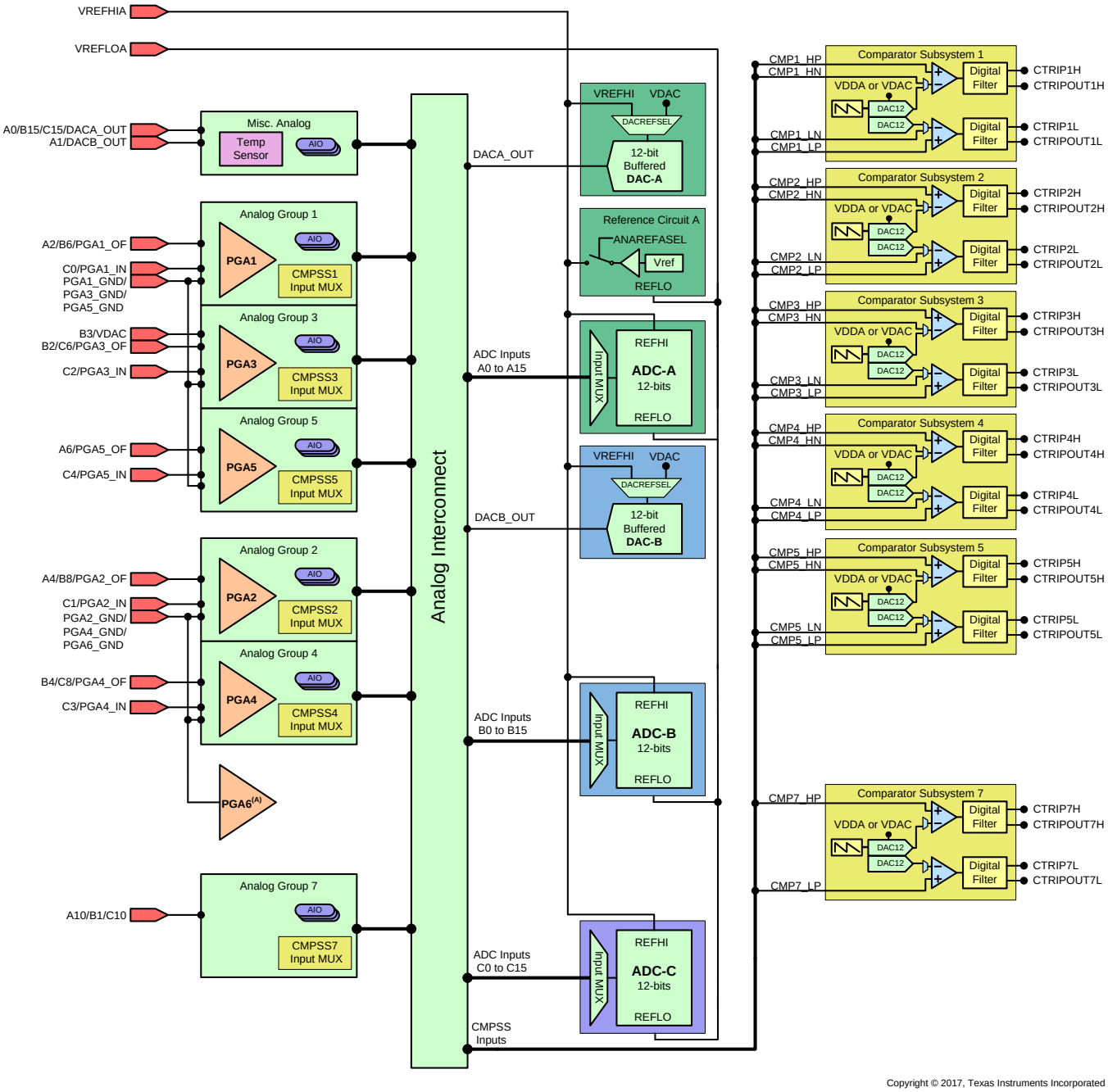



**Figure 5-28. Analog Subsystem Block Diagram (100-Pin PZ LQFP)**

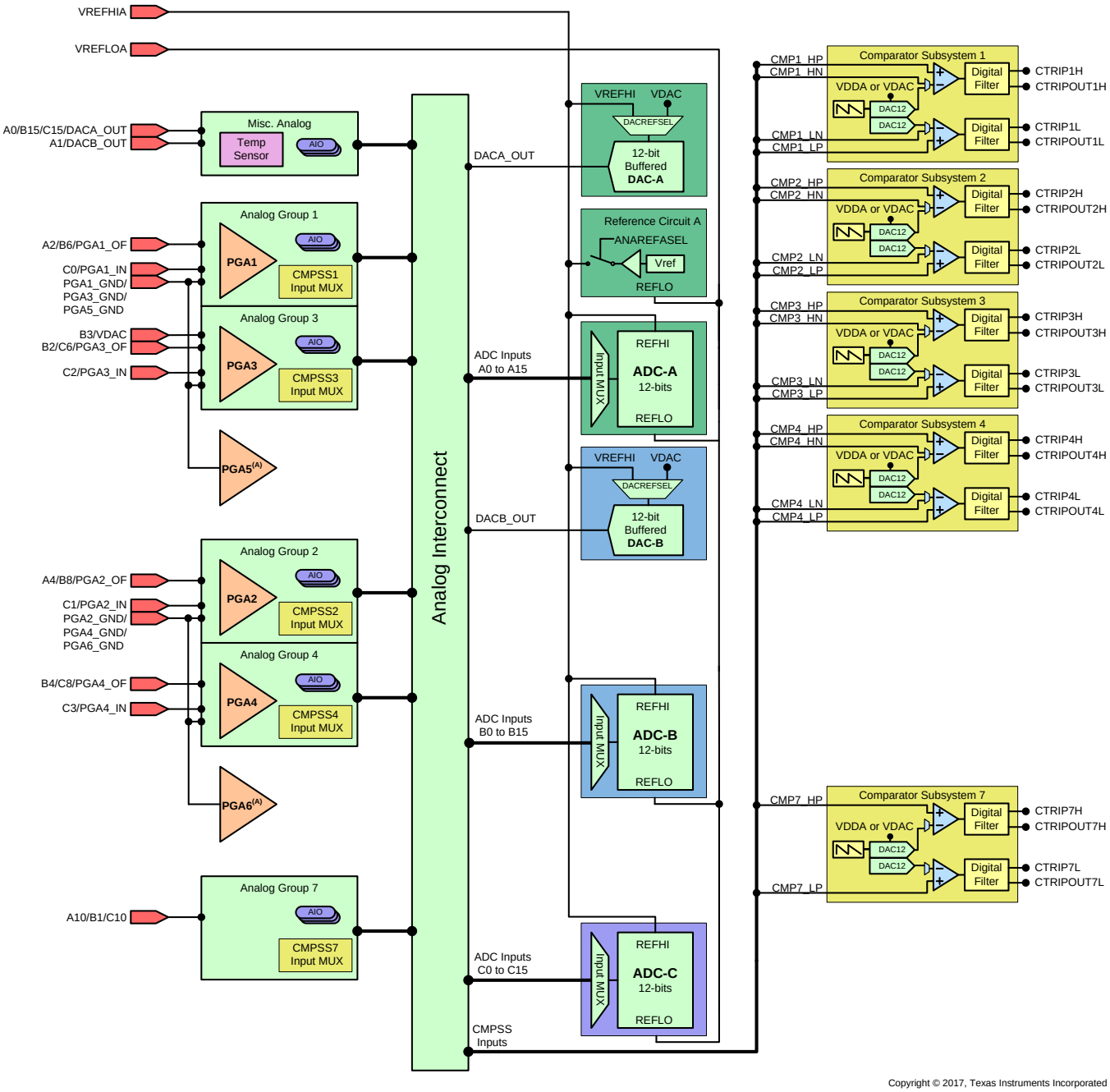

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A. This PGA has no input/output connections on this package, but should be enabled and disabled at the same time as other PGAs with a shared PGA ground.

**Figure 5-29. Analog Subsystem Block Diagram (64-Pin PM LQFP)**



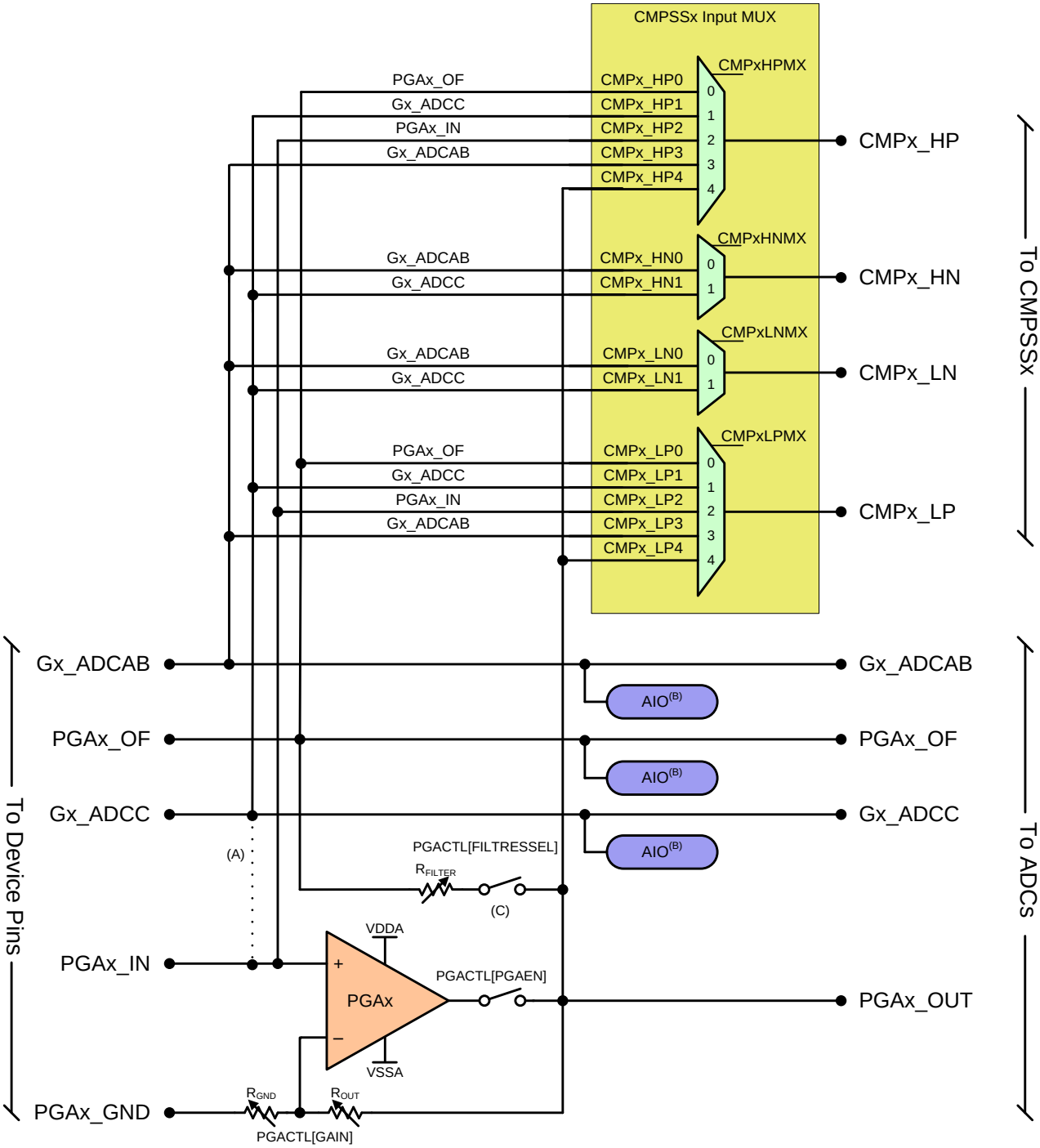

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A. This PGA has no input/output connections on this package, but should be enabled and disabled at the same time as other PGAs with a shared PGA ground.

**Figure 5-30. Analog Subsystem Block Diagram (56-Pin RSH VQFN)**


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Figure 5-31 shows the analog group connections. See Table 5-39 for the specific connections for each group for each package. Table 5-40 provides descriptions of the analog signals.




A. On lower pin-count packages, the input to Gx_ADCC will share a pin with the PGA input. If the PGA input is unused, then the ADCC input can allow the pin to be used as an ADC input, a negative comparator input, or a digital input.

B. AIOs support digital input mode only.

C. The PGA RFILTER path is not available on some device revisions. See the *TMS320F28004x Piccolo™ Microcontrollers Silicon Errata* for more information.

**Figure 5-31. Analog Group Connections**

## Table 5-39. Analog Pins and Internal Connections

| PIN NAME | GROUP NAME | PACKAGE | | | ALWAYS CONNECTED (NO MUX) | | | | | COMPARATOR SUBSYSTEM (MUX) | | | | AIO INPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 100 PZ | 64 PM | 56 RSH | ADCA | ADCB | ADCC | PGA | DAC | HIGH POSITIVE | HIGH NEGATIVE | LOW POSITIVE | LOW NEGATIVE | |
| VREFHIA | - | 25 | 16 | 14 | | | | | | | | | | |
| VREFHIB | - | 24 | | | | | | | | | | | | |
| VREFHIC | - | | | | | | | | | | | | | |
| VREFLOA | - | 27 | 17 | 15 | A13 | | | | | | | | | |
| VREFLOB | - | 26 | | | | B13 | | | | | | | | |
| VREFLOC | - | | | | | | C13 | | | | | | | |
| **Analog Group 1** | | | | | | | | | | **CMP1** | | | | |
| A3 | G1_ADCAB | 10 | | | A3 | | | | | HPMXSEL = 3 | HNMXSEL = 0 | LPMXSEL = 3 | LNMXSEL = 0 | AIO233 |
| A2/B6/PGA1_OF | PGA1_OF | 9 | 9 | 8 | A2 | B6 | | PGA1_OF | | HPMXSEL = 0 | | LPMXSEL = 0 | | AIO224 |
| C0 | G1_ADCC | 19 | 12 | 10 | | | C0 | | | HPMXSEL = 1 | HNMXSEL = 1 | LPMXSEL = 1 | LNMXSEL = 1 | AIO237 |
| PGA1_IN | PGA1_IN | 18 | | | | | | PGA1_IN | | HPMXSEL = 2 | | LPMXSEL = 2 | | |
| PGA1_GND | PGA1_GND | 14 | 10 | 9 | | | | PGA1_GND | | | | | | |
| - | PGA1_OUT(1) | | | | A11 | B7 | | PGA1_OUT | | HPMXSEL = 4 | | LPMXSEL = 4 | | |
| **Analog Group 2** | | | | | | | | | | **CMP2** | | | | |
| A5 | G2_ADCAB | 35 | | | A5 | | | | | HPMXSEL = 3 | HNMXSEL = 0 | LPMXSEL = 3 | LNMXSEL = 0 | AIO234 |
| A4/B8/PGA2_OF | PGA2_OF | 36 | 23 | 21 | A4 | B8 | | PGA2_OF | | HPMXSEL = 0 | | LPMXSEL = 0 | | AIO225 |
| C1 | G2_ADCC | 29 | 18 | 16 | | | C1 | | | HPMXSEL = 1 | HNMXSEL = 1 | LPMXSEL = 1 | LNMXSEL = 1 | AIO238 |
| PGA2_IN | PGA2_IN | 30 | | | | | | PGA2_IN | | HPMXSEL = 2 | | LPMXSEL = 2 | | |
| PGA2_GND | PGA2_GND | 32 | 20 | 18 | | | | PGA2_GND | | | | | | |
| - | PGA2_OUT(1) | | | | A12 | B9 | | PGA2_OUT | | HPMXSEL = 4 | | LPMXSEL = 4 | | |
| **Analog Group 3** | | | | | | | | | | **CMP3** | | | | |
| B3/VDAC | G3_ADCAB | 8 | 8 | 7 | | B3 | | | VDAC | HPMXSEL = 3 | HNMXSEL = 0 | LPMXSEL = 3 | LNMXSEL = 0 | AIO242 |
| B2/C6/PGA3_OF | PGA3_OF | 7 | 7 | 6 | | B2 | C6 | PGA3_OF | | HPMXSEL = 0 | | LPMXSEL = 0 | | AIO226 |
| C2 | G3_ADCC | 21 | 13 | 11 | | | C2 | | | HPMXSEL = 1 | HNMXSEL = 1 | LPMXSEL = 1 | LNMXSEL = 1 | AIO244 |
| PGA3_IN | PGA3_IN | 20 | | | | | | PGA3_IN | | HPMXSEL = 2 | | LPMXSEL = 2 | | |
| PGA3_GND | PGA3_GND | 15 | 10 | 9 | | | | PGA3_GND | | | | | | |
| - | PGA3_OUT(1) | | | | | B10 | C7 | PGA3_OUT | | HPMXSEL = 4 | | LPMXSEL = 4 | | |
| **Analog Group 4** | | | | | | | | | | **CMP4** | | | | |
| B5 | G4_ADCAB | | | | | B5 | | | | HPMXSEL = 3 | HNMXSEL = 0 | LPMXSEL = 3 | LNMXSEL = 0 | AIO243 |
| B4/C8/PGA4_OF | PGA4_OF | 39 | 24 | 22 | | B4 | C8 | PGA4_OF | | HPMXSEL = 0 | | LPMXSEL = 0 | | AIO227 |
| C3 | G4_ADCC | 31 | 19 | 17 | | | C3 | | | HPMXSEL = 1 | HNMXSEL = 1 | LPMXSEL = 1 | LNMXSEL = 1 | AIO245 |
| PGA4_IN | PGA4_IN | | | | | | | PGA4_IN | | HPMXSEL = 2 | | LPMXSEL = 2 | | |
| PGA4_GND | PGA4_GND | 32 | 20 | 18 | | | | PGA4_GND | | | | | | |
| - | PGA4_OUT(1) | | | | | B11 | C9 | PGA4_OUT | | HPMXSEL = 4 | | LPMXSEL = 4 | | |

(1) Internal connection only; does not come to a device pin.


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**Table 5-39. Analog Pins and Internal Connections (continued)**

| PIN NAME | GROUP NAME | PACKAGE | | | ALWAYS CONNECTED (NO MUX) | | | | | COMPARATOR SUBSYSTEM (MUX) | | | | AIO INPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 100 PZ | 64 PM | 56 RSH | ADCA | ADCB | ADCC | PGA | DAC | HIGH POSITIVE | HIGH NEGATIVE | LOW POSITIVE | LOW NEGATIVE | |
| **Analog Group 5** | | | | | | | | | | **CMP5** | | | | |
| A7 | G5_ADCAB | | | | A7 | | | | | HPMXSEL = 3 | HNMXSEL = 0 | LPMXSEL = 3 | LNMXSEL = 0 | AIO235 |
| A6/PGA5_OF | PGA5_OF | 6 | 6 | | A6 | | | PGA5_OF | | HPMXSEL = 0 | | LPMXSEL = 0 | | AIO228 |
| C4 | G5_ADCC | 17 | 11 | | | | C4 | | | HPMXSEL = 1 | HNMXSEL = 1 | LPMXSEL = 1 | LNMXSEL = 1 | AIO239 |
| PGA5_IN | PGA5_IN | 16 | | | | | | PGA5_IN | | HPMXSEL = 2 | | LPMXSEL = 2 | | |
| PGA5_GND | PGA5_GND | 13 | 10 | 9 | | | | PGA5_GND | | | | | | |
| - | PGA5_OUT(1) | | | | A14 | | | PGA5_OUT | | HPMXSEL = 4 | | LPMXSEL = 4 | | |
| **Analog Group 6** | | | | | | | | | | **CMP6** | | | | |
| A9 | G6_ADCAB | 38 | | | A9 | | | | | HPMXSEL = 3 | HNMXSEL = 0 | LPMXSEL = 3 | LNMXSEL = 0 | AIO236 |
| A8/PGA6_OF | PGA6_OF | 37 | | | A8 | | | PGA6_OF | | HPMXSEL = 0 | | LPMXSEL = 0 | | AIO229 |
| C5 | G6_ADCC | 28 | | | | | C5 | | | HPMXSEL = 1 | HNMXSEL = 1 | LPMXSEL = 1 | LNMXSEL = 1 | AIO240 |
| PGA6_IN | PGA6_IN | | | | | | | PGA6_IN | | HPMXSEL = 2 | | LPMXSEL = 2 | | |
| PGA6_GND | PGA6_GND | 32 | 20 | 18 | | | | PGA6_GND | | | | | | |
| - | PGA6_OUT(1) | | | | A15 | | | PGA6_OUT | | HPMXSEL = 4 | | LPMXSEL = 4 | | |
| **Analog Group 7** | | | | | | | | | | **CMP7** | | | | |
| B0 | G7_ADCAB | 41 | | | | B0 | | | | HPMXSEL = 3 | HNMXSEL = 0 | LPMXSEL = 3 | LNMXSEL = 0 | AIO241 |
| A10/B1/C10/PGA7_OF | PGA7_OF(2) | 40 | 25 | 23 | A10 | B1 | C10 | PGA7_OF | | HPMXSEL = 0 | | LPMXSEL = 0 | | AIO230 |
| C14 | G7_ADCC | 44 | | | | | C14 | | | HPMXSEL = 1 | HNMXSEL = 1 | LPMXSEL = 1 | LNMXSEL = 1 | AIO246 |
| PGA7_IN | PGA7_IN | 43 | | | | | | PGA7_IN | | HPMXSEL = 2 | | LPMXSEL = 2 | | |
| PGA7_GND | PGA7_GND | 42 | | | | | | PGA7_GND | | | | | | |
| - | PGA7_OUT(1) | | | | | B12 | C11 | PGA7_OUT | | HPMXSEL = 4 | | LPMXSEL = 4 | | |
| **Other Analog** | | | | | | | | | | | | | | |
| A0/B15/C15/DACA_OUT | | 23 | 15 | 13 | A0 | B15 | C15 | | DACA_OUT | | | | | AIO231 |
| A1/DACB_OUT | | 22 | 14 | 12 | A1 | | | | DACB_OUT | | | | | AIO232 |
| C12 | | | | | | | C12 | | | | | | | AIO247 |
| - | TempSensor(1) | | | | | B14 | | | | | | | | |

(2) PGA functionality not available on 64-pin and 56-pin packages.

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**Table 5-40. Analog Signal Descriptions**

| SIGNAL NAME | DESCRIPTION |
|---|---|
| AIOx | Digital input on ADC pin |
| Ax | ADC A Input |
| Bx | ADC B Input |
| Cx | ADC C Input |
| CMPx_DACH | Comparator subsystem high DAC output |
| CMPx_DACL | Comparator subsystem low DAC output |
| CMPx_HNy | Comparator subsystem high comparator negative input |
| CMPx_HPy | Comparator subsystem high comparator positive input |
| CMPx_LNy | Comparator subsystem low comparator negative input |
| CMPx_LPy | Comparator subsystem low comparator positive input |
| DACx_OUT | Buffered DAC Output |
| PGAx_GND | PGA Ground |
| PGAx_IN | PGA Input |
| PGAx_OF | PGA Output for filter |
| PGAx_OUT | PGA Output to internal ADC |
| TempSensor | Internal temperature sensor |
| VDAC | Optional external reference voltage for on-chip DACs. There is a 100-pF capacitor to VSSA on this pin whether used for ADC input or DAC reference which cannot be disabled. If this pin is used as a reference for the on-chip DACs, place at least a 1-µF capacitor on this pin. |


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### 5.10.1 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with resolution of 12 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC)-based (see the SOC Principle of Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*).

Each ADC has the following features:

- Resolution of 12 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended signaling
- Input multiplexer with up to 16 channels
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
  - S/W: software immediate start
  - All ePWMs: ADCSOC A or B
  - GPIO XINT2
  - CPU Timers 0/1/2
  - ADCINT1/2
- Four flexible PIE interrupts
- Burst-mode triggering option
- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
  - Trigger-to-sample delay capture

**NOTE**

Not every channel may be pinned out from all ADCs. See Section 4 to determine which channels are available.

The block diagram for the ADC core and ADC wrapper are shown in Figure 5-32.

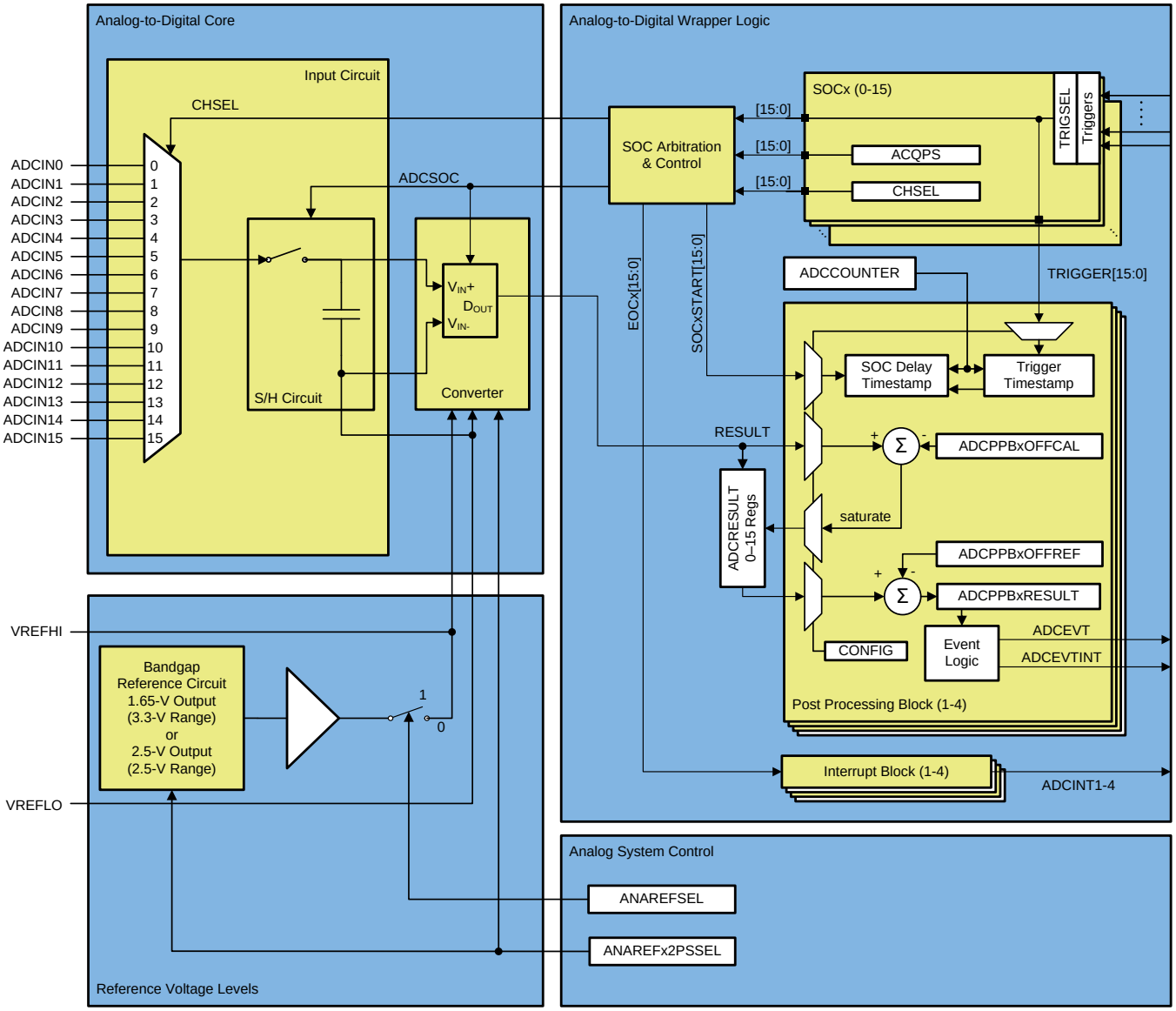



**Figure 5-32. ADC Module Block Diagram**


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#### 5.10.1.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 5-41 summarizes the basic ADC options and their level of configurability.

**Table 5-41. ADC Options and Configuration Levels**

| OPTIONS | CONFIGURABILITY |
|---|---|
| Clock | Per module(1) |
| Resolution | Not configurable (12-bit resolution only) |
| Signal mode | Not configurable (single-ended signal mode only) |
| Reference voltage source | Per module |
| Trigger source | Per SOC(1) |
| Converted channel | Per SOC |
| Acquisition window duration | Per SOC(1) |
| EOC location | Per module |
| Burst mode | Per module(1) |

(1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the Ensuring Synchronous Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

##### *5.10.1.1.1 Signal Mode*

The ADC supports single-ended signaling. In single-ended mode, the input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO. Figure 5-33 shows the single-ended signaling mode.

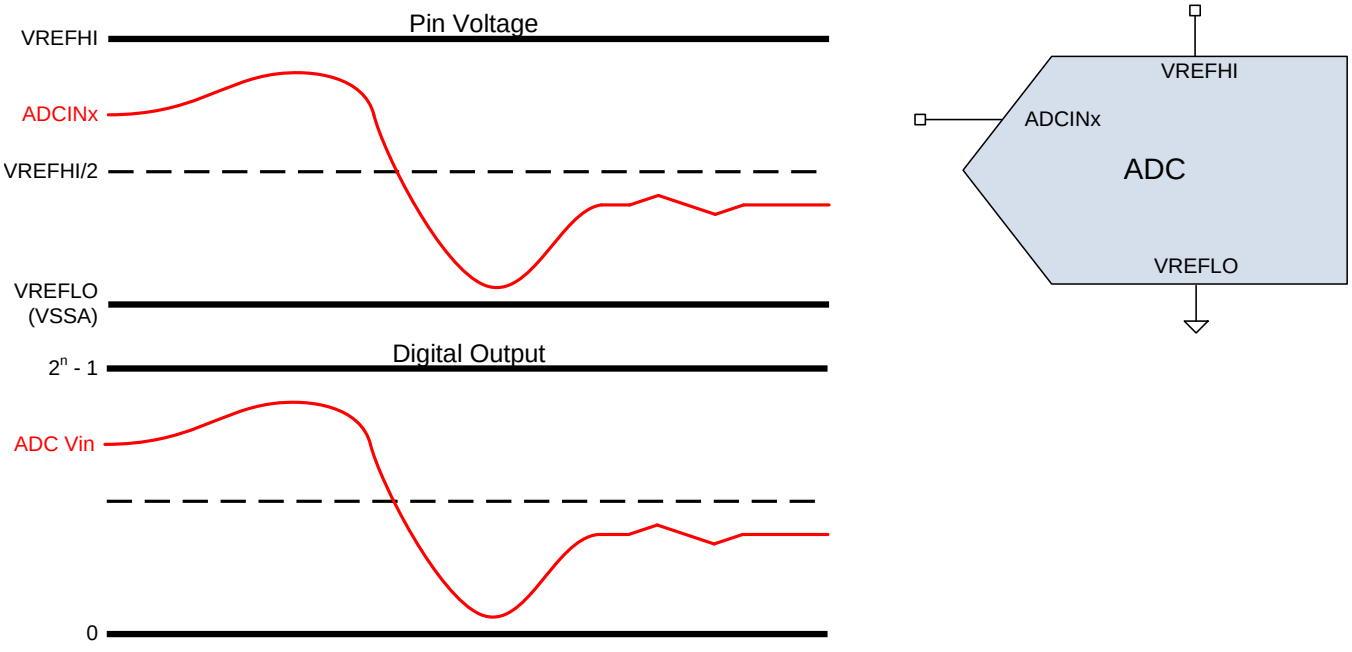



**Figure 5-33. Single-ended Signaling Mode**

### 5.10.1.2 ADC Electrical Data and Timing

Table 5-42 lists the ADC operating conditions. Table 5-43 lists the ADC electrical characteristics.

**Table 5-42. ADC Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| ADCCLK (derived from PERx.SYSCLK) | | 5 | | 50 | MHz |
| Sample rate | 100-MHz SYSCLK | | | 3.45 | MSPS |
| Sample window duration (set by ACQPS and PERx.SYSCLK)(1) | With 50 Ω or less $R_s$ | 75 | | | ns |
| VREFHI | | 2.4 | 2.5 or 3.0 | VDDA | V |
| VREFLO | | VSSA | VSSA | VSSA | V |
| VREFHI - VREFLO | | 2.4 | 3.3 | VDDA | V |
| Conversion range | Internal reference = 3.3 V | 0 | | 3.3 | V |
| Conversion range | Internal reference = 2.5 V | 0 | | 2.5 | V |
| Conversion range | External reference | VREFLO | | VREFHI | V |

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.

**NOTE**

The ADC inputs should be kept below VDDA + 0.3 V during operation. If an ADC input exceeds this level, the $V_{REF}$ internal to the device may be disturbed, which can impact results for other ADC or DAC inputs using the same $V_{REF}$.


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**Table 5-43. ADC Characteristics**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **General** | | | | | |
| ADCCLK Conversion Cycles | 100-MHz SYSCLK | 10.1 | | 11 | ADCCLKs |
| Power Up Time | External Reference mode | | | 500 | µs |
| | Internal Reference mode | | | 5000 | µs |
| | Internal Reference mode, when switching between 2.5-V range and 3.3-V range. | | | 5000 | µs |
| VREFHI input current(1) | | | 130 | | µA |
| Internal Reference Capacitor Value(2) | | 2.2 | | | µF |
| External Reference Capacitor Value(2) | | 2.2 | | | µF |
| **DC Characteristics** | | | | | |
| Gain Error | Internal reference | –45 | | 45 | LSB |
| | External reference | –5 | ±3 | 5 | LSB |
| Offset Error | | –5 | ±2 | 5 | LSB |
| Channel-to-Channel Gain Error | | | ±2 | | LSB |
| Channel-to-Channel Offset Error | | | ±2 | | LSB |
| ADC-to-ADC Gain Error | Identical VREFHI and VREFLO for all ADCs | | ±4 | | LSB |
| ADC-to-ADC Offset Error | Identical VREFHI and VREFLO for all ADCs | | ±2 | | LSB |
| DNL Error | | >–1 | ±0.5 | 1 | LSB |
| INL Error | | –2 | ±1.0 | 2 | LSB |
| ADC-to-ADC Isolation | VREFHI = 2.5 V, synchronous ADCs | –1 | | 1 | LSBs |
| | VREFHI = 2.5 V, asynchronous ADCs | Not Supported | | | |
| **AC Characteristics** | | | | | |
| SNR(3) | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 | | 68.8 | | dB |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC | | 60.1 | | dB |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, VDD supplied from internal DC-DC regulator(4) | | 67.5 | | dB |
| THD(3) | VREFHI = 2.5 V, fin = 100 kHz | | –80.6 | | dB |
| SFDR(3) | VREFHI = 2.5 V, fin = 100 kHz | | 79.2 | | dB |
| SINAD(3) | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 | | 68.5 | | dB |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC | | 60.0 | | dB |
| ENOB(3) | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC | | 11.0 | | bits |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs | | 11.0 | | bits |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs | | Not Supported | | bits |

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Noise impact from the DCDC regulator to the ADC will be strongly dependent on PCB layout.

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**Table 5-43. ADC Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| PSRR | VDD = 1.2-V DC + 100mV<br>DC up to Sine at 1 kHz | | 60 | | dB |
| | VDD = 1.2-V DC + 100 mV<br>DC up to Sine at 300 kHz | | 57 | | |
| | VDDA = 3.3-V DC + 200 mV<br>DC up to Sine at 1 kHz | | 60 | | |
| | VDDA = 3.3-V DC + 200 mV<br>Sine at 900 kHz | | 57 | | |


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#### 5.10.1.2.1 ADC Input Model

The ADC input characteristics are given by Table 5-44 and Figure 5-34.

**Table 5-44. Input Model Parameters**

| | DESCRIPTION | REFERENCE MODE | VALUE |
|---|---|---|---|
| $C_p$ | Parasitic input capacitance | All | See Table 5-45 |
| $R_{on}$ | Sampling switch resistance | External Reference, 2.5-V Internal Reference | 500 Ω |
| | | 3.3-V Internal Reference | 860 Ω |
| $C_h$ | Sampling capacitor | External Reference, 2.5-V Internal Reference | 12.5 pF |
| | | 3.3-V Internal Reference | 7.5 pF |
| $R_s$ | Nominal source impedance | All | 50 Ω |

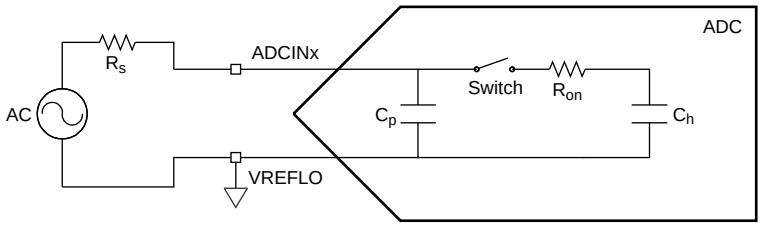



**Figure 5-34. Input Model**

This input model should be used with actual signal source impedance to determine the acquisition window duration. For more information, see the Choosing an Acquisition Window Duration section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

Table 5-45 lists the parasitic capacitance on each channel.

**Table 5-45. Per-Channel Parasitic Capacitance**

| ADC CHANNEL | $C_p$ (pF) | |
|---|---|---|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| ADCINA0 | 12.7 | 15.2 |
| ADCINA1 | 13.7 | 16.2 |
| ADCINA2 | 9.2 | 11.7 |
| ADCINA3 | 6.9 | 9.4 |
| ADCINA4 | 9.2 | 11.7 |
| ADCINA5 | 7.5 | 10 |
| ADCINA6 | 8.0 | 10.5 |
| ADCINA7 | 7.0 | 9.5 |
| ADCINA8 | 10.0 | 12.5 |
| ADCINA9 | 8.1 | 10.6 |
| ADCINA10 | 9.3 | 11.8 |
| ADCINB0 | 7.1 | 9.6 |
| ADCINB1 | 9.3 | 11.8 |
| ADCINB2 | 9.6 | 12.1 |
| ADCINB3(1) | 125.6 | 128.1 |
| ADCINB4 | 8.8 | 11.3 |
| ADCINB5 | 7.1 | 9.6 |
| ADCINB6 | 9.2 | 11.7 |
| ADCINB8 | 9.2 | 11.7 |
| ADCINB15 | 12.7 | 15.2 |
| ADCINC0 | 6.4 | 8.9 |
| ADCINC1 | 6.1 | 8.6 |
| ADCINC2 | 5.24 | 7.74 |
| ADCINC3 | 5.5 | 8 |
| ADCINC4 | 6.2 | 8.7 |
| ADCINC5 | 5.6 | 8.1 |
| ADCINC6 | 9.6 | 12.1 |
| ADCINC8 | 8.8 | 11.3 |
| ADCINC10 | 9.3 | 11.8 |
| ADCINC12 | 4.1 | 6.6 |
| ADCINC14 | 4.5 | 7 |
| ADCINC15 | 12.7 | 15.2 |

(1) This pin is also used to supply reference voltage for COMPDAC and GPDAC, and includes an internal decoupling capacitor.


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#### 5.10.1.2.2 ADC Timing Diagrams

Figure 5-35 shows the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round-robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

Table 5-46 lists the descriptions of the ADC timing parameters. Table 5-47 lists the ADC timings.

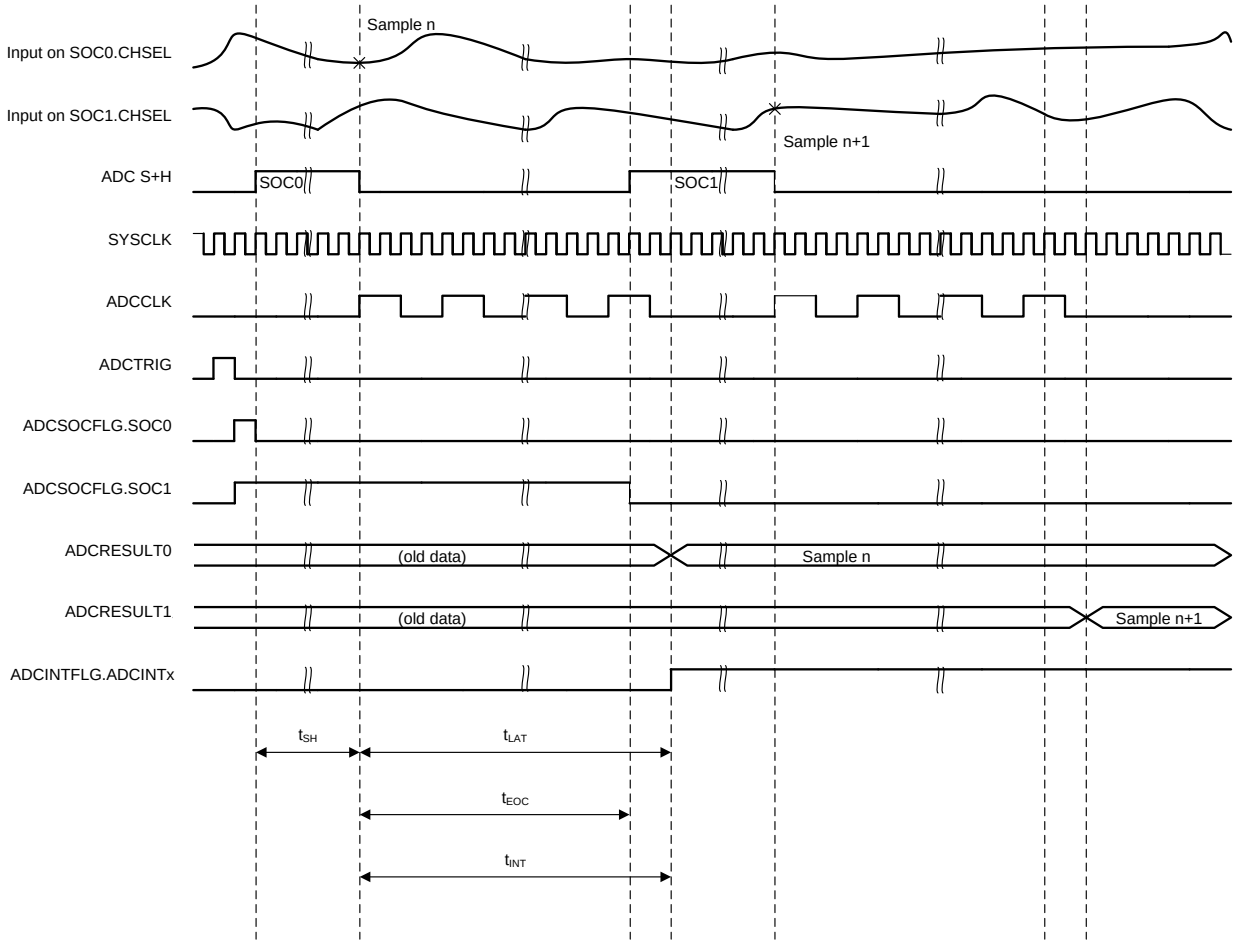



**Figure 5-35. ADC Timings**

## Table 5-46. ADC Timing Parameters

| PARAMETER | DESCRIPTION |
|---|---|
| $t_{SH}$ | The duration of the S+H window.<br><br>At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so $t_{SH}$ will not necessarily be the same for different SOCs.<br><br>**Note:** The value on the S+H capacitor will be captured approximately 5 ns before the end of the S+H window regardless of device clock settings. |
| $t_{LAT}$ | The time from the end of the S+H window until the ADC results latch in the ADCRESULTx register.<br><br>If the ADCRESULTx register is read before this time, the previous conversion results will be returned. |
| $t_{EOC}$ | The time from the end of the S+H window until the S+H window for the next ADC conversion can begin. The subsequent sample can start before the conversion results are latched. |
| $t_{INT}$ | The time from the end of the S+H window until an ADCINT flag is set (if configured).<br><br>If the INTPULSEPOS bit in the ADCCTL1 register is set, $t_{INT}$ will coincide with the conversion results being latched into the result register.<br><br>If the INTPULSEPOS bit is 0, $t_{INT}$ will coincide with the end of the S+H window. If $t_{INT}$ triggers a read of the ADC result register (directly through DMA or indirectly by triggering an ISR that reads the result), care must be taken to ensure the read occurs after the results latch (otherwise, the previous results will be read).<br><br>If the INTPULSEPOS bit is 0, and the OFFSET field in the ADCINTCYCLE register is not 0, then there will be a delay of OFFSET SYSCLK cycles before the ADCINT flag is set. This delay can be used to enter the ISR or trigger the DMA at exactly the time the sample is ready. |

## Table 5-47. ADC Timings

| ADCCLK PRESCALE | | SYSCLK CYCLES | | | | ADCCLK CYCLES |
|---|---|---|---|---|---|---|
| ADCCTL2 [PRESCALE] | RATIO ADCCLK:SYSCLK | $t_{EOC}$ | $t_{LAT}$ | $t_{INT(EARLY)}$ (1) | $t_{INT(LATE)}$ | $t_{EOC}$ |
| 0 | 1 | 11 | 13 | 1 | 11 | 11 |
| 2 | 2 | 21 | 23 | 1 | 21 | 10.5 |
| 4 | 3 | 31 | 34 | 1 | 31 | 10.3 |
| 6 | 4 | 41 | 44 | 1 | 41 | 10.3 |
| 8 | 5 | 51 | 55 | 1 | 51 | 10.2 |
| 10 | 6 | 61 | 65 | 1 | 61 | 10.2 |
| 12 | 7 | 71 | 76 | 1 | 71 | 10.1 |
| 14 | 8 | 81 | 86 | 1 | 81 | 10.1 |

(1) By default, $t_{INT}$ occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.


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### 5.10.2 Programmable Gain Amplifier (PGA)

The Programmable Gain Amplifier (PGA) is used to amplify an input voltage for the purpose of increasing the effective resolution of the downstream ADC and CMPSS modules.

The integrated PGA helps to reduce cost and design effort for many control applications that traditionally require external, stand-alone amplifiers. On-chip integration ensures that the PGA is compatible with the downstream ADC and CMPSS modules. Software-selectable gain and filter settings make the PGA adaptable to various performance needs.

The PGA has the following features:

- Four programmable gain modes: 3x, 6x, 12x, 24x
- Internally powered by VDDA and VSSA
- Support for Kelvin ground connections using PGA_GND pin
- Embedded series resistors for RC filtering

The active component in the PGA is an embedded operational amplifier (op amp) that is configured as a noninverting amplifier with internal feedback resistors. These internal feedback resistor values are paired to produce software selectable voltage gains.

Three PGA signals are available at the device pins:

- PGA_IN is the positive input to the PGA op amp. The signal applied to this pin will be amplified by the PGA.
- PGA_GND is the Kelvin ground reference for the PGA_IN signal. Ideally, the PGA_GND reference is equal to VSSA; however, the PGA can tolerate small voltage offsets from VSSA.
- PGA_OF supports op amp output filtering with RC components. The filtered signal is available for sampling and monitoring by internal ADC and CMPSS modules. The PGA RFILTER path is not available on some device revisions. See the *TMS320F28004x Piccolo™ Microcontrollers Silicon Errata* for more information.

PGA_OUT is an internal signal at the op amp output. It is available for sampling and monitoring by the internal ADC and CMPSS modules. Figure 5-36 shows the PGA block diagram.

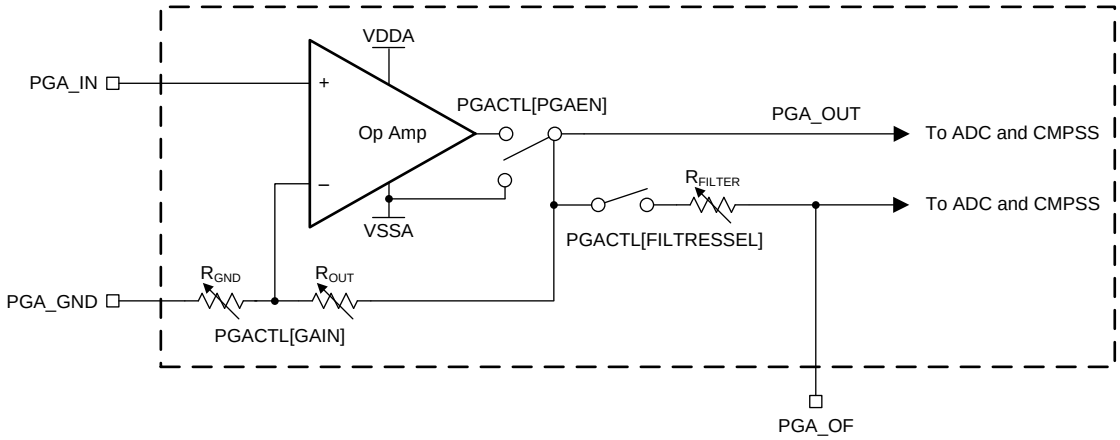



**Figure 5-36. PGA Block Diagram**

### 5.10.2.1 PGA Electrical Data and Timing

Table 5-48 lists the PGA operating conditions. Table 5-49 lists the PGA characteristics.

**Table 5-48. PGA Operating Conditions**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| PGA Output Range(1) | | VSSA + 0.35 | | VDDA – 0.35 | V |
| PGA GND Range | | –50 | | 200 | mV |
| Min ADC S+H (No Filter; Gain = 3, 6, 12) | Settling within ±1 ADC LSB Accuracy | 160 | | | ns |
| Min ADC S+H (No Filter; Gain = 24) | Settling within ±2 ADC LSB Accuracy | 200 | | | ns |

(1) This is the linear output range of the PGA. The PGA can output voltages outside this range, but the voltages will not be linear.

**Table 5-49. PGA Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **General** | | | | | |
| Gain Settings | | | 3, 6, 12, 24 | | |
| Input Bias Current | | | 2 | | nA |
| Short Circuit Current | | | 35 | | mA |
| Full Scale Step Response (No Filter) | Settling within ±2 ADC LSB Accuracy | | | 450 | ns |
| Settling Time | Gain Switching | | | 10 | µs |
| Slew Rate | Gain = 3 | 15 | 20 | | V/µs |
| | Gain = 6 | 31 | 37 | | V/µs |
| | Gain = 12 | 61 | 73 | | V/µs |
| | Gain = 24 | 78 | 98 | | V/µs |
| $R_{GND}$ | Gain = 3 | | 9 | | kΩ |
| | Gain = 6 | | 4.5 | | kΩ |
| | Gain = 12 | | 2.25 | | kΩ |
| | Gain = 24 | | 1.125 | | kΩ |
| $R_{OUT}$ | Gain = 3 | | 18 | | kΩ |
| | Gain = 6 | | 22.5 | | kΩ |
| | Gain = 12 | | 24.75 | | kΩ |
| | Gain = 24 | | 25.875 | | kΩ |
| Filter Resistor Targets | $R_{FILT}$ = 200 Ω | 145 | 190 | 234 | Ω |
| | $R_{FILT}$ = 160 Ω | 117 | 153 | 188 | Ω |
| | $R_{FILT}$ = 130 Ω | 95 | 125 | 154 | Ω |
| | $R_{FILT}$ = 100 Ω | 71 | 96 | 120 | Ω |
| | $R_{FILT}$ = 80 Ω | 55 | 77 | 98 | Ω |
| | $R_{FILT}$ = 50 Ω | 31 | 49 | 66 | Ω |
| Power Up Time | | | | 500 | µs |
| **DC Characteristics** | | | | | |
| Gain Error(1) | Gain = 3, 6, 12 | –0.5 | | 0.5 | % |
| | Gain = 24 | –0.8 | | 0.8 | % |
| Gain Temp Coefficient | | | ±0.004 | | %/C |
| Offset Error(2) | Input Referred | –1.5 | | 1.5 | mV |
| Offset Temp Coefficient | Input Referred | | ±5.5 | | µV/C |

(1) Includes ADC gain error.
(2) Includes ADC offset error.


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**Table 5-49. PGA Characteristics (continued)**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| DC Code Spread | | | 2.5 | | 12b LSB |
| **AC Characteristics** | | | | | |
| Bandwidth(3) | All Gain Modes | | 7 | | MHz |
| THD(4) | DC | | –78 | | dB |
| | Up to 100 kHz | | –70 | | dB |
| CMRR | DC | | –60 | | dB |
| | Up to 100 kHz | | –50 | | dB |
| PSRR(4) | DC | | –75 | | dB |
| | Up to 100 kHz | | –50 | | dB |
| Noise PSD(4) | 1 kHz | | 200 | | nV/sqrt(Hz) |
| Integrated Noise (Input Referred)(4) | 3 Hz to 30 MHz | | 100 | | µV |

(3) 3dB bandwidth.
(4) Performance of PGA alone.

#### 5.10.2.1.1 PGA Typical Characteristics Graphs

Figure 5-37 shows the input bias current versus temperature.

**NOTE**

For Figure 5-37, the following conditions apply (unless otherwise noted):

- $T_A$ = 30°C
- VDDA = 3.3 V
- VDD = 1.2 V

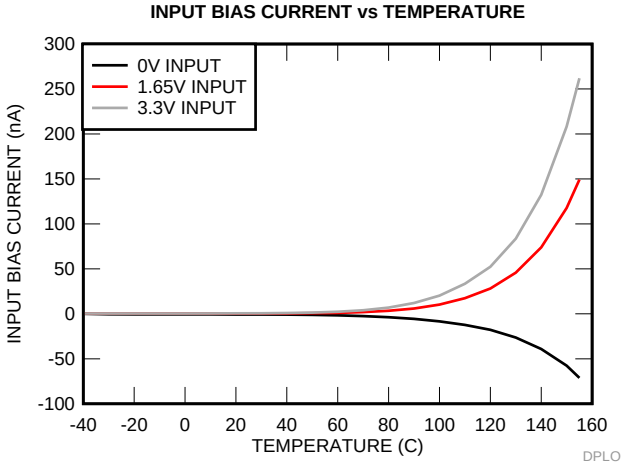



**Figure 5-37. Input Bias Current Versus Temperature**

### 5.10.3 Temperature Sensor

#### 5.10.3.1 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in Table 5-50.

**Table 5-50. Temperature Sensor Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{acc}$ | Temperature Accuracy | External reference | | ±15 | | °C |
| $t_{startup}$ | Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor) | | | 500 | | µs |
| $t_{acq}$ | ADC acquisition time | | 450 | | | ns |


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### 5.10.4 Buffered Digital-to-Analog Converter (DAC)

The buffered DAC module consists of an internal 12-bit DAC and an analog output buffer that can drive an external load. For driving even higher loads than typical, a trade-off can be made between load size and output voltage swing. For the load conditions of the buffered DAC, see Section 5.10.4.1. The buffered DAC is a general-purpose DAC that can be used to generate a DC voltage or AC waveforms such as sine waves, square waves, triangle waves and so forth. Software writes to the DAC value register can take effect immediately or can be synchronized with EPWMSYNCO events.

Each buffered DAC has the following features:

- 12-bit resolution
- Selectable reference voltage source
- x1 and x2 gain modes when using internal VREFHI
- Ability to synchronize with EPWMSYNCO

The block diagram for the buffered DAC is shown in Figure 5-38.

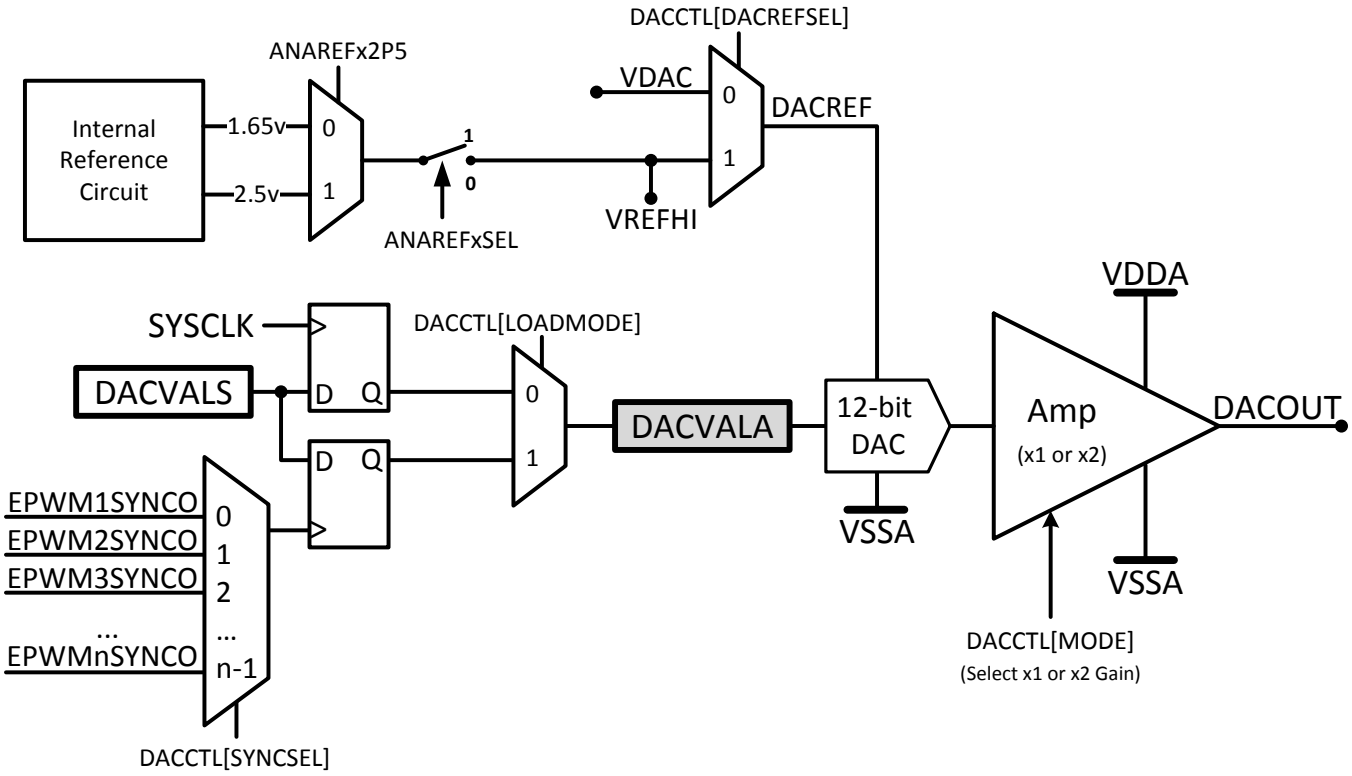



**Figure 5-38. DAC Module Block Diagram**

### 5.10.4.1 Buffered DAC Electrical Data and Timing

Table 5-51 lists the buffered DAC operating conditions. Table 5-52 lists the buffered DAC electrical characteristics.

**Table 5-51. Buffered DAC Operating Conditions**

over recommended operating conditions (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_L$ | Resistive Load(2) | | 5 | | | kΩ |
| $C_L$ | Capacitive Load | | | | 100 | pF |
| $V_{OUT}$ | Valid Output Voltage Range(3) | $R_L$ = 5 kΩ | 0.3 | | VDDA – 0.3 | V |
| | | $R_L$ = 1 kΩ | 0.6 | | VDDA – 0.6 | V |
| Reference Voltage(4) | | VDAC or VREFHI | 2.4 | 2.5 or 3.0 | VDDA | V |

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
(2) DAC can drive a minimum resistive load of 1 kΩ, but the output range will be limited.
(3) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
(4) For best PSRR performance, VDAC or VREFHI should be less than VDDA.

**Table 5-52. Buffered DAC Electrical Characteristics**

over recommended operating conditions (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| Resolution | | | | 12 | | bits |
| Load Regulation | | | –1 | | 1 | mV/V |
| Glitch Energy | | | | 1.5 | | V-ns |
| Voltage Output Settling Time Full-Scale | | Settling to 2 LSBs after 0.3V-to-3V transition | | | 2 | µs |
| Voltage Output Settling Time 1/4th Full-Scale | | Settling to 2 LSBs after 0.3V-to-0.75V transition | | | 1.6 | µs |
| Voltage Output Slew Rate | | Slew rate from 0.3V-to-3V transition | 2.8 | | 4.5 | V/µs |
| Load Transient Settling Time | | 5-kΩ Load | | | 328 | ns |
| | | 1-kΩ Load | | | 557 | ns |
| Reference Input Resistance(2) | | VDAC or VREFHI | 160 | 200 | 240 | kΩ |
| TPU | Power Up Time | External Reference mode | | | 500 | µs |
| | | Internal Reference mode | | | 5000 | µs |
| **DC Characteristics** | | | | | | |
| Offset | Offset Error | Midpoint | –10 | | 10 | mV |
| Gain | Gain Error(3) | | –2.5 | | 2.5 | % of FSR |
| DNL | Differential Non Linearity(4) | Endpoint corrected | –1 | ±0.4 | 1 | LSB |
| INL | Integral Non Linearity | Endpoint corrected | –5 | ±2 | 5 | LSB |
| **AC Characteristics** | | | | | | |
| Output Noise | | Integrated noise from 100 Hz to 100 kHz | | 600 | | µVrms |
| | | Noise density at 10 kHz | | 800 | | nVrms/√Hz |
| SNR | Signal to Noise Ratio | 1 kHz, 200 KSPS | | 64 | | dB |
| THD | Total Harmonic Distortion | 1 kHz, 200 KSPS | | –64.2 | | dB |

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
(2) Per active Buffered DAC module.
(3) Gain error is calculated for linear output range.
(4) The DAC output is monotonic.


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**Table 5-52. Buffered DAC Electrical Characteristics (continued)**

over recommended operating conditions (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| SFDR | Spurious Free Dynamic Range | 1 kHz, 200 KSPS | | 66 | | dB |
| SINAD | Signal to Noise and Distortion Ratio | 1 kHz, 200 KSPS | | 61.7 | | dB |
| PSRR | Power Supply Rejection Ratio(5) | DC | | 70 | | dB |
| | | 100 kHz | | 30 | | dB |

(5) VREFHI = 3.2 V, VDDA = 3.3 V DC + 100 mV Sine.

**NOTE**

The VDAC pin must be kept below VDDA + 0.3 V to ensure proper functional operation. If the VDAC pin exceeds this level, a blocking circuit may activate, and the internal value of VDAC may float to 0 V internally, giving improper DAC output.

#### *5.10.4.1.1 Buffered DAC Illustrative Graphs*

Figure 5-39 shows the buffered DAC offset. Figure 5-40 shows the buffered DAC gain. Figure 5-41 shows the buffered DAC linearity.

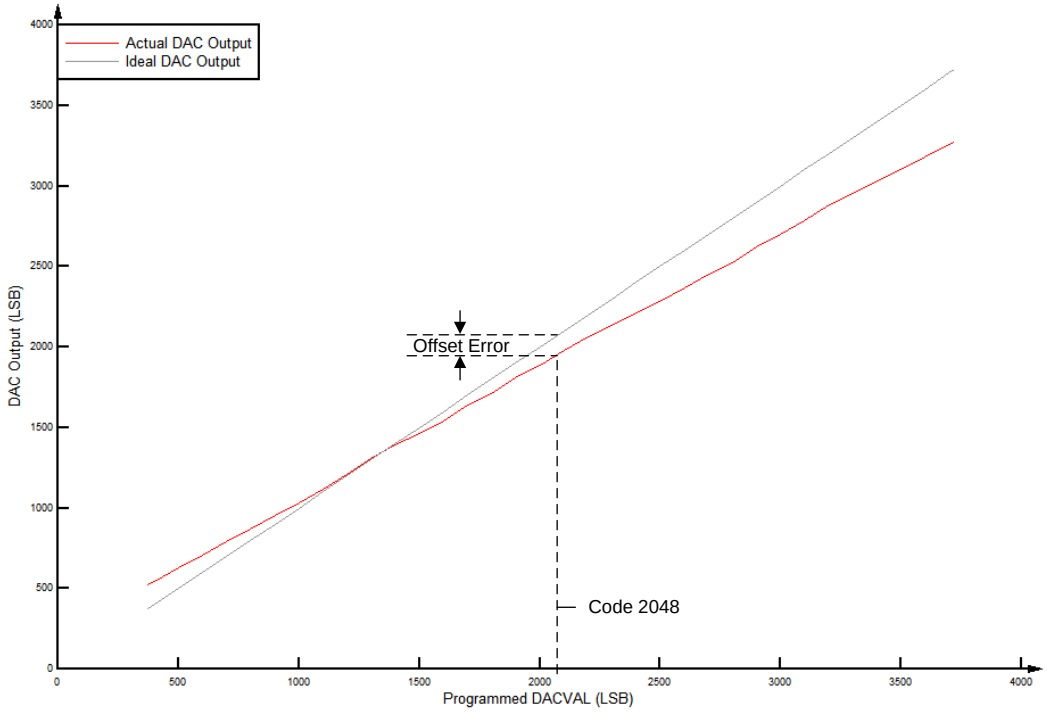



**Figure 5-39. Buffered DAC Offset**

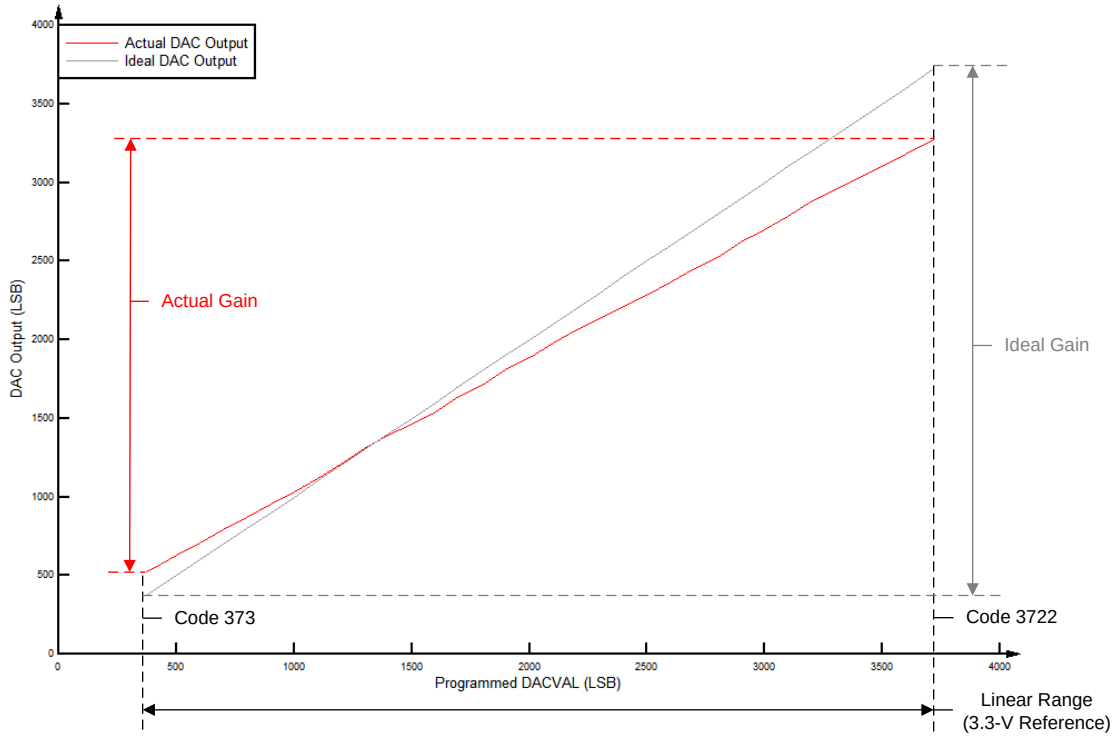



**Figure 5-40. Buffered DAC Gain**

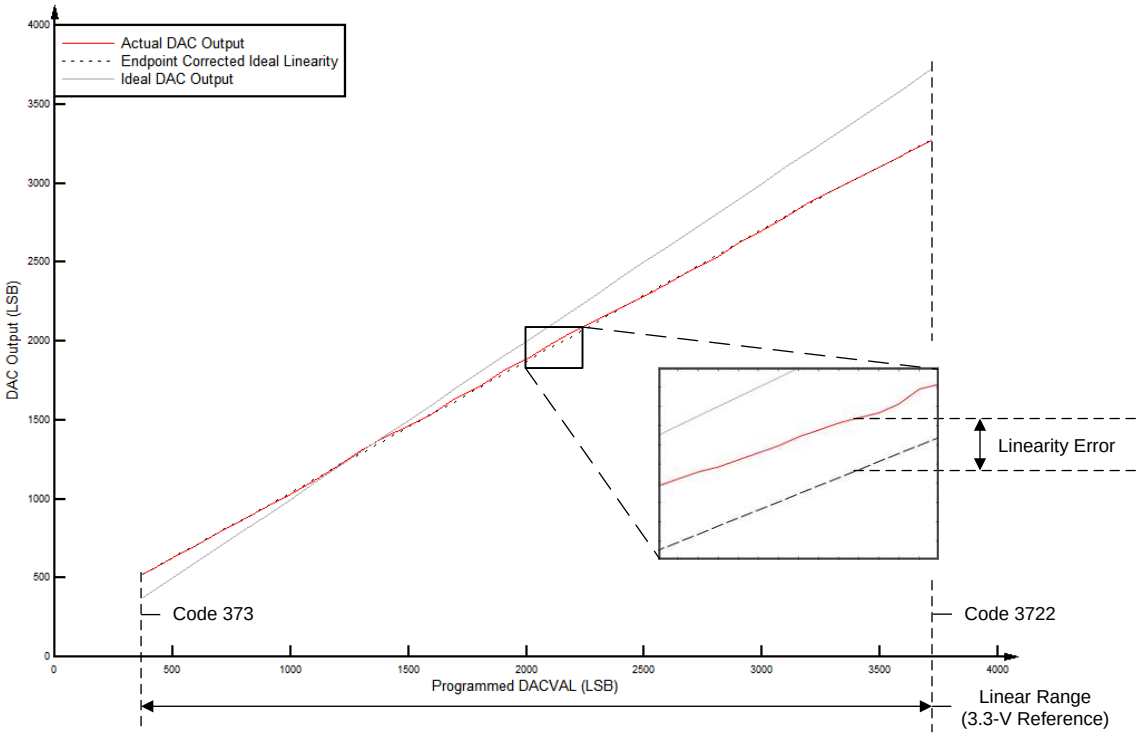



**Figure 5-41. Buffered DAC Linearity**


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#### 5.10.4.1.2 Buffered DAC Typical Characteristics Graphs

Figure 5-42 to Figure 5-47 show the typical performance for some buffered DAC parameters. Figure 5-42 shows the DNL. Figure 5-43 shows the INL. Figure 5-44 shows the glitch response (511 to 512 DACVAL) and Figure 5-45 shows the glitch response (512 to 511 DACVAL). Note that the glitch only happens at MSB transitions, with 511-to-512 and 512-to-511 transitions being the worst case. Figure 5-46 shows the 1-kΩ load transient. Figure 5-47 shows the 5-kΩ load transient.

**NOTE**

For Figure 5-42 to Figure 5-47, the following conditions apply (unless otherwise noted):

- $T_A$ = 30°C
- VDDA = 3.3 V
- VDD = 1.2 V

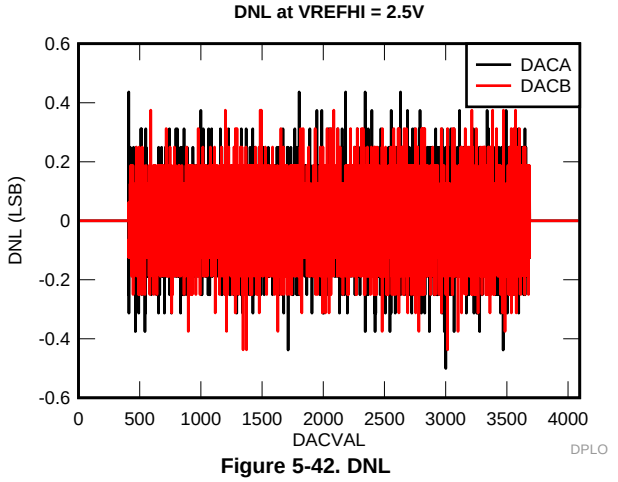



Figure 5-42. DNL

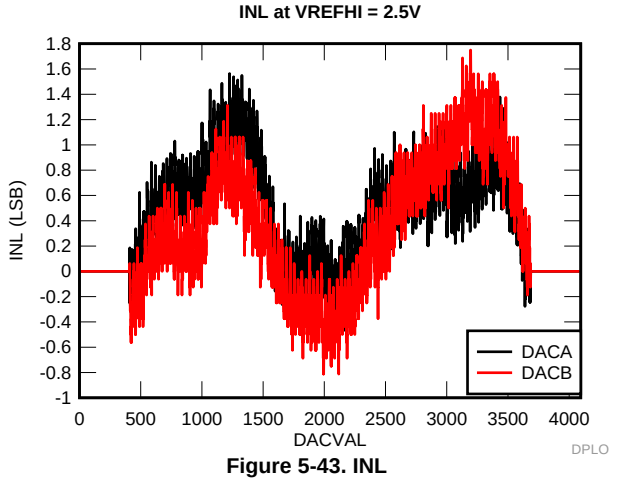



Figure 5-43. INL

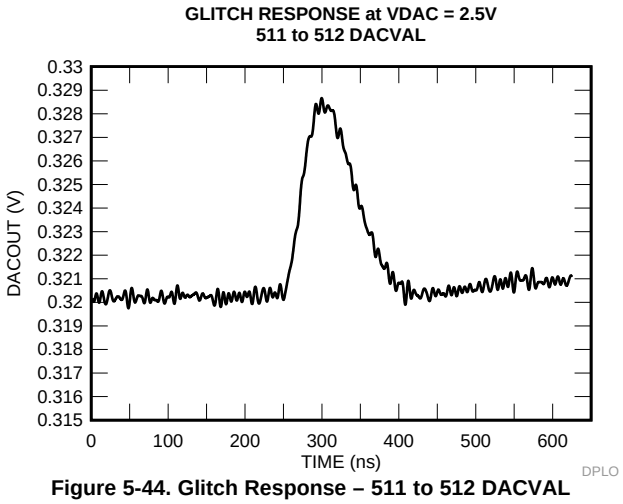



Figure 5-44. Glitch Response – 511 to 512 DACVAL

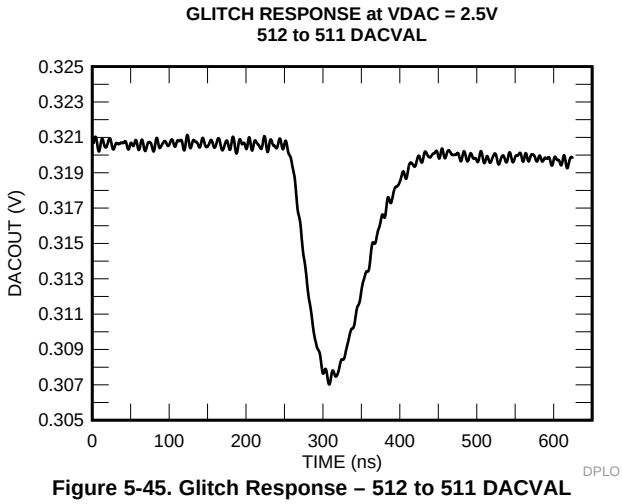



Figure 5-45. Glitch Response – 512 to 511 DACVAL

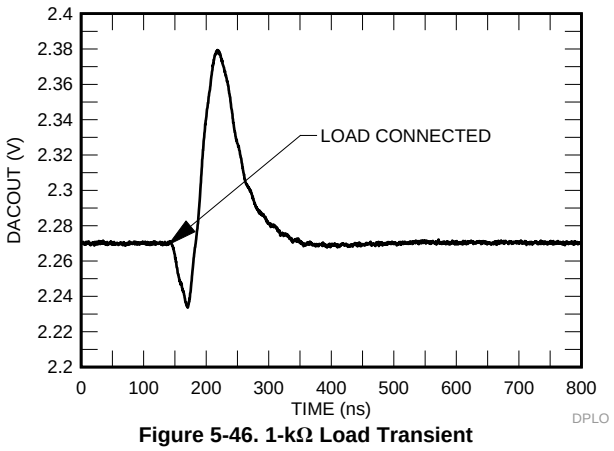



**Figure 5-46. 1-kΩ Load Transient**

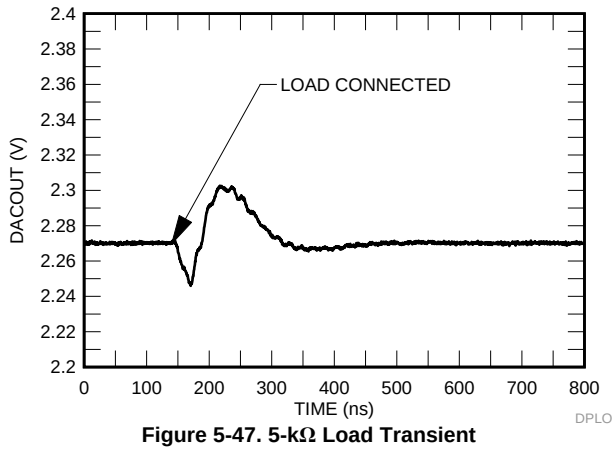



**Figure 5-47. 5-kΩ Load Transient**


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### 5.10.5 Comparator Subsystem (CMPSS)

Each CMPSS contains two comparators, two reference 12-bit DACs, two digital filters, and one ramp generator. Comparators are denoted "H" or "L" within each module, where “H” and “L” represent high and low, respectively. Each comparator generates a digital output that indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator can be driven from an external pin or by the PGA. The negative input can be driven by an external pin or by the programmable reference 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required. A ramp generator circuit is optionally available to control the reference 12-bit DAC value for the high comparator in the subsystem. There are two outputs from each CMPSS module. These two outputs pass through the digital filters and crossbar before connecting to the ePWM modules or GPIO pin. Figure 5-48 shows the CMPSS connectivity.

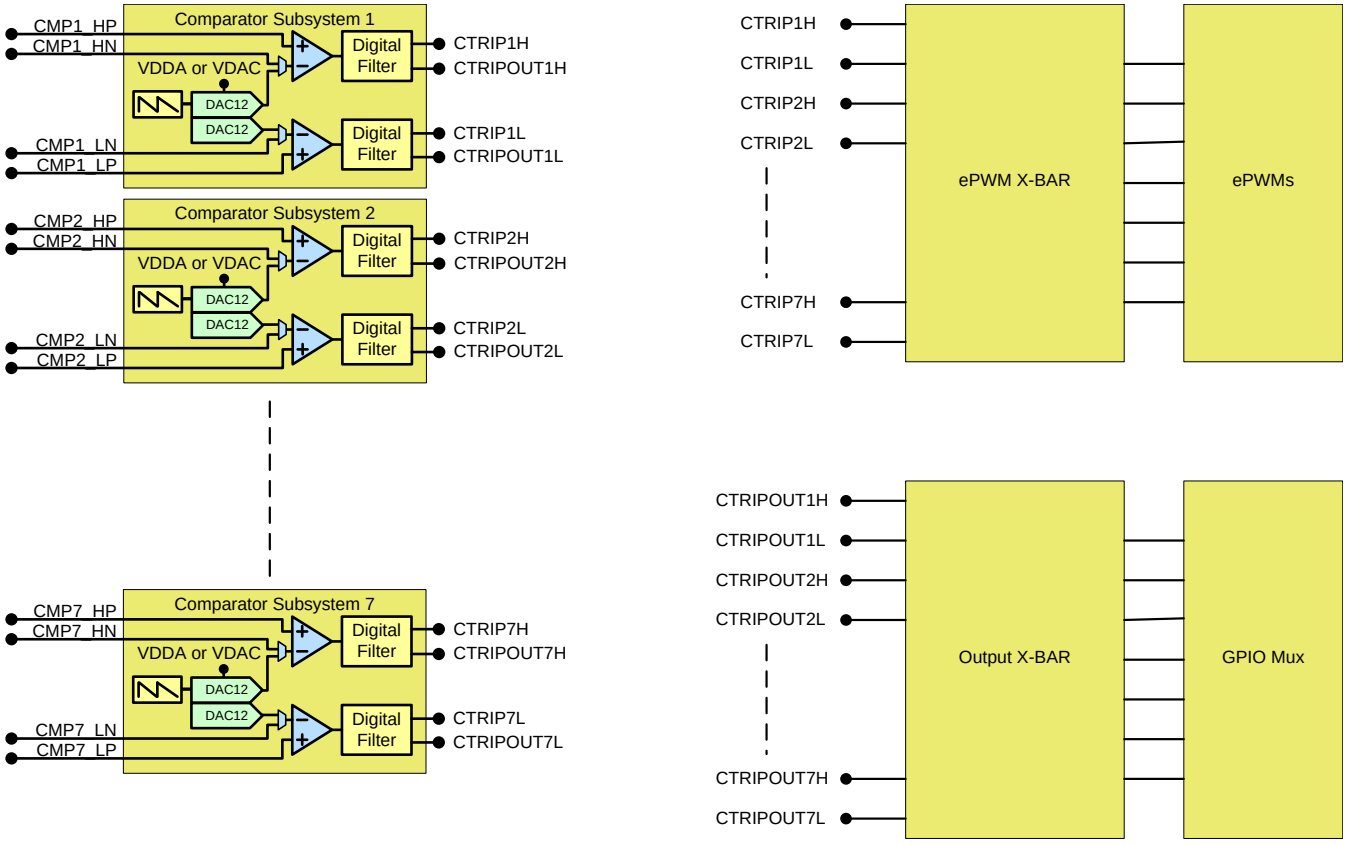



**Figure 5-48. CMPSS Connectivity**

**NOTE**

Not all packages have all CMPSS pins. See Table 5-39.

### 5.10.5.1 CMPSS Electrical Data and Timing

Table 5-53 lists the comparator electrical characteristics. Figure 5-49 shows the CMPSS comparator input referred offset. Figure 5-50 shows the CMPSS comparator hysteresis.

**Table 5-53. Comparator Electrical Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| TPU | Power-up time | | | | 500 | µs |
| Comparator input (CMPINxx) range | | | 0 | | VDDA | V |
| Input referred offset error | | | –20 | | 20 | mV |
| Hysteresis(1) | | 1x | | 12 | | LSB |
| | | 2x | | 24 | | |
| | | 3x | | 36 | | |
| | | 4x | | 48 | | |
| Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR) | | Step response | | 21 | 60 | ns |
| | | Ramp response (1.65V/µs) | | 26 | | |
| | | Ramp response (8.25mV/µs) | | 30 | | ns |
| PSRR | Power Supply Rejection Ratio | Up to 250 kHz | | 46 | | dB |
| CMRR | Common Mode Rejection Ratio | | 40 | | | dB |

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

**NOTE**

The CMPSS inputs must be kept below VDDA + 0.3 V to ensure proper functional operation. If a CMPSS input exceeds this level, an internal blocking circuit isolates the internal comparator from the external pin until the external pin voltage returns below VDDA + 0.3 V. During this time, the internal comparator input is floating and can decay below VDDA within approximately 0.5 µs. After this time, the comparator could begin to output an incorrect result depending on the value of the other comparator input.

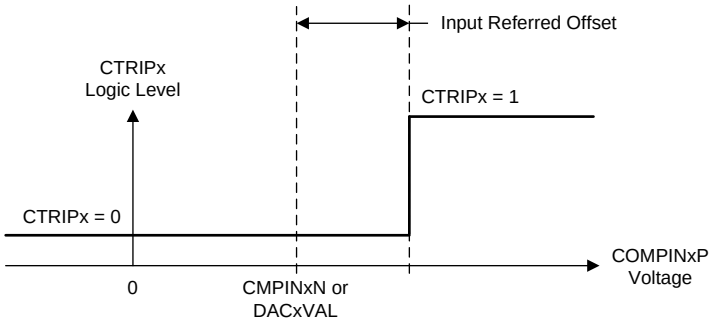



**Figure 5-49. CMPSS Comparator Input Referred Offset**


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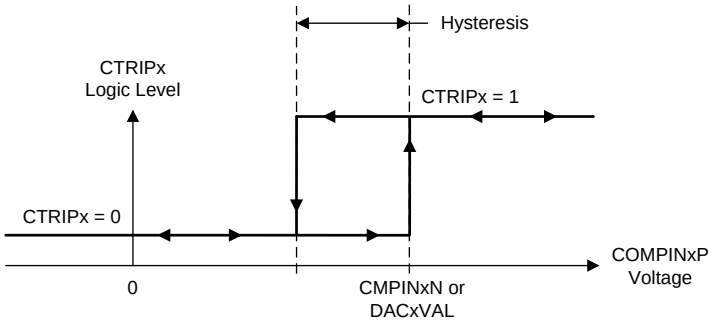



**Figure 5-50. CMPSS Comparator Hysteresis**

Table 5-54 lists the CMPSS DAC static electrical characteristics.

**Table 5-54. CMPSS DAC Static Electrical Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| CMPSS DAC output range | Internal reference | 0 | | VDDA | V |
| | External reference | 0 | | VDAC(1) | |
| Static offset error(2) | | –25 | | 25 | mV |
| Static gain error(2) | | –2 | | 2 | % of FSR |
| Static DNL | Endpoint corrected | >–1 | | 4 | LSB |
| Static INL | Endpoint corrected | –16 | | 16 | LSB |
| Settling time | Settling to 1LSB after full-scale output change | | | 1 | µs |
| Resolution | | | 12 | | bits |
| CMPSS DAC output disturbance(3) | Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module | –100 | | 100 | LSB |
| CMPSS DAC disturbance time(3) | | | | 200 | ns |
| VDAC reference voltage | When VDAC is reference | 2.4 | 2.5 or 3.0 | VDDA | V |
| VDAC load(4) | When VDAC is reference | 6 | 8 | 10 | kΩ |

(1) The maximum output voltage is VDDA when VDAC > VDDA.
(2) Includes comparator input referred errors.
(3) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.
(4) Per active CMPSS module.

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#### 5.10.5.1.1 CMPSS Illustrative Graphs

Figure 5-51 shows the CMPSS DAC static offset. Figure 5-52 shows the CMPSS DAC static gain. Figure 5-53 shows the CMPSS DAC static linearity.

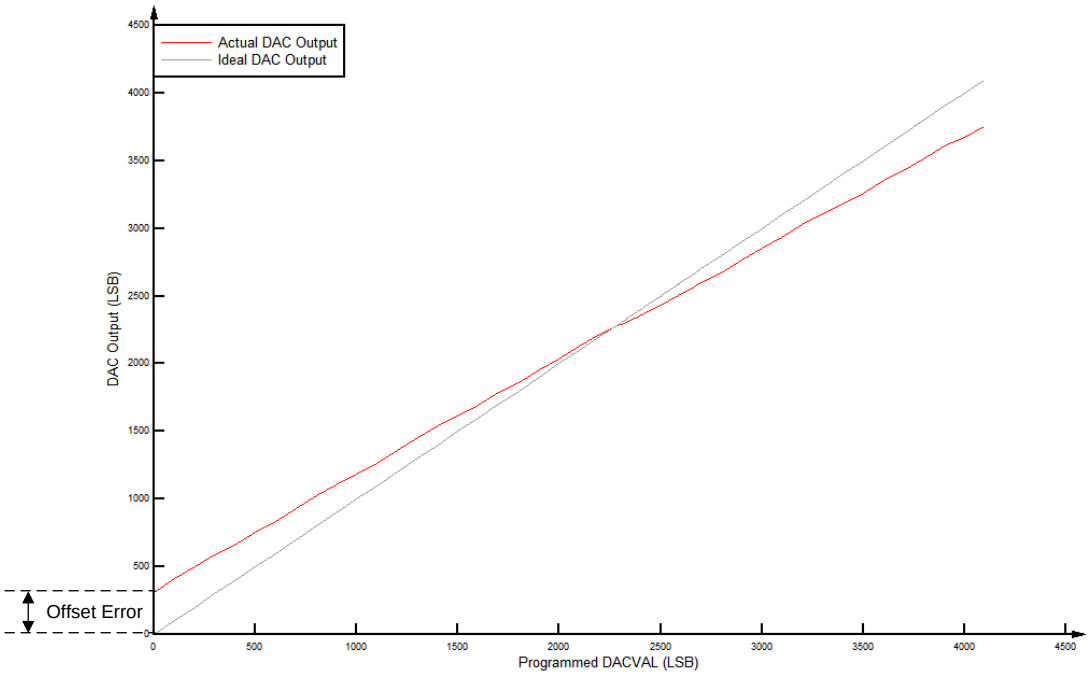



**Figure 5-51. CMPSS DAC Static Offset**

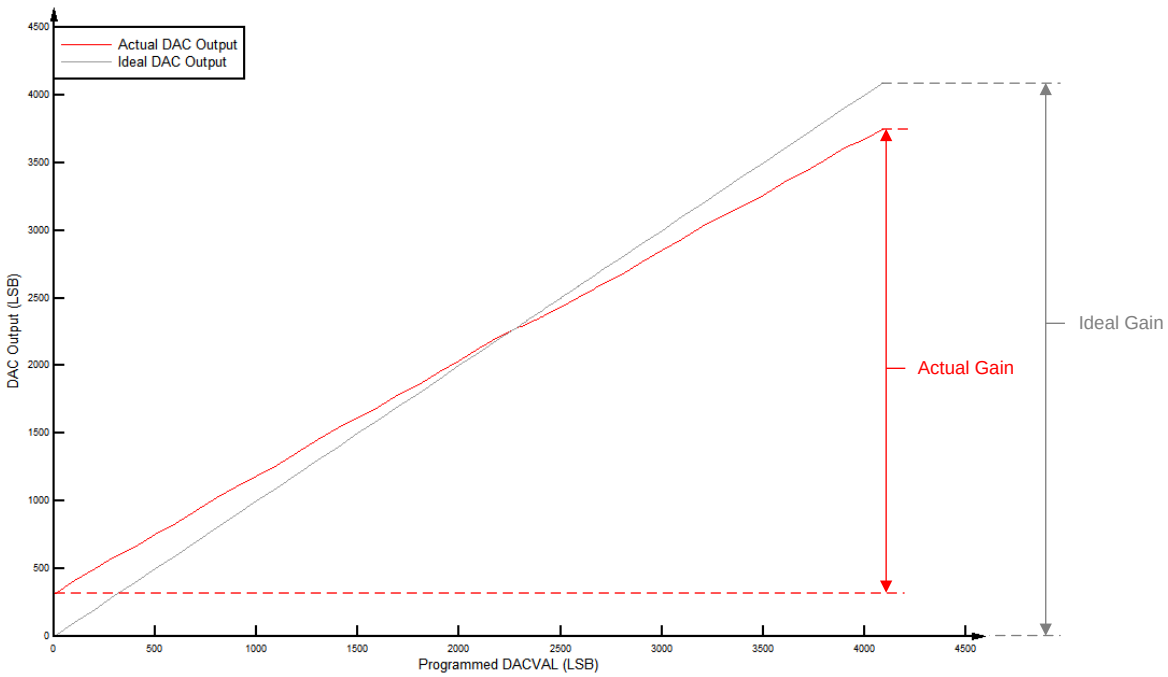



**Figure 5-52. CMPSS DAC Static Gain**


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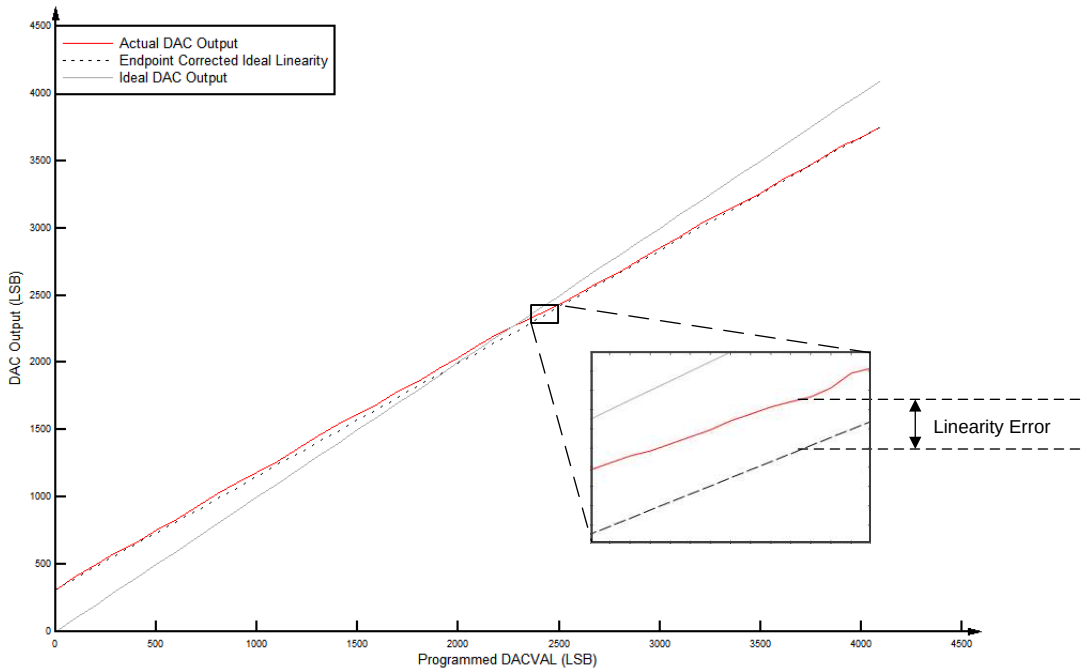



**Figure 5-53. CMPSS DAC Static Linearity**

## 5.11 Control Peripherals

### 5.11.1 Enhanced Capture (eCAP)

The Type 1 enhanced capture (eCAP) module is used in systems where accurate timing of external events is important.

Applications for the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module includes the following features:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- CPU interrupt on any one of the four events
- Independent DMA trigger
- Single-shot capture of up to four event timestamps
- Continuous mode capture of timestamps in a 4-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- 128:1 input multiplexer
- Event Prescaler
- When not used in capture mode, the eCAP module can be configured as a single channel PWM output.

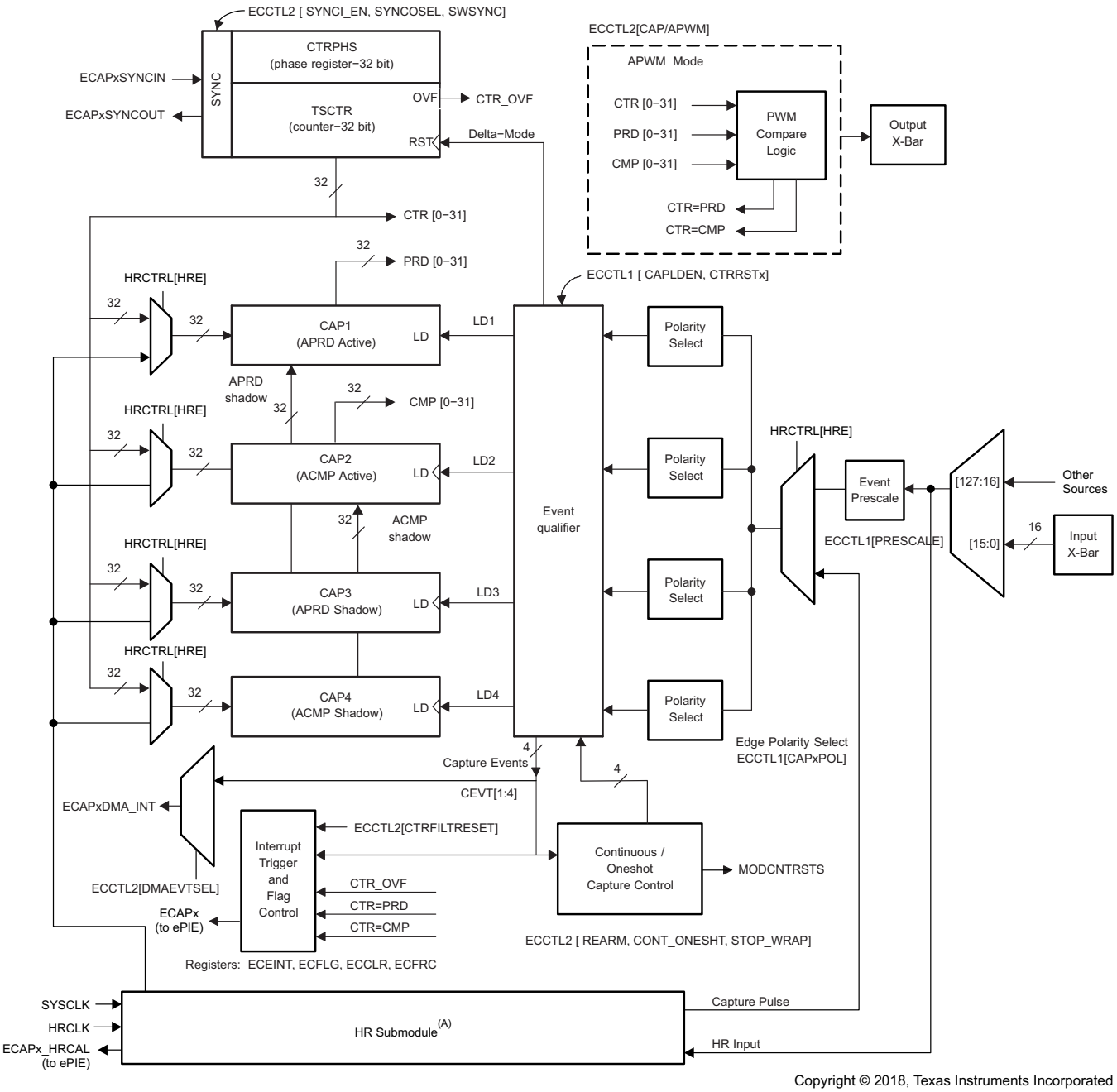
The capture functionality of the Type-1 eCAP is enhanced from the Type-0 eCAP with the following added features:

- Event filter reset bit
  - Writing a 1 to ECCTL2[CTRFILTRESET] will clear the event filter, the modulo counter, and any pending interrupts flags. This is useful for initialization and debug.
- Modulo counter status bits
  - The modulo counter (ECCTL2[MODCTRSTS]) indicates which capture register will be loaded next. In the Type-0 eCAP, it was not possible to know the current state of modulo counter.
- DMA trigger source
  - eCAPxDMA was added as a DMA trigger. CEVT[1–4] can be configured as the source for eCAPxDMA.
- Input multiplexer
  - ECCTL0[INPUTSEL] selects one of 128 input signals.
- EALLOW protection
  - EALLOW protection was added to critical registers.

The Input X-BAR must be used to connect the device input pins to the module. The Output X-BAR must be used to connect output signals to the OUTPUTXBARx output locations. See Section 4.4.3 and Section 4.4.4.

Figure 5-54 shows the eCAP block diagram.


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A. The HRCAP submodule is not available on all eCAP modules; in this case, the high-resolution muxes and hardware are not implemented.

**Figure 5-54. eCAP Block Diagram**

#### 5.11.1.1 eCAP Electrical Data and Timing

Table 5-55 lists the eCAP timing requirements. Table 5-56 lists the eCAP switching characteristics.

**Table 5-55. eCAP Timing Requirements**

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{w(CAP)}$ | Capture input pulse width | Asynchronous | $2t_{c(SCO)}$ | | | ns |
| | | Synchronous | $2t_{c(SCO)}$ | | | |
| | | With input qualifier | $1t_{c(SCO)} + t_{w_(QSW)}$ | | | |

**Table 5-56. eCAP Switching Charcteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(APWM)}$ | Pulse duration, APWMx output high/low | 20 | | | ns |


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### 5.11.2 High-Resolution Capture Submodule (HRCAP6–HRCAP7)

The device contains up to two high-resolution capture (HRCAP) submodules. The HRCAP submodule measures the difference, in time, between pulses asynchronously to the system clock. This submodule is new to the eCAP Type 1 module, and features many enhancements over the Type 0 HRCAP module.

Applications for the HRCAP include:

- Capacitive touch applications
- High-resolution period and duty-cycle measurements of pulse train cycles
- Instantaneous speed measurements
- Instantaneous frequency measurements
- Voltage measurements across an isolation boundary
- Distance/sonar measurement and scanning
- Flow measurements

The HRCAP submodule includes the following features:

- Pulse-width capture in either non-high-resolution or high-resolution modes
- Absolute mode pulse-width capture
- Continuous or "one-shot" capture
- Capture on either falling or rising edge
- Continuous mode capture of pulse widths in 4-deep buffer
- Hardware calibration logic for precision high-resolution capture
- All of the resources in this list are available on any pin using the Input X-BAR.

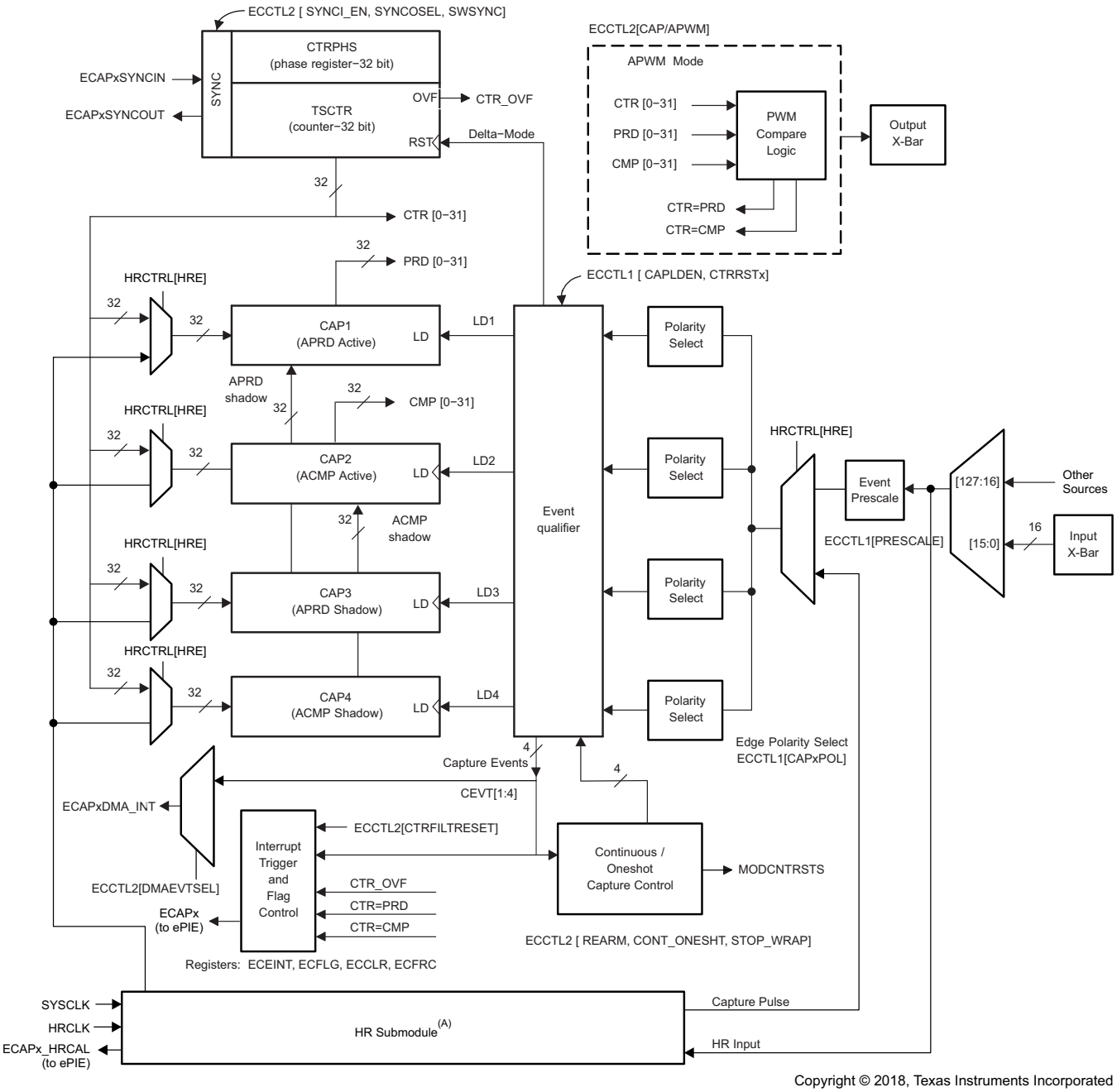
The HRCAP submodule includes one high-resolution capture channel in addition to a calibration block. The calibration block allows the HRCAP submodule to be continually recalibrated, at a set interval, with no “down time”. Because the HRCAP submodule now uses the same hardware as its respective eCAP, if the HRCAP is used, the corresponding eCAP will be unavailable.

Each high-resolution-capable channel has the following independent key resources.

- All hardware of the respective eCAP
- High-resolution calibration logic
- Dedicated calibration interrupt

Figure 5-55 shows the HRCAP block diagram.

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A. The HRCAP submodule is not available on all eCAP modules; in this case, the high-resolution muxes and hardware are not implemented.

**Figure 5-55. HRCAP Block Diagram**


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#### 5.11.2.1 HRCAP Electrical Data and Timing

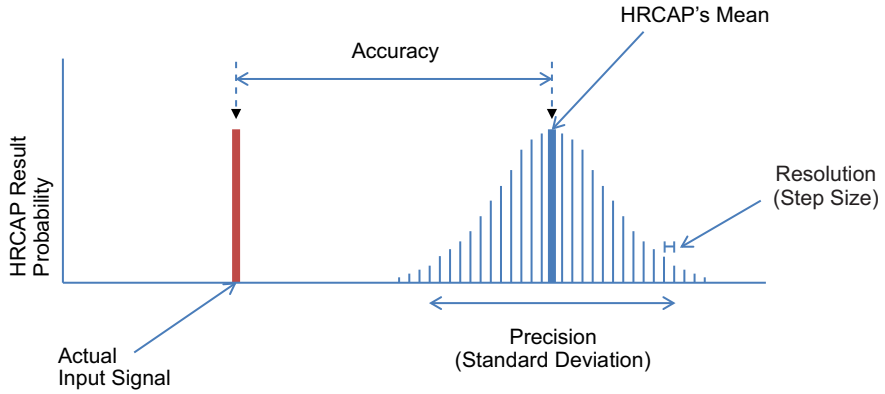
Table 5-57 lists the HRCAP switching characteristics. Figure 5-56 shows the HRCAP accuracy precision and resolution. Figure 5-57 shows the HRCAP standard deviation characteristics.

**Table 5-57. HRCAP Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

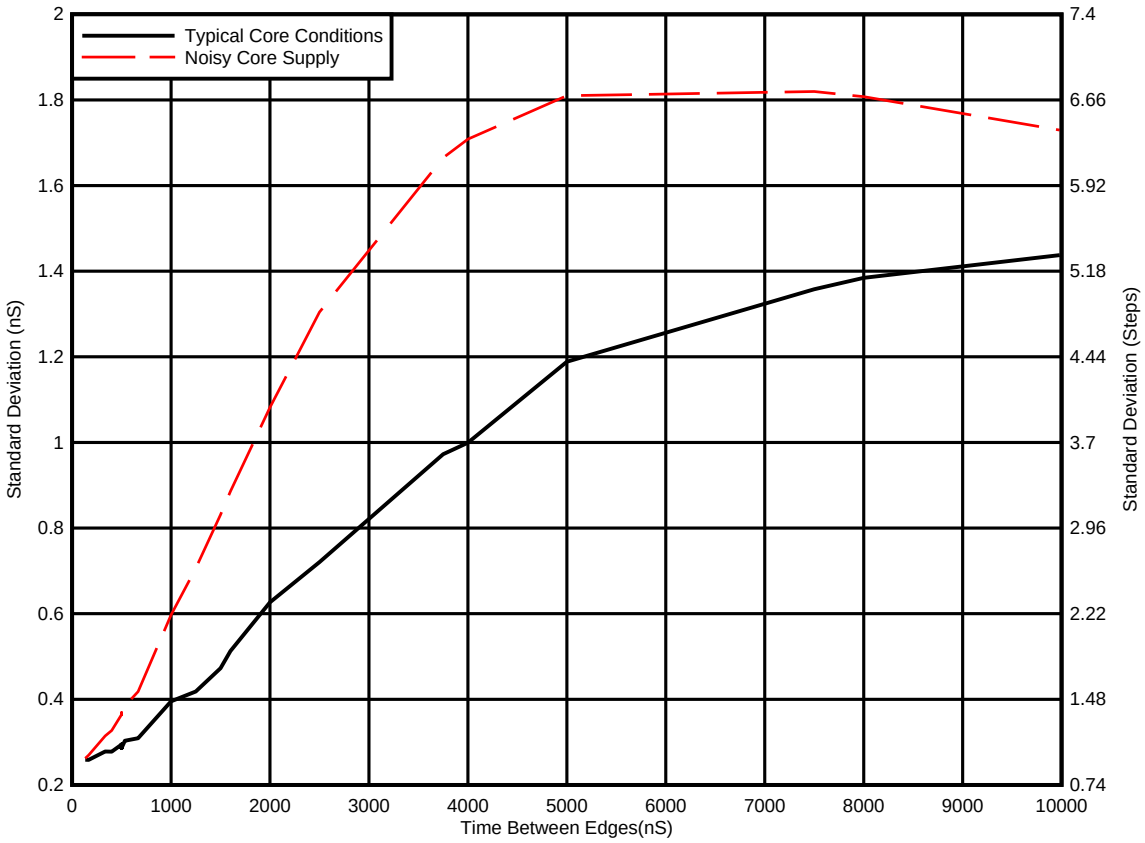
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input pulse width | | 110 | | | ns |
| Accuracy(1)(2)(3)(4) | Measurement length ≤ 5 µs | | ±390 | 540 | ps |
| | Measurement length > 5 µs | | ±450 | 1450 | ps |
| Standard deviation | | | See Figure 5-57 | | |
| Resolution | | | 300 | | ps |

(1) Value obtained using an oscillator of 100 PPM, oscillator accuracy directly affects the HRCAP accuracy.
(2) Measurement is completed using rising-rising or falling-falling edges
(3) Opposite polarity edges will have an additional inaccuracy due to the difference between $V_{IH}$ and $V_{IL}$. This effect is dependent on the signal's slew rate.
(4) Accuracy only applies to time-converted measurements.




A. The HRCAP has some variation in performance, this results in a probability distribution which is described using the following terms:
- Accuracy: The time difference between the input signal and the mean of the HRCAP's distribution.
- Precision: The width of the HRCAP's distribution, this is given as a standard deviation.
- Resolution: The minimum measurable increment.

**Figure 5-56. HRCAP Accuracy Precision and Resolution**




A. Typical core conditions: All peripheral clocks are enabled.

B. Noisy core supply: All core clocks are enabled and disabled with a regular period during the measurement. This resulted in the 1.2-V rail experiencing a 18.5-mA swing during the measurement.

C. Fluctuations in current and voltage on the 1.2-V rail cause the standard deviation of the HRCAP to rise. Care should be taken to ensure that the 1.2-V supply is clean, and that noisy internal events, such as enabling and disabling clock trees, have been minimized while using the HRCAP.

**Figure 5-57. HRCAP Standard Deviation Characteristics**

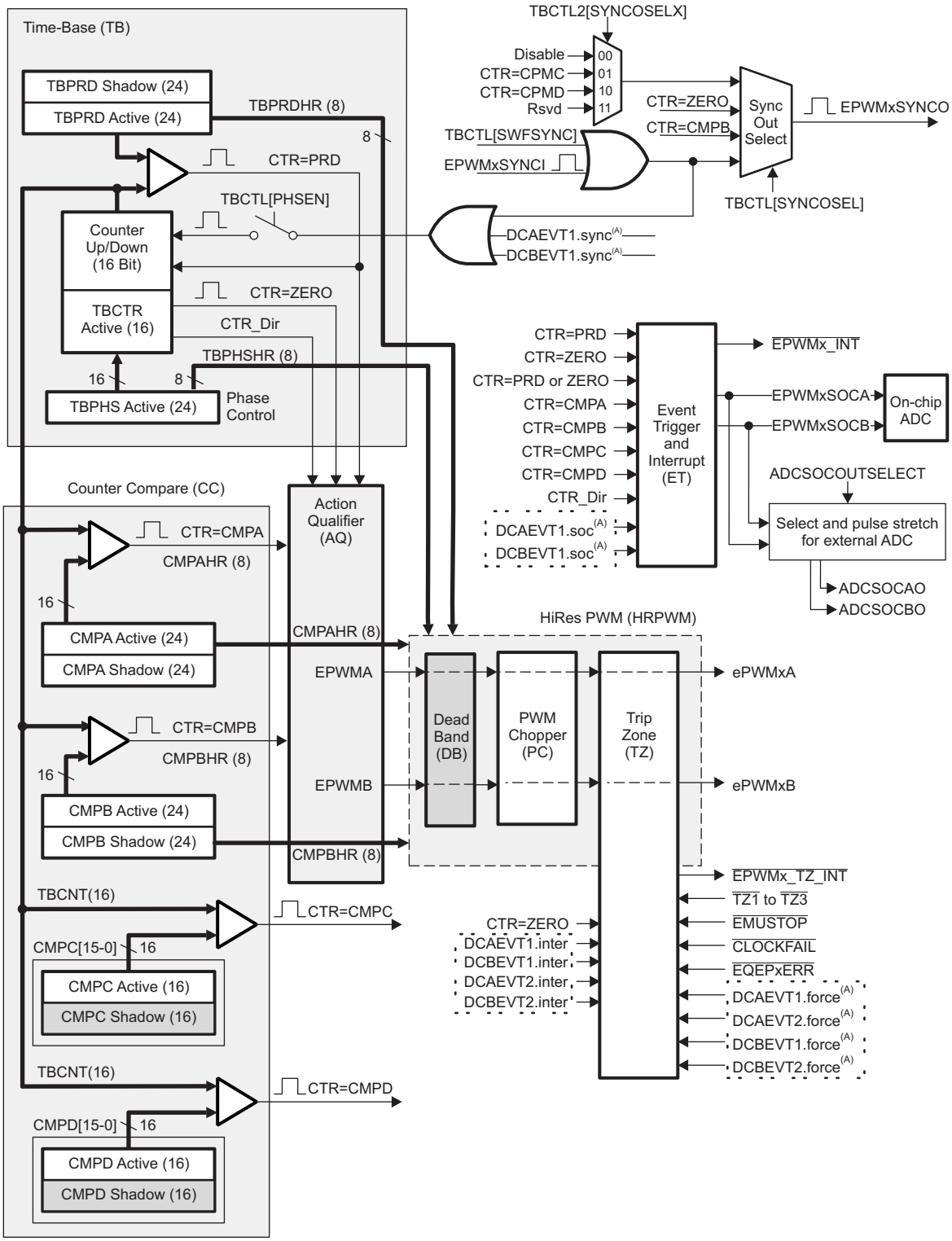

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### 5.11.3 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module generates complex pulse width waveforms with minimal CPU overhead. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

Figure 5-58 shows the signal interconnections with the ePWM. Figure 5-59 shows the ePWM trip input connectivity.

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A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

**Figure 5-58. ePWM Submodules and Critical Internal Signal Interconnects**


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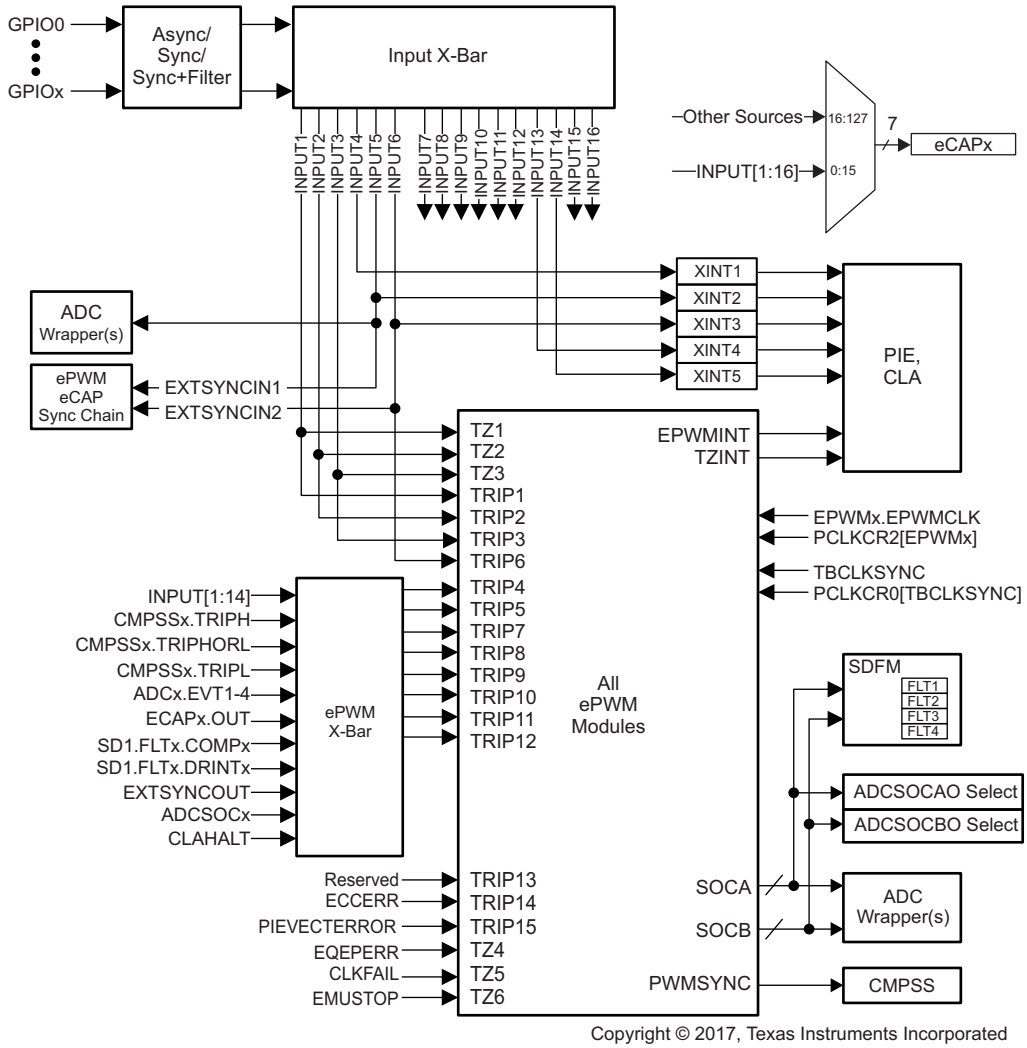



**Figure 5-59. ePWM Trip Input Connectivity**

### 5.11.3.1 Control Peripherals Synchronization

The ePWM and eCAP Synchronization Chain allows synchronization between multiple modules for the system. Figure 5-60 shows the Synchronization Chain Architecture.

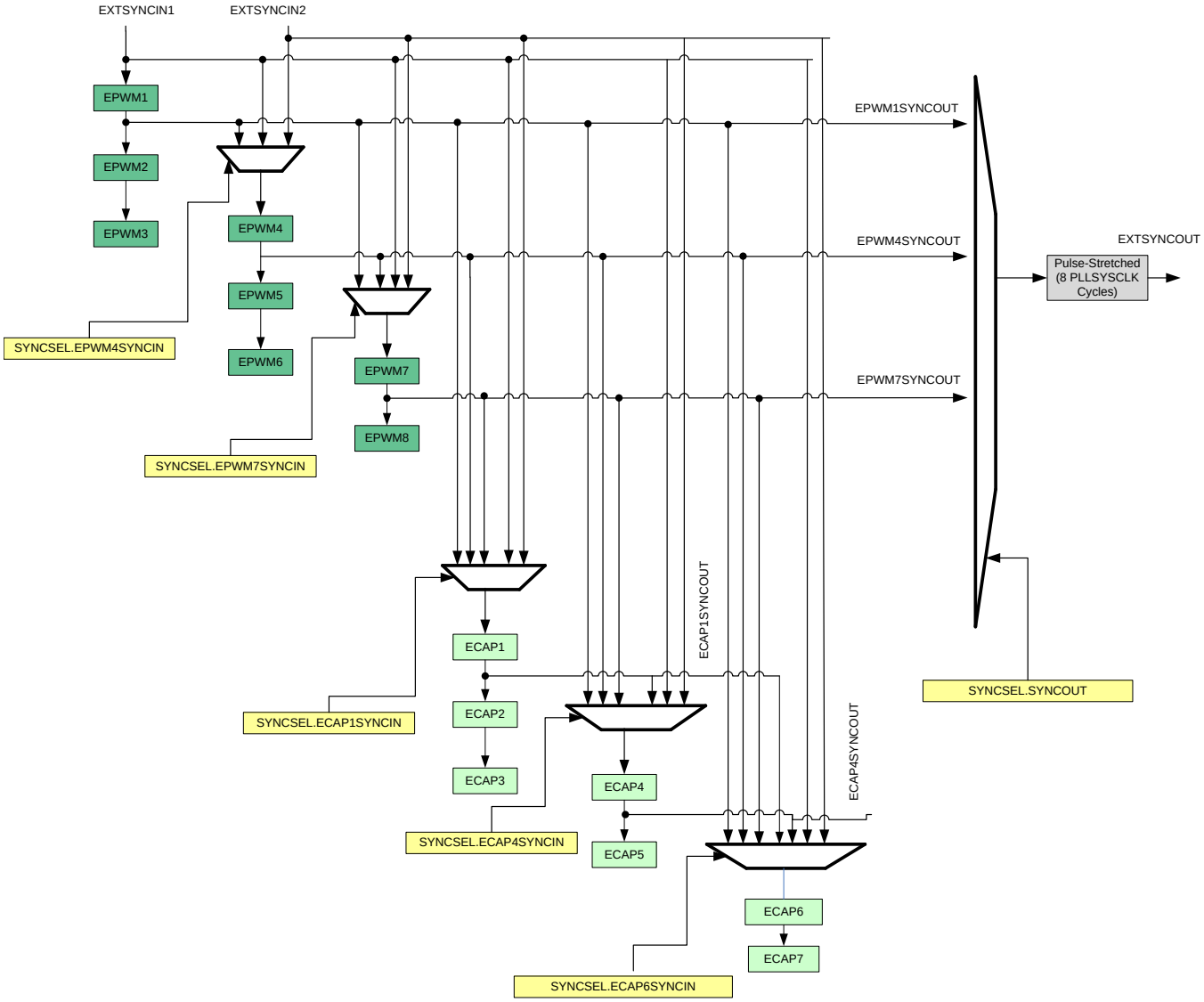



**Figure 5-60. Synchronization Chain Architecture**


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### 5.11.3.2 ePWM Electrical Data and Timing

Table 5-58 lists the ePWM timing requirements and Table 5-59 lists the ePWM switching characteristics.

**Table 5-58. ePWM Timing Requirements(1)**

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(SYNCIN)}$ | Sync input pulse width | Asynchronous | $2t_{c(EPWMCLK)}$ | | cycles |
| | | Synchronous | $2t_{c(EPWMCLK)}$ | | |
| | | With input qualifier | $1t_{c(EPWMCLK)} + t_{w(IQSW)}$ | | |

(1) For an explanation of the input qualifier parameters, see Table 5-31.

**Table 5-59. ePWM Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{w(PWM)}$ | Pulse duration, PWMx output high/low | 20 | | ns |
| $t_{w(SYNCOUT)}$ | Sync output pulse width | $8t_{c(SYSCLK)}$ | | cycles |
| $t_{d(TZ-PWM)}$ | Delay time, trip input active to PWM forced high<br>Delay time, trip input active to PWM forced low<br>Delay time, trip input active to PWM Hi-Z | | 25 | ns |

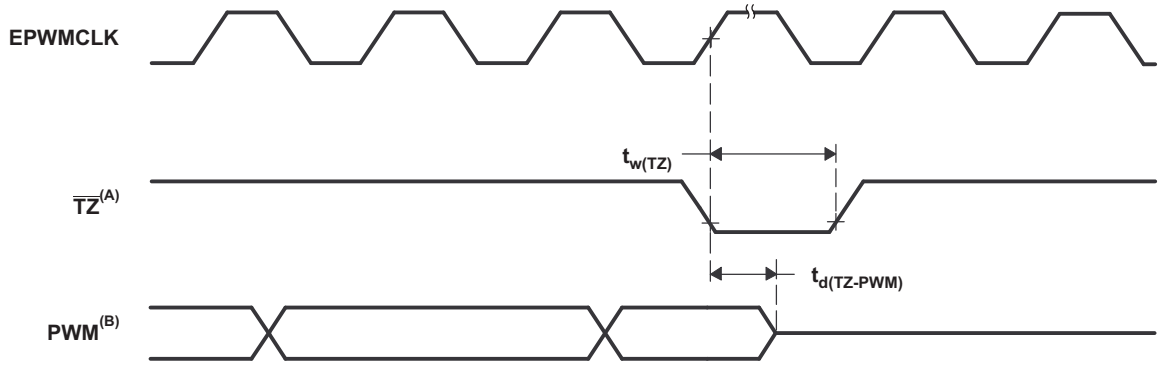
#### *5.11.3.2.1 Trip-Zone Input Timing*

Table 5-60 lists the trip-zone input timing requirements. Figure 5-61 shows the PWM Hi-Z characteristics.

**Table 5-60. Trip-Zone Input Timing Requirements(1)**

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(TZ)}$ | Pulse duration, $\overline{TZx}$ input low | Asynchronous | $1t_{c(EPWMCLK)}$ | | cycles |
| | | Synchronous | $2t_{c(EPWMCLK)}$ | | |
| | | With input qualifier | $1t_{c(EPWMCLK)} + t_{w(IQSW)}$ | | |

(1) For an explanation of the input qualifier parameters, see Table 5-31.




A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

**Figure 5-61. PWM Hi-Z Characteristics**

#### 5.11.3.3 External ADC Start-of-Conversion Electrical Data and Timing

Table 5-61 lists the external ADC start-of-conversion switching characteristics. Figure 5-62 shows the ADCSOCAO or ADCSOCBO timing.

**Table 5-61. External ADC Start-of-Conversion Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{w(ADCSOCL)}$ | Pulse duration, ADCSOCxO low | $32t_{c(SYSCLK)}$ | | cycles |

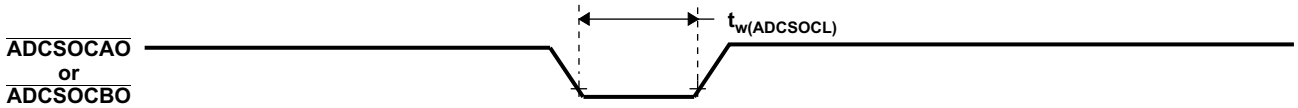



**Figure 5-62. ADCSOCAO or ADCSOCBO Timing**


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### 5.11.4 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual-edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period, and deadband registers of the ePWM module.

**NOTE**

The minimum HRPWMCLK frequency allowed for HRPWM is 60 MHz.

#### 5.11.4.1 HRPWM Electrical Data and Timing

Table 5-62 lists the high-resolution PWM switching characteristics.

**Table 5-62. High-Resolution PWM Characteristics**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Micro Edge Positioning (MEP) step size(1) | | 150 | 310 | ps |

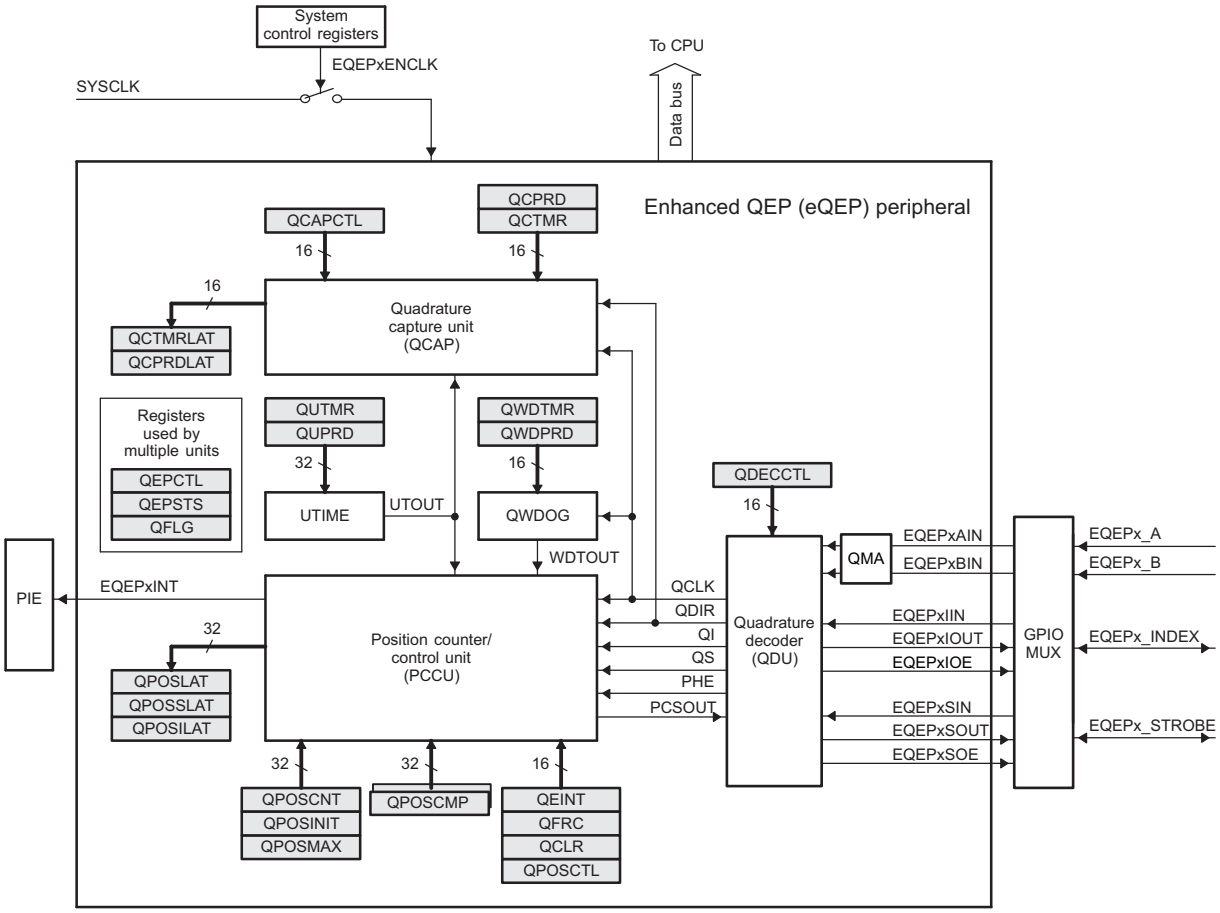
(1) The MEP step size will be largest at high temperature and minimum voltage on VDD. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

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### 5.11.5 Enhanced Quadrature Encoder Pulse (eQEP)

The Type-1 eQEP peripheral contains the following major functional units (see Figure 5-63):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)




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**Figure 5-63. eQEP Block Diagram**

#### 5.11.5.1 eQEP Electrical Data and Timing

Table 5-63 lists the eQEP timing requirements and Table 5-64 lists the eQEP switching characteristics.

**Table 5-63. eQEP Timing Requirements(1)**

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(QEPP)}$ | QEP input period | Asynchronous(2)/Synchronous | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$ | | |
| $t_{w(INDEXH)}$ | QEP Index Input High time | Asynchronous(2)/Synchronous | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(INDEXL)}$ | QEP Index Input Low time | Asynchronous(2)/Synchronous | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(STROBH)}$ | QEP Strobe High time | Asynchronous(2)/Synchronous | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(STROBL)}$ | QEP Strobe Input Low time | Asynchronous(2)/Synchronous | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |

(1) For an explanation of the input qualifier parameters, see Table 5-31.
(2) See the TMS320F28004x Piccolo™ Microcontrollers Silicon Errata for limitations in the asynchronous mode.

**Table 5-64. eQEP Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(CNTR)xin}$ | Delay time, external clock to counter increment | | $5t_{c(SYSCLK)}$ | cycles |
| $t_{d(PCS-OUT)QEP}$ | Delay time, QEP input edge to position compare sync output | | $7t_{c(SYSCLK)}$ | cycles |

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### 5.11.6 Sigma-Delta Filter Module (SDFM)

The SDFM is a 4-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each channel can receive an independent sigma-delta (ΣΔ) modulated bit stream. The bit streams are processed by four individually programmable digital decimation filters. The filter set includes a fast comparator for immediate digital threshold comparisons for overcurrent and undercurrent monitoring.

The SDFM features include:

- 8 external pins per SDFM module
  - 4 sigma-delta data input pins per SDFM module (SDx_D1-4)
  - 4 sigma-delta clock input pins per SDFM module (SDx_C1-4)
- 4 different configurable modulator clock modes:
  - Mode 0: Modulator clock rate equals modulator data rate
  - Mode 1: Modulator clock rate running at half the modulator data rate
  - Mode 2: Modulator data is Manchester encoded. Modulator clock not required.
  - Mode 3: Modulator clock rate is double that of modulator data rate
- 4 independent configurable secondary filter (comparator) units per SDFM module:
  - 4 different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - Ability to detect over-value, under-value, and zero-crossing conditions
  - OSR value for comparator filter unit (COSR) programmable from 1 to 32
- 4 independent configurable primary filter (data filter) units per SDFM module:
  - 4 different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - OSR value for data filter unit (DOSR) programmable from 1 to 256
  - Ability to enable individual filter modules
  - Ability to synchronize all the 4 independent filters of an SDFM module using Master Filter Enable (MFE) bit or using PWM signals
- Data filter unit has programmable FIFO to reduce interrupt overhead. FIFO has the following features:
  - Primary filter (data filter) has 16 deep × 32-bit FIFO
  - FIFO can interrupt CPU after programmable number of data ready events
  - FIFO Wait-for-Sync feature: Ability to ignore data ready events until PWM synchronization signal (SDSYNC) is received. Once SDSYNC event is received, FIFO is populated on every data ready event
  - Data filter output can be represented in either 16 bits or 32 bits
- PWMx.SOCA/SOCB can be configured to serve as SDSYNC source on per data filter channel basis
- PWMs can be used to generate a modulator clock for sigma delta modulators

**NOTE**

Care should be taken to avoid noise on the SDx_Cy input. If the minimum pulse width requirements are not met (for example, through a noise glitch), then the SDFM results could become undefined.

Figure 5-64 shows the SDFM block diagram.


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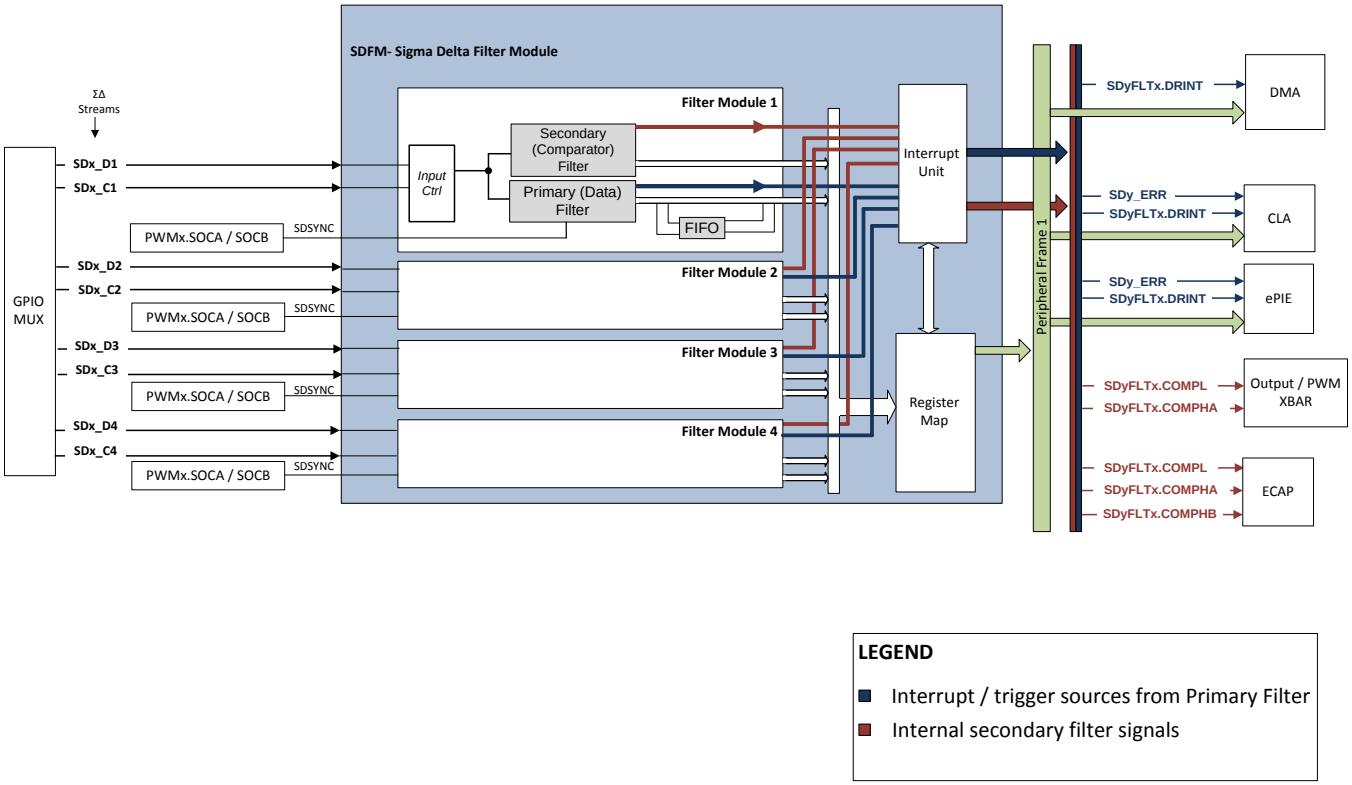



**Figure 5-64. SDFM Block Diagram**

#### 5.11.6.1 SDFM Electrical Data and Timing

SDFM operation with asynchronous GPIO is defined by setting GPyQSELn = 0b11. Table 5-65 lists the SDFM timing requirements when using the asynchronous GPIO (ASYNC) option. Figure 5-65, Figure 5-66, Figure 5-67, and Figure 5-68 show the SDFM timing diagrams.

**Table 5-65. SDFM Timing Requirements When Using Asynchronous GPIO (ASYNC) Option**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **Mode 0** | | | | |
| $t_{c(SDC)M0}$ | Cycle time, SDx_Cy | 40 | 256 * SYSCLK period | ns |
| $t_{w(SDCH)M0}$ | Pulse duration, SDx_Cy high | 10 | $t_{c(SDC)M0}$ – 10 | ns |
| $t_{su(SDDV-SDCH)M0}$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 5 | | ns |
| $t_{h(SDCH-SDD)M0}$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 5 | | ns |
| **Mode 1** | | | | |
| $t_{c(SDC)M1}$ | Cycle time, SDx_Cy | 80 | 256 * SYSCLK period | ns |
| $t_{w(SDCH)M1}$ | Pulse duration, SDx_Cy high | 10 | $t_{c(SDC)M1}$ – 10 | ns |
| $t_{su(SDDV-SDCL)M1}$ | Setup time, SDx_Dy valid before SDx_Cy goes low | 5 | | ns |
| $t_{su(SDDV-SDCH)M1}$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 5 | | ns |
| $t_{h(SDCL-SDD)M1}$ | Hold time, SDx_Dy wait after SDx_Cy goes low | 5 | | ns |
| $t_{h(SDCH-SDD)M1}$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 5 | | ns |
| **Mode 2** | | | | |
| $t_{c(SDD)M2}$ | Cycle time, SDx_Dy | 8 * $t_{c(SYSCLK)}$ | 20 * $t_{c(SYSCLK)}$ | ns |
| $t_{w(SDDH)M2}$ | Pulse duration, SDx_Dy high | 10 | | ns |
| **Mode 3** | | | | |
| $t_{c(SDC)M3}$ | Cycle time, SDx_Cy | 40 | 256 * SYSCLK period | ns |
| $t_{w(SDCH)M3}$ | Pulse duration, SDx_Cy high | 10 | $t_{c(SDC)M3}$ – 5 | ns |
| $t_{su(SDDV-SDCH)M3}$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 5 | | ns |
| $t_{h(SDCH-SDD)M3}$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 5 | | ns |

**WARNING**

**The SDFM clock inputs (SDx_Cy pins) directly clock the SDFM module when there is no GPIO input synchronization. Any glitches or ringing noise on these inputs can corrupt the SDFM module operation. Special precautions should be taken on these signals to ensure a clean and noise-free signal that meets SDFM timing requirements. Precautions such as series termination for ringing due to any impedance mismatch of the clock driver and spacing of traces from other noisy signals are recommended.**


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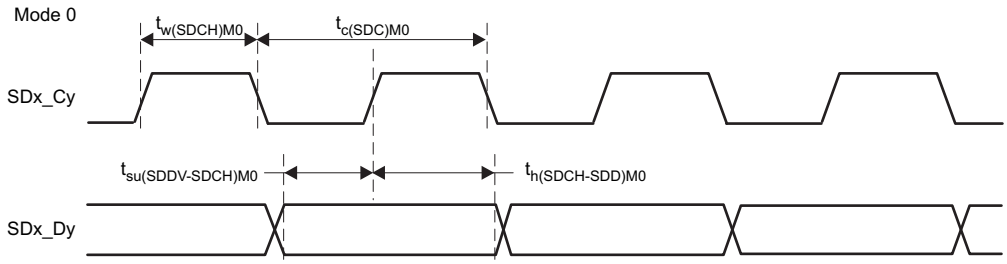



**Figure 5-65. SDFM Timing Diagram – Mode 0**

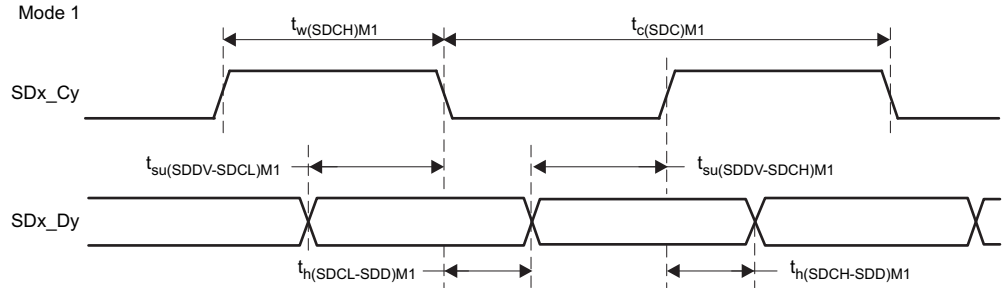



**Figure 5-66. SDFM Timing Diagram – Mode 1**

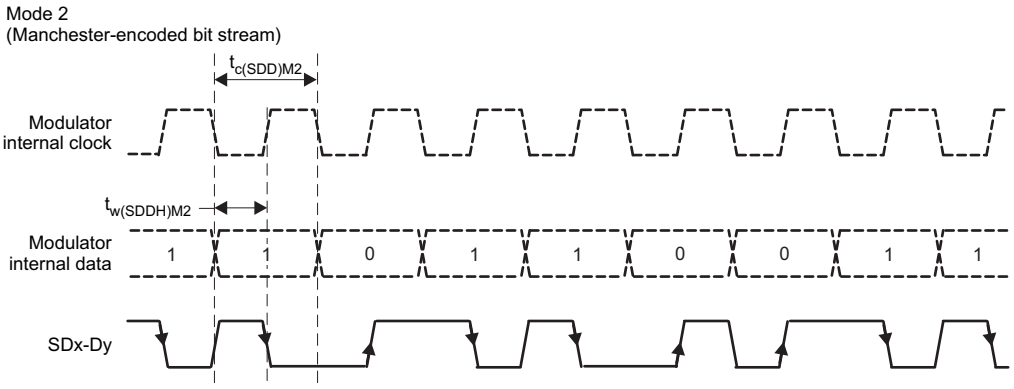



**Figure 5-67. SDFM Timing Diagram – Mode 2**

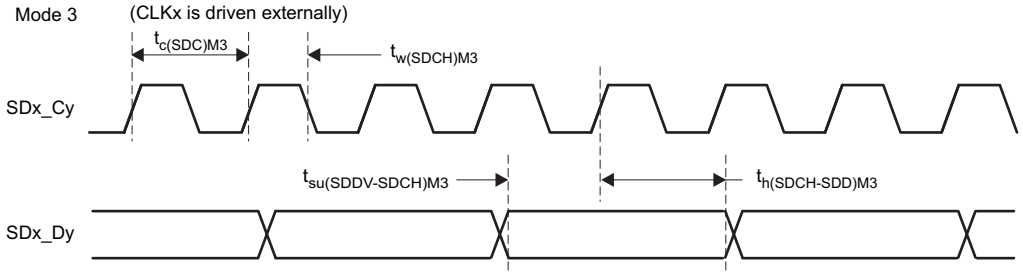



**Figure 5-68. SDFM Timing Diagram – Mode 3**

### 5.11.6.2 SDFM Electrical Data and Timing (Synchronized GPIO)

SDFM operation with synchronous GPIO is defined by setting GPyQSELn = 0b00. When using this synchronized GPIO mode, the timing requirement for $t_{w(GPI)}$ pulse duration of $2t_{c(SYSCLK)}$ must be met. It is important for both SD-Cx and SD-Dx pairs be configured with SYNC option. Table 5-66 lists the SDFM timing requirements when using the synchronized GPIO (SYNC) option. Figure 5-65, Figure 5-66, Figure 5-67, and Figure 5-68 show the SDFM timing diagrams.

**Table 5-66. SDFM Timing Requirements When Using Synchronized GPIO (SYNC) Option**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **Mode 0** | | | | |
| $t_{c(SDC)M0}$ | Cycle time, SDx_Cy | 5 * SYSCLK period | 256 * SYSCLK period | ns |
| $t_{w(SDCHL)M0}$ | Pulse duration, SDx_Cy high/low | 2 * SYSCLK period | 3 * SYSCLK period | ns |
| $t_{su(SDDV-SDCH)M0}$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 2 * SYSCLK period | | ns |
| $t_{h(SDCH-SDD)M0}$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 2 * SYSCLK period | | ns |
| **Mode 1** | | | | |
| $t_{c(SDC)M1}$ | Cycle time, SDx_Cy | 10 * SYSCLK period | 256 * SYSCLK period | ns |
| $t_{w(SDCHL)M1}$ | Pulse duration, SDx_Cy high/low | 2 * SYSCLK period | 8 * SYSCLK period | ns |
| $t_{su(SDDV-SDCL)M1}$ | Setup time, SDx_Dy valid before SDx_Cy goes low | 2 * SYSCLK period | | ns |
| $t_{su(SDDV-SDCH)M1}$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 2 * SYSCLK period | | ns |
| $t_{h(SDCL-SDD)M1}$ | Hold time, SDx_Dy wait after SDx_Cy goes low | 2 * SYSCLK period | | ns |
| $t_{h(SDCH-SDD)M1}$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 2 * SYSCLK period | | ns |
| **Mode 2** | | | | |
| $t_{c(SDD)M2}$ | Cycle time, SDx_Dy | Option unavailable | | |
| $t_{w(SDDH)M2}$ | Pulse duration, SDx_Dy high | | | |
| **Mode 3** | | | | |
| $t_{c(SDC)M3}$ | Cycle time, SDx_Cy | 5 * SYSCLK period | 256 * SYSCLK period | ns |
| $t_{w(SDCHL)M3}$ | Pulse duration, SDx_Cy high/low | 2 * SYSCLK period | 3 * SYSCLK period | ns |
| $t_{su(SDDV-SDCH)M3}$ | Setup time, SDx_Dy valid before SDx_Cy goes high | 2 * SYSCLK period | | ns |
| $t_{h(SDCH-SDD)M3}$ | Hold time, SDx_Dy wait after SDx_Cy goes high | 2 * SYSCLK period | | ns |

**NOTE**

The SDFM Synchronized GPIO (SYNC) option provides protection against SDFM module corruption due to occasional random noise glitches on the SDx_Cy pin that may result in a false comparator trip and filter output.

The SDFM Synchronized GPIO (SYNC) mode does not provide protection against persistent violations of the above timing requirements. Timing violations will result in data corruption proportional to the number of bits which violate the requirements.


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## 5.12 Communications Peripherals

### 5.12.1 Controller Area Network (CAN)

**NOTE**

The CAN module uses the IP known as *DCAN*. This document uses the names *CAN* and *DCAN* interchangeably to reference this peripheral.

The CAN module implements the following features:

- Complies with ISO11898-1 ( Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 Mbps
- Multiple clock sources
- 32 message objects (mailboxes), each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard (11-bit) or extended (29-bit) identifier
  - Supports programmable identifier receive mask
  - Supports data and remote frames
  - Holds 0 to 8 bytes of data
  - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loopback modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after bus-off state by a programmable 32-bit timer
- Two interrupt lines
- DMA support

**NOTE**

For a CAN bit clock of 100 MHz, the smallest bit rate possible is 3.90625 kbps.

**NOTE**

The accuracy of the on-chip zero-pin oscillator is in Table 5-23. Depending on parameters such as the CAN bit timing settings, bit rate, bus length, and propagation delay, the accuracy of this oscillator may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

Figure 5-69 shows the CAN block diagram.

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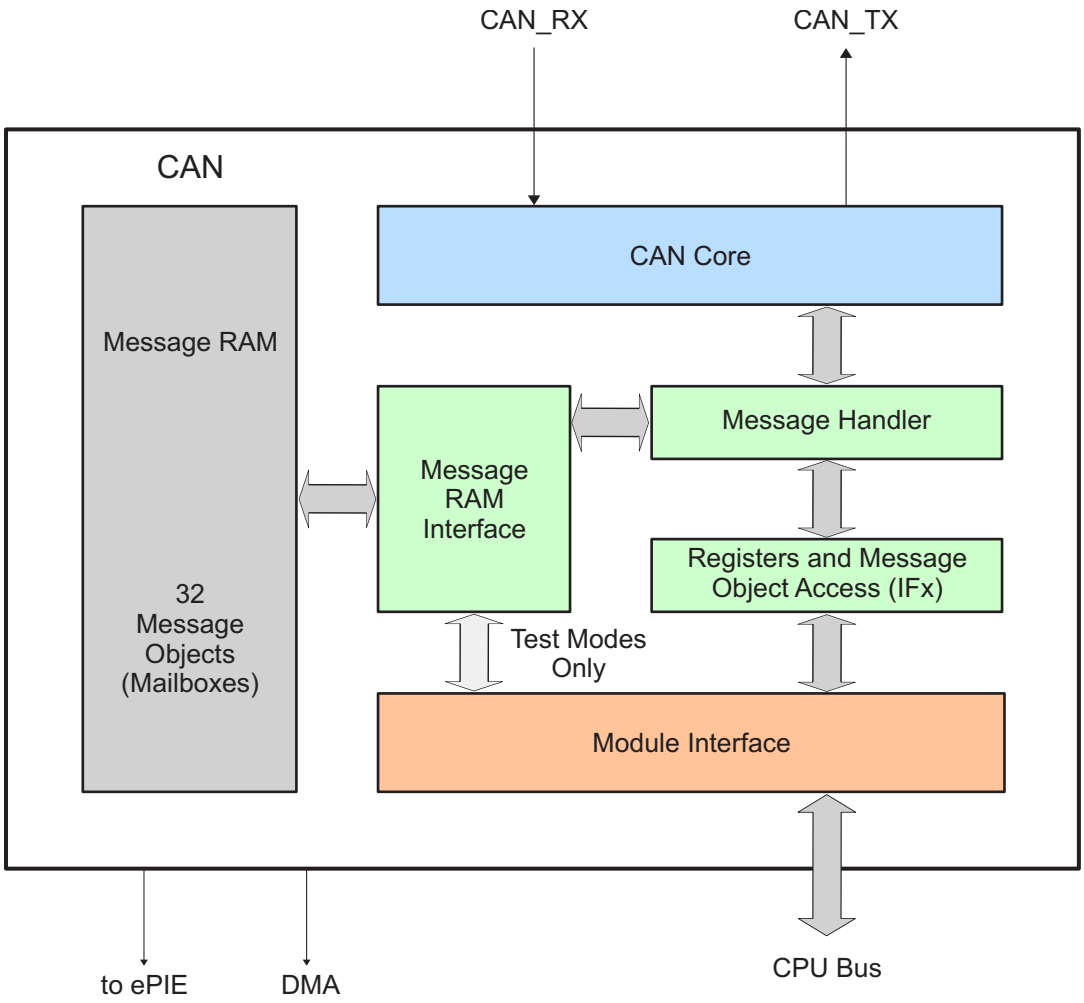



**Figure 5-69. CAN Block Diagram**


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### 5.12.2 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the NXP Semiconductors $I^2C$-bus specification (version 2.1):
  - Support for 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate from 10 kbps up to 400 kbps (Fast-mode)
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- Supports two ePIE interrupts
  - I2Cx interrupt – Any of the below conditions can be configured to generate an I2Cx interrupt:
    - Transmit Ready
    - Receive Ready
    - Register-Access Ready
    - No-Acknowledgment
    - Arbitration-Lost
    - Stop Condition Detected
    - Addressed-as-Slave
  - I2Cx_FIFO interrupts:
    - Transmit FIFO interrupt
    - Receive FIFO interrupt
- Module enable and disable capability
- Free data format mode

Figure 5-70 shows how the I2C peripheral module interfaces within the device.

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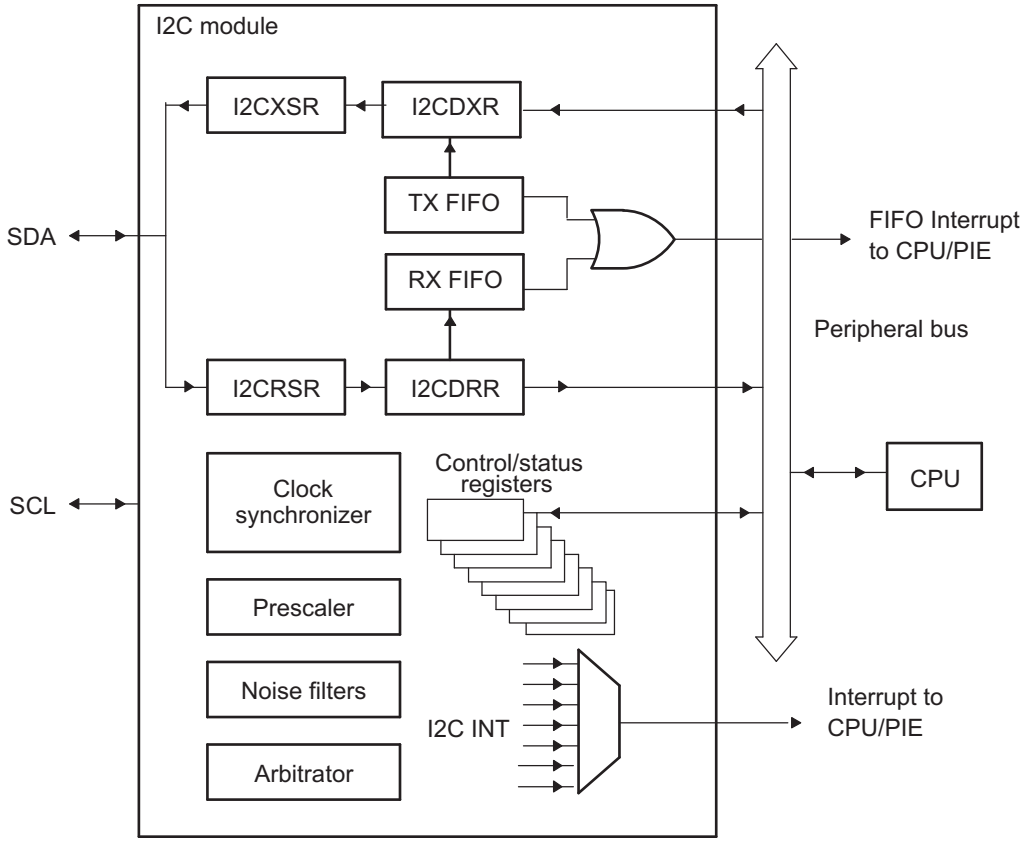



**Figure 5-70. I2C Peripheral Module Interfaces**


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#### 5.12.2.1 I2C Electrical Data and Timing

Table 5-67 lists the I2C timing requirements. Table 5-68 lists the I2C switching characteristics.

**Table 5-67. I2C Timing Requirements**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{h(SDA-SCL)START}$ | Hold time, START condition, SCL fall delay after SDA fall | 0.6 | | µs |
| $t_{su(SCL-SDA)START}$ | Setup time, Repeated START, SCL rise before SDA fall delay | 0.6 | | µs |
| $t_{h(SCL-DAT)}$ | Hold time, data after SCL fall | 0 | | µs |
| $t_{su(DAT-SCL)}$ | Setup time, data before SCL rise | 100 | | ns |
| $t_{r(SDA)}$ | Rise time, SDA | 20 | 300 | ns |
| $t_{r(SCL)}$ | Rise time, SCL | 20 | 300 | ns |
| $t_{f(SDA)}$ | Fall time, SDA | 11.4 | 300 | ns |
| $t_{f(SCL)}$ | Fall time, SCL | 11.4 | 300 | ns |
| $t_{su(SCL-SDA)STOP}$ | Setup time, STOP condition, SCL rise before SDA rise delay | 0.6 | | µs |

**Table 5-68. I2C Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | 0 | 400 | kHz |
| $t_{w(SCLL)}$ | Pulse duration, SCL clock low | | 1.3 | | µs |
| $t_{w(SCLH)}$ | Pulse duration, SCL clock high | | 0.6 | | µs |
| $t_{w(SP)}$ | Pulse duration of spikes that will be suppressed by the input filter | | 0 | 50 | ns |
| $t_{BUF}$ | Bus free time between STOP and START conditions | | 1.3 | | µs |
| $t_{v(SCL-DAT)}$ | Valid time, data after SCL fall | | | 0.9 | µs |
| $t_{v(SCL-ACK)}$ | Valid time, Acknowledge after SCL fall | | | 0.9 | µs |
| $V_{IL}$ | Valid low-level input voltage | | –0.3 | 0.3 * $V_{DDIO}$ | V |
| $V_{IH}$ | Valid high-level input voltage | | 0.7 * $V_{DDIO}$ | $V_{DDIO}$ + 0.3 | V |
| $V_{OL}$ | Low-level output voltage | Sinking 3 mA | 0 | 0.4 | V |
| $I_I$ | Input current on pins | 0.1 $V_{bus}$ < $V_i$ < 0.9 $V_{bus}$ | –10 | 10 | µA |

**NOTE**

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz.

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### 5.12.3 Power Management Bus (PMBus) Interface

The PMBus module has the following features:

- Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1)
- Support for master and slave modes
- Support for I2C mode
- Support for three speeds:
  - Standard Mode: Up to 100 kHz
  - Fast Mode: 400 kHz
  - Fast Mode+: 1000 kHz. This mode applies only to the PMBus module operating in I2C mode, with an input clock frequency of 20 MHz.
- Packet error checking
- CONTROL and ALERT signals
- Clock high and low time-outs
- Four-byte transmit and receive buffers
- One maskable interrupt, which can be generated by several conditions:
  - Receive data ready
  - Transmit buffer empty
  - Slave address received
  - End of message
  - ALERT input asserted
  - Clock low time-out
  - Clock high time-out
  - Bus free

Figure 5-71 shows the PMBus block diagram.

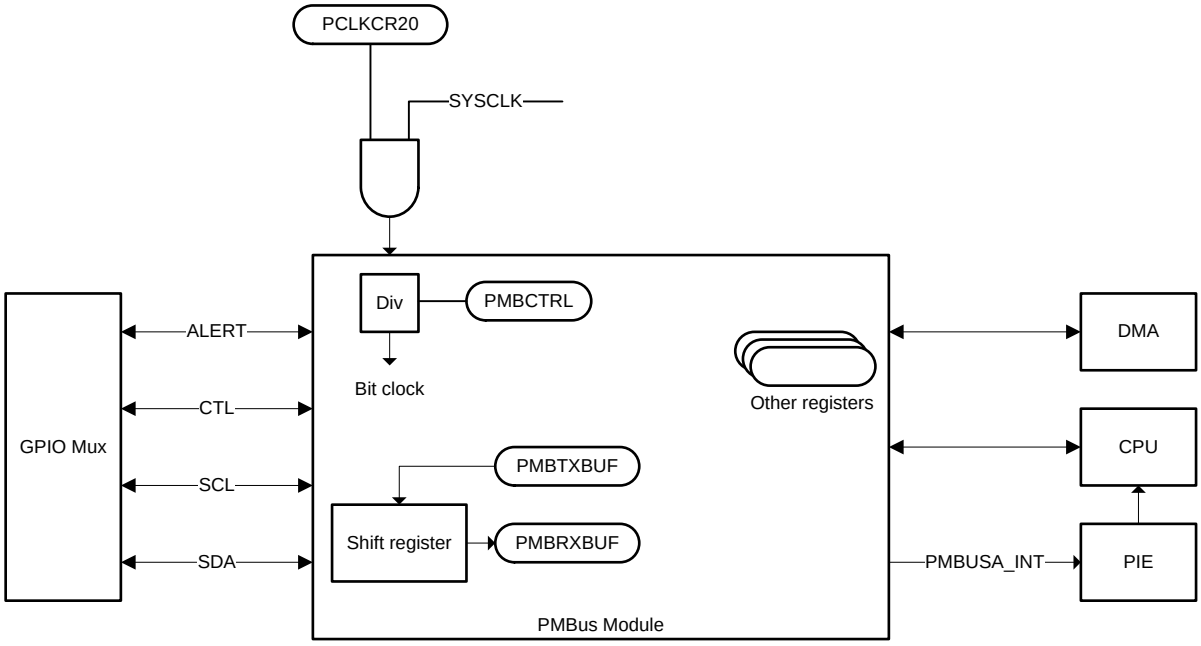



**Figure 5-71. PMBus Block Diagram**


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#### 5.12.3.1 PMBus Electrical Data and Timing

Table 5-69 lists the PMBus electrical characteristics. Table 5-70 lists the PMBUS fast mode switching characteristics. Table 5-71 lists the PMBUS standard mode switching characteristics.

**Table 5-69. PMBus Electrical Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Valid low-level input voltage | | | | 0.8 | V |
| $V_{IH}$ | Valid high-level input voltage | | 2.1 | | VDDIO | V |
| $V_{OL}$ | Low-level output voltage | At $I_{pullup}$ = 4 mA | | | 0.4 | V |
| $I_{OL}$ | Low-level output current | $V_{OL}$ ≤ 0.4 V | 4 | | | mA |
| $t_{SP}$ | Pulse width of spikes that must be suppressed by the input filter | | 0 | | 50 | ns |
| $I_i$ | Input leakage current on each pin | 0.1 Vbus < Vi < 0.9 Vbus | –10 | | 10 | µA |
| $C_i$ | Capacitance on each pin | | | | 10 | pF |

**Table 5-70. PMBus Fast Mode Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | 10 | | 400 | kHz |
| $t_{BUF}$ | Bus free time between STOP and START conditions | | 1.3 | | | µs |
| $t_{HD;STA}$ | START condition hold time -- SDA fall to SCL fall delay | | 0.6 | | | µs |
| $t_{SU;STA}$ | Repeated START setup time -- SCL rise to SDA fall delay | | 0.6 | | | µs |
| $t_{SU;STO}$ | STOP condition setup time -- SCL rise to SDA rise delay | | 0.6 | | | µs |
| $t_{HD;DAT}$ | Data hold time after SCL fall | | 300 | | | ns |
| $t_{SU;DAT}$ | Data setup time before SCL rise | | 100 | | | ns |
| $t_{Timeout}$ | Clock low time-out | | 25 | | 35 | ms |
| $t_{LOW}$ | Low period of the SCL clock | | 1.3 | | | µs |
| $t_{HIGH}$ | High period of the SCL clock | | 0.6 | | 50 | µs |
| $t_{LOW;SEXT}$ | Cumulative clock low extend time (slave device) | From START to STOP | | | 25 | ms |
| $t_{LOW;MEXT}$ | Cumulative clock low extend time (master device) | Within each byte | | | 10 | ms |
| $t_r$ | Rise time of SDA and SCL | 5% to 95% | 20 | | 300 | ns |
| $t_f$ | Fall time of SDA and SCL | 95% to 5% | 20 | | 300 | ns |

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**Table 5-71. PMBus Standard Mode Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | 10 | | 100 | kHz |
| $t_{BUF}$ | Bus free time between STOP and START conditions | | 4.7 | | | µs |
| $t_{HD;STA}$ | START condition hold time -- SDA fall to SCL fall delay | | 4 | | | µs |
| $t_{SU;STA}$ | Repeated START setup time -- SCL rise to SDA fall delay | | 4.7 | | | µs |
| $t_{SU;STO}$ | STOP condition setup time -- SCL rise to SDA rise delay | | 4 | | | µs |
| $t_{HD;DAT}$ | Data hold time after SCL fall | | 300 | | | ns |
| $t_{SU;DAT}$ | Data setup time before SCL rise | | 250 | | | ns |
| $t_{Timeout}$ | Clock low time-out | | 25 | | 35 | ms |
| $t_{LOW}$ | Low period of the SCL clock | | 4.7 | | | µs |
| $t_{HIGH}$ | High period of the SCL clock | | 4 | | 50 | µs |
| $t_{LOW;SEXT}$ | Cumulative clock low extend time (slave device) | From START to STOP | | | 25 | ms |
| $t_{LOW;MEXT}$ | Cumulative clock low extend time (master device) | Within each byte | | | 10 | ms |
| $t_r$ | Rise time of SDA and SCL | | | | 1000 | ns |
| $t_f$ | Fall time of SDA and SCL | | | | 300 | ns |


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### 5.12.4 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

    **NOTE:** Both pins can be used as GPIO if not used for SCI.
  - Baud rate programmable to 64K different rates
- Data-word format
  - 1 start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

**NOTE**

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

Figure 5-72 shows the SCI block diagram.

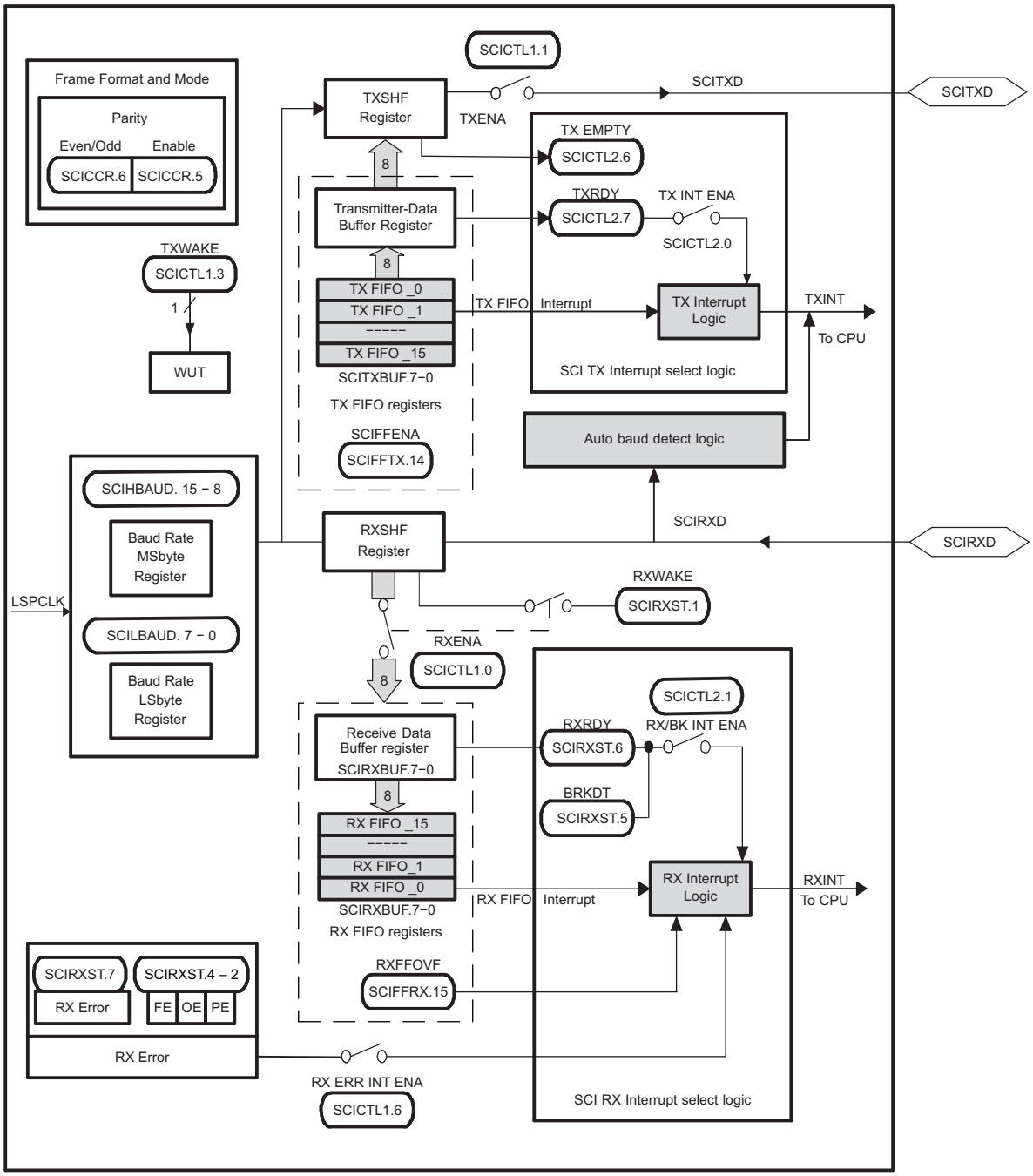



**Figure 5-72. SCI Block Diagram**


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### 5.12.5 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input and output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the MCU controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multidevice communications are supported by the master or slave operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin

**NOTE**

All four pins can be used as GPIO, if the SPI module is not used.

- Two operational modes: Master and Slave
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins.
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithm
- 16-level transmit/receive FIFO
- DMA support
- High-speed mode
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPISTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules

Figure 5-73 shows the SPI CPU interfaces.

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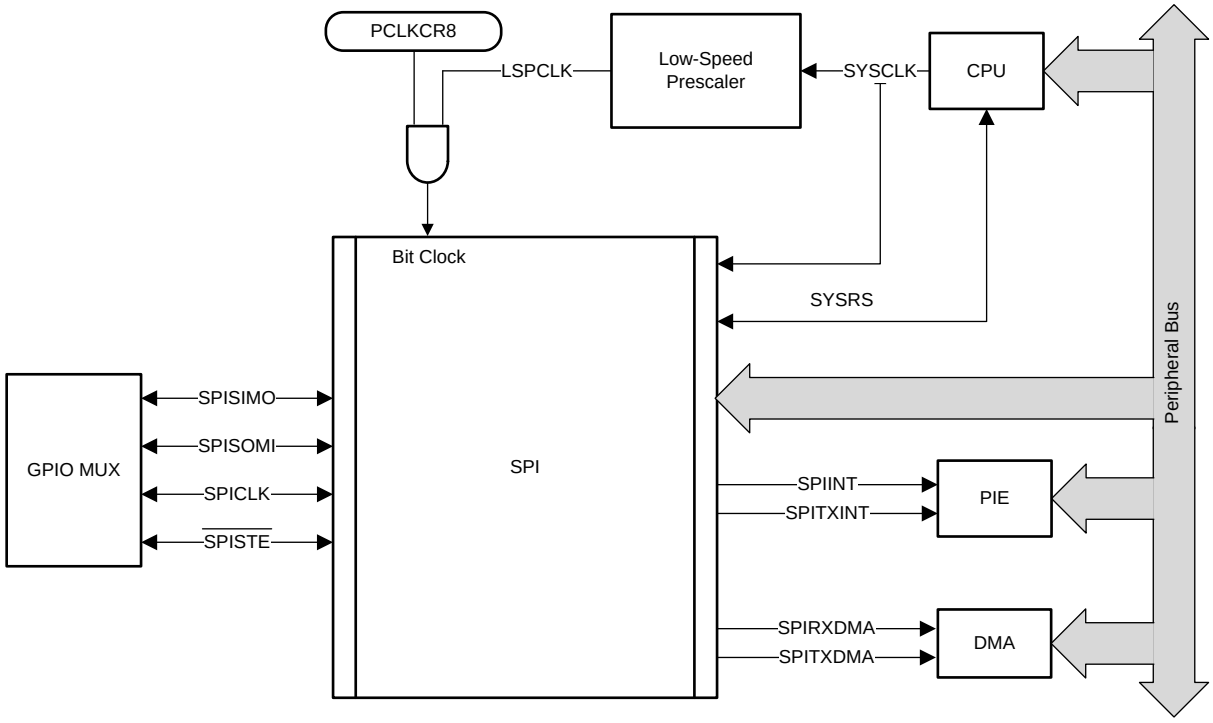



**Figure 5-73. SPI CPU Interface**


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#### 5.12.5.1 SPI Electrical Data and Timing

The following sections contain the SPI External Timings in Non-High-Speed Mode:

Section 5.12.5.1.1 Non-High-Speed Master Mode Timings
Section 5.12.5.1.2 Non-High-Speed Slave Mode Timings

The following sections contain the SPI External Timings in High-Speed Mode:

Section 5.12.5.1.3 High-Speed Master Mode Timings
Section 5.12.5.1.4 High-Speed Slave Mode Timings

**NOTE**

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPISIMO, and SPISOMI.

For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

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#### 5.12.5.1.1 Non-High-Speed Master Mode Timings

Table 5-72 lists the SPI master mode switching characteristics where the clock phase = 0. Figure 5-74 shows the SPI master mode external timing where the clock phase = 0.

Table 5-73 lists the SPI master mode switching characteristics where the clock phase = 1. Figure 5-75 shows the SPI master mode external timing where the clock phase = 1.

Table 5-74 lists the SPI master mode timing requirements.

**Table 5-72. SPI Master Mode Switching Characteristics (Clock Phase = 0)**

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | (BRR + 1) CONDITION(1) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPC1)M}$ | Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 3$ | |
| 3 | $t_{w(SPC2)M}$ | Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$ | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPICLK to SPISIMO valid | Even, Odd | | 5 | ns |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 6$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| 23 | $t_{d(SPC)M}$ | Delay time, $\overline{\text{SPISTE}}$ valid to SPICLK | Even | $0.5t_{c(SPC)M} - 6$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| 24 | $t_{d(STE)M}$ | Delay time, SPICLK to $\overline{\text{SPISTE}}$ invalid | Even | $0.5t_{c(SPC)M} - 6$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.


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### Table 5-73. SPI Master Mode Switching Characteristics (Clock Phase = 1)

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | (BRR + 1) CONDITION(1) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPC1)M}$ | Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$ | |
| 3 | $t_{w(SPC2)M}$ | Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 3$ | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPISIMO valid to SPICLK | Even | $0.5t_{c(SPC)M} - 4$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ | | |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 6$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |
| 23 | $t_{d(SPC)M}$ | Delay time, $\overline{\text{SPISTE}}$ valid to SPICLK | Even, Odd | $t_{c(SPC)M} - 3$ | | ns |
| 24 | $t_{d(STE)M}$ | Delay time, SPICLK to $\overline{\text{SPISTE}}$ invalid | Even | $0.5t_{c(SPC)M} - 6$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |

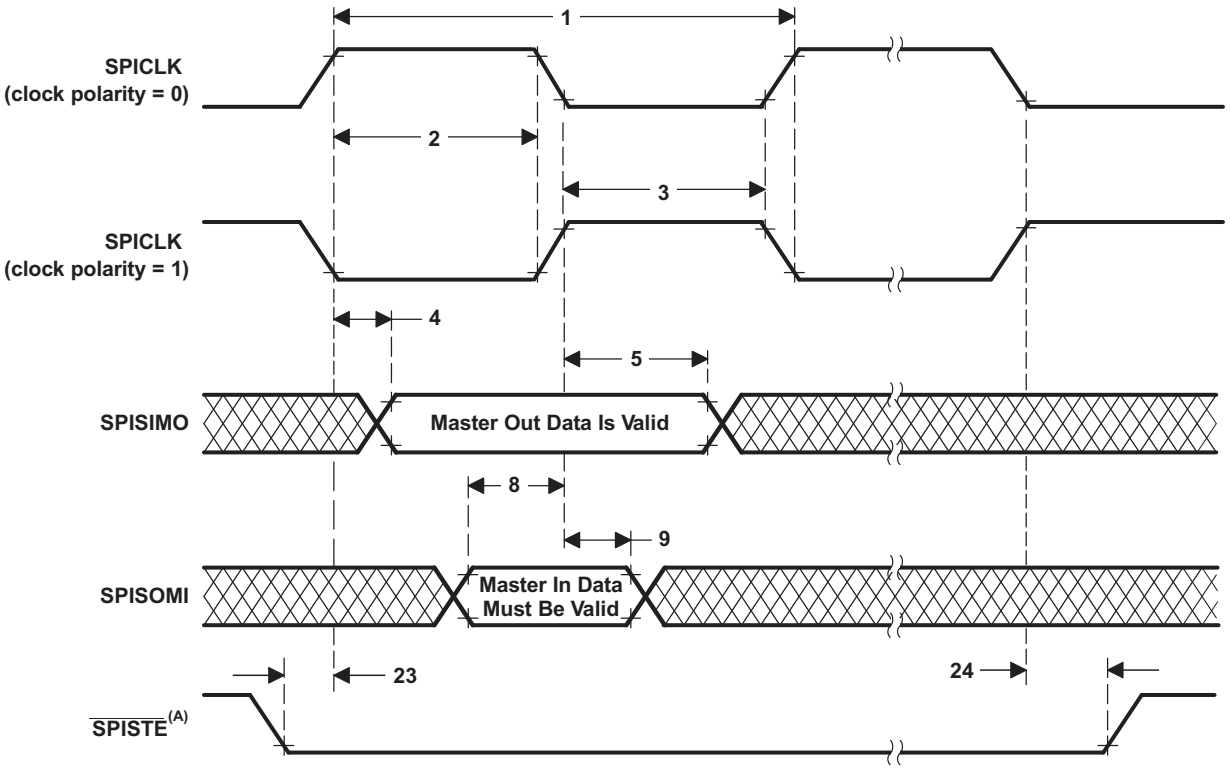
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

### Table 5-74. SPI Master Mode Timing Requirements

| NO. | | | (BRR + 1) CONDITION(1) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 8 | $t_{su(SOMI)M}$ | Setup time, SPISOMI valid before SPICLK | Even, Odd | 20 | | ns |
| 9 | $t_{h(SOMI)M}$ | Hold time, SPISOMI valid after SPICLK | Even, Odd | 0 | | ns |

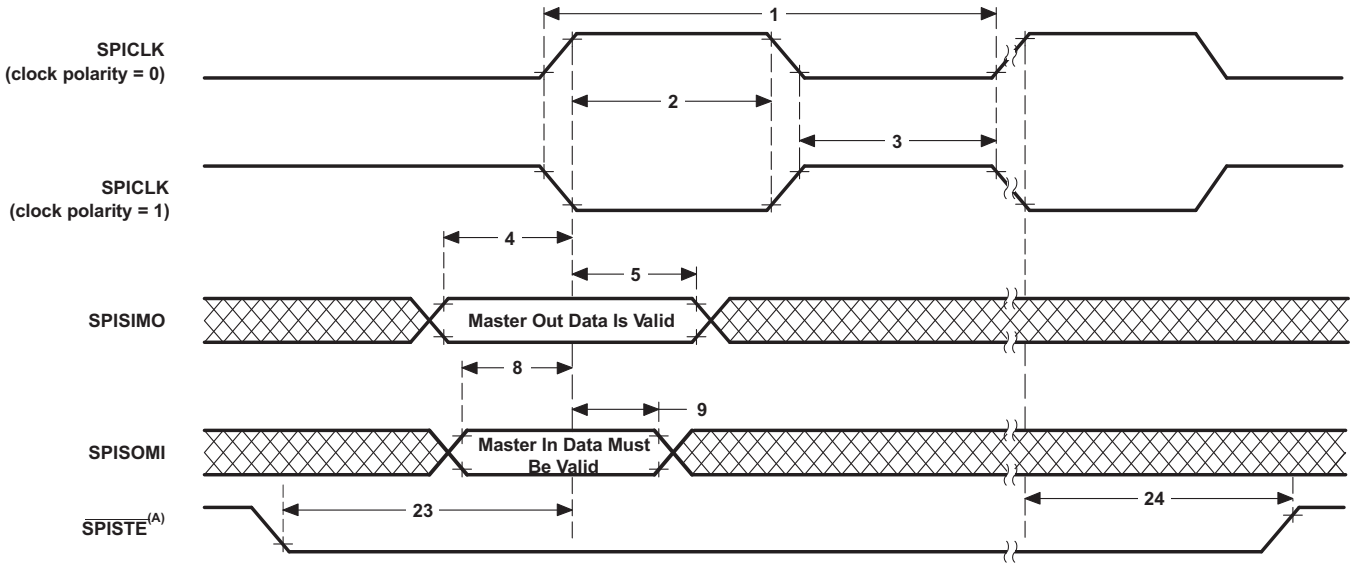
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

**Figure 5-74. SPI Master Mode External Timing (Clock Phase = 0)**




A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

**Figure 5-75. SPI Master Mode External Timing (Clock Phase = 1)**


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#### 5.12.5.1.2 Non-High-Speed Slave Mode Timings

Table 5-75 lists the SPI slave mode switching characteristics. Table 5-76 lists the SPI slave mode timing requirements.

Figure 5-76 shows the SPI slave mode external timing where the clock phase = 0. Figure 5-77 shows the SPI slave mode external timing where the clock phase = 1.

**Table 5-75. SPI Slave Mode Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 15 | $t_{d(SOMI)S}$ | Delay time, SPICLK to SPISOMI valid | | 16 | ns |
| 16 | $t_{v(SOMI)S}$ | Valid time, SPISOMI valid after SPICLK | 0 | | ns |

**Table 5-76. SPI Slave Mode Timing Requirements**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 12 | $t_{c(SPC)S}$ | Cycle time, SPICLK | $4t_{c(SYSCLK)}$ | | ns |
| 13 | $t_{w(SPC1)S}$ | Pulse duration, SPICLK, first pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 14 | $t_{w(SPC2)S}$ | Pulse duration, SPICLK, second pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 19 | $t_{su(SIMO)S}$ | Setup time, SPISIMO valid before SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 20 | $t_{h(SIMO)S}$ | Hold time, SPISIMO valid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 25 | $t_{su(STE)S}$ | Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 26 | $t_{h(STE)S}$ | Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |

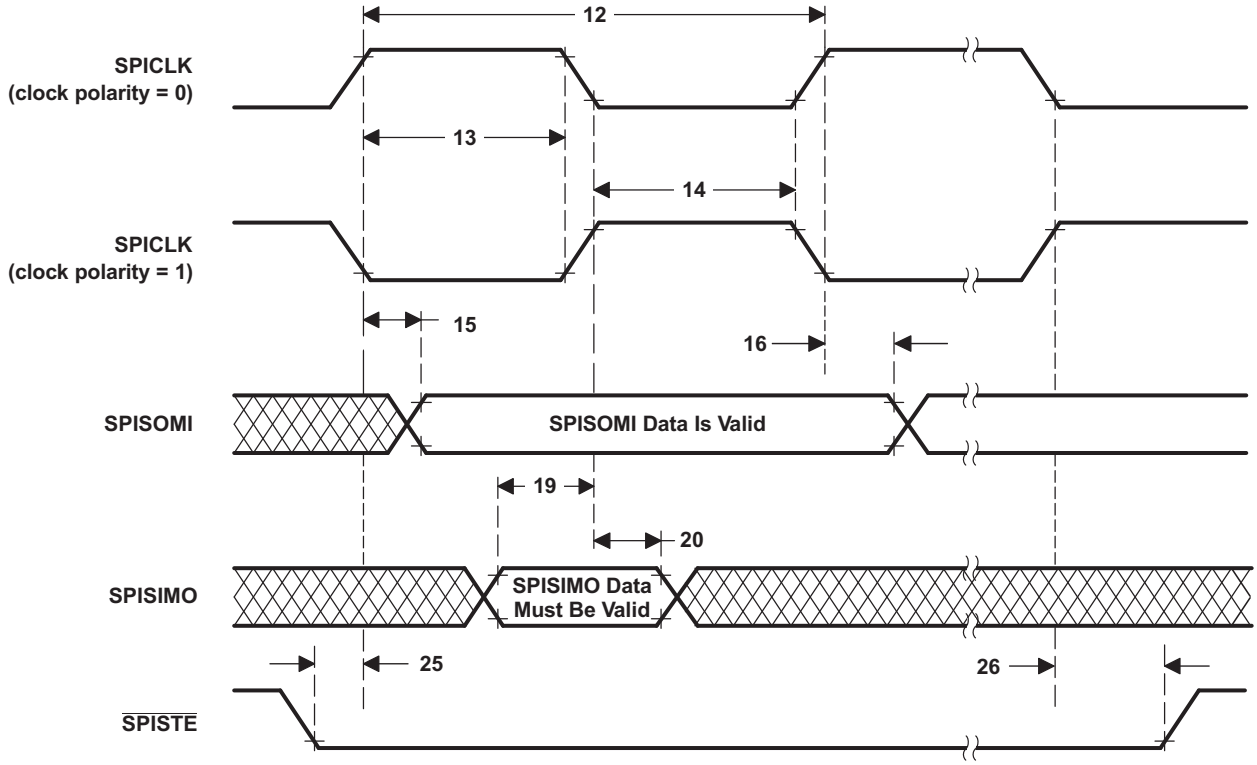



**Figure 5-76. SPI Slave Mode External Timing (Clock Phase = 0)**

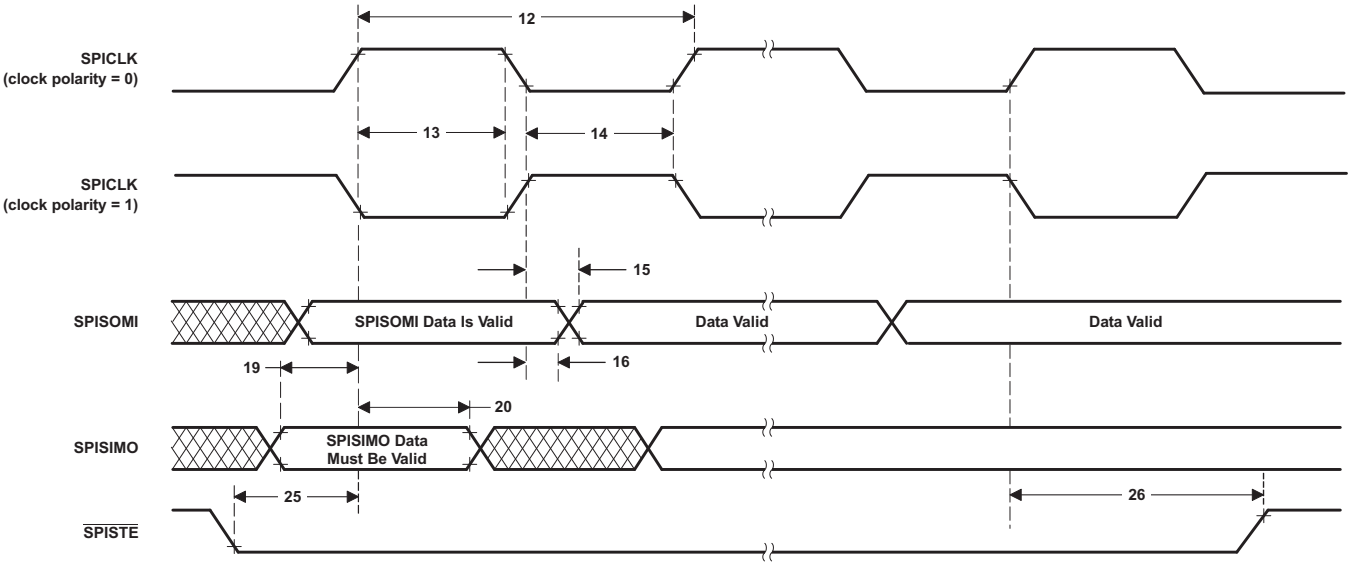



**Figure 5-77. SPI Slave Mode External Timing (Clock Phase = 1)**


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#### 5.12.5.1.3 High-Speed Master Mode Timings

Table 5-77 lists the SPI high-speed master mode switching characteristics where the clock phase = 0. Figure 5-78 shows the high-speed SPI master mode external timing where the clock phase = 0.

Table 5-78 lists the SPI high-speed master mode switching characteristics where the clock phase = 1. Figure 5-79 shows the high-speed SPI master mode external timing where the clock phase = 1.

Table 5-79 lists the SPI high-speed master mode timing requirements.

**Table 5-77. SPI High-Speed Master Mode Switching Characteristics (Clock Phase = 0)**

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | (BRR + 1) CONDITION(1) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPC1)M}$ | Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$ | |
| 3 | $t_{w(SPC2)M}$ | Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$ | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPICLK to SPISIMO valid | Even, Odd | | 3 | ns |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 4$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |
| 23 | $t_{d(SPC)M}$ | Delay time, $\overline{\text{SPISTE}}$ valid to SPICLK | Even | $0.5t_{c(SPC)M} - 4$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |
| 24 | $t_{d(STE)M}$ | Delay time, SPICLK to $\overline{\text{SPISTE}}$ invalid | Even | $0.5t_{c(SPC)M} - 4$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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### Table 5-78. SPI High-Speed Master Mode Switching Characteristics (Clock Phase = 1)

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | (BRR + 1) CONDITION(1) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPCH)M}$ | Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$ | |
| 3 | $t_{w(SPC2)M}$ | Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 3$ | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPISIMO valid to SPICLK | Even | $0.5t_{c(SPC)M} - 4$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ | | |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 6$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |
| 23 | $t_{d(SPC)M}$ | Delay time, $\overline{\text{SPISTE}}$ valid to SPICLK | Even, Odd | $t_{c(SPC)M} - 3$ | | ns |
| 24 | $t_{d(STE)M}$ | Delay time, SPICLK to $\overline{\text{SPISTE}}$ invalid | Even | $0.5t_{c(SPC)M} - 6$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | | |

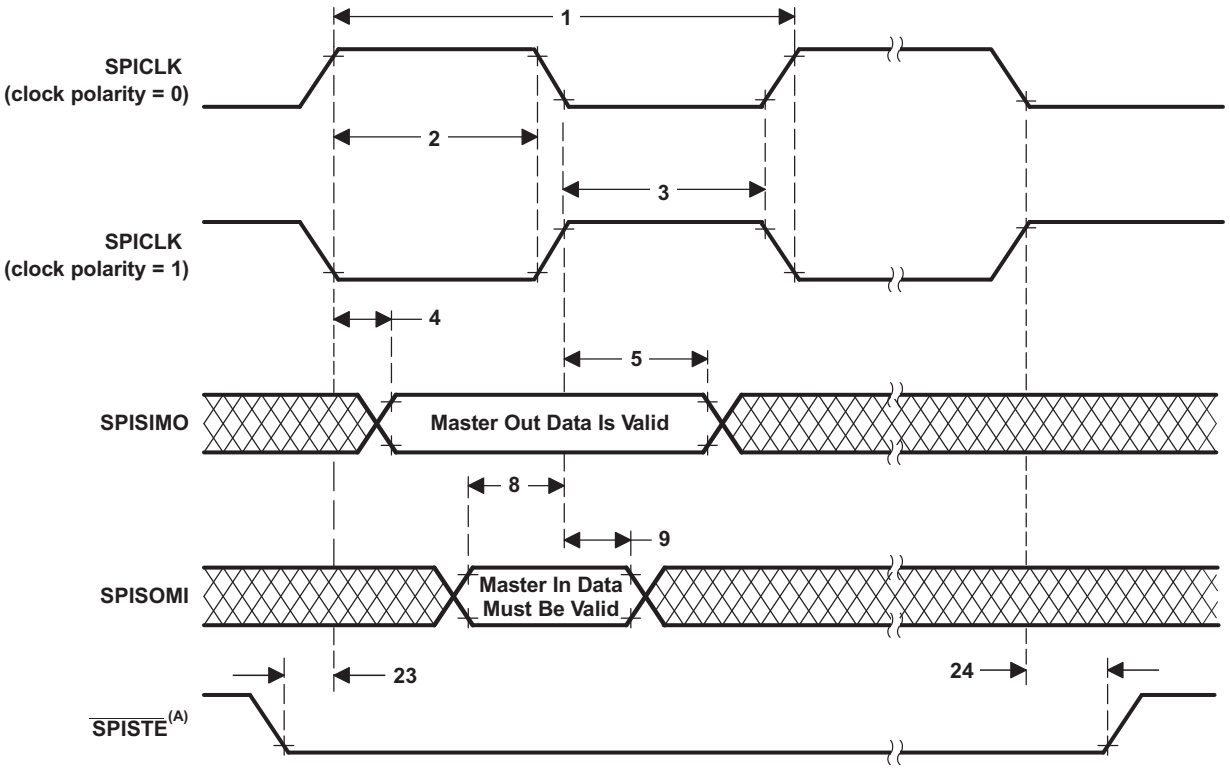
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

### Table 5-79. SPI High-Speed Master Mode Timing Requirements

| NO. | | | (BRR + 1) CONDITION(1) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 8 | $t_{su(SOMI)M}$ | Setup time, SPISOMI valid before SPICLK | Even, Odd | 2 | | ns |
| 9 | $t_{h(SOMI)M}$ | Hold time, SPISOMI valid after SPICLK | Even, Odd | 11 | | ns |

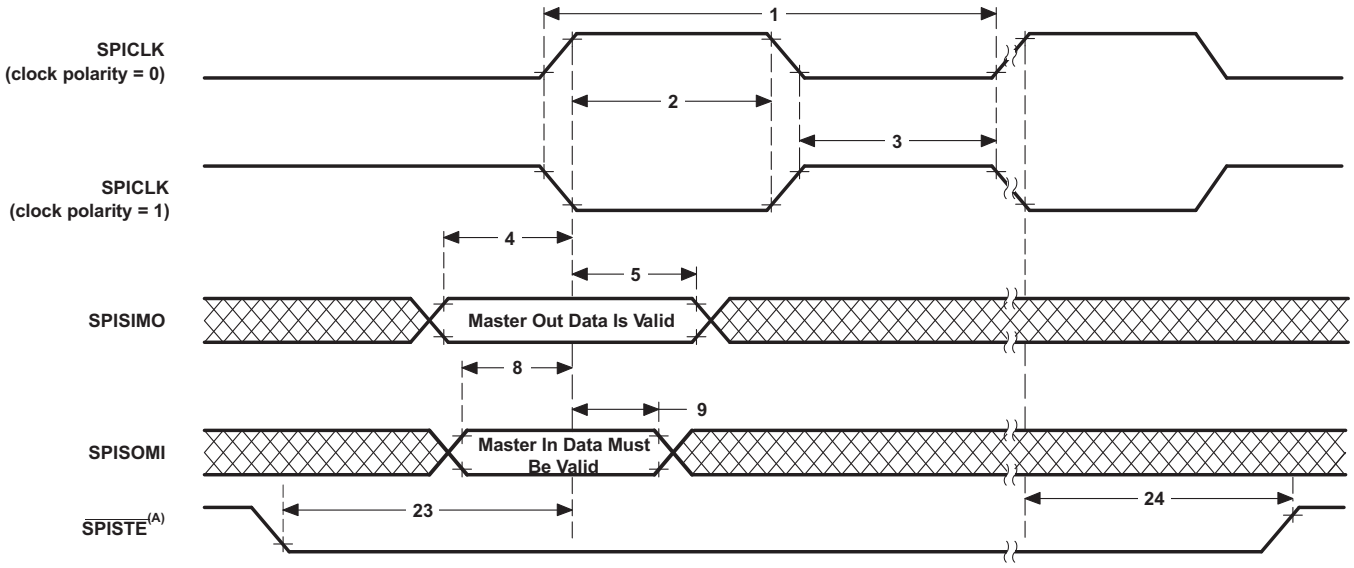
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.


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A. On the trailing end of the word, SPISTE will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

**Figure 5-78. High-Speed SPI Master Mode External Timing (Clock Phase = 0)**




A. On the trailing end of the word, SPISTE will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

**Figure 5-79. High-Speed SPI Master Mode External Timing (Clock Phase = 1)**

#### 5.12.5.1.4 High-Speed Slave Mode Timings

Table 5-80 lists the SPI high-speed slave mode switching characteristics. Table 5-81 lists the SPI high-speed slave mode timing requirements.

Figure 5-80 shows the high-speed SPI slave mode external timing where the clock phase = 0. Figure 5-81 shows the high-speed SPI slave mode external timing where the clock phase = 1.

**Table 5-80. SPI High-Speed Slave Mode Switching Characteristics**

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 15 | $t_{d(SOMI)S}$ | Delay time, SPICLK to SPISOMI valid | | 14 | ns |
| 16 | $t_{v(SOMI)S}$ | Valid time, SPISOMI valid after SPICLK | 0 | | ns |

**Table 5-81. SPI High-Speed Slave Mode Timing Requirements**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 12 | $t_{c(SPC)S}$ | Cycle time, SPICLK | $4t_{c(SYSCLK)}$ | | ns |
| 13 | $t_{w(SPC1)S}$ | Pulse duration, SPICLK, first pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 14 | $t_{w(SPC2)S}$ | Pulse duration, SPICLK, second pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 19 | $t_{su(SIMO)S}$ | Setup time, SPISIMO valid before SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 20 | $t_{h(SIMO)S}$ | Hold time, SPISIMO valid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 25 | $t_{su(STE)S}$ | Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 26 | $t_{h(STE)S}$ | Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |

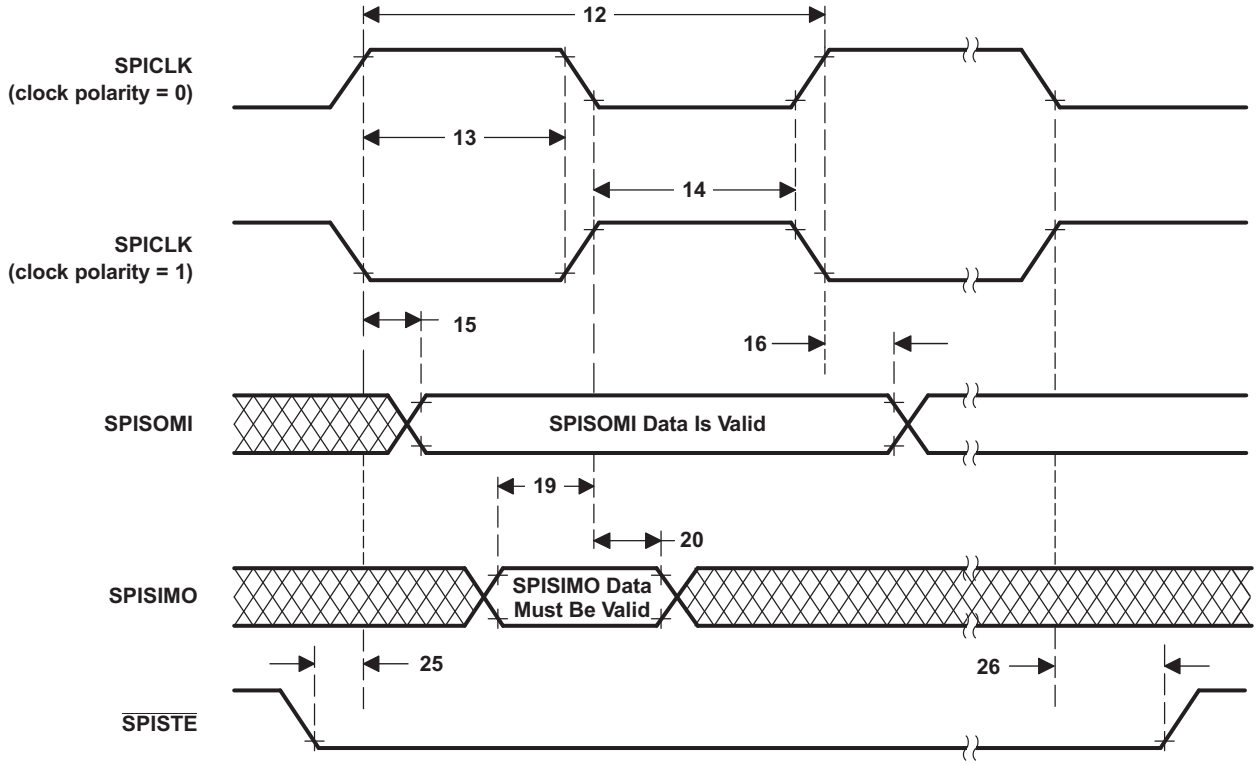



**Figure 5-80. High-Speed SPI Slave Mode External Timing (Clock Phase = 0)**


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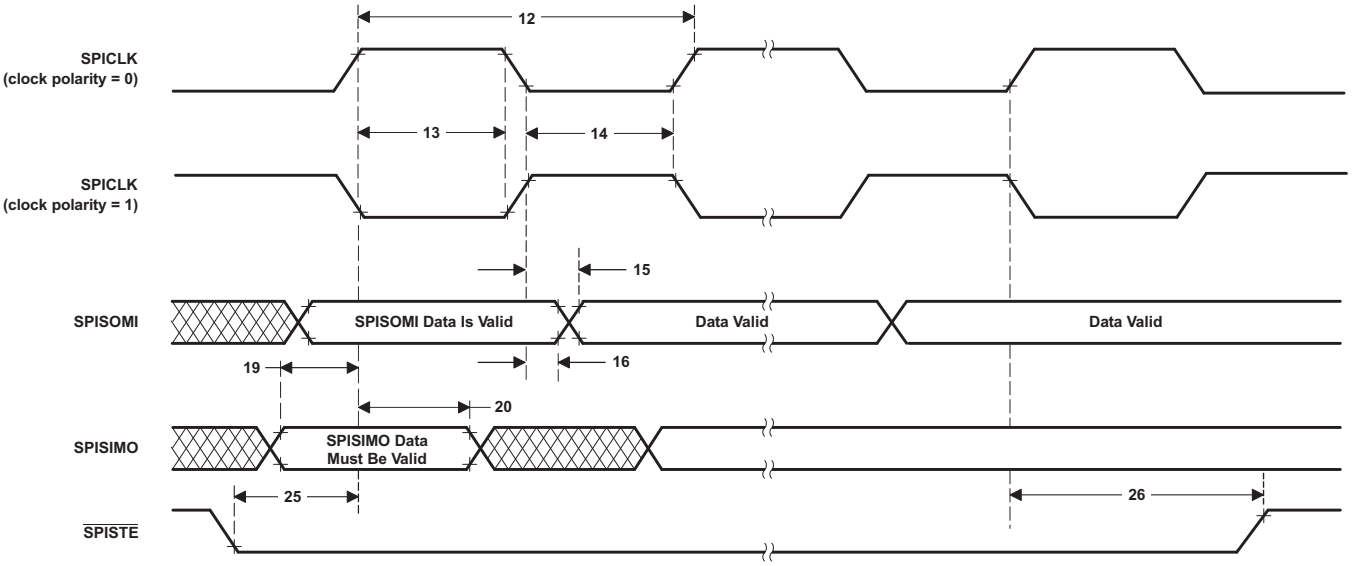



**Figure 5-81. High-Speed SPI Slave Mode External Timing (Clock Phase = 1)**

### 5.12.6 Local Interconnect Network (LIN)

This device contains one Local Interconnect Network (LIN) module. The LIN module adheres to the LIN 2.1 standard as defined by the *LIN Specification Package Revision 2.1*. The LIN is a low-cost serial interface designed for applications where the CAN protocol may be too expensive to implement, such as small subnetworks for cabin comfort functions like interior lighting or window control in an automotive application.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master and multiple-slave with a message identification for multicast transmission between any network nodes.

The LIN module can be programmed to work either as an SCI or as a LIN as the core of the module is an SCI. The hardware features of the SCI are augmented to achieve LIN compatibility. The SCI module is a universal asynchronous receiver-transmitter (UART) that implements the standard non-return-to-zero format.

Though the registers are common for LIN and SCI, the register descriptions have notes to identify the register/bit usage in different modes. Because of this, code written for this module cannot be directly ported to the stand-alone SCI module and vice versa.

The LIN module has the following features:

- Compatibility with LIN 1.3, 2.0 and 2.1 protocols
- Configurable baud rate up to 20 kbps (as per LIN 2.1 protocol)
- Two external pins: LINRX and LINTX
- Multibuffered receive and transmit units
- Identification masks for message filtering
- Automatic master header generation
  - Programmable synchronization break field
  - Synchronization field
  - Identifier field
- Slave automatic synchronization
  - Synchronization break detection
  - Optional baud rate update
  - Synchronization validation
- $2^{31}$ programmable transmission rates with 7 fractional bits
- Wakeup on LINRX dominant level from transceiver
- Automatic wakeup support
  - Wakeup signal generation
  - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
  - Bit error
  - Bus error
  - No-response error
  - Checksum error
  - Synchronization field error
  - Parity error
- Capability to use direct memory access (DMA) for transmit and receive data


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- Two interrupt lines with priority encoding for:
  - Receive
  - Transmit
  - ID, error, and status
- Support for LIN 2.0 checksum
- Enhanced synchronizer finite state machine (FSM) support for frame processing
- Enhanced handling of extended frames
- Enhanced baud rate generator
- Update wakeup/go to sleep

Figure 5-82 shows the LIN block diagram.

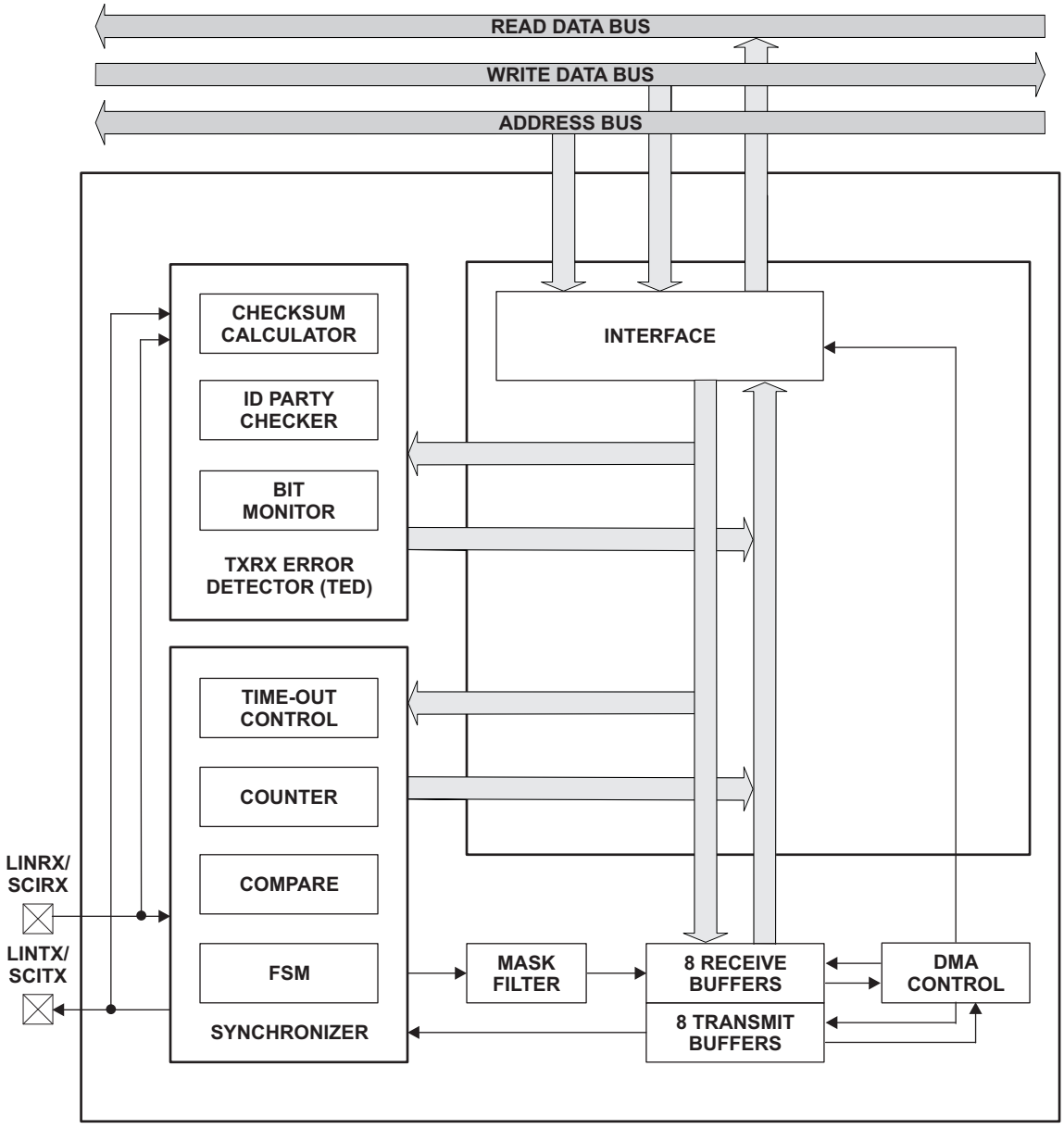



**Figure 5-82. LIN Block Diagram**

### 5.12.7 Fast Serial Interface (FSI)

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable and robust high-speed communications. The FSI is designed to ensure data robustness across many system conditions such as chip-to-chip as well as board-to-board across an isolation barrier. Payload integrity checks such as CRC, start- and end-of-frame patterns, and user-defined tags, are encoded before transmit and then verified after receipt without additional CPU interaction. Line breaks can be detected using periodic transmissions, all managed and monitored by hardware. The FSI is also tightly integrated with other control peripherals on the device. To ensure that the latest sensor data or control parameters are available, frames can be transmitted on every control loop period. An integrated skew-compensation block has been added on the receiver to handle skew that may occur between the clock and data signals due to a variety of factors, including trace-length mismatch and skews induced by an isolation chip. With embedded data robustness checks, data-link integrity checks, skew compensation, and integration with control peripherals, the FSI can enable high-speed, robust communication in any system. These and many other features of the FSI follow.

The FSI module includes the following features:

- Independent transmitter and receiver cores
- Source-synchronous transmission
- Dual data rate (DDR)
- One or two data lines
- Programmable data length
- Skew adjustment block to compensate for board and system delay mismatches
- Frame error detection
- Programmable frame tagging for message filtering
- Hardware ping to detect line breaks during communication (ping watchdog)
- Two interrupts per FSI core
- Externally triggered frame generation
- Hardware- or software-calculated CRC
- Embedded ECC computation module
- Register write protection
- DMA support
- CLA task triggering
- SPI compatibility mode (limited features available)

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently. The features available on the FSITX and FSIRX are described in Section 5.12.7.1 and Section 5.12.7.2, respectively.

#### 5.12.7.1 FSI Transmitter

The FSI transmitter module handles the framing of data, CRC generation, signal generation of TXCLK, TXD0, and TXD1, as well as interrupt generation. The operation of the transmitter core is controlled and configured through programmable control registers. The transmitter control registers let the CPU (or the CLA) program, control, and monitor the operation of the FSI transmitter. The transmit data buffer is accessible by the CPU, CLA, and the DMA.

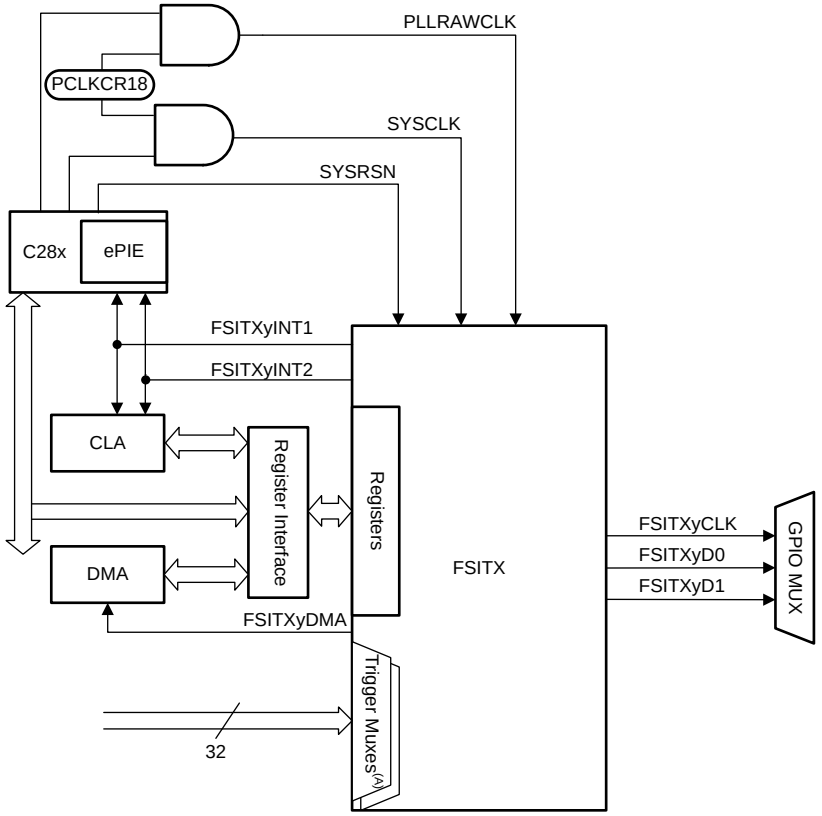
The transmitter has the following features:

- Automated ping frame generation
- Externally triggered ping frames
- Externally triggered data frames
- Software-configurable frame lengths
- 16-word data buffer


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- Data buffer underrun and overrun detection
- Hardware-generated CRC on data bits
- Software ECC calculation on select data
- DMA support
- CLA task triggering

Figure 5-83 shows the FSITX CPU interface. Figure 5-84 shows the high-level block diagram of the FSITX. Not all data paths and internal connections are shown. This diagram provides a high-level overview of the internal modules present in the FSITX.




A. The signals connected to the trigger muxes are described in the External Frame Trigger Mux section of the Fast Serial Interface (FSI) chapter in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

**Figure 5-83. FSITX CPU Interface**

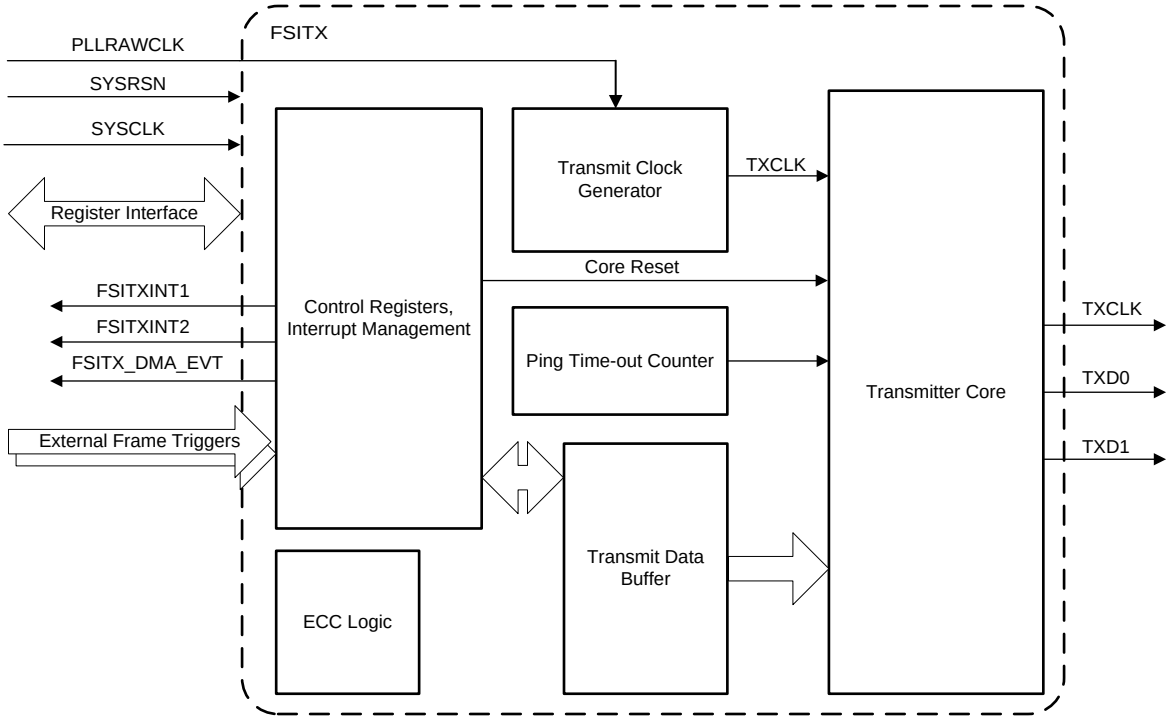



**Figure 5-84. FSITX Block Diagram**


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#### 5.12.7.1.1 FSITX Electrical Data and Timing

FSITX signals must be used in sets as shown in Table 5-82. For example, GPIO10 (CLK), GPIO9 (D0), and GPIO8 (D1) from SET 2 must all be used together to ensure the timings from Table 5-83 are met.

**Table 5-82. FSITX GPIO Mux Groups**

| FSI SIGNAL | GPIO MUX SET | | | |
|---|---|---|---|---|
| | SET 1 | SET 2 | SET 3 | SET 4 |
| FSITXA_CLK | GPIO7 | GPIO10 | GPIO27 | GPIO44 |
| FSITXA_D0 | GPIO6 | GPIO9 | GPIO26 | GPIO45 |
| FSITXA_D1 | GPIO5 | GPIO8 | GPIO25 | GPIO46 |

Table 5-83 lists the FSITX switching characteristics. Figure 5-85 shows the FSITX timings.

**Table 5-83. FSITX Switching Characteristics**

over operating free-air temperature range (unless otherwise noted)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(TXCLK)}$ | Cycle time, TXCLK | 20 | | ns |
| 2 | $t_{w(TXCLK)}$ | Pulse width, TXCLK low or TXCLK high | $(0.5t_{c(TXCLK)}) - 1$ | $(0.5t_{c(TXCLK)}) + 1$ | ns |
| 3 | $t_{d(TXCLKL-TXD)}$ | Delay time, Data valid after TXCLK rising or falling | $(0.25t_{c(TXCLK)}) - 3.2$ | $(0.25t_{c(TXCLK)}) + 4.7$ | ns |

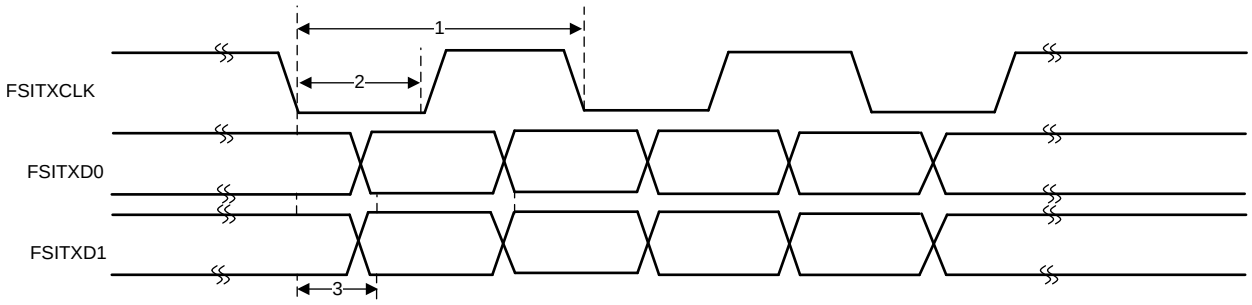



**Figure 5-85. FSITX Timings**

### 5.12.7.2 FSI Receiver

The receiver module interfaces to the FSI clock (RXCLK), and data lines (RXD0 and RXD1) after they pass through an optional programmable delay line. The receiver core handles the data framing, CRC computation, and frame-related error checking. The receiver bit clock and state machine are run by the RXCLK input, which is asynchronous to the device system clock.

The receiver control registers let the CPU (or the CLA) program, control, and monitor the operation of the FSIRX. The receive data buffer is accessible by the CPU, CLA, and the DMA.

The receiver core has the following features:

- 16-word data buffer
- Multiple supported frame types
- Ping frame watchdog
- Frame watchdog
- CRC calculation and comparison in hardware
- ECC detection
- Programmable delay line control on incoming signals
- DMA support
- CLA task triggering
- SPI compatibility mode

Figure 5-86 shows the FSIRX CPU interface. Figure 5-87 provides a high-level overview of the internal modules present in the FSIRX. Not all data paths and internal connections are shown.

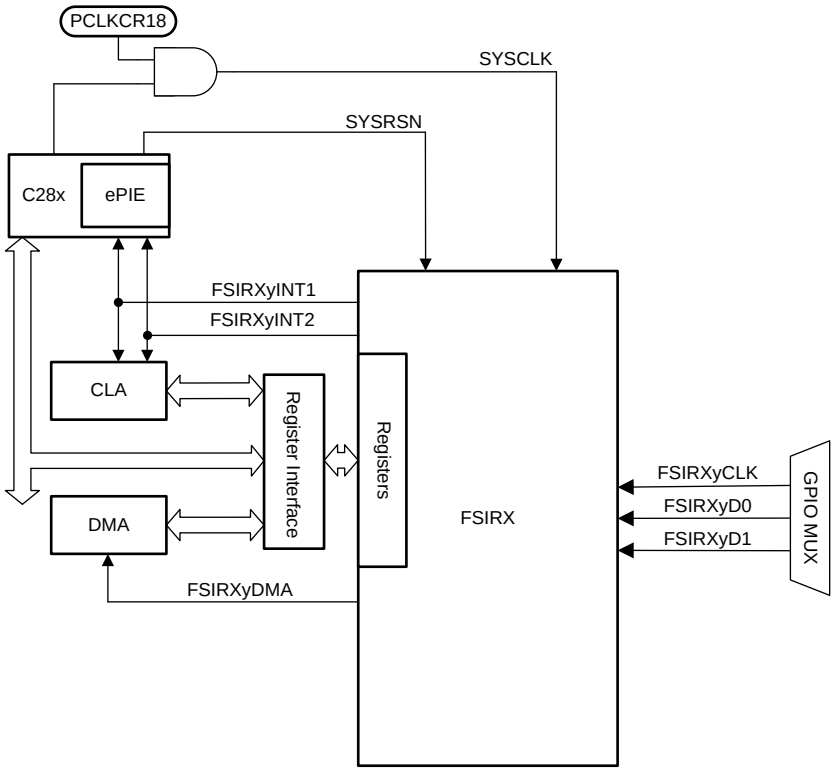



**Figure 5-86. FSIRX CPU Interface**


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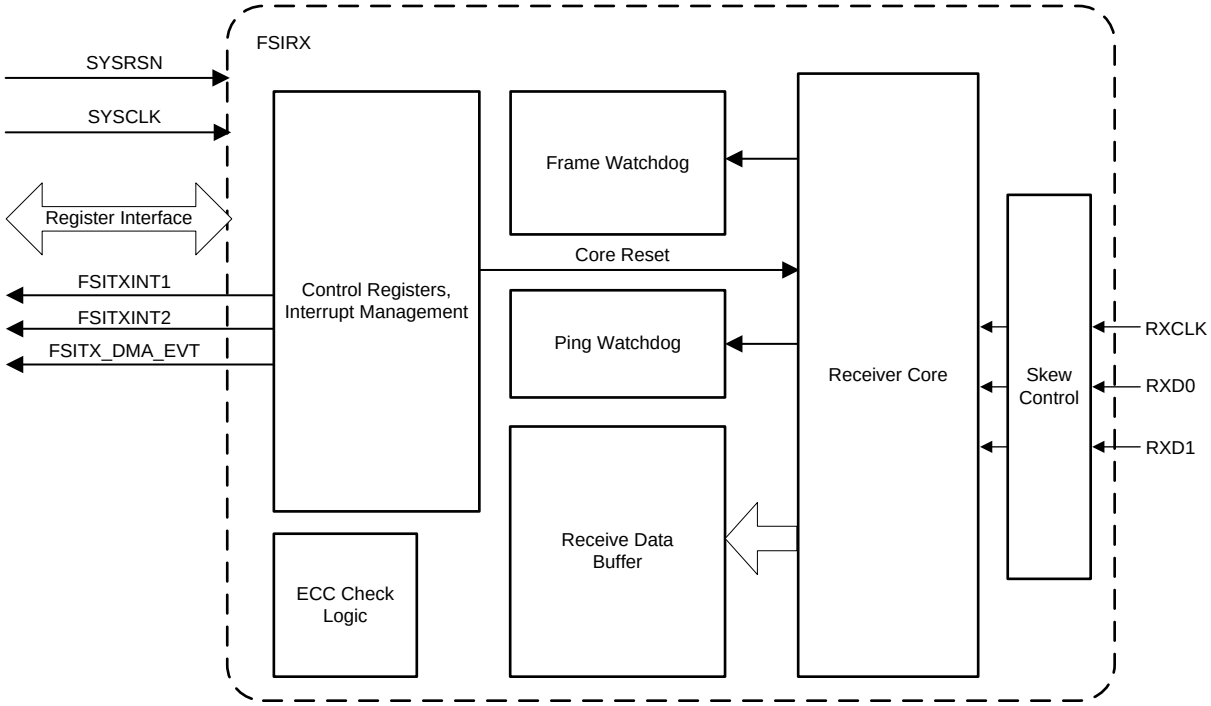



**Figure 5-87. FSIRX Block Diagram**

#### 5.12.7.2.1 FSIRX Electrical Data and Timing

Table 5-84 lists the FSIRX timing requirements. Figure 5-88 shows the FSIRX timings.

**Table 5-84. FSIRX Timing Requirements**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(RXCLK)}$ | Cycle time, RXCLK | 20 | | ns |
| 2 | $t_{w(RXCLK)}$ | Pulse width, RXCLK low or RXCLK high | $(0.5t_{c(RXCLK)}) - 1$ | $(0.5t_{c(RXCLK)}) + 1$ | ns |
| 3 | $t_{su(RXCLK–RXD)}$ | Setup time with respect to RXCLK, applies to both edges of the clock | 1.7 | | ns |
| 4 | $t_{h(RXCLK–RXD)}$ | Hold time with respect to RXCLK, applies to both edges of the clock | 3.8 | | ns |

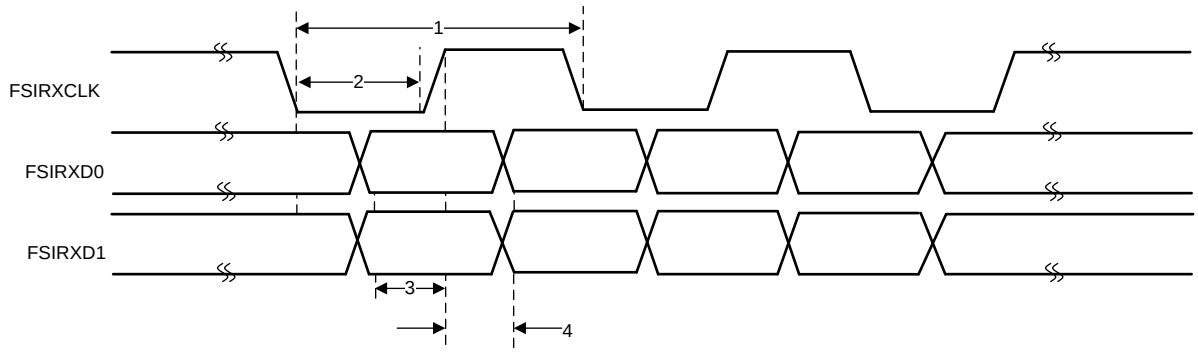



**Figure 5-88. FSIRX Timings**


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#### 5.12.7.3 FSI SPI Compatibility Mode

The FSI supports a SPI compatibility mode to enable communication with programmable SPI devices. In this mode, the FSI transmits its data in the same manner as a SPI in a single clock configuration mode. While the FSI is able to physically interface with a SPI in this mode, the external device must be able to encode and decode an FSI frame to communicate successfully. This is because the FSI transmits all SPI frame phases with the exception of the preamble and postamble. The FSI provides the same data validation and frame checking as if it was in standard FSI mode, allowing for more robust communication without consuming CPU cycles. The external SPI is required to send all relevant information and can access standard FSI features such as the ping frame watchdog on the FSIRX, frame tagging, or custom CRC values. The list of features of SPI compatibility mode follows:

- Data will transmit on rising edge and receive on falling edge of the clock.
- Only 16-bit word size is supported.
- TXD1 will be driven like an active-low chip-select signal. The signal will be low for the duration of the full frame transmission.
- No receiver chip-select input is required. RXD1 is not used. Data is shifted into the receiver on every active clock edge.
- No preamble or postamble clocks will be transmitted. All signals return to the idle state after the frame phase is finished.
- It is not possible to transmit in the SPI slave configuration because the FSI TXCLK cannot take an external clock source.

##### *5.12.7.3.1 FSITX SPI Mode Electrical Data and Timing*

Table 5-85 lists the FSITX SPI mode switching characteristics. Figure 5-89 shows the FSITX SPI mode timings. Special timings are not required for the FSIRX in SPI mode. FSIRX timings listed in Table 5-84 are applicable in SPI compatibility mode. Setup and Hold times are only valid on the falling edge of FSIRXCLK because this is the active edge in SPI mode.

**Table 5-85. FSITX SPI Mode Switching Characteristics**

over operating free-air temperature range (unless otherwise noted)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(TXCLK)}$ | Cycle time, TXCLK | 20 | | ns |
| 2 | $t_{w(TXCLK)}$ | Pulse width, TXCLK low or TXCLK high | $(0.5t_{c(TXCLK)}) - 1$ | $(0.5t_{c(TXCLK)}) + 1$ | ns |
| 3 | $t_{d(TXCLKH–TXD0)}$ | Delay time, Data valid after TXCLK high | | 3 | ns |
| 4 | $t_{d(TXD1-TXCLK)}$ | Delay time, TXCLK high after TXD1 low | $t_{w(TXCLK)} - 1$ | | ns |
| 5 | $t_{d(TXCLK-TXD1)}$ | Delay time, TXD1 high after TXCLK low | $t_{w(TXCLK)} - 1$ | | ns |

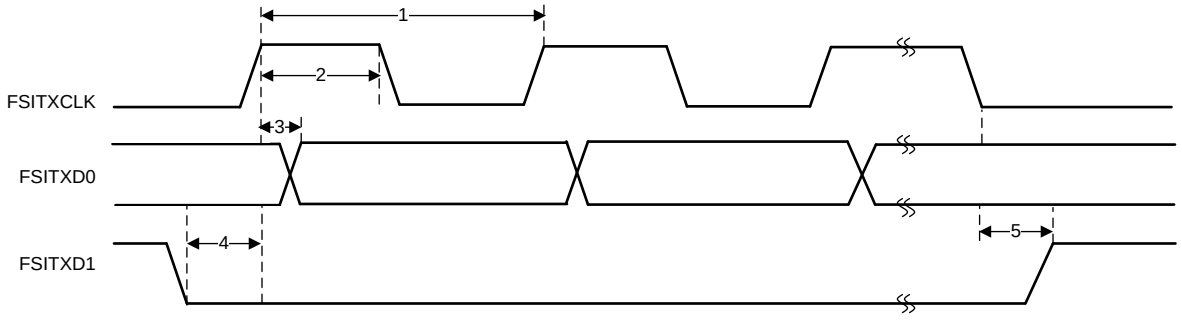



**Figure 5-89. FSITX SPI Mode Timings**

# 6 Detailed Description

## 6.1 Overview

The Piccolo™ TMS320F28004x (F28004x) is a powerful 32-bit floating-point microcontroller unit (MCU) that lets designers incorporate crucial control peripherals, differentiated analog, and nonvolatile memory on a single device.

The real-time control subsystem is based on TI's 32-bit C28x CPU, which provides 100 MHz of signal processing performance. The C28x CPU is further boosted by the new TMU extended instruction set, which enables fast execution of algorithms with trigonometric operations commonly found in transforms and torque loop calculations; and the VCU-I extended instruction set, which reduces the latency for complex math operations commonly found in encoded applications.

The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has its own dedicated memory resources and it can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching.

The F28004x supports up to 256KB (128KW) of flash memory divided into two 128KB (64KW) banks, which enables programming and execution in parallel. Up to 100KB (50KW) of on-chip SRAM is also available in blocks of 4KB (2KW) and 16KB (8KW) for efficient system partitioning. Flash ECC, SRAM ECC/parity, and dual-zone security are also supported.

High-performance analog blocks are integrated on the F28004x MCU to further enable system consolidation. Three separate 12-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. Seven PGAs on the analog front end enable on-chip voltage scaling before conversion. Seven analog comparator modules provide continuous monitoring of input voltage levels for trip conditions.

The TMS320C2000™ devices contain industry-leading control peripherals with frequency-independent ePWM/HRPWM and eCAP allow for a best-in-class level of control to the system. The built-in 4-channel SDFM allows for seamless integration of an oversampling sigma-delta modulator across an isolation barrier.

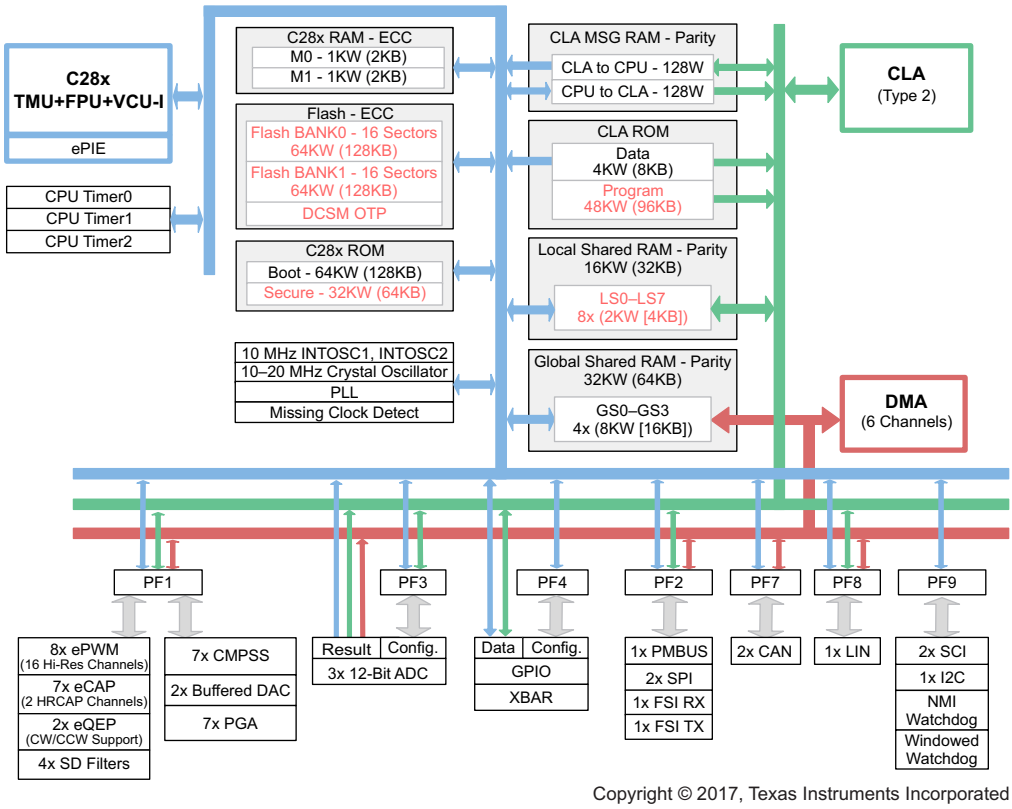
Connectivity is supported through various industry-standard communication ports (such as SPI, SCI, I2C, LIN, and CAN) and offers multiple muxing options for optimal signal placement in a variety of applications. New to the C2000™ platform is the fully compliant PMBus. Additionally, in an industry first, the FSI enables high-speed, robust communication to complement the rich set of peripherals that are embedded in the device.

A specially enabled device variant, TMS320F28004xC, allows access to the Configurable Logic Block (CLB) for additional interfacing features and allows access to the secure ROM, which includes a library to enable InstaSPIN-FOC™. See Device Comparison for more information.


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## 6.2 Functional Block Diagram

Figure 6-1 shows the CPU system and associated peripherals.




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**Figure 6-1. Functional Block Diagram**

## 6.3 Memory

### 6.3.1 C28x Memory Map

Table 6-1 describes the C28x memory map. Memories accessible by the CLA or DMA (direct memory access) are also noted. See the Memory Controller Module section of the System Control chapter in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

**Table 6-1. C28x Memory Map**

| MEMORY | SIZE | START ADDRESS | END ADDRESS | CLA ACCESS | DMA ACCESS | ECC-CAPABLE | PARITY | MEMORY ACCESS PROTECTION | SECURE |
|---|---|---|---|---|---|---|---|---|---|
| M0 RAM | 1K × 16 | 0x0000 0000 | 0x0000 03FF | | | Yes | | | |
| M1 RAM | 1K × 16 | 0x0000 0400 | 0x0000 07FF | | | Yes | | | |
| PieVectTable | 512 × 16 | 0x0000 0D00 | 0x0000 0EFF | | | | | | |
| CLA-to-CPU MSGRAM | 128 × 16 | 0x0000 1480 | 0x0000 14FF | Read/Write | | | Yes | | |
| CPU-to-CLA MSGRAM | 128 × 16 | 0x0000 1500 | 0x0000 157F | Read | | | Yes | | |
| LS0 RAM | 2K × 16 | 0x0000 8000 | 0x0000 87FF | Configurable | | | Yes | Yes | Yes |
| LS1 RAM | 2K × 16 | 0x0000 8800 | 0x0000 8FFF | Configurable | | | Yes | Yes | Yes |
| LS2 RAM | 2K × 16 | 0x0000 9000 | 0x0000 97FF | Configurable | | | Yes | Yes | Yes |
| LS3 RAM | 2K × 16 | 0x0000 9800 | 0x0000 9FFF | Configurable | | | Yes | Yes | Yes |
| LS4 RAM | 2K × 16 | 0x0000 A000 | 0x0000 A7FF | Configurable | | | Yes | Yes | Yes |
| LS5 RAM | 2K × 16 | 0x0000 A800 | 0x0000 AFFF | Configurable | | | Yes | Yes | Yes |
| LS6 RAM | 2K × 16 | 0x0000 B000 | 0x0000 B7FF | Configurable | | | Yes | Yes | Yes |
| LS7 RAM | 2K × 16 | 0x0000 B800 | 0x0000 BFFF | Configurable | | | Yes | Yes | Yes |
| GS0 RAM | 8K × 16 | 0x0000 C000 | 0x0000 DFFF | | Yes | | Yes | Yes | |
| GS1 RAM | 8K × 16 | 0x0000 E000 | 0x0000 FFFF | | Yes | | Yes | Yes | |
| GS2 RAM | 8K × 16 | 0x0001 0000 | 0x0001 1FFF | | Yes | | Yes | Yes | |
| GS3 RAM | 8K × 16 | 0x0001 2000 | 0x0001 3FFF | | Yes | | Yes | Yes | |
| CAN A Message RAM | 2K × 16 | 0x0004 9000 | 0x0004 97FF | | Yes | | | | |
| CAN B Message RAM | 2K × 16 | 0x0004 B000 | 0x0004 B7FF | | Yes | | | | |
| Flash Bank 0 | 64K × 16 | 0x0008 0000 | 0x0008 FFFF | | | Yes | | N/A | Yes |
| Flash Bank 1 | 64K × 16 | 0x0009 0000 | 0x0009 FFFF | | | Yes | | N/A | Yes |
| Secure ROM | 32K × 16 | 0x003E 8000 | 0x003E FFFF | | | | | | Yes |
| Boot ROM | 64K × 16 | 0x003F 0000 | 0x003F FFBF | | | | | | |
| Vectors | 64 × 16 | 0x003F FFC0 | 0x003F FFFF | | | | | | |
| CLA Data ROM | 4K × 16 | 0x0100 1000 | 0x0100 1FFF | Read | | | | | |
| CLA Program ROM | 48K × 16 | 0x0102 0000 | 0x0102 BFFF | Read | | | | | Yes |

### 6.3.2 Control Law Accelerator (CLA) ROM Memory Map

Table 6-2 shows the CLA data ROM memory map. For information about the CLA program ROM, see the CLA Program ROM (CLAPROMCRC) chapter in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

**Table 6-2. CLA Data ROM Memory Map**

| MEMORY | START ADDRESS | END ADDRESS | LENGTH |
|---|---|---|---|
| FFT Tables (Load) | 0x0100 1070 | 0x0100 186F | 0x0800 |
| Data (Load) | 0x0100 1870 | 0x0100 1FF9 | 0x078A |
| Version (Load) | 0x0100 1FFA | 0x0100 1FFF | 0x0006 |
| FFT Tables (Run) | 0x0000 F070 | 0x0000 F86F | 0x0800 |
| Data (Run) | 0x0000 F870 | 0x0000 FFF9 | 0x078A |
| Version (Run) | 0x0000 FFFA | 0x0000 FFFF | 0x0006 |


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### 6.3.3 Flash Memory Map

On the F28004x devices, up to two flash banks (each 128KB [64KW]) are available. The flash banks are controlled by a single FMC (flash module controller). On the devices in which there is only one flash bank (F280041 and F280040), the code to program the flash should be executed out of RAM. On the devices in which there are two flash banks (F280049, F280048, and F280045), only one bank at a time can be programmed or erased. In the dual-bank devices, the code to program the flash can be executed from one flash bank to erase or program the other flash bank, or the code can be executed from RAM. There should not be any kind of access to the flash bank on which an erase/program operation is in progress. Table 6-3 lists the addresses of flash sectors for F280049, F280048, and F280045. Table 6-4 lists the addresses of flash sectors for F280041 and F280040.

**Table 6-3. Addresses of Flash Sectors for F280049, F280048, and F280045**

| SECTOR | SIZE | START ADDRESS | END ADDRESS |
|---|---|---|---|
| **OTP SECTORS** | | | |
| TI OTP Bank 0 | 1K × 16 | 0x0007 0000 | 0x0007 03FF |
| User-configurable DCSM OTP Bank 0 | 1K × 16 | 0x0007 8000 | 0x0007 83FF |
| TI OTP Bank 1 | 1K × 16 | 0x0007 0400 | 0x0007 07FF |
| User-configurable DCSM OTP Bank 1 | 1K × 16 | 0x0007 8400 | 0x0007 87FF |
| **BANK 0 SECTORS** | | | |
| Sector 0 | 4K × 16 | 0x0008 0000 | 0x0008 0FFF |
| Sector 1 | 4K × 16 | 0x0008 1000 | 0x0008 1FFF |
| Sector 2 | 4K × 16 | 0x0008 2000 | 0x0008 2FFF |
| Sector 3 | 4K × 16 | 0x0008 3000 | 0x0008 3FFF |
| Sector 4 | 4K × 16 | 0x0008 4000 | 0x0008 4FFF |
| Sector 5 | 4K × 16 | 0x0008 5000 | 0x0008 5FFF |
| Sector 6 | 4K × 16 | 0x0008 6000 | 0x0008 6FFF |
| Sector 7 | 4K × 16 | 0x0008 7000 | 0x0008 7FFF |
| Sector 8 | 4K × 16 | 0x0008 8000 | 0x0008 8FFF |
| Sector 9 | 4K × 16 | 0x0008 9000 | 0x0008 9FFF |
| Sector 10 | 4K × 16 | 0x0008 A000 | 0x0008 AFFF |
| Sector 11 | 4K × 16 | 0x0008 B000 | 0x0008 BFFF |
| Sector 12 | 4K × 16 | 0x0008 C000 | 0x0008 CFFF |
| Sector 13 | 4K × 16 | 0x0008 D000 | 0x0008 DFFF |
| Sector 14 | 4K × 16 | 0x0008 E000 | 0x0008 EFFF |
| Sector 15 | 4K × 16 | 0x0008 F000 | 0x0008 FFFF |
| **BANK 1 SECTORS** | | | |
| Sector 0 | 4K × 16 | 0x0009 0000 | 0x0009 0FFF |
| Sector 1 | 4K × 16 | 0x0009 1000 | 0x0009 1FFF |
| Sector 2 | 4K × 16 | 0x0009 2000 | 0x0009 2FFF |
| Sector 3 | 4K × 16 | 0x0009 3000 | 0x0009 3FFF |
| Sector 4 | 4K × 16 | 0x0009 4000 | 0x0009 4FFF |
| Sector 5 | 4K × 16 | 0x0009 5000 | 0x0009 5FFF |
| Sector 6 | 4K × 16 | 0x0009 6000 | 0x0009 6FFF |
| Sector 7 | 4K × 16 | 0x0009 7000 | 0x0009 7FFF |
| Sector 8 | 4K × 16 | 0x0009 8000 | 0x0009 8FFF |
| Sector 9 | 4K × 16 | 0x0009 9000 | 0x0009 9FFF |
| Sector 10 | 4K × 16 | 0x0009 A000 | 0x0009 AFFF |
| Sector 11 | 4K × 16 | 0x0009 B000 | 0x0009 BFFF |
| Sector 12 | 4K × 16 | 0x0009 C000 | 0x0009 CFFF |
| Sector 13 | 4K × 16 | 0x0009 D000 | 0x0009 DFFF |

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**Table 6-3. Addresses of Flash Sectors for F280049, F280048, and F280045 (continued)**

| SECTOR | SIZE | START ADDRESS | END ADDRESS |
|---|---|---|---|
| Sector 14 | 4K × 16 | 0x0009 E000 | 0x0009 EFFF |
| Sector 15 | 4K × 16 | 0x0009 F000 | 0x0009 FFFF |
| **FLASH ECC LOCATIONS** | | | |
| TI OTP ECC Bank 0 | 128 × 16 | 0x0107 0000 | 0x0107 007F |
| TI OTP ECC Bank 1 | 128 × 16 | 0x0107 0080 | 0x0107 00FF |
| User-configurable DCSM OTP ECC Bank 0 | 128 × 16 | 0x0107 1000 | 0x0107 107F |
| User-configurable DCSM OTP ECC Bank 1 | 128 × 16 | 0x0107 1080 | 0x0107 10FF |
| Flash ECC Bank 0 | 8K × 16 | 0x0108 0000 | 0x0108 1FFF |
| Flash ECC Bank 1 | 8K × 16 | 0x0108 2000 | 0x0108 3FFF |

**Table 6-4. Addresses of Flash Sectors for F280041 and F280040**

| SECTOR | SIZE | START ADDRESS | END ADDRESS |
|---|---|---|---|
| **OTP SECTORS** | | | |
| TI OTP Bank 0 | 1K × 16 | 0x0007 0000 | 0x0007 03FF |
| User-configurable DCSM OTP Bank 0 | 1K × 16 | 0x0007 8000 | 0x0007 83FF |
| **BANK 0 SECTORS** | | | |
| Sector 0 | 4K × 16 | 0x0008 0000 | 0x0008 0FFF |
| Sector 1 | 4K × 16 | 0x0008 1000 | 0x0008 1FFF |
| Sector 2 | 4K × 16 | 0x0008 2000 | 0x0008 2FFF |
| Sector 3 | 4K × 16 | 0x0008 3000 | 0x0008 3FFF |
| Sector 4 | 4K × 16 | 0x0008 4000 | 0x0008 4FFF |
| Sector 5 | 4K × 16 | 0x0008 5000 | 0x0008 5FFF |
| Sector 6 | 4K × 16 | 0x0008 6000 | 0x0008 6FFF |
| Sector 7 | 4K × 16 | 0x0008 7000 | 0x0008 7FFF |
| Sector 8 | 4K × 16 | 0x0008 8000 | 0x0008 8FFF |
| Sector 9 | 4K × 16 | 0x0008 9000 | 0x0008 9FFF |
| Sector 10 | 4K × 16 | 0x0008 A000 | 0x0008 AFFF |
| Sector 11 | 4K × 16 | 0x0008 B000 | 0x0008 BFFF |
| Sector 12 | 4K × 16 | 0x0008 C000 | 0x0008 CFFF |
| Sector 13 | 4K × 16 | 0x0008 D000 | 0x0008 DFFF |
| Sector 14 | 4K × 16 | 0x0008 E000 | 0x0008 EFFF |
| Sector 15 | 4K × 16 | 0x0008 F000 | 0x0008 FFFF |
| **FLASH ECC LOCATIONS** | | | |
| TI OTP ECC Bank 0 | 128 × 16 | 0x0107 0000 | 0x0107 007F |
| User-configurable DCSM OTP ECC Bank 0 | 128 × 16 | 0x0107 1000 | 0x0107 107F |
| Flash ECC Bank 0 | 8K × 16 | 0x0108 0000 | 0x0108 1FFF |


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### 6.3.4 Peripheral Registers Memory Map

Table 6-5 lists the peripheral registers.

**Table 6-5. Peripheral Registers Memory Map**

| REGISTER | STRUCTURE NAME | START ADDRESS | END ADDRESS | PIPELINE PROTECTION(1) | CLA ACCESS | DMA ACCESS |
|---|---|---|---|---|---|---|
| **Peripheral Frame 0** | | | | | | |
| AdcaResultRegs(2) | ADC_RESULT_REGS | 0x0000 0B00 | 0x0000 0B1F | | Yes | Yes |
| AdcbResultRegs(2) | ADC_RESULT_REGS | 0x0000 0B20 | 0x0000 0B3F | | Yes | Yes |
| AdccResultRegs(2) | ADC_RESULT_REGS | 0x0000 0B40 | 0x0000 0B5F | | Yes | Yes |
| Cla1OnlyRegs | CLA_ONLY_REGS | 0x0000 0C00 | 0x0000 0CFF | | Yes - CLA only no CPU access | |
| CpuTimer0Regs | CPUTIMER_REGS | 0x0000 0C00 | 0x0000 0C07 | | | |
| CpuTimer1Regs | CPUTIMER_REGS | 0x0000 0C08 | 0x0000 0C0F | | | |
| CpuTimer2Regs | CPUTIMER_REGS | 0x0000 0C10 | 0x0000 0C17 | | | |
| PieCtrlRegs | PIE_CTRL_REGS | 0x0000 0CE0 | 0x0000 0CFF | | | |
| Cla1SoftIntRegs | CLA_SOFTINT_REGS | 0x0000 0CE0 | 0x0000 0CFF | | Yes - CLA only no CPU access | |
| DmaRegs | DMA_REGS | 0x0000 1000 | 0x0000 11FF | | | |
| Cla1Regs | CLA_REGS | 0x0000 1400 | 0x0000 147F | Yes | | |
| **Peripheral Frame 1** | | | | | | |
| EPwm1Regs | EPWM_REGS | 0x0000 4000 | 0x0000 40FF | Yes | Yes | Yes |
| EPwm2Regs | EPWM_REGS | 0x0000 4100 | 0x0000 41FF | Yes | Yes | Yes |
| EPwm3Regs | EPWM_REGS | 0x0000 4200 | 0x0000 42FF | Yes | Yes | Yes |
| EPwm4Regs | EPWM_REGS | 0x0000 4300 | 0x0000 43FF | Yes | Yes | Yes |
| EPwm5Regs | EPWM_REGS | 0x0000 4400 | 0x0000 44FF | Yes | Yes | Yes |
| EPwm6Regs | EPWM_REGS | 0x0000 4500 | 0x0000 45FF | Yes | Yes | Yes |
| EPwm7Regs | EPWM_REGS | 0x0000 4600 | 0x0000 46FF | Yes | Yes | Yes |
| EPwm8Regs | EPWM_REGS | 0x0000 4700 | 0x0000 47FF | Yes | Yes | Yes |
| EQep1Regs | EQEP_REGS | 0x0000 5100 | 0x0000 513F | Yes | Yes | Yes |
| EQep2Regs | EQEP_REGS | 0x0000 5140 | 0x0000 517F | Yes | Yes | Yes |
| ECap1Regs | ECAP_REGS | 0x0000 5200 | 0x0000 521F | Yes | Yes | Yes |
| ECap2Regs | ECAP_REGS | 0x0000 5240 | 0x0000 525F | Yes | Yes | Yes |
| ECap3Regs | ECAP_REGS | 0x0000 5280 | 0x0000 529F | Yes | Yes | Yes |
| ECap4Regs | ECAP_REGS | 0x0000 52C0 | 0x0000 52DF | Yes | Yes | Yes |
| ECap5Regs | ECAP_REGS | 0x0000 5300 | 0x0000 531F | Yes | Yes | Yes |
| ECap6Regs | ECAP_REGS | 0x0000 5340 | 0x0000 535F | Yes | Yes | Yes |
| Hrcap6Regs | HRCAP_REGS | 0x0000 5360 | 0x0000 537F | Yes | Yes | Yes |
| ECap7Regs | ECAP_REGS | 0x0000 5380 | 0x0000 539F | Yes | Yes | Yes |
| Hrcap7Regs | HRCAP_REGS | 0x0000 53A0 | 0x0000 53BF | Yes | Yes | Yes |
| Pga1Regs | PGA_REGS | 0x0000 5B00 | 0x0000 5B0F | Yes | Yes | Yes |
| Pga2Regs | PGA_REGS | 0x0000 5B10 | 0x0000 5B1F | Yes | Yes | Yes |
| Pga3Regs | PGA_REGS | 0x0000 5B20 | 0x0000 5B2F | Yes | Yes | Yes |
| Pga4Regs | PGA_REGS | 0x0000 5B30 | 0x0000 5B3F | Yes | Yes | Yes |
| Pga5Regs | PGA_REGS | 0x0000 5B40 | 0x0000 5B4F | Yes | Yes | Yes |
| Pga6Regs | PGA_REGS | 0x0000 5B50 | 0x0000 5B5F | Yes | Yes | Yes |
| Pga7Regs | PGA_REGS | 0x0000 5B60 | 0x0000 5B6F | Yes | Yes | Yes |
| DacaRegs | DAC_REGS | 0x0000 5C00 | 0x0000 5C0F | Yes | Yes | Yes |
| DacbRegs | DAC_REGS | 0x0000 5C10 | 0x0000 5C1F | Yes | Yes | Yes |
| Cmpss1Regs | CMPSS_REGS | 0x0000 5C80 | 0x0000 5C9F | Yes | Yes | Yes |
| Cmpss2Regs | CMPSS_REGS | 0x0000 5CA0 | 0x0000 5CBF | Yes | Yes | Yes |
| Cmpss3Regs | CMPSS_REGS | 0x0000 5CC0 | 0x0000 5CDF | Yes | Yes | Yes |
| Cmpss4Regs | CMPSS_REGS | 0x0000 5CE0 | 0x0000 5CFF | Yes | Yes | Yes |

(1) The CPU (not applicable for CLA or DMA) contains a write-followed-by-read protection mode to ensure that any read operation that follows a write operation within a protected address range is executed as written by delaying the read operation until the write is initiated.
(2) ADC result register has no arbitration. Each master can access any ADC result register without any arbitration.

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## Table 6-5. Peripheral Registers Memory Map (continued)

| REGISTER | STRUCTURE NAME | START ADDRESS | END ADDRESS | PIPELINE PROTECTION(1) | CLA ACCESS | DMA ACCESS |
|---|---|---|---|---|---|---|
| Cmpss5Regs | CMPSS_REGS | 0x0000 5D00 | 0x0000 5D1F | Yes | Yes | Yes |
| Cmpss6Regs | CMPSS_REGS | 0x0000 5D20 | 0x0000 5D3F | Yes | Yes | Yes |
| Cmpss7Regs | CMPSS_REGS | 0x0000 5D40 | 0x0000 5D5F | Yes | Yes | Yes |
| Sdfm1Regs | SDFM_REGS | 0x0000 5E00 | 0x0000 5E7F | Yes | Yes | Yes |
| **Peripheral Frame 2** | | | | | | |
| SpiaRegs(3) | SPI_REGS | 0x0000 6100 | 0x0000 610F | Yes | Yes | Yes |
| SpibRegs(3) | SPI_REGS | 0x0000 6110 | 0x0000 611F | Yes | Yes | Yes |
| PmbusaRegs | PMBUS_REGS | 0x0000 6400 | 0x0000 641F | Yes | Yes | Yes |
| FsiTxaRegs | FSI_TX_REGS | 0x0000 6600 | 0x0000 667F | Yes | Yes | Yes |
| FsiRxaRegs | FSI_RX_REGS | 0x0000 6680 | 0x0000 66FF | Yes | Yes | Yes |
| **Peripheral Frame 3** | | | | | | |
| AdcaRegs | ADC_REGS | 0x0000 7400 | 0x0000 747F | Yes | Yes | |
| AdcbRegs | ADC_REGS | 0x0000 7480 | 0x0000 74FF | Yes | Yes | |
| AdccRegs | ADC_REGS | 0x0000 7500 | 0x0000 757F | Yes | Yes | |
| **Peripheral Frame 4** | | | | | | |
| InputXbarRegs | INPUT_XBAR_REGS | 0x0000 7900 | 0x0000 791F | Yes | | |
| XbarRegs | XBAR_REGS | 0x0000 7920 | 0x0000 793F | Yes | | |
| SyncSocRegs | SYNC_SOC_REGS | 0x0000 7940 | 0x0000 794F | Yes | | |
| DmaClaSrcSelRegs | DMA_CLA_SRC_SEL_REGS | 0x0000 7980 | 0x0000 79BF | Yes | | |
| EPwmXbarRegs | EPWM_XBAR_REGS | 0x0000 7A00 | 0x0000 7A3F | Yes | | |
| OutputXbarRegs | OUTPUT_XBAR_REGS | 0x0000 7A80 | 0x0000 7ABF | Yes | | |
| GpioCtrlRegs | GPIO_CTRL_REGS | 0x0000 7C00 | 0x0000 7EFF | Yes | | |
| GpioDataRegs(4) | GPIO_DATA_REGS | 0x0000 7F00 | 0x0000 7FFF | Yes | Yes | |
| **Peripheral Frame 5** | | | | | | |
| DevCfgRegs | DEV_CFG_REGS | 0x0005 D000 | 0x0005 D17F | Yes | | |
| ClkCfgRegs | CLK_CFG_REGS | 0x0005 D200 | 0x0005 D2FF | Yes | | |
| CpuSysRegs | CPU_SYS_REGS | 0x0005 D300 | 0x0005 D3FF | Yes | | |
| PeriphAcRegs | PERIPH_AC_REGS | 0x0005 D500 | 0x0005 D6FF | Yes | | |
| AnalogSubsysRegs | ANALOG_SUBSYS_REGS | 0x0005 D700 | 0x0005 D7FF | Yes | | |
| **Peripheral Frame 6** | | | | | | |
| EnhancedDebugGlobalRegs | ERAD_GLOBAL_REGS | 0x0005 E800 | 0x0005 E80A | | | |
| EnhancedDebugHWBP1Regs | ERAD_HWBP_REGS | 0x0005 E900 | 0x0005 E907 | | | |
| EnhancedDebugHWBP2Regs | ERAD_HWBP_REGS | 0x0005 E908 | 0x0005 E90F | | | |
| EnhancedDebugHWBP3Regs | ERAD_HWBP_REGS | 0x0005 E910 | 0x0005 E917 | | | |
| EnhancedDebugHWBP4Regs | ERAD_HWBP_REGS | 0x0005 E918 | 0x0005 E91F | | | |
| EnhancedDebugHWBP5Regs | ERAD_HWBP_REGS | 0x0005 E920 | 0x0005 E927 | | | |
| EnhancedDebugHWBP6Regs | ERAD_HWBP_REGS | 0x0005 E928 | 0x0005 E92F | | | |
| EnhancedDebugHWBP7Regs | ERAD_HWBP_REGS | 0x0005 E930 | 0x0005 E937 | | | |
| EnhancedDebugHWBP8Regs | ERAD_HWBP_REGS | 0x0005 E938 | 0x0005 E93F | | | |
| EnhancedDebugCounter1Regs | ERAD_COUNTER_REGS | 0x0005 E980 | 0x0005 E98F | | | |
| EnhancedDebugCounter2Regs | ERAD_COUNTER_REGS | 0x0005 E990 | 0x0005 E99F | | | |
| EnhancedDebugCounter3Regs | ERAD_COUNTER_REGS | 0x0005 E9A0 | 0x0005 E9AF | | | |
| EnhancedDebugCounter4Regs | ERAD_COUNTER_REGS | 0x0005 E9B0 | 0x0005 E9BF | | | |
| DcsmBank0Z1Regs | DCSM_BANK0_Z1_REGS | 0x0005 F000 | 0x0005 F022 | Yes | | |
| DcsmBank0Z2Regs | DCSM_BANK0_Z2_REGS | 0x0005 F040 | 0x0005 F062 | Yes | | |
| DcsmBank1Z1Regs | DCSM_BANK1_Z1_REGS | 0x0005 F100 | 0x0005 F122 | Yes | | |
| DcsmBank1Z2Regs | DCSM_BANK1_Z2_REGS | 0x0005 F140 | 0x0005 F162 | Yes | | |
| DcsmCommonRegs | DCSM_COMMON_REGS | 0x0005 F070 | 0x0005 F07F | Yes | | |
| DcsmCommon2Regs | DCSM_COMMON_REGS | 0x0005 F080 | 0x0005 F087 | Yes | | |
| MemCfgRegs | MEM_CFG_REGS | 0x0005 F400 | 0x0005 F47F | Yes | | |
| AccessProtectionRegs | ACCESS_PROTECTION_REGS | 0x0005 F4C0 | 0x0005 F4FF | Yes | | |
| MemoryErrorRegs | MEMORY_ERROR_REGS | 0x0005 F500 | 0x0005 F53F | Yes | | |

(3) Registers with 16-bit access only.
(4) Both CPU and CLA have their own copy of GPIO_DATA_REGS, and hence, no arbitration is required between CPU and CLA. For more details, see the General-Purpose Input/Output (GPIO) chapter of the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.


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**Table 6-5. Peripheral Registers Memory Map (continued)**

| REGISTER | STRUCTURE NAME | START ADDRESS | END ADDRESS | PIPELINE PROTECTION(1) | CLA ACCESS | DMA ACCESS |
|---|---|---|---|---|---|---|
| Flash0CtrlRegs | FLASH_CTRL_REGS | 0x0005 F800 | 0x0005 FAFF | Yes | | |
| Flash0EccRegs | FLASH_ECC_REGS | 0x0005 FB00 | 0x0005 FB3F | Yes | | |
| **Peripheral Frame 7** | | | | | | |
| CanaRegs | CAN_REGS | 0x0004 8000 | 0x0004 87FF | Yes | | Yes |
| CanbRegs | CAN_REGS | 0x0004 A000 | 0x0004 A7FF | Yes | | Yes |
| RomPrefetchRegs | ROM_PREFETCH_REGS | 0x0005 E608 | 0x0005 E609 | Yes | | |
| DccRegs | DCC_REGS | 0x0005 E700 | 0x0005 E73F | Yes | | |
| **Peripheral Frame 8** | | | | | | |
| LinaRegs | LIN_REGS | 0x0000 6A00 | 0x0000 6AFF | Yes | Yes | Yes |
| **Peripheral Frame 9** | | | | | | |
| WdRegs(3) | WD_REGS | 0x0000 7000 | 0x0000 703F | Yes | | |
| NmiIntruptRegs(3) | NMI_INTRUPT_REGS | 0x0000 7060 | 0x0000 706F | Yes | | |
| XintRegs(3) | XINT_REGS | 0x0000 7070 | 0x0000 707F | Yes | | |
| SciaRegs(3) | SCI_REGS | 0x0000 7200 | 0x0000 720F | Yes | | |
| ScibRegs(3) | SCI_REGS | 0x0000 7210 | 0x0000 721F | Yes | | |
| I2caRegs(3) | I2C_REGS | 0x0000 7300 | 0x0000 733F | Yes | | |

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### 6.3.5 Memory Types

#### 6.3.5.1 Dedicated RAM (Mx RAM)

The CPU subsystem has two dedicated ECC-capable RAM blocks: M0 and M1. These memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them).

#### 6.3.5.2 Local Shared RAM (LSx RAM)

RAM blocks which are dedicated to each subsystem and are accessible only to its CPU and CLA, are called local shared RAMs (LSx RAMs).

All LSx RAM blocks have parity. These memories are secure and have the access protection (CPU write/CPU fetch) feature.

By default, these memories are dedicated only to the CPU, and the user could choose to share these memories with the CLA by configuring the MSEL_LSx bit field in the LSxMSEL registers appropriately (see Table 6-6).

**Table 6-6. Master Access for LSx RAM (With Assumption That all Other Access Protections are Disabled)**

| MSEL_LSx | CLAPGM_LSx | CPU ALLOWED ACCESS | CLA1 ALLOWED ACCESS | COMMENT |
|---|---|---|---|---|
| 00 | X | All | – | LSx memory is configured as CPU dedicated RAM. |
| 01 | 0 | All | Data Read<br>Data Write<br>Emulation Data Read<br>Emulation Data Write | LSx memory is shared between CPU and CLA1. |
| 01 | 1 | Emulation Read<br>Emulation Write | Fetch Only<br>Emulation Program Read<br>Emulation Program Write | LSx memory is CLA1 program memory. |

#### 6.3.5.3 Global Shared RAM (GSx RAM)

RAM blocks which are accessible from both the CPU and DMA are called global shared RAMs (GSx RAMs). Both the CPU and DMA have full read and write access to these memories. Table 6-7 shows the features of the GSx RAM.

**Table 6-7. Global Shared RAM**

| CPU (FETCH) | CPU (READ) | CPU (WRITE) | CPU.DMA (READ) | CPU.DMA (WRITE) |
|---|---|---|---|---|
| Yes | Yes | Yes | Yes | Yes |

All GSx RAM blocks have parity.

The GSx RAMs have access protection (CPU write/CPU fetch/DMA write).

#### 6.3.5.4 CLA Message RAM (CLA MSGRAM)

These RAM blocks can be used to share data between the CPU and CLA. The CLA has read and write access to the "CLA to CPU MSGRAM." The CPU has read and write access to the "CPU to CLA MSGRAM." The CPU and CLA both have read access to both MSGRAMs.

This RAM has parity.


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## 6.4 Identification

Table 6-8 lists the Device Identification Registers. Additional information on device identification can be found in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*. See the register descriptions of PARTIDH and PARTIDL for identification of production status (TMX or TMS); availability of InstaSPIN-FOC™; and other device information.

**Table 6-8. Device Identification Registers**

| NAME | ADDRESS | SIZE (x16) | DESCRIPTION | |
|---|---|---|---|---|
| PARTIDH | 0x0005 D00A | 2 | Device part identification number | |
| | | | TMS320F280049 | 0x01FF 0500 |
| | | | TMS320F280049C | 0x01FF 0500 |
| | | | TMS320F280048 | 0x01FE 0500 |
| | | | TMS320F280048C | 0x01FE 0500 |
| | | | TMS320F280045 | 0x01FB 0500 |
| | | | TMS320F280041 | 0x01F7 0500 |
| | | | TMS320F280041C | 0x01F7 0500 |
| | | | TMS320F280040 | 0x01F6 0500 |
| | | | TMS320F280040C | 0x01F6 0500 |
| REVID | 0x0005 D00C | 2 | Silicon revision number | |
| | | | Revision 0 | 0x0000 0000 |
| | | | Revision A | 0x0000 0001 |
| | | | Revision B | 0x0000 0002 |
| UID_UNIQUE | 0x0007 03CC | 2 | Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS Revision B devices. | |

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## 6.5 Bus Architecture – Peripheral Connectivity

Table 6-9 lists a broad view of the peripheral and configuration register accessibility from each bus master.

**Table 6-9. Bus Master Peripheral Access**

| PERIPHERALS | DMA | CLA | CPU |
|---|---|---|---|
| **SYSTEM PERIPHERALS** | | | |
| CPU Timers | | | Y |
| System Configuration (WD, NMIWD, LPM, Peripheral Clock Gating) | | | Y |
| Device Capability, Peripheral Reset | | | Y |
| Clock and PLL Configuration | | | Y |
| Flash Configuration | | | Y |
| Reset Configuration | | | Y |
| GPIO Pin Mapping and Configuration | | | Y |
| GPIO Data (1) | | Y | Y |
| DMA and CLA Trigger Source Select | | | Y |
| **CONTROL PERIPHERALS** | | | |
| ePWM/HRPWM | Y | Y | Y |
| eCAP/HRCAP | Y | Y | Y |
| eQEP (2) | Y | Y | Y |
| SDFM | Y | Y | Y |
| **ANALOG PERIPHERALS** | | | |
| Analog System Control | | | Y |
| ADC Configuration | | Y | Y |
| ADC Result (3) | Y | Y | Y |
| CMPSS (2) | Y | Y | Y |
| DAC (2) | Y | Y | Y |
| PGA (2) | Y | Y | Y |
| **COMMUNICATION PERIPHERALS** | | | |
| CAN | Y | | Y |
| SPI | Y | Y | Y |
| I2C | | | Y |
| PMBus | Y | Y | Y |
| SCI | | | Y |
| LIN | Y | Y | Y |
| FSI | Y | Y | Y |

(1) The GPIO Data Registers are unique for the CPU and CLA. When the GPIO Pin Mapping Register is configured to assign a GPIO to a particular master, the respective GPIO Data Register will control the GPIO. See the General-Purpose Input/Output (GPIO) chapter of the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual* for more details.
(2) These modules are accessible from DMA but cannot trigger a DMA transfer.
(3) ADC result registers are duplicated for each master. This allows them to be read with 0-wait states with no arbitration from any or all masters.


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## 6.6 C28x Processor

The CPU is a 32-bit fixed-point processor which draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The features include:

- CPU – modified Harvard architecture and circular addressing. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address and data buses.
- RISC – single-cycle instruction execution, register-to-register operations, and modified Harvard architecture.
- Microcontroller – ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation.

For more information on CPU architecture and instruction set, see the *TMS320C28x CPU and Instruction Set Reference Guide*. For more information on the C28x Floating-Point Unit (FPU), see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*. All of the features of the C28x documented in the *TMS320C28x CPU and Instruction Set Reference Guide* apply to the C28x+VCU. All features documented in the *TMS320C28x Extended Instruction Sets Technical Reference Manual* apply to the C28x+FPU+VCU. A brief overview of the FPU, TMU, and VCU-Type 0 is provided here.

An overview of the VCU-I instructions can be found in the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

### 6.6.1 Embedded Real-Time Analysis and Diagnostic (ERAD)

The ERAD module enhances the debug and system-analysis capabilities of the device. The debug and system-analysis enhancements provided by the ERAD module is done outside of the CPU. The ERAD module consists of the Enhanced Bus Comparator units and the Benchmark System Event Counter units. The Enhanced Bus Comparator units are used to generate hardware breakpoints, hardware watch points, and other output events. The Benchmark System Event Counter units are used to analyze and profile the system. The ERAD module is accessible by the debugger and by the application software, which significantly increases the debug capabilities of many real-time systems, especially in situations where debuggers are not connected. In the TMS320F28004x devices, the ERAD module contains eight Enhanced Bus Comparator units and four Benchmark System Event Counter units.

### 6.6.2 Floating-Point Unit (FPU)

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating-point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the RB, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

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### 6.6.3 Trigonometric Math Unit (TMU)

The TMU extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in Table 6-10.

**Table 6-10. TMU Supported Instructions**

| INSTRUCTIONS | C EQUIVALENT OPERATION | PIPELINE CYCLES |
|---|---|---|
| MPY2PIF32 RaH,RbH | a = b * 2pi | 2/3 |
| DIV2PIF32 RaH,RbH | a = b / 2pi | 2/3 |
| DIVF32 RaH,RbH,RcH | a = b/c | 5 |
| SQRTF32 RaH,RbH | a = sqrt(b) | 5 |
| SINPUF32 RaH,RbH | a = sin(b*2pi) | 4 |
| COSPUF32 RaH,RbH | a = cos(b*2pi) | 4 |
| ATANPUF32 RaH,RbH | a = atan(b)/2pi | 4 |
| QUADF32 RaH,RbH,RcH,RdH | Operation to assist in calculating ATANPU2 | 5 |

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations.

### 6.6.4 Viterbi, Complex Math and CRC Unit (VCU-I)

The C28x with VCU (C28x+VCU) processor extends the capabilities of the C28x fixed-point or floating-point CPU by adding registers and instructions to support the following algorithm types:

- **Viterbi decoding**

  Viterbi decoding is commonly used in baseband communications applications. The viterbi decode algorithm consists of three main parts: branch metric calculations, compare-select (viterbi butterfly), and a traceback operation. Table 6-11 lists a summary of the VCU-I performance for each of these operations.

**Table 6-11. Viterbi Decode Performance**

| VITERBI OPERATION | VCU CYCLES |
|---|---|
| Branch Metric Calculation (code rate = 1/2) | 1 |
| Branch Metric Calculation (code rate = 1/3) | 2p |
| Viterbi Butterfly (add-compare-select) | 2 (1) |
| Traceback per Stage | 3 (2) |

(1) C28x CPU takes 15 cycles per butterfly.
(2) C28x CPU takes 22 cycles per stage.

- **Cyclic redundancy check (CRC)**

  CRC algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCU can perform 8-, 16-, and 32-bit CRCs. For example, the VCU can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC which is updated whenever a CRC instruction is executed.

- **Complex math**

  Complex math is used in many applications; a few of which are:

  – Fast fourier transform (FFT)

    The complex FFT is used in spread spectrum communications, as well as many signal processing algorithms.

  – Complex filters

    Complex filters improve data reliability, transmission distance, and power efficiency. The C28x+VCU can perform a complex I and Q multiply with coefficients (four multiplies) in a single cycle. In addition, the C28x+VCU can read/write the real and imaginary parts of 16-bit complex data to memory in a single cycle.

Table 6-12 lists a summary of a few complex math operations enabled by the VCU.


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**Table 6-12. Complex Math Performance**

| COMPLEX MATH OPERATION | VCU CYCLES | NOTES |
|---|---|---|
| Add or Subtract | 1 | 32 ± 32 = 32-bit (Useful for filters) |
| Add or Subtract | 1 | 16 ± 32 = 15-bit (Useful for FFT) |
| Multiply | 2p | 16 × 16 = 32-bit |
| Multiply and Accumulate (MAC) | 2p | 32 + 32 = 32-bit, 16 × 16 = 32-bit |
| RPT MAC | 2p+N | Repeat MAC. Single cycle after the first operation. |

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## 6.7 Control Law Accelerator (CLA)

The CLA Type-2 is an independent, fully programmable, 32-bit floating-point math processor that brings concurrent control-loop execution to the C28x family. The low interrupt-latency of the CLA allows it to read ADC samples "just-in-time." This significantly reduces the ADC sample to output delay to enable faster system response and higher MHz control loops. By using the CLA to service time-critical control loops, the main CPU is free to perform other system tasks such as communications and diagnostics.

The control law accelerator extends the capabilities of the C28x CPU by adding parallel processing. Time-critical control loops serviced by the CLA can achieve low ADC sample to output delay. Thus, the CLA enables faster system response and higher frequency control loops. Using the CLA for time-critical tasks frees up the main CPU to perform other system and communication functions concurrently.

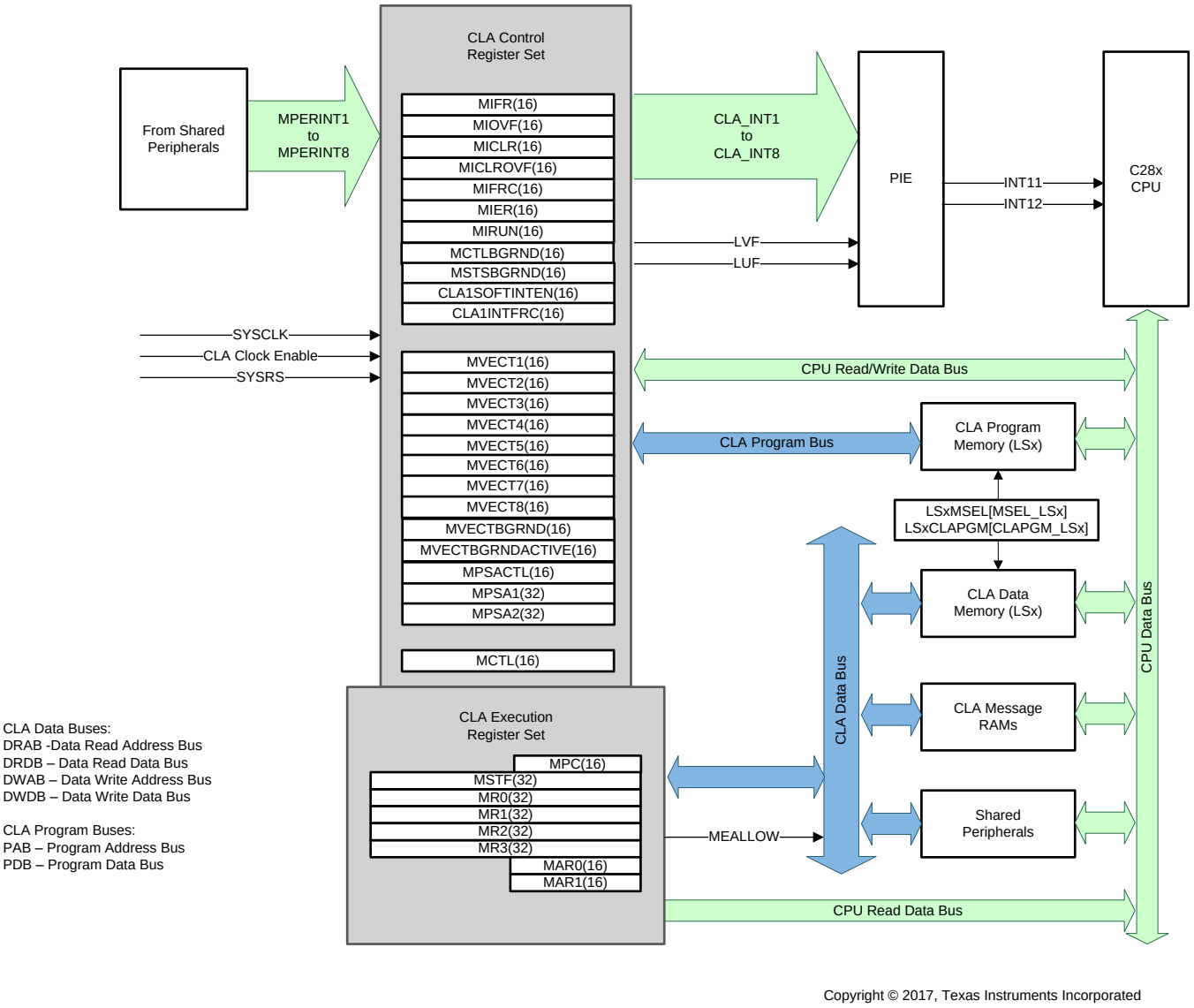
The following is a list of major features of the CLA:

- Clocked at the same rate as the main CPU (SYSCLKOUT).
- An independent architecture allowing CLA algorithm execution independent of the main C28x CPU.
  - Complete bus architecture:
    - Program Address Bus (PAB) and Program Data Bus (PDB)
    - Data Read Address Bus (DRAB), Data Read Data Bus (DRDB), Data Write Address Bus (DWAB), and Data Write Data Bus (DWDB)
  - Independent 8-stage pipeline.
  - 16-bit program counter (MPC)
  - Four 32-bit result registers (MR0 to MR3)
  - Two 16-bit auxiliary registers (MAR0, MAR1)
  - Status register (MSTF)
- Instruction set includes:
  - IEEE single-precision (32-bit) floating-point math operations
  - Floating-point math with parallel load or store
  - Floating-point multiply with parallel add or subtract
  - 1/X and 1/sqrt(X) estimations
  - Data type conversions
  - Conditional branch and call
  - Data load/store operations
- The CLA program code can consist of up to eight tasks or interrupt service routines, or seven tasks and a main background task.
  - The start address of each task is specified by the MVECT registers.
  - No limit on task size as long as the tasks fit within the configurable CLA program memory space.
  - One task is serviced at a time until its completion. There is no nesting of tasks.
  - Upon task completion a task-specific interrupt is flagged within the PIE.
  - When a task finishes the next highest-priority pending task is automatically started.
  - The Type-2 CLA can have a main task that runs continuously in the background, while other high-priority events trigger a foreground task.
- Task trigger mechanisms:
  - C28x CPU through the IACK instruction
  - Task1 to Task8: up to 256 possible trigger sources from peripherals connected to the shared bus on which the CLA assumes secondary ownership.
  - Task8 can be set to be the background task, while Tasks 1 to 7 take peripheral triggers.


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- Memory and Shared Peripherals:
  - Two dedicated message RAMs for communication between the CLA and the main CPU.
  - The C28x CPU can map CLA program and data memory to the main CPU space or CLA space.
  - The CLA, on reset, is the secondary master for all peripherals which can have either the CLA or DMA as their secondary master.

Figure 6-2 shows the CLA block diagram.




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**Figure 6-2. CLA Block Diagram**

## 6.8 Direct Memory Access (DMA)

The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing.

DMA features include:

- Six channels with independent PIE interrupts
- Peripheral interrupt trigger sources
  - ADC interrupts and EVT signals
  - External Interrupts
  - ePWM SOC signals
  - CPU timers
  - eCAP
  - Sigma-Delta Filter Module
  - SPI transmit and receive
  - CAN transmit and receive
  - LIN transmit and receive
- Data sources and destinations:
  - GSx RAM
  - ADC result registers
  - Control peripheral registers (ePWM, eQEP, eCAP, SDFM)
  - DAC and PGA registers
  - SPI, LIN, CAN, and PMBus registers
- Word Size: 16-bit or 32-bit (SPI limited to 16-bit)
- Throughput: Four cycles per word without arbitration

Figure 6-3 shows a device-level block diagram of the DMA.

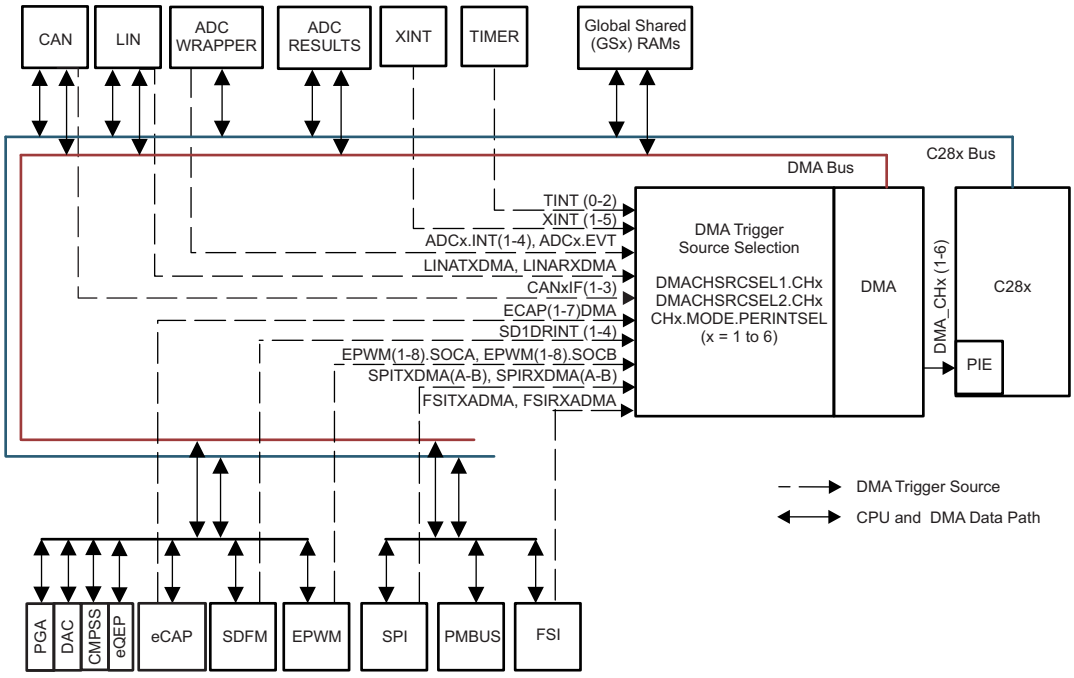



**Figure 6-3. DMA Block Diagram**


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## 6.9 Boot ROM and Peripheral Booting

The device boot ROM contains bootloading software. The device ROM has an internal bootloader (programmed by TI) that is executed when the device is powered ON, and each time the device is reset. The bootloader is used as an initial program to load the application on to device RAM through any of the bootable peripherals, or it is configured to start the application in flash, if any.

Table 6-13 lists the default boot mode options. Users have the option to customize the boot modes supported as well as the boot mode select pins.

**Table 6-13. Device Default Boot Modes**

| BOOT MODE | GPIO24 (DEFAULT BOOT MODE SELECT PIN 1) | GPIO32 (DEFAULT BOOT MODE SELECT PIN 0) |
|---|---|---|
| Parallel IO | 0 | 0 |
| SCI/Wait boot | 0 | 1 |
| CAN | 1 | 0 |
| Flash | 1 | 1 |

Table 6-14 lists the possible boot modes supported on the device. The default boot mode pins are GPIO24 (boot mode pin 1) and GPIO32 (boot mode pin 0). Users may choose to have weak pullups for boot mode pins if they use a peripheral on these pins as well, so the pullups can be overdriven. On this device, customers can change the factory default boot mode pins by programming user-configurable Dual Code Security Module (DCSM) OTP locations.

**Table 6-14. All Available Boot Modes**

| BOOT MODE NUMBER | BOOT MODE |
|---|---|
| 0 | Parallel IO |
| 1 | SCI/Wait boot |
| 2 | CAN |
| 3 | Flash |
| 4 | Wait |
| 5 | RAM |
| 6 | SPI Master |
| 7 | I2C Master |
| 8 | PLC |

**NOTE**

All the peripheral boot modes supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this section, such as SCI boot, it is actually referring to the first module instance, meaning SCI boot on the SCIA port. The same applies to the other peripheral boots.

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### 6.9.1 Configuring Alternate Boot Mode Select Pins

This section explains how the boot mode select pins can be customized by the user, by programming the BOOTPIN_CONFIG location in user-configurable DCSM OTP. The location in user DCSM OTP is Z1-OTP-BOOTPIN-CONFIG. When debugging, EMU-BOOTPIN-CONFIG is the emulation equivalent of Z1-OTP-BOOTPIN-CONFIG, and can be programmed to experiment with different boot modes without writing to OTP. The device can be programmed to use 0, 1, 2, or 3 boot mode select pins as needed.

**Table 6-15. BOOTPIN_CONFIG Bit Fields**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31–24 | Key | Write 0x5A to these 8 bits to tell the boot ROM code that the bits in this register are valid |
| 23–16 | Boot Mode Select Pin 2 (BMSP2) | See BMPS0 description |
| 15–8 | Boot Mode Select Pin 1 (BMSP1) | See BMSP0 description |
| 7–0 | Boot Mode Select Pin 0 (BMSP0) | Set to the GPIO pin to be used during boot (up to 255).<br>0x0 = GPIO0; 0x01 = GPIO1 and so on<br>0xFF is invalid and selects the factory default chosen BMSP0, if all other BMSPs are also set to 0xFF.<br>If any other BMSPs are not set to 0xFF, then setting a BMSP to 0xFF will disable that particular BMSP. |

**NOTE**

The following GPIOs cannot be used as a BMSP. If selected for a particular BMSP, the boot ROM automatically selects the factory default GPIO (the factory default for BMSP2 is 0xFF, which disables the BMSP).

- GPIO 20 to 23
- GPIO 36
- GPIO 38
- GPIO 60 to 223

**Table 6-16. Stand-alone Boot Mode Select Pin Decoding**

| BOOTPIN_CONFIG KEY | BMSP0 | BMSP1 | BMSP2 | REALIZED BOOT MODE |
|---|---|---|---|---|
| != 0x5A | Don't Care | Don't Care | Don't Care | Boot as defined by the factory default BMSPs (GPIO24, GPIO32) |
| = 0x5A | 0xFF | 0xFF | 0xFF | Boot as defined in the boot table for boot mode 0 (All BMSPs disabled) |
| | Valid GPIO | 0xFF | 0xFF | Boot as defined by the value of BMSP0 (BMSP1 and BMSP2 disabled) |
| | 0xFF | Valid GPIO | 0xFF | Boot as defined by the value of BMSP1 (BMSP0 and BMSP2 disabled) |
| | 0xFF | 0xFF | Valid GPIO | Boot as defined by the value of BMSP2 (BMSP0 and BMSP1 disabled) |
| | Valid GPIO | Valid GPIO | 0xFF | Boot as defined by the values of BMSP0 and BMSP1 (BMSP2 disabled) |
| | Valid GPIO | 0xFF | Valid GPIO | Boot as defined by the values of BMSP0 and BMSP2 (BMSP1 disabled) |
| | 0xFF | Valid GPIO | Valid GPIO | Boot as defined by the values of BMSP1 and BMSP2 (BMSP0 disabled) |
| | Valid GPIO | Valid GPIO | Valid GPIO | Boot as defined by the values of BMSP0, BMPS1, and BMSP2 |


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### 6.9.2 Configuring Alternate Boot Mode Options

This section explains how to configure the boot definition table, BOOTDEF, for the device and the associated boot options. The 64-bit location is in user-configurable DCSM OTP in the Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations. When debugging, EMU-BOOTDEF-LOW and EMU-BOOTDEF-HIGH are the emulation equivalents of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH, and can be programmed to experiment with different boot mode options without writing to OTP. The range of customization to the boot definition table depends on how many boot mode select pins are being used. For examples on how to use the BOOTPIN_CONFIG and BOOTDEF values, see the Boot Mode Example Use Cases section of the ROM Code and Peripheral Booting chapter in the *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*.

**Table 6-17. BOOTDEF Bit Fields**

| BOOTDEF NAME | BYTE POSITION | NAME | DESCRIPTION |
|---|---|---|---|
| BOOT_DEF0 | 7–0 | BOOT_DEF0 Mode and Options | Set the boot mode and boot mode options. This can include changing the GPIOs for a particular boot peripheral or specifying a different flash entry point. Any unsupported boot mode will cause the device to reset.<br>See *GPIO Assignments* for valid BOOTDEF values. |
| BOOT_DEF1 | 15–8 | BOOT_DEF1 Mode and Options | Refer to BOOT_DEF0 descriptions. |
| BOOT_DEF2 | 23–16 | BOOT_DEF2 Mode and Options | |
| BOOT_DEF3 | 31–24 | BOOT_DEF3 Mode and Options | |
| BOOT_DEF4 | 39–32 | BOOT_DEF4 Mode and Options | |
| BOOT_DEF5 | 47–40 | BOOT_DEF5 Mode and Options | |
| BOOT_DEF6 | 55–48 | BOOT_DEF6 Mode and Options | |
| BOOT_DEF7 | 63–56 | BOOT_DEF7 Mode and Options | |

### 6.9.3 GPIO Assignments

This section details the GPIOs and boot options used for each boot mode set in BOOT_DEFx located at Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH. See *Configuring Alternate Boot Mode Select Pins* on how to manipulate BOOT_DEFx. When selecting a boot mode option, verify that the necessary pins are available in the pin mux options for the specific device package being used.

**Table 6-18. SCI Boot Options**

| OPTION | BOOTDEFx VALUE | SCIATX GPIO | SCIARX GPIO |
|---|---|---|---|
| 0 (default) | 0x01 | GPIO29 | GPIO28 |
| 1 | 0x21 | GPIO16 | GPIO17 |
| 2 | 0x41 | GPIO8 | GPIO9 |
| 3 | 0x61 | GPIO48 | GPIO49 |
| 4 | 0x81 | GPIO24 | GPIO25 |

**NOTE**

Pullups are enabled on the SCIATX and SCIARX pins.

**Table 6-19. CAN Boot Options**

| OPTION | BOOTDEFx VALUE | CANTXA GPIO | CANRXA GPIO |
|---|---|---|---|
| 0 (default) | 0x02 | GPIO32 | GPIO33 |
| 1 | 0x22 | GPIO4 | GPIO5 |
| 2 | 0x42 | GPIO31 | GPIO30 |
| 3 | 0x62 | GPIO37 | GPIO35 |

**NOTE**

Pullups are enabled on the CANTXA and SCIARX pins.

**Table 6-20. Flash Boot Options**

| OPTION | BOOTDEFx VALUE | FLASH ENTRY POINT (ADDRESS) | FLASH BANK, SECTOR |
|---|---|---|---|
| 0 (default) | 0x03 | Flash – Default Option 1 (0x00080000) | Bank 0, Sector 0 |
| 1 | 0x23 | Flash – Option 2 (0x0008EFF0) | Bank 0, Sector 14 |
| 2 | 0x43 | Flash – Option 3 (0x00090000) | Bank 1, Sector 0 |
| 3 | 0x63 | Flash – Option 4 (0x0009EFF0) | Bank 1, Sector 14 |

**Table 6-21. Wait Boot Options**

| OPTION | BOOTDEFx VALUE | WATCHDOG STATUS |
|---|---|---|
| 0 | 0x04 | Enabled |
| 1 | 0x24 | Disabled |

**Table 6-22. SPI Boot Options**

| OPTION | BOOTDEFx VALUE | SPIA_SIMO | SPIA_SOMI | SPIA_CLK | SPIA_STE |
|---|---|---|---|---|---|
| 1 | 0x26 | GPIO8 | GPIO10 | GPIO9 | GPIO11 |
| 2 | 0x46 | GPIO54 | GPIO55 | GPIO56 | GPIO57 |
| 3 | 0x66 | GPIO16 | GPIO17 | GPIO56 | GPIO57 |
| 4 | 0x86 | GPIO8 | GPIO17 | GPIO9 | GPIO11 |

**NOTE**

Pullups are enabled on the SPIA_SIMO, SPIA_SOMI, SPIA_CLK, and SPIA_STE pins.


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**Table 6-23. I2C Boot Options**

| OPTION | BOOTDEFx VALUE | SDAA GPIO | SCLA GPIO |
|---|---|---|---|
| 0 | 0x07 | GPIO32 | GPIO33 |
| 1 | 0x47 | GPIO26 | GPIO27 |
| 2 | 0x67 | GPIO42 | GPIO43 |

**NOTE**

Pullups are enabled on the SDAA and SCLA pins.

**Table 6-24. Parallel Boot Options**

| OPTION | BOOTDEFx VALUE | D0 to D7 GPIO | DSP CONTROL GPIO | HOST CONTROL GPIO |
|---|---|---|---|---|
| 0 (default) | 0x00 | GPIO0 to GPIO7 | GPIO16 | GPIO11 |

**NOTE**

Pullups are enabled on GPIO0 to GPIO7.

**Table 6-25. RAM Boot Options**

| OPTION | BOOTDEFx VALUE | RAM ENTRY POINT ADDRESS |
|---|---|---|
| 0 | 0x05 | 0x00000000 |

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## 6.10 Dual Code Security Module

The dual code security module (DCSM) prevents access to on-chip secure memories. The term “secure” means access to secure memories and resources is blocked. The term “unsecure” means access is allowed; for example, through a debugging tool such as Code Composer Studio™ (CSS).

The code security mechanism offers protection for two zones, Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both the zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (CLA, LSx RAM, and flash sectors).

The security of each zone is ensured by its own 128-bit password (CSM password). The password for each zone is stored in an OTP memory location based on a zone-specific link pointer. The link pointer value can be changed to program a different set of security settings (including passwords) in OTP.

**Code Security Module Disclaimer**

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

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## 6.11 Watchdog

The watchdog module is the same as the one on previous TMS320C2000 devices, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backward-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 6-4 shows the various functional blocks within the watchdog module.

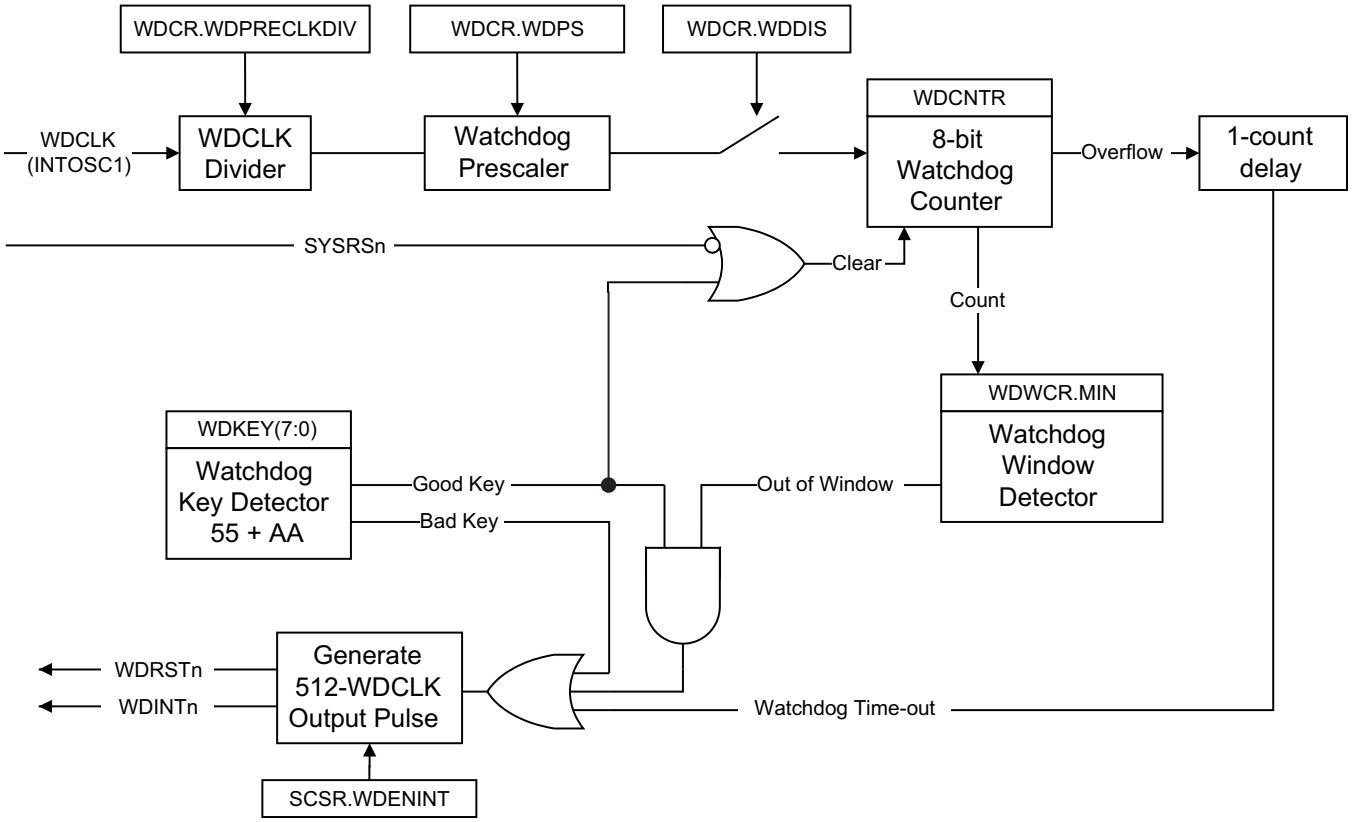



**Figure 6-4. Windowed Watchdog**

## 6.12 Configurable Logic Block (CLB)

TI uses the CLB to offer additional interfacing and control features for select C2000 devices. Functions that would otherwise be accomplished using external logic devices are now provided by on-chip TI solutions. For example, absolute encoder master protocol interfaces such as EnDat and BiSS are now provided as Position Manager solutions. In some solutions, the TI-configured CLB is used with other on-chip resources, such as the SPI port or the C28x CPU, to perform more complex functionality. In some cases, external communications transceivers may need to be added.

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# 7 Applications, Implementation, and Layout

**NOTE**

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 7.1 TI Design or Reference Design

The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at TIDesigns.


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# 8 Device and Documentation Support

## 8.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320 MCU devices and support tools. Each TMS320™ MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**320F280049). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

**TMX** Experimental device that is not necessarily representative of the final device's electrical specifications

**TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

**TMS** Fully qualified production device

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing

**TMDS** Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

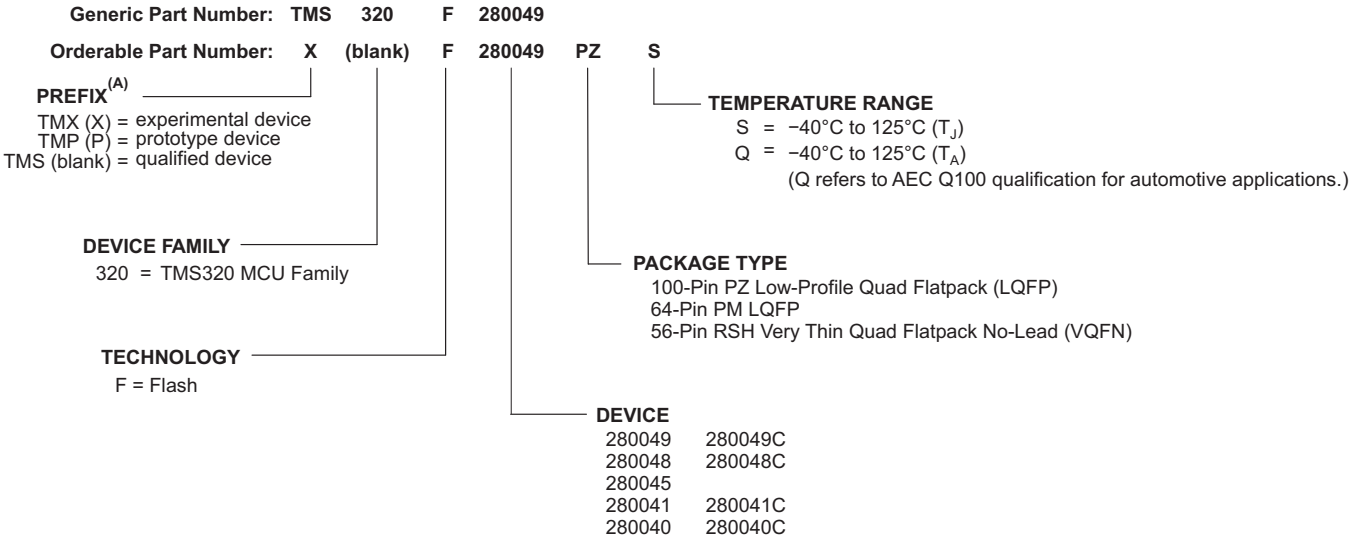
Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZ) and temperature range (for example, S).

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320F28004x Piccolo™ Microcontrollers Silicon Errata*.

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A. Prefixes X and P are used in orderable part numbers.

**Figure 8-1. Device Nomenclature**

## 8.2 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions follow. To view all available tools and software for C2000™ real-time control MCUs, visit the Tools & software for C2000™ real-time control MCUs page.

### Development Tools

F280049C controlCARD Evaluation Module

The F280049C controlCARD Evaluation Module is an HSEC180 controlCARD-based evaluation and development tool for the C2000™ Piccolo F28004x series of microcontroller products. controlCARDs are ideal to use for initial evaluation and system prototyping. controlCARDs are complete board-level modules that utilize one of two standard form factors (100-pin DIMM or 180-pin HSEC) to provide a low-profile single-board controller solution. For first evaluation, controlCARDs are typically purchased bundled with a baseboard or bundled in an application kit.

### Software Tools

C2000Ware for C2000 MCUs

C2000Ware for C2000™ microcontrollers is a cohesive set of development software and documentation designed to minimize software development time. From device-specific drivers and libraries to device peripheral examples, C2000Ware provides a solid foundation to begin development and evaluation of your product.

Code Composer Studio™ (CCS) Integrated Development Environment (IDE) for C2000 Microcontrollers

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking the user through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.


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Pin Mux Tool
The Pin Mux Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs.

F021 Flash Application Programming Interface (API)
The F021 Flash Application Programming Interface (API) provides a software library of functions to program, erase, and verify F021 on-chip Flash memory.

UniFlash Standalone Flash Tool
UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

**Models**

Various models are available for download from the product Tools & Software pages. These models include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Models section of the Tools & Software page for each device, which can be found in Table 8-1.

**Training**

Technical Introduction to the New C2000 TMS320F28004x Device Family

Discover the newest member to the C2000 MCU family. This presentation will cover the technical details of the Piccolo TMS320F28004x architecture and highlight the new improvements to various key peripherals, such as an enhanced Type 2 CLA capable of running a background task, and the inclusion of a set of high-speed programmable gain amplifiers. Also, a completely new boot mode flow enables expanded booting options. Where applicable, a comparison to the Piccolo TMS320F2807x MCU device series will be used, and some knowledge about the previous device architectures will be helpful in understanding the topics presented in this presentation.

C2000 Multi-Day Workshop
The C2000™ Microcontroller 3-Day Workshop will decrease the learning curve from months to days, reduce development time, and accelerate product time to market! The workshop is perfect for both the beginner and advanced users. Based on TI's latest F28x7x devices, this workshop combines many of the common features and peripherals found on the Piccolo™ and Delfino™ families, making it ideal for anyone interested in learning about the C2000 MCU family of devices.

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## 8.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral follows.

**Errata**

TMS320F28004x Piccolo™ Microcontrollers Silicon Errata describes known advisories on silicon and provides workarounds.

**Technical Reference Manual**

TMS320F28004x Piccolo Microcontrollers Technical Reference Manual details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the F28004x microcontrollers.

**InstaSPIN Technical Reference Manuals**

InstaSPIN-FOC™ and InstaSPIN-MOTION™ User's Guide describes the InstaSPIN-FOC and InstaSPIN-MOTION devices.

**CPU User's Guides**

TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

TMS320C28x Extended Instruction Sets Technical Reference Manual describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

**Peripheral Guides**

C2000 Real-Time Control Peripherals Reference Guide describes the peripheral reference guides of the 28x DSPs.

**Tools Guides**

TMS320C28x Assembly Language Tools v18.1.0.LTS User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

TMS320C28x Optimizing C/C++ Compiler v18.1.0.LTS User's Guide describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

**Application Reports**

Semiconductor Packing Methodology describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

Calculating Useful Lifetimes of Embedded Processors provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

An Introduction to IBIS (I/O Buffer Information Specification) Modeling discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures, and future trends.


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## 8.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 8-1. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TMS320F280049 | Click here | Click here | Click here | Click here | Click here |
| TMS320F280049C | Click here | Click here | Click here | Click here | Click here |
| TMS320F280048 | Click here | Click here | Click here | Click here | Click here |
| TMS320F280048C | Click here | Click here | Click here | Click here | Click here |
| TMS320F280045 | Click here | Click here | Click here | Click here | Click here |
| TMS320F280041 | Click here | Click here | Click here | Click here | Click here |
| TMS320F280041C | Click here | Click here | Click here | Click here | Click here |
| TMS320F280040 | Click here | Click here | Click here | Click here | Click here |
| TMS320F280040C | Click here | Click here | Click here | Click here | Click here |

## 8.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.6 Trademarks

InstaSPIN-FOC, FAST, Piccolo, TMS320C2000, C2000, Code Composer Studio, TMS320, Delfino, E2E are trademarks of Texas Instruments.
Bosch is a registered trademark of Robert Bosch GmbH Corporation.
All other trademarks are the property of their respective owners.

## 8.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.8 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

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# 9 Mechanical, Packaging, and Orderable Information

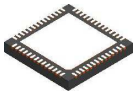
## 9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

For packages with a thermal pad, the MECHANICAL DATA figure shows a generic thermal pad without dimensions. For the actual thermal pad dimensions that are applicable to this device, see the THERMAL PAD MECHANICAL DATA figure.


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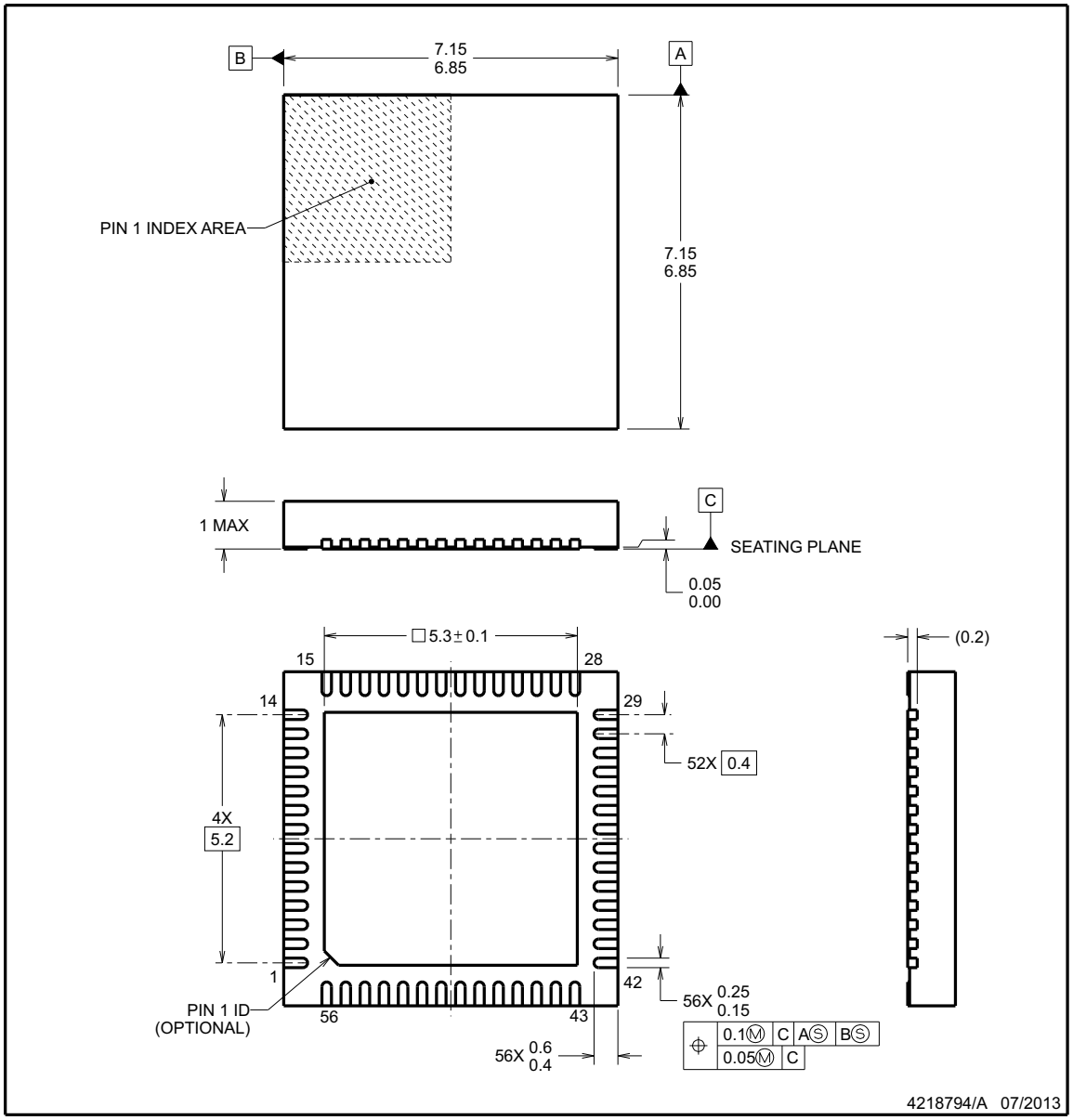
# PACKAGE OUTLINE



## RSH0056D

VQFN - 1 mm max height

VQFN




NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

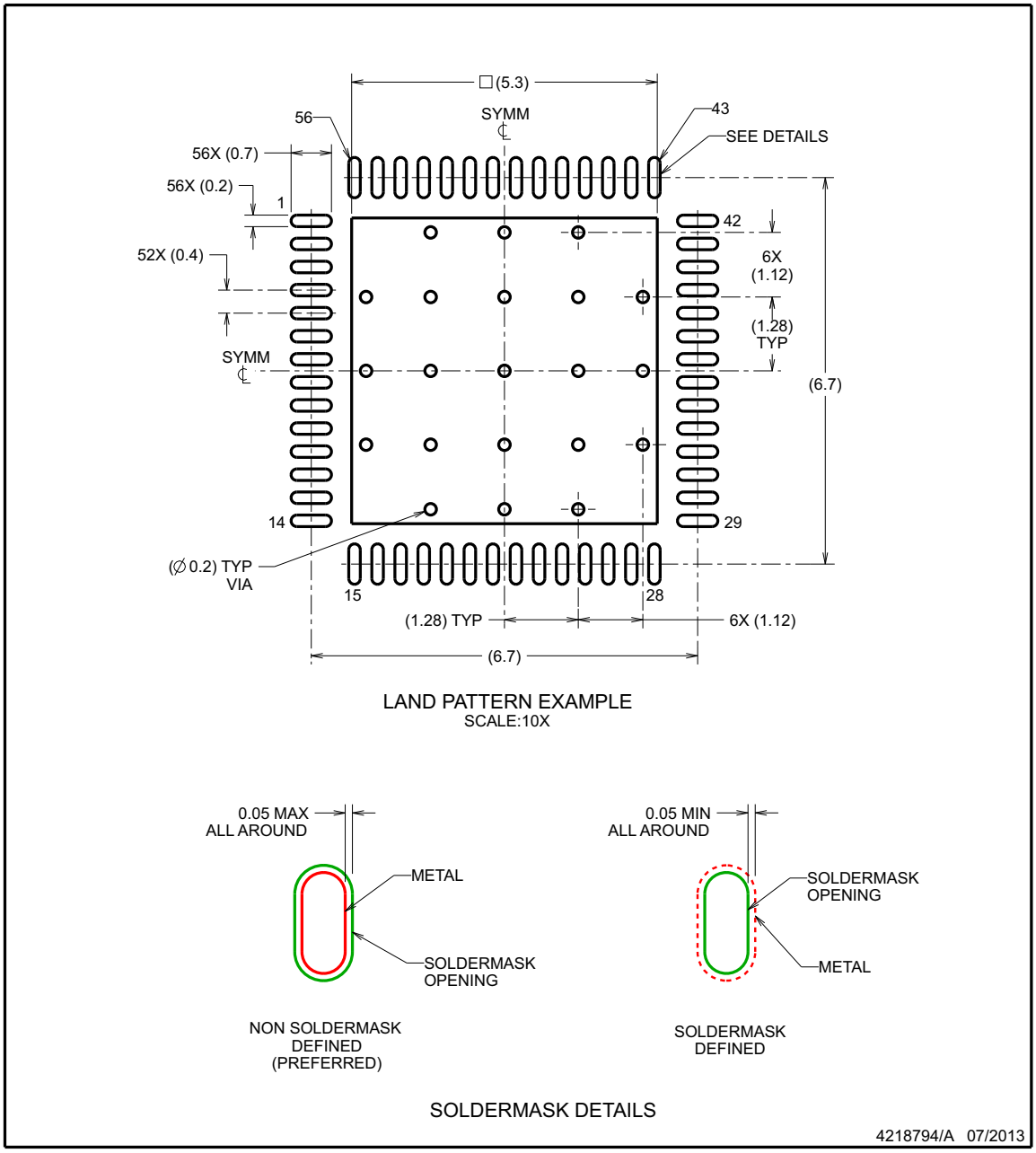


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## EXAMPLE BOARD LAYOUT

### RSH0056D — VQFN - 1 mm max height

VQFN




NOTES: (continued)

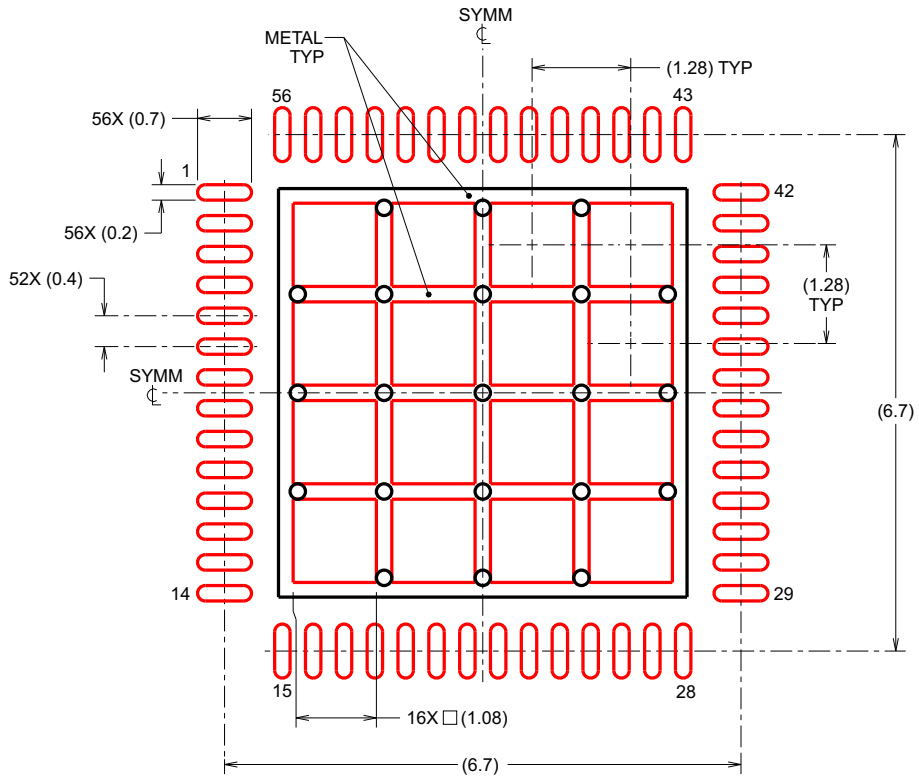
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).


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# EXAMPLE STENCIL DESIGN

## RSH0056D VQFN - 1 mm max height

VQFN




SOLDERPASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:12X

4218794/A 07/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| F280040CPMQR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280040CPMQ | Samples |
| F280040PMQR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280040PMQ | Samples |
| F280041CPMS | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280041CPMS | Samples |
| F280041CPZQR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280041CPZQ | Samples |
| F280041CPZS | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280041CPZS | Samples |
| F280041CRSHSR | ACTIVE | VQFN | RSH | 56 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280041C RSHS | Samples |
| F280041PMS | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280041PMS | Samples |
| F280041PMSR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280041PMS | Samples |
| F280041PZQR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280041PZQ | Samples |
| F280041PZS | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280041PZS | Samples |
| F280041PZSR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280041PZS | Samples |
| F280041RSHSR | ACTIVE | VQFN | RSH | 56 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280041 RSHS | Samples |
| F280045PMS | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280045PMS | Samples |
| F280045PMSR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280045PMS | Samples |
| F280045PZS | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280045PZS | Samples |
| F280045PZSR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280045PZS | Samples |
| F280045RSHSR | ACTIVE | VQFN | RSH | 56 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280045 RSHS | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| F280048CPMQR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280048CPMQ | Samples |
| F280048PMQR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280048PMQ | Samples |
| F280049CPMS | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049CPMS | Samples |
| F280049CPZQR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049CPZQ | Samples |
| F280049CPZS | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049CPZS | Samples |
| F280049CRSHS | PREVIEW | VQFN | RSH | 56 | 90 | TBD | Call TI | Call TI | -40 to 125 | | |
| F280049CRSHSR | ACTIVE | VQFN | RSH | 56 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049C RSHS | Samples |
| F280049PMS | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049PMS | Samples |
| F280049PMSR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049PMS | Samples |
| F280049PZQ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049PZQ | Samples |
| F280049PZQR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049PZQ | Samples |
| F280049PZS | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049PZS | Samples |
| F280049PZSR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049PZS | Samples |
| F280049RSHSR | ACTIVE | VQFN | RSH | 56 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280049 RSHS | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

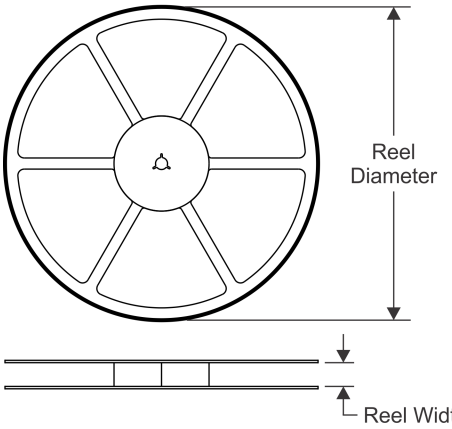
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

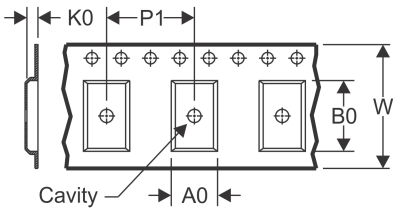
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

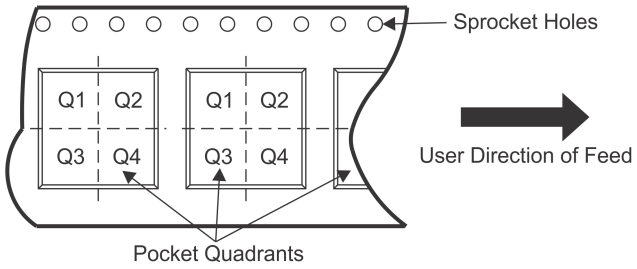



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

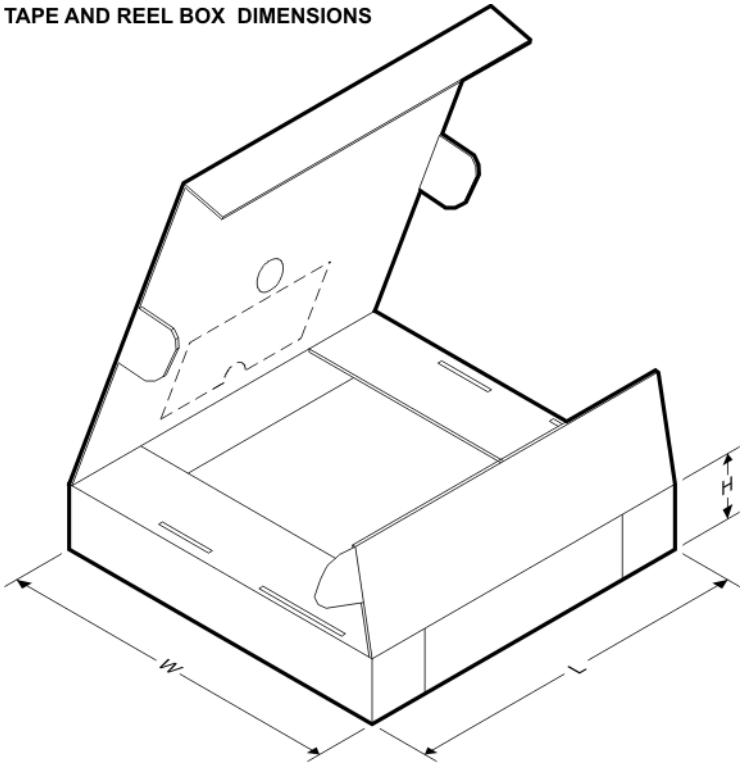
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F280040CPMQR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280040PMQR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280041CPZQR | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| F280041CRSHSR | VQFN | RSH | 56 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| F280041PMSR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280041PZQR | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| F280041RSHSR | VQFN | RSH | 56 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| F280045PMSR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280045PZSR | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| F280045RSHSR | VQFN | RSH | 56 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| F280048CPMQR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280048PMQR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280049CPZQR | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| F280049CRSHSR | VQFN | RSH | 56 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| F280049PMSR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280049PZQR | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| F280049PZSR | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| F280049RSHSR | VQFN | RSH | 56 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

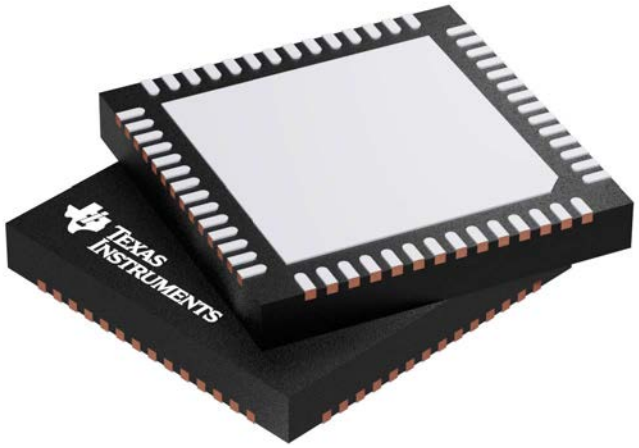
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| F280040CPMQR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280040PMQR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280041CPZQR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| F280041CRSHSR | VQFN | RSH | 56 | 2500 | 336.6 | 336.6 | 31.8 |
| F280041PMSR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280041PZQR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| F280041RSHSR | VQFN | RSH | 56 | 2500 | 336.6 | 336.6 | 31.8 |
| F280045PMSR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280045PZSR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| F280045RSHSR | VQFN | RSH | 56 | 2500 | 336.6 | 336.6 | 31.8 |
| F280048CPMQR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280048PMQR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280049CPZQR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| F280049CRSHSR | VQFN | RSH | 56 | 2500 | 336.6 | 336.6 | 31.8 |
| F280049PMSR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280049PZQR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| F280049PZSR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| F280049RSHSR | VQFN | RSH | 56 | 2500 | 336.6 | 336.6 | 31.8 |

# GENERIC PACKAGE VIEW

## RSH 56

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

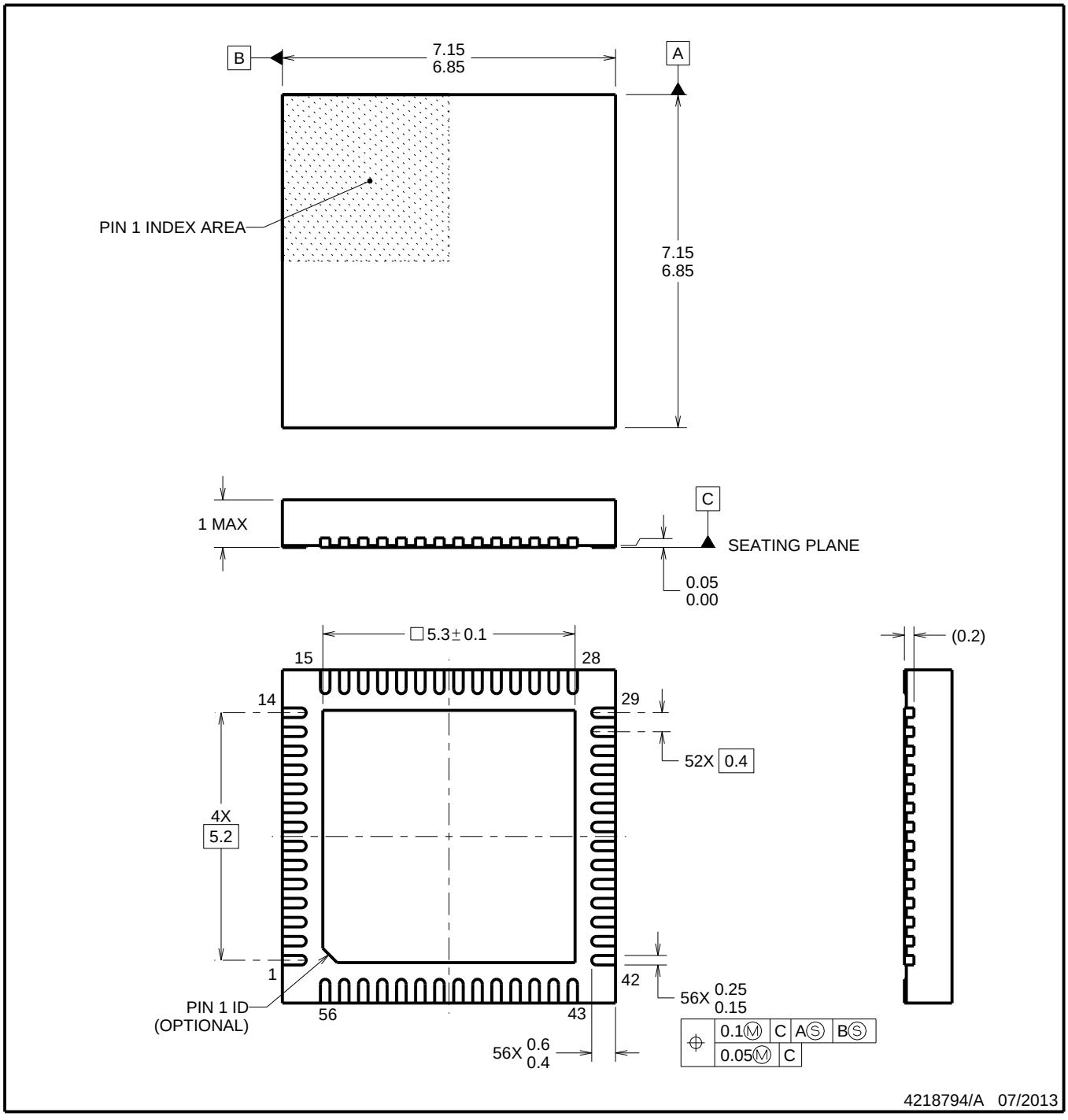
4207513/D



# RSH0056D

## VQFN - 1 mm max height

VQFN




NOTES:

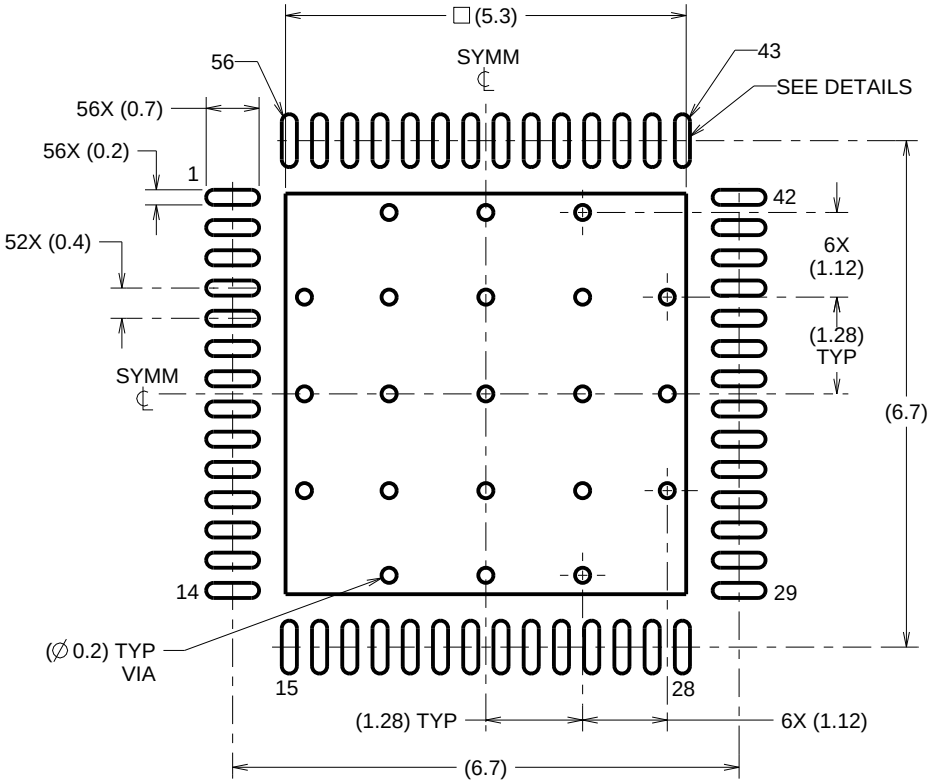
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

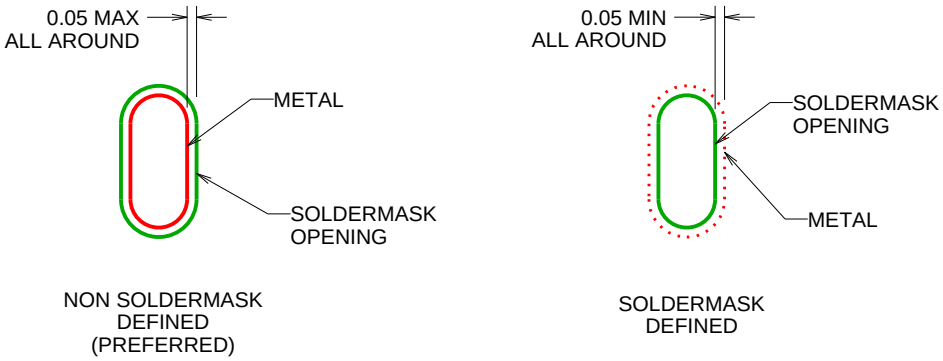
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

RSH0056D VQFN - 1 mm max height

VQFN




LAND PATTERN EXAMPLE
SCALE:10X




SOLDERMASK DETAILS

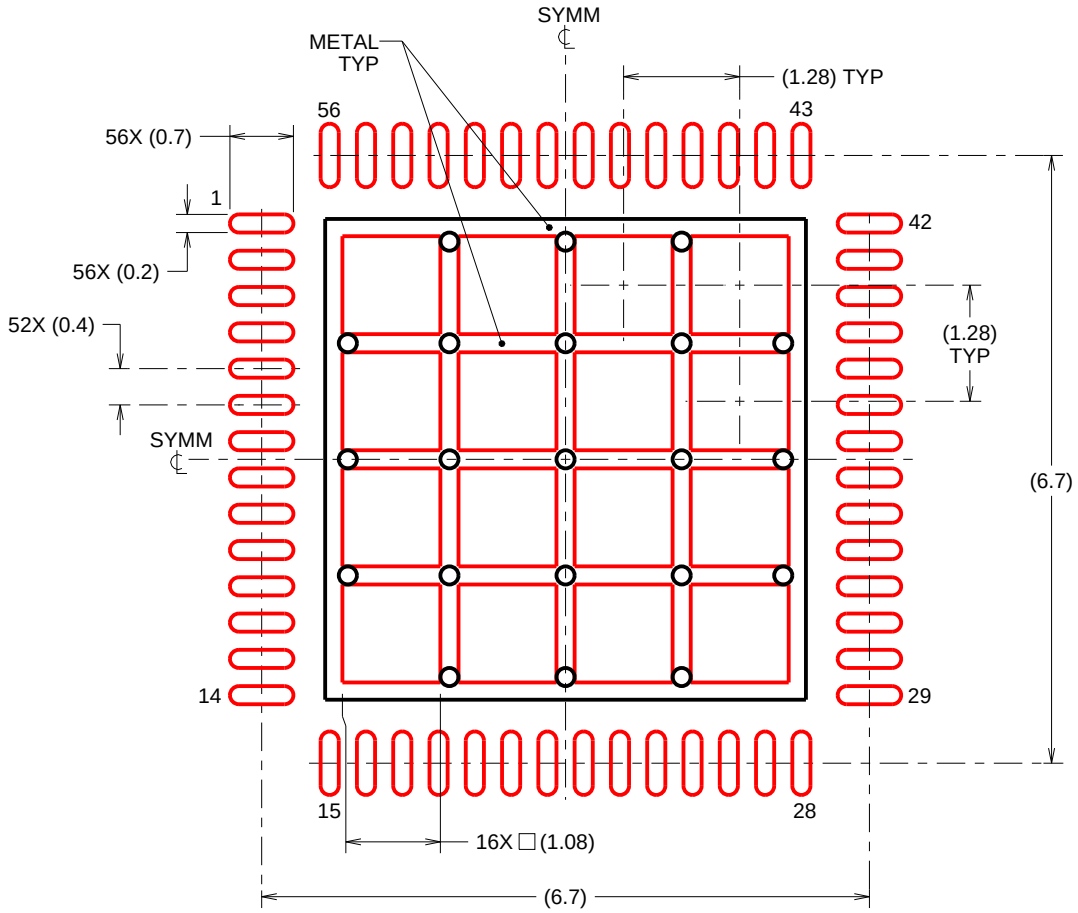
4218794/A 07/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

RSH0056D VQFN - 1 mm max height

VQFN




SOLDERPASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

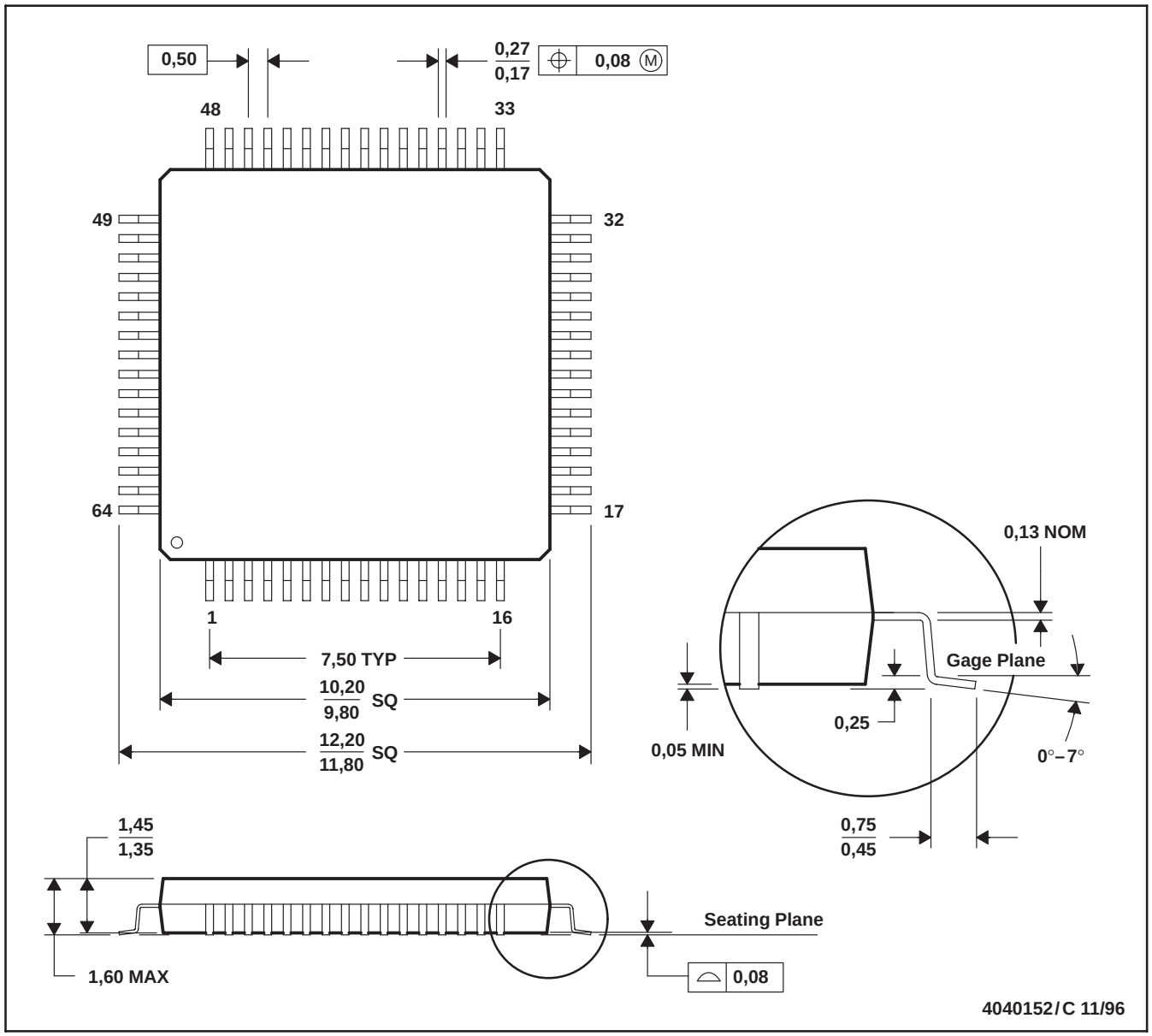
EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:12X

4218794/A 07/2013

NOTES: (continued)

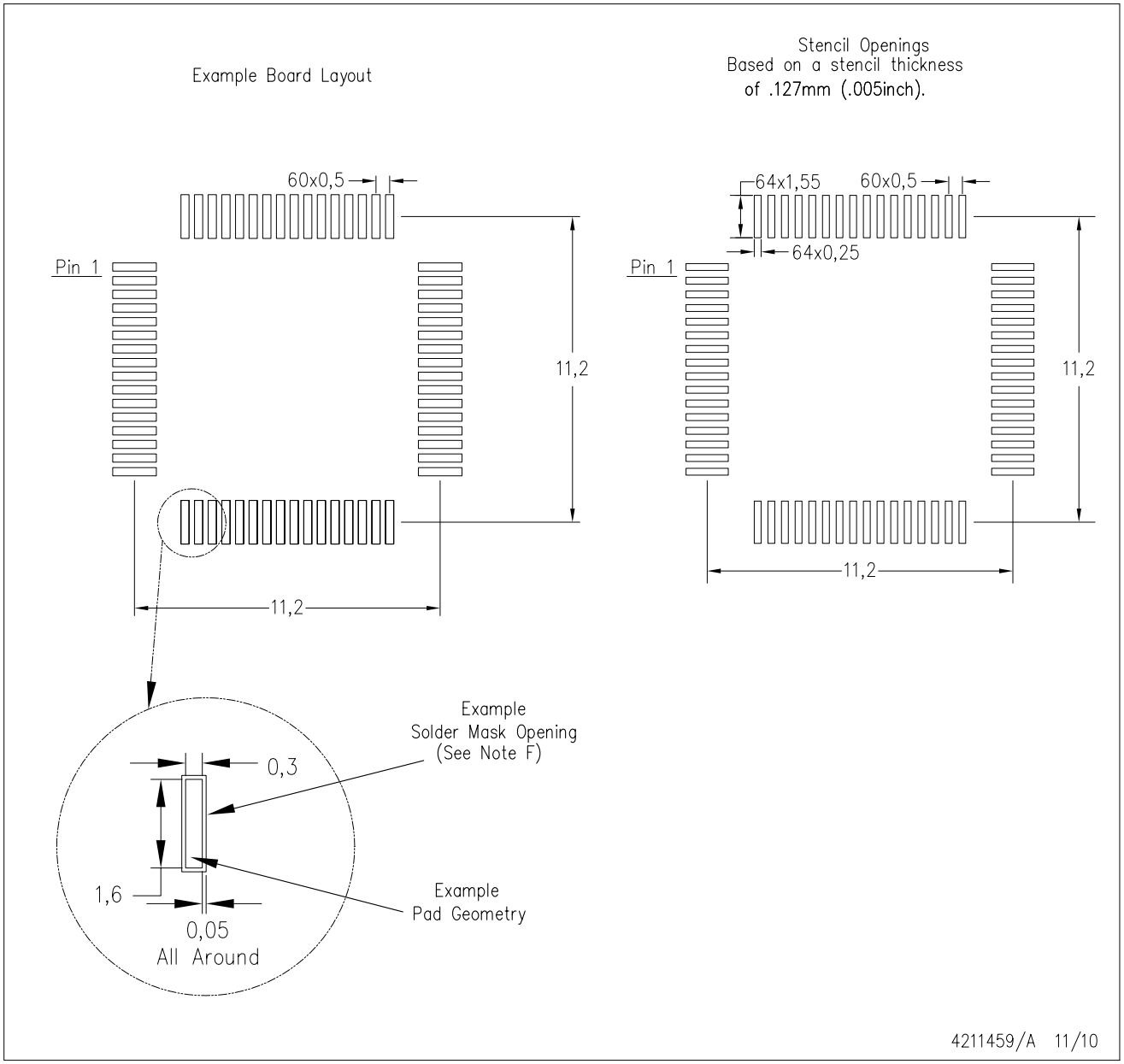
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PM (S-PQFP-G64)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

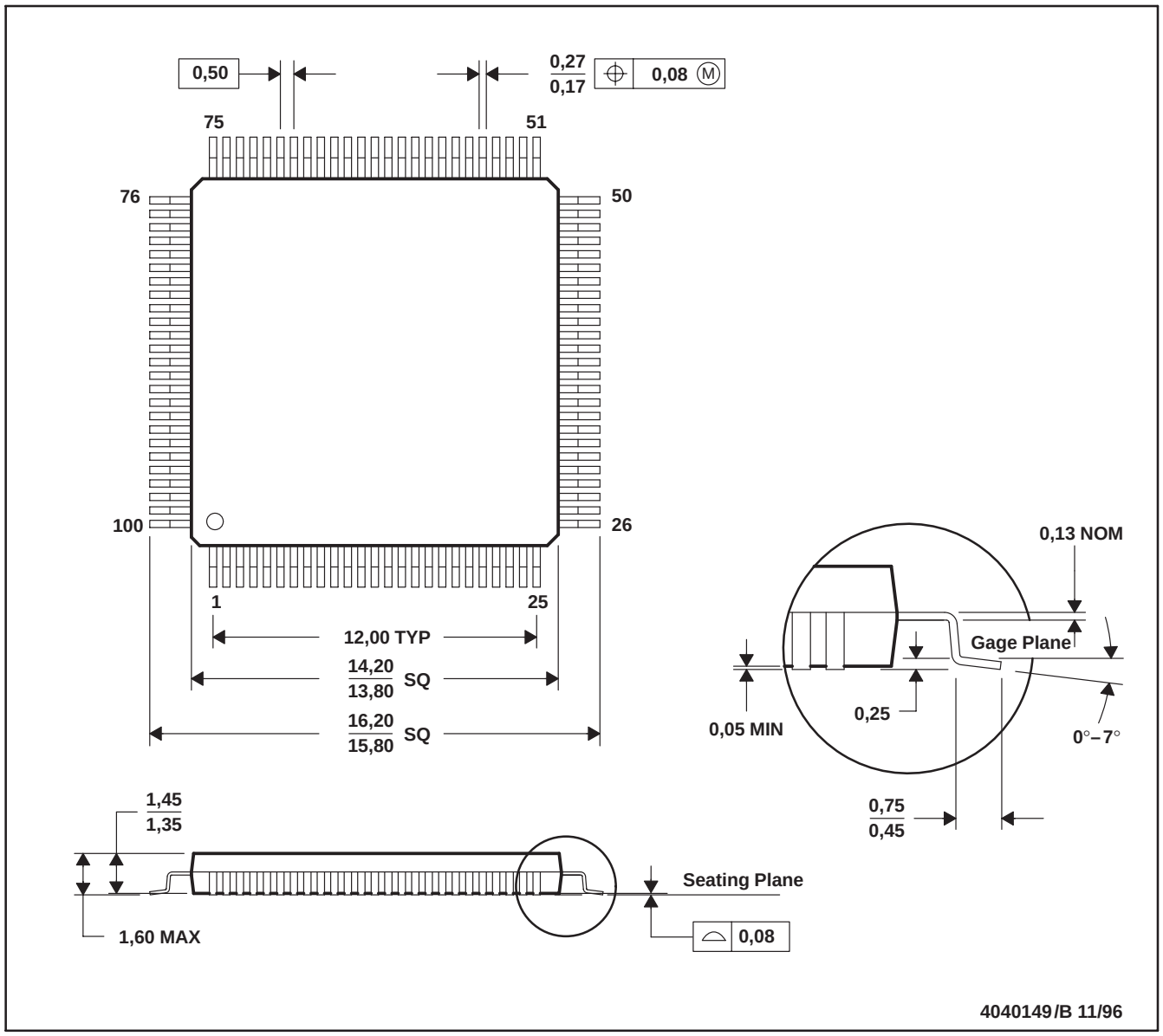
PM (S–PQFP–G64) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

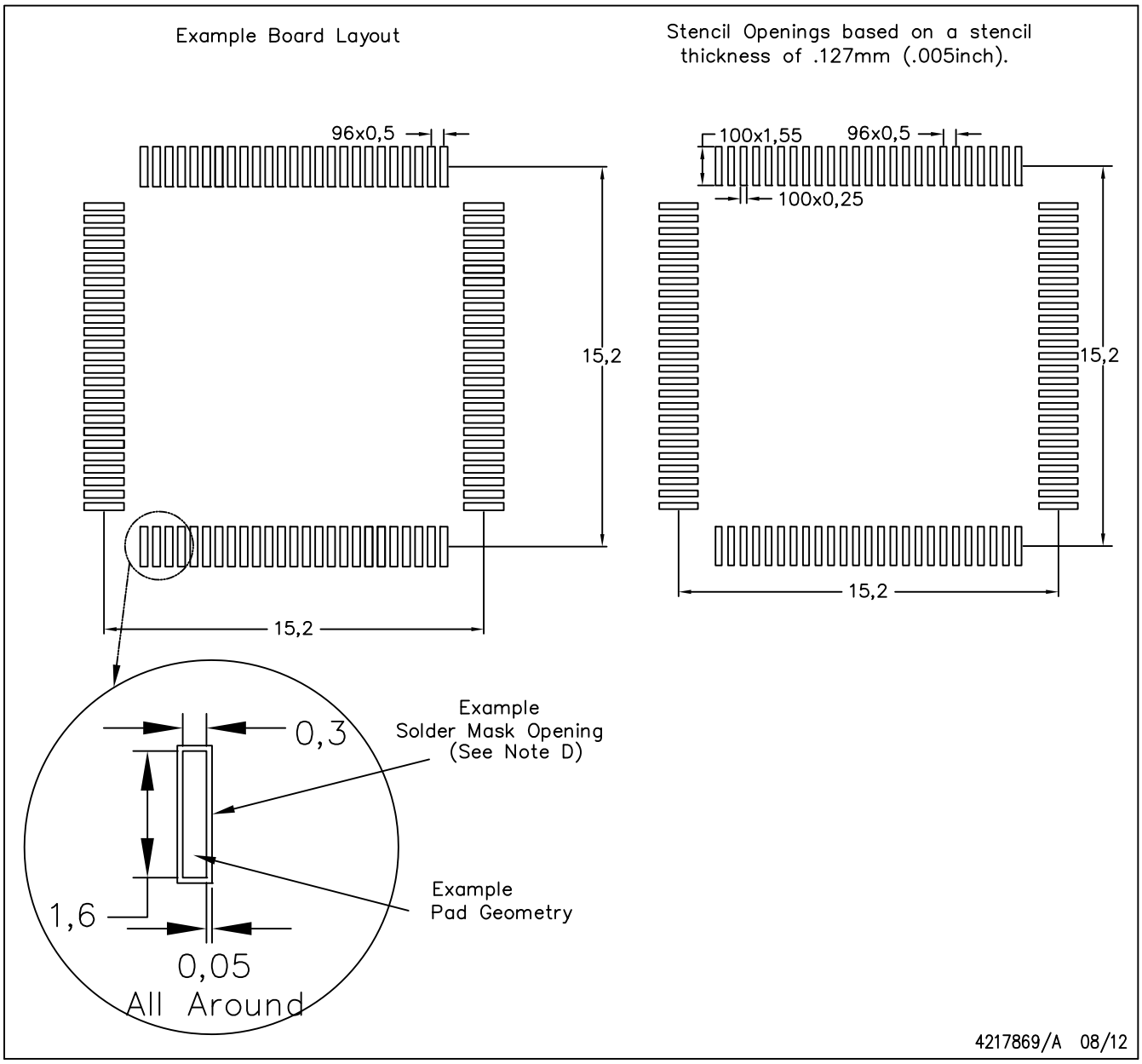
MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

**PZ (S-PQFP-G100)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

# PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK




NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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