The Analog Mixed Signal Company

Data Sheet

Rev. 1.08 / August 2011

ZSC31150

Fast Automotive Sensor Signal Conditioner



ZSC31150

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Brief Description

The ZSC31150 is a CMOS integrated circuit for highly-accurate amplification and sensor-specific correction of bridge sensor signals. Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via an internal 16-bit RISC microcontroller running a correction algorithm, with calibration coefficients stored in an EEPROM.

The ZSC31150 is adjustable to nearly all bridge sensor types. Measured values are provided at the analog voltage output or at the digital ZACwire™ and I²C™ interface. The digital interface can be used for a simple PC-controlled calibration procedure, in order to program a set of calibration coefficients into an on-chip EEPROM. Thus, a specific sensor and a ZSC31150 are mated digitally: fast, precise, and without the cost overhead associated with trimming by external devices or a laser.

Features

- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity
- Adjustable to nearly all bridge sensor types, analog gain of 420, overall gain up to 2000
- Output options: ratiometric analog voltage output (5 - 95% in maximum, 12.4 bit resolution) or ZACwire™ (digital one-wire-interface)
- Temperature compensation: internal or external diode, bridge resistance, thermistor
- Sensor biasing by voltage or constant current
- Sample rate up to 7.8 kHz
- High voltage protection up to 33 V
- Supply current: max. 5.5mA
- Reverse polarity and short circuit protection
- Wide operation temperature up to -40…+150°C
- Traceability by user-defined EEPROM entries
- Several safety and diagnostic functions

Benefits

- No external trimming components required
- Only a few external protection devices needed
- PC-controlled configuration and One-Shot calibration via I²C™ or ZACwire™ interface: Simple, cost efficient, quick, and precise
- End-of-Line calibration via I²C™ or ZACwire™ interface
- High accuracy (0.25% FSO @ -25 to 85°C; 0.5% FSO @ -40 to 125°C)
- The ZSC31150 is optimized for automotive environments by its special protection circuitry and excellent electromagnetic compatibility

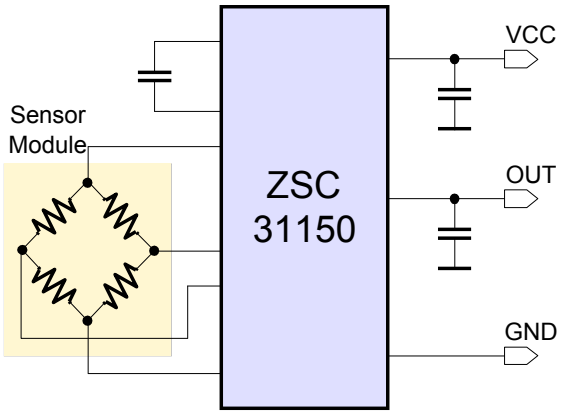
Available Support

- Evaluation Kits
- Application Notes
- Mass calibration setup

Physical Characteristics

- Supply voltage 4.5 to 5.5 V
- Operation temperature: -40°C to 125°C (-40°C to +150°C derated, depending on product version)
- Available in SSOP14 or as die

ZSC31150 Application Circuit



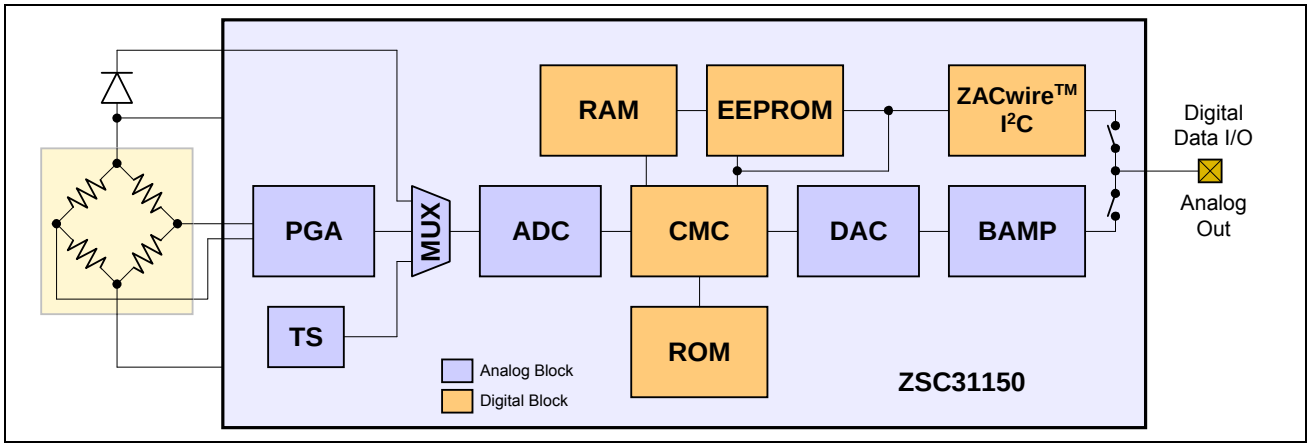
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ZSC31150

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ZSC31150 Block Diagram



Ordering Information

Example: **ZSC31150 F A G1 - T**

ZMDI Product Sales Name

Design Revision
The revision level is indicated alphabetically beginning with A for first revision level

Target Application Area/
Normal Operating Temperature Range
A = Automotive (-40°C to +125°C)
E = Extended Automotive (-40°C to +150°C, 1000h@150°C)
L = Long Life Automotive (-40°C to +150°C, 5000h@150°C)

Delivery Form *
T = Delivery in tube
R = Delivery in tape on reel

Die/Package Options
B = Tested dice on unsawn wafer
C = Tested dice on frame
D = Tested dice in waffle pack
G1 = Finished parts, RoHS-compliant, in plastic package

* Only for finished parts in plastic package
Not all possible combinations are available. Please ask ZMDI sales

Product Sales Code	Description	Package
ZSC31150KIT Evaluation Kit V1.0	Modular evaluation and development boards for ZSC31150	KIT boards, IC samples, USB cable, DVD with software and documentation
ZSC31150 Mass Calibration System V1.1	Modular Mass Calibration System (MSC) for ZSC31150	MCS boards, cable, connectors, DVD with software and documentation

Sales and Further Information

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Contents

1 Electrical Characteristics 6
1.1. Absolute Maximum Ratings 6
1.2. Operating Conditions 6
1.3. Electrical Parameters 7
1.3.1. Supply Current and System Operation Conditions 7
1.3.2. Analog Front-End (AFE) Characteristics 7
1.3.3. Temperature Measurement (refer chapter 2.4) 7
1.3.4. AD-Conversion 7
1.3.5. Sensor Connection Check 8
1.3.6. DAC & Analog Output (Pin AOUT) 8
1.3.7. System Response 8
1.4. Interface Characteristics & EEPROM 9
1.4.1. I²C™ Interface (refer 'ZSC31150 Functional Description' for timing details) 9
1.4.2. ZACwire™ One Wire Interface (OWI) 9
1.4.3. EEPROM 9
2 Circuit Description 10
2.1. Signal Flow 10
2.2. Application Modes 11
2.3. Analog Front End (AFE) 11
2.3.1. Programmable Gain Amplifier (PGA) 11
2.3.2. Offset Compensation 12
2.3.3. Measurement Cycle 12
2.3.4. Analog-to-Digital Converter 13
2.4. Temperature Measurement 14
2.5. System Control and Conditioning Calculation 15
2.5.1. Operation Modes 15
2.5.2. Start Up Phase 15
2.5.3. Conditioning Calculation 15
2.6. Analog Output AOUT 16
2.7. Serial Digital Interface 16
2.8. Failsafe Features, Watchdog and Error Detection 16
2.9. High Voltage, Reverse Polarity and Short Circuit Protection 17
3 Application Circuit Examples 18
4 Pin Configuration, Latch-Up and ESD Protection 20
4.1. Pin Configuration and Latch-up Conditions 20
4.2. ESD-Protection 20
5 Package 21
6 Quality and Reliability 21
7 Customization 21
8 Ordering Information 22
9 Additional Documents 22
10 Glossary 23
11 Document Revision History 24

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List of Figures

Figure 2.1 Block Diagram of the ZSC31150 10
Figure 2.2: Measurement Cycle 13
Figure 3.1: Bridge in Voltage Mode, External Diode Temperature Sensor 18
Figure 3.2: Bridge in Voltage Mode, External Thermistor 19
Figure 3.3: Bridge in Current Mode, Temperature Measurement via Bridge TC 19
Figure 5.1: ZSC31150 Pin Diagram 21

List of Tables

Table 1.1 Absolute Maximum Ratings 6
Table 1.2 Operating Conditions 6
Table 2.1 Adjustable Gains, Resulting Sensor Signal Spans and Common Mode Ranges 11
Table 2.2 Analog Zero Point Shift Ranges (XZC) 12
Table 2.3: Analog Output Resolution Versus Sample Rate 14
Table 3.1: Application Circuit Parameters 18
Table 4.1: Pin Configuration and Latch-Up Conditions 20

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1 Electrical Characteristics

1.1. Absolute Maximum Ratings

Parameters apply in operation temperature range and without time limitations.

Table 1.1 Absolute Maximum Ratings

No.	Parameter	Symbol	Conditions	Min	Max	Unit
1.1.1	Supply Voltage [1]	$VDDE_{AMR}$	To VSSE, refer to chapter 3 for application circuits	-33	33	VDC
1.1.2	Potential at pin AOUT [1]	V_{OUT}	Related to VSSE	-33	33	VDC
1.1.3	Analog Supply Voltage [1]	$VDDA_{AMR}$	Related to VSSA, VDDE - VDDA < 0.35 V	-0.3	6.5	VDC
1.1.4	Voltage at all analog and digital IO – Pins	V_{A_IO} V_{D_IO}	Related to VSSA	-0.3	VDDA + 0.3	VDC
1.1.5	Storage temperature	T_{STG}		-55	150	°C

1.2. Operating Conditions

All voltages are related to VSSA.

Table 1.2 Operating Conditions

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.2.1	Ambient temperature [2]	T_{AMB}	TQE	-40		150	°C
1.2.2.1	Ambient temperature advanced performance [4]	T_{AMB_TQA}	TQA	-40		125	°C
1.2.2.2	Ambient temperature advanced performance [4]	T_{AMB_TQI}	TQI	-25		85	°C
1.2.3	Supply Voltage	VDDE		4.5	5.0	5.5	VDC
1.2.4	Bridge Resistance [3, 4]	R_{BR_V}	Bridge Voltage Mode	2		25	kΩ
1.2.5	Bridge Resistance [3, 4]	R_{BR_C}	Bridge Current Excitation, note I_{BR_MAX}			10	kΩ
1.2.6	Resistor R_{IBR} [4]	R_{IBR}	I_{BR} = VDDA / (16 * R_{IBR})	0.07 * R_{BR}			kΩ
1.2.7	Maximum Bridge Current	I_{BR_MAX}				2	mA
1.2.8	Maximum Bridge Top Voltage	V_{BR_TOP}				($^{15}/_{16}$ * VDDA) - 0.3	V
1.2.9	TC Current Reference Resistor [4]	TC R_{IBR}	Behavior influences generated current		50		ppm/K

[1] Refer to the 'ZSC31150 High Voltage Protection Description' for specification and detailed conditions
[2] Notice temperature profile description in the 'ZSC31150 Dice Package Document' for operation in temperature range > 125 °C
[3] Symmetric behavior and identical electrical properties (especially with regard to the low pass characteristic) of both sensor inputs of the ZSC31150 are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins of ZSC31150 can generate a failure in signal operation
[4] No measurement in mass production, parameter is guaranteed by design and/or quality observation.

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1.3. Electrical Parameters

All parameter values are valid on behalf on in chapter 1.2 specified operating conditions (special definitions excluded). All Voltages related to VSSA.

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.1. Supply Current and System Operation Conditions							
1.3.1.1	Supply current	T_{ADV}	Without bridge and load current, $f_{CLK} \leq 3$ MHz			5.5	mA
1.3.1.2	Clock frequency	T_{AMB_TQA}	Guaranteed adjustment range	2 [1]	3	4 [1]	MHz
1.3.2. Analog Front-End (AFE) Characteristics							
1.3.2.1	Input Span	V_{IN_SP}	Analog gain: 420 to 2.8	1		275	mV/V
1.3.2.2	Analog Offset Compensation Range		Depends on gain adjust, refer to chapter 2.3.2	-300		300	% V_{IN_SP}
1.3.2.3	Parasitic differential input offset current [1]	I_{IN_OFF}	Within T_{AMB}; Within T_{AMB_TQI}	-10 -2		10 2	nA nA
1.3.2.4	Common mode input range	V_{IN_CM}	Depends on gain adjust, no XZC, refer to chapter 2.3.1	0.29 * VDDA		0.65 * VDDA	V
1.3.3. Temperature Measurement (refer chapter 2.4)							
1.3.3.1	External temperature diode channel gain	A_{TSED}		300		1300	ppm FS / (mV/V)
1.3.3.2	External temperature diode bias current	I_{TSE}		6	10	20	µA
1.3.3.3	External temperature diode input range [1]			0		1.5	V
1.3.3.4	External temperature resistor channel gain	A_{TSER}		1200		3500	ppm FS / (mV/V)
1.3.3.5	External temperature resistor / input voltage range [1]	V_{TSER}		0		600	mV/V
1.3.3.6	Internal temperature diode sensitivity	ST_{TSI}	raw values – without conditioning	700		2700	ppm FS / K
1.3.4. AD-Conversion							
1.3.4.1	A/D Resolution [1]	r_{ADC}		13		16	Bit
1.3.4.2	DNL [1]	DNL_{ADC}	r_{ADC} =13Bit, f_{CLK}=3MHz, best fit, 2nd order, complete AFE, 1.3.4.5			0.95	LSB
1.3.4.3	INL TQA [1]	INL_{ADC}				4	LSB
1.3.4.4	INL TQE	INL_{ADC}				5	LSB
1.3.4.5	ADC Input Range	Range		10		90	%VDDA

[1] No measurement in mass production, parameter is guaranteed by design and/or quality observation.

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No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.5. Sensor Connection Check							
1.3.5.1	Sensor connection loss	R_{SCC_min}	detection threshold	100			kΩ
1.3.5.2	Sensor input short	R_{SSC_short}	short detection guaranteed	0		50	Ω
1.3.5.3	Sensor input no short	R_{SSC_pass}	short is never detected	1000			Ω
1.3.6. DAC & Analog Output (Pin AOUT)							
1.3.6.1	D/A Resolution	r_{DAC}	analog output, 10-90%		12		Bit
1.3.6.2	Output current sink and source for VDDE=5V	$I_{SRC/SINK_OUT}$	V_{OUT}: 5-95%, R_{LOAD}>=2kΩ V_{OUT}: 10-90%, R_{LOAD}>=1kΩ			2.5 5	mA
1.3.6.3	Short circuit current	I_{OUT_max}	to VSSE/VDDE [1]	-25		25	mA
1.3.6.4	Addressable output signal range	V_{SR_OUT95} V_{SR_OUT90}	@ R_{LOAD}>=2kΩ @ R_{LOAD}>=1kΩ	0.05 0.1		0.95 0.9	VDDE
1.3.6.5	Output slew rate [2]	SR_{OUT}	C_{LOAD} < 50nF	0.1			V/µs
1.3.6.6	Output resistance in diagnostic mode	R_{OUT_DIA}	Diagnostic Range: <4|96>%, R_{LOAD}>=2kΩ <8|92>%, R_{LOAD}>=1kΩ			82	Ω
1.3.6.7	Load capacitance [2]	C_{LOAD}	C3 + CL (refer chapter 3)			150	nF
1.3.6.8	DNL	DNL_{OUT}		-1.5		1.5	LSB
1.3.6.9	INL TQA [2]	INL_{OUT}	best fit, r_{DAC} =12Bit	-5		5	LSB
1.3.6.10	INL TQE	INL_{OUT}	best fit, r_{DAC} =12Bit	-8		8	LSB
1.3.6.11	Output Leakage current @ 150grd	I_{LEAK_OUT}	in case of power or ground loss	-25		25	µA
1.3.7. System Response							
1.3.7.1	Startup time [3]	t_{STA}	to 1st output, f_{CLK}=3MHz, no ROM check, ADC: 14bit & 2nd order			5	ms
1.3.7.2	Response time (100% jump) [2]	t_{RESP}	f_{CLK}=4MHz, 13Bit, 2nd order, refer Table 2.3	256		512	µs
1.3.7.3	Bandwidth [2]		comparable to analog SSCs		5		kHz
1.3.7.4	Analog Output Noise Peak-to-Peak [2]	$V_{NOISE,PP}$	shorted inputs, gain= bandwidth ≤ 10kHz			10	mV
1.3.7.5	Analog Output Noise RMS [2]	$V_{NOISE,RMS}$	shorted inputs, gain= bandwidth ≤ 10kHz			3	mV

1 minimum output voltage to VDDE or maximum output voltage to VSSE
2 No measurement in mass production, parameter is guaranteed by design and/or quality observation.
3 Depends on resolution and configuration - start routine begins approximately 0.8ms after power on

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No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.7.6	Ratiometricity Error	RE_{OUT_5}	maximum error of VDDE=5V to 4.5/5.5V			1000	ppm
1.3.7.7	Overall failure (deviation from ideal line including INL, gain, offset & temp errors)	F_{ALL} TQI F_{ALL} TQA F_{ALL} TQE	13Bit 2nd order ADC, f_{CLK}<=3MHz, XZC=0[1], no sensor caused effects; inside of parenthesis: digital readout		0.25 (0.1) 0.5 (0.25) 1.0 (0.5)		% FS

1.4. Interface Characteristics & EEPROM

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.4.1. I²C™ Interface (refer 'ZSC31150 Functional Description' for timing details)							
1.4.1.1	Input-High-Level [2]	$V_{I^2C_IN_H}$		0.8			VDDA
1.4.1.2	Input-Low-Level [2]	$V_{I^2C_IN_L}$				0.2	VDDA
1.4.1.3	Output-Low-Level [2]	$V_{I^2C_OUT_L}$	Open Drain, I_{OL}<2mA			0.15	VDDA
1.4.1.4	SDA load capacitance [2]	C_{SDA}				400	pF
1.4.1.5	SCL clock frequency [2]	f_{SCL}				400	kHz
1.4.1.6	Internal pull-up resistor [2]	R_{I^2C}		25		100	kΩ
1.4.2. ZACwire™ One Wire Interface (OWI)							
1.4.2.1	Input-Low-Level [2]	$V_{OWI_IN_L}$				0.2	VDDA
1.4.2.2	Input-High-Level [2]	$V_{OWI_IN_H}$		0.75			VDDA
1.4.2.3	Output-Low-Level [2]	$V_{OWI_OUT_L}$	Open Drain, I_{OL}<2mA			t.b.d.	VDDA
1.4.2.4	Start Window [2]		typ: @ f_{CLK}=3MHz	96	175	455	ms
1.4.3. EEPROM							
1.4.3.1	Ambient temperature EEPROM programming [2]	T_{AMB_EEP}		-40		150	°C
1.4.3.2	Write cycles [2]	n_{WRI_EEP}	@write <= 85°C @write up to 150°C			100k 100	
1.4.3.3	Read cycles [2]	n_{READ_EEP}	<=175°C [3]			$8 * 10^8$	
1.4.3.4	Data retention [2]	t_{RET_EEP}	1300h @ 175°C [4] (=100000h@55°C & 27000h@125°C & 3000h@150°C)			15	a
1.4.3.5	Programming time [2]	t_{WRI_EEP}	per written word, f_{CLK}=3MHz		12		ms

1 XZC is active: additional overall failure of 25ppm/K for XZC=31 in maximum, failure decreases linear for XZC adjusts lower than 31
2 No measurement in mass production, parameter is guaranteed by design and/or quality observation.
3 valid for the dice, notice additional package and temperature version caused restrictions
4 over lifetime and valid for the dice, use calculation sheet 'ZMDI Temperature Profile Calculation Sheet' for temperature stress calculation, notice additional package and temperature version caused restrictions

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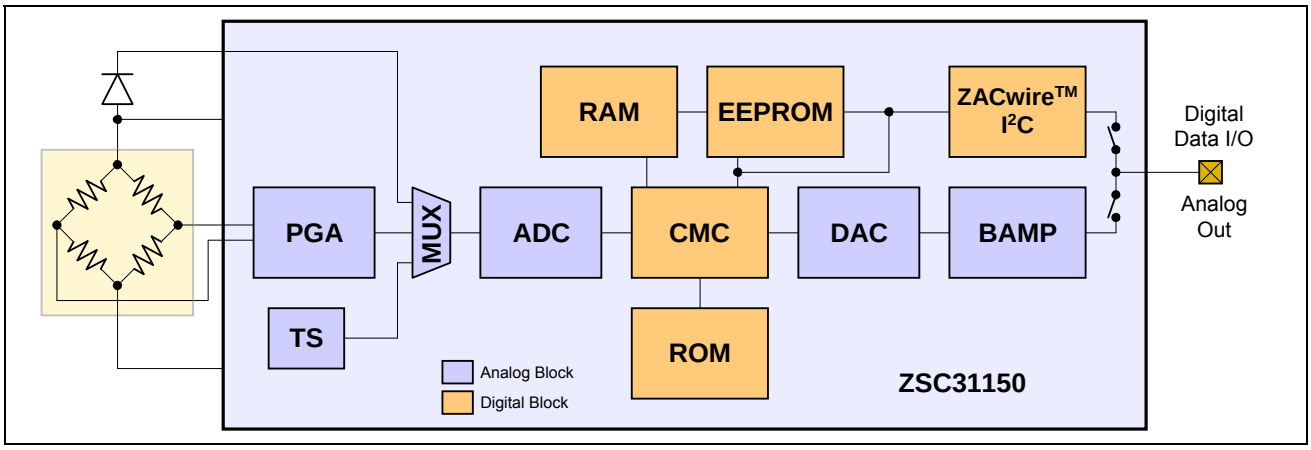
2 Circuit Description

2.1. Signal Flow

The ZSC31150's signal path is partly analog and partly digital. The analog part is realized differentially – this means, the differential bridge sensor signal is internally handled via two signal lines, which are rejected symmetrically around an internal common mode potential (analog ground = VDDA/2).

Consequently, it is possible to amplify positive and negative input signals, which are located within the common mode range of the signal input.

Figure 2.1 Block Diagram of the ZSC31150



PGA	Programmable Gain Amplifier
MUX	Multiplexer
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
DAC	Digital-to-Analog Converter
BAMP	Buffer Amplifier – output buffer OPAMP
EEPROM	Non Volatile Memory for Calibration Parameters and Configuration
TS	On-chip Temperature Sensor (pn-junction)
ROM	Memory for Correction Formula and –Algorithm
RAM	Volatile Memory for Calibration Parameters and Configuration

The differential signal from the bridge sensor is pre-amplified by the Programmable Gain Amplifier (PGA). The Multiplexer (MUX) transmits the signals from either the bridge sensor, the external diode, or the separate temperature sensor, to the Analog-to-Digital Converter (ADC) in a certain sequence (instead of the temperature diode, the internal pn-junction (TS) can be used optionally). Afterwards, the ADC converts these signals into digital values.

The digital signal correction takes place in the calibration microcontroller (CMC). It is based on a correction formula located in the ROM and on sensor-specific coefficients stored in the EEPROM during calibration. Dependent on the programmed output configuration, the corrected sensor signal is output as an analog value or in a digital format (I²C™ or ZACwire™). The configuration data and the correction parameters can be programmed into the EEPROM via the digital interfaces.

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2.2. Application Modes

For each application, a configuration set has to be established (generally prior to calibration) by programming the on-chip EEPROM regarding to the following modes:

- Sensor Channel
  - Sensor Mode: Ratiometric bridge excitation in voltage or current supply mode.
  - Input Range: The gain adjustment of the AFE with respect to the maximum sensor signal span and the zero point of the ADC have to be chosen.
  - Additional Offset Compensation (XZC): The extended analog offset compensation has to be enabled, if required; e.g., if the sensor offset voltage is near to or larger than the sensor span.
  - Resolution/Response Time: The A/D converter has to be configured for resolution and converting scheme or ADC order (first or second order). These settings influence the sampling rate and the signal integration time, and thus, the noise immunity.
- Temperature
  - Temperature Measurement: The source for the temperature correction has to be chosen.

2.3. Analog Front End (AFE)

The Analog Front End (AFE) consists of the Programmable Gain Amplifier (PGA), the Multiplexer (MUX), and the Analog-to-Digital Converter (ADC).

2.3.1. Programmable Gain Amplifier (PGA)

Table 2.1 shows the adjustable gains, the sensor signal spans, and the allowed common mode range.

Table 2.1 Adjustable Gains, Resulting Sensor Signal Spans and Common Mode Ranges

No.	Overall Gain a_{IN}	Max. Span V_{IN_SP} [mV/V] [13]	Gain Amp1	Gain Amp2	Gain Amp3	Input common mode range V_{IN_CM} as % of VDDA [14]	
						XZC = Off	XZC = On
1	420	1.8	30	7	2	29 to 65	45 to 55
2	280	2.7	30	4.66	2	29 to 65	45 to 55
3	210	3.6	15	7	2	29 to 65	45 to 55
4	140	5.4	15	4.66	2	29 to 65	45 to 55
5	105	7.1	7.5	7	2	29 to 65	45 to 55
6	70	10.7	7.5	4.66	2	29 to 65	45 to 55
7	52.5	14.3	3.75	7	2	29 to 65	45 to 55
8	35	21.4	3.75	4.66	2	29 to 65	45 to 55
9	26.3	28.5	3.75	3.5	2	29 to 65	45 to 55
10	14	53.75	1	7	2	29 to 65	45 to 55
11	9.3	80	1	4.66	2	29 to 65	45 to 55
12	7	107	1	3.5	2	29 to 65	45 to 55
13	2.8	267	1	1.4	2	32 to 57	not applicable

[13] Recommended internal signal range is 75% of supply voltage in maximum.
Span is calculated by the following formula: Span = 75% / gain

[14] Bridge in voltage mode, containing maximum input signal (with XZC: +300% Offset), 14-bit accuracy. Refer to the 'ZSC31150 Functional Description' for usable input signal/common mode range at bridge in current mode.

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2.3.2. Offset Compensation

The ZSC31150 supports two methods of sensor offset compensation (zero shift):

- Digital offset correction
- XZC - Analog compensation for large offset values (up to in maximum approximately 300% of span, depending on gain adjustment)

Digital sensor offset correction will be processed during the digital signal correction/conditioning by the calibration microcontroller (CMC). Analog sensor offset pre-compensation will be needed for compensation of large offset values, which would overdrive the analog signal path by uncompensated gaining. For analog sensor offset pre-compensation, a compensation voltage will be added in the analog pre-gaining signal path (coarse offset removal). The analog offset compensation in the AFE can be adjusted by 6 EEPROM bits.

Table 2.2 Analog Zero Point Shift Ranges (XZC)

PGA gain a_{IN}	Max. Span V_{IN_SP} [mV/V]	Offset shift per step in % of full span	Approx. maximum offset shift [mV/V]	Approx. maximum shift [% V_{IN_SP}] (@ ± 31)
420	1.8	12.5 %	7.8	388 %
280	2.7	7.6 %	7.1	237 %
210	3.6	12.5 %	15.5	388 %
140	5.4	7.6 %	14.2	237 %
105	7.1	12,5 %	31	388 %
70	10.7	7.6 %	28	237 %
52.5	14.3	12,5 %	32	388 %
35	21.4	7.6 %	57	237 %
26.3	28.5	5.2 %	52	161 %
14	53.75	12.5 %	194	388 %
9.3	80	7.6 %	189	237 %
7	107	5.2 %	161	161 %
2.8	267	0.83 %	72	26 %

2.3.3. Measurement Cycle

The Multiplexer selects, depending on EEPROM settings, the following inputs in a certain sequence.

- Temperature measured by external diode or thermistor, internal pn-junction or bridge
- Internal offset of the input channel (V_{OFF})
- Pre-amplified bridge sensor signal

The complete measurement cycle is controlled by the CMC. The cycle diagram at Figure 2.2 shows its principle structure.

The EEPROM adjustable parameters are:

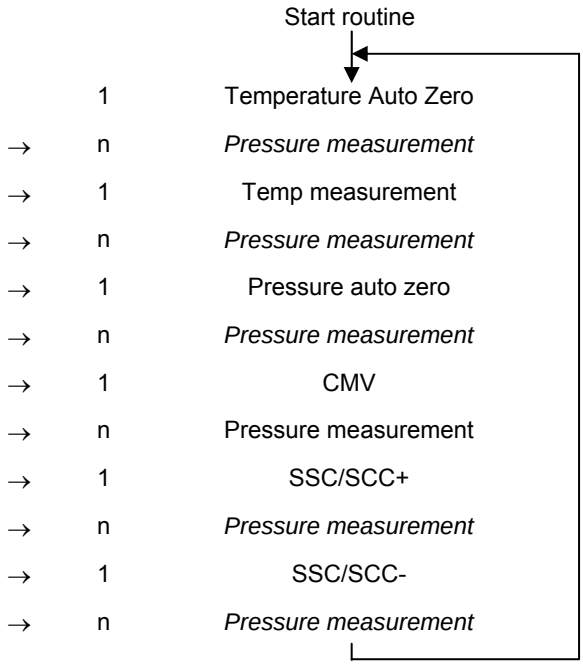
- n=<1,31>: Pressure measurement count

After power on the start routine is called, that contains all needed measurements once.

Remark: The tasks “CMV”, “SSC/SCC+” and “SSC/SCC-“ are contained independent from EEPROM configuration always in every cycle.

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Figure 2.2: Measurement Cycle



2.3.4. Analog-to-Digital Converter

The ADC is an integrating AD-Converter in full differential switched capacitor technique.

- Programmable ADC-resolutions are r_{ADC}=<13, 14> and with segmentation <15, 16> bit.

It can be used as first or second order converter. In the **first order** mode it is inherently monotone and insensitive against short and long term instability of the clock frequency. The conversion cycle time depends on the desired resolution and can be roughly calculated by:

$$t_{CYC_1} = 2^r / 2 / f_{CLK}$$

In the **second order** mode two conversions are stacked with the advantage of much shorter conversion cycle time and the drawback of a lower noise immunity caused by the shorter signal integration period. The conversion cycle time at this mode is roughly calculated by:

$$t_{CYC_2} = 2^{(r+3)/2} / 2 / f_{CLK}$$

The calculation formulas give an overview about conversion time for one AD-conversion. Refer Calculation sheet 'ZSC31150 Bandwidth Calculation Sheet' for detailed calculation of sampling time and bandwidth.

The result of the AD conversion is a relative counter result corresponding to the following equation:

$$Z_{ADC} = 2^r * (V_{ADC_DIFF} / V_{ADC_REF} - RS_{ADC})$$

Z_{ADC}: number of counts (result of the conversion)

r: adjusted resolution in bit

V_{ADC/REF_DIFF}: differential input/reference voltage of ADC

RS_{ADC}: digital ADC Range Shift (RS_{ADC} = $^1/_{16}$, $^1/_8$, $^1/_4$, $^1/_2$, controlled by the EEPROM content)

With the RS_{ADC} value a sensor input signal can be shifted in the optimal input range of the ADC.

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Table 2.3: Analog Output Resolution Versus Sample Rate

ADC Adjustment		Approximated Output Resolution [15]		Sample Rate f_{CON} [16]		Averaged Bandwidth @	
Order	r_{ADC}	Digital	Analog	f_{CLK}=3MHz	f_{CLK}=4MHz	f_{CLK}=3MHz	f_{CLK}=4MHz
O_{ADC}	[Bit]	[Bit]	[Bit]	[Hz]	[Hz]	[Hz]	[Hz]
1	13	13	12	345	460	130	172
	14	14	12	178	237	67	89
	15	14	12	90	120	34	45
	16	14	12	45	61	17	23
2	13	13	12	5859	7813	2203	2937
	14	14	12	3906	5208	1469	1958
	15	14	12	2930	3906	1101	1468
	16	14	12	1953	2604	734	979

Remark: ADCs reference voltage ADC_{VREF} is defined by the potential between <VBR_T> and <VBR_B> (or <VDDA> to <VSSA>, if CFGAPP:BREF=1). The theoretically input range ADC_{RANGE_INP} of the ADC is equivalent to ADCs reference voltage.

In practice ADCs input range should be used in maximum from 10% to 90% of ADC_{RANGE_INP} - a necessary condition for abiding specified accuracy, stability and nonlinearity parameters of AFE. This condition is also valid for whole temperature range and all applicable sensor tolerances. Inside of ZSC31150 is no failsafe task implemented, which verifies abiding of this condition.

2.4. Temperature Measurement

The ZSC31150 supports four different methods for temperature data acquiring needed for calibration of the sensor signal in temperature range. Temperature data can be acquired using:

- an internal pn-junction temperature sensor,
- an external pn-junction temperature sensor connected to sensor top potential (V_{BRTOP}),
- an external resistive half bridge temperature sensor and
- the temperature coefficient of the sensor bridge at bridge current excitation.

Refer 'ZSC31150 Functional Description' for a detailed explanation of temperature sensor adaptation and adjustment.

[15] ADC resolution should be one bit higher then applied output resolution, if AFE gain is adjusted in such manner, that input range is used more than 50%. Otherwise ADC resolution should be more than one bit higher than applied output resolution.
[16] The sampling rate (AD conversion time) is only a part of the whole cycle, refer “ZSC31150 bandwidth calculation sheet” for detailed information

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2.5. System Control and Conditioning Calculation

The system control supports the following tasks/features:

- control the measurement cycle regarding to the EEPROM-stored configuration data
- 16 bit correction calculation for each measurement signal using the EEPROM stored calibration coefficients and ROM-based algorithms = signal conditioning
- manage start up sequence and start signal conditioning
- handle communication requests received by the digital interface
- failsafe tasks for the functions of ZSC31150 and message detected errors with diagnostic states

Refer 'ZSC31150 Functional Description' for a detailed description.

2.5.1. Operation Modes

The internal state machine represents three main states:

- the continuous running signal conditioning mode – called Normal Operation Mode: NOM
- the calibration mode with access to all internal registers and states – called Command Mode: CM
- the failure messaging mode – called Diagnostic Mode: DM

2.5.2. Start Up Phase[17]

The start up phase consists of following parts:

1. internal supply voltage settling phase (=potential VDDA-VSSA) – finished by disabling the reset signal through the power on clear block (POC). Refer 'ZSC31150 High Voltage Protection Description', chapter 4 for power on/off thresholds.
   Time (for beginning with VDDA-VSSA=0V): 500µs to 2000µs, AOUT: tristate
2. system start, EEPROM read out and signature check (and ROM-check, if CFGAPP:CHKROM=1).
   Time: ~200µs (~9000µs with ROM-check – 28180clocks), AOUT: LOW (DM)
3. processing the start routine of signal conditioning (all measures & conditioning calculation).
   Time: 5x AD conversion time, AOUT behavior depending on adjusted OWI mode (refer 2.6):
   - OWIANA & OWIDIS => AOUT: LOW (DM)
   - OWIWIN & OWIENA => AOUT: tristate

The analog output AOUT will be activated at the end of start up phase depending on adjusted output and communication mode (refer chapter 2.6). In case of detected errors Diagnostic Mode (DM) is activated and diagnostic output signal is driven at the output.

After the start up phase the continuous running measurement and calibration cycle is started. Refer 'ZSC31150 Bandwidth Calculation Sheet' for detailed information about output update rate.

2.5.3. Conditioning Calculation

The digitalized value for pressure (acquired raw data) is processed with the correction formula to remove offset and temperature dependency and to compensate non-linearity up to 3rd order. The result of the correction calculation is a non-negative 15 Bit value for pressure (P) in the range [0; 1). This value P is clipped with programmed limitation coefficients and continuously written to the output register of the digital serial interface and the output DAC.

Note: The conditioning includes up to third order nonlinearity sensor input correction. The available adjustment ranges depend on the specific calibration parameters, for a detailed description refer to 'ZSC31150 Functional Description'. To give a rough idea: Offset compensation and linear correction are only limited by the loose of resolution it will cause, the second order correction is possible up to about 30% full scale difference to straight line, third order up to about 20% (ADC resolution = 13bit). The used calibration principle is able to reduce present nonlinearity errors of

[17] All described timings are roughly estimated values and correlates with internal clock frequency. Timings estimated for fclk=3MHz.

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the sensor up to 90%. The temperature calibration includes first and second order correction and should be fairly sufficient in all relevant cases. ADC resolution influences also calibration possibilities – 1 bit more resolution reduces calibration range by approximately 50%. Calculation input data width is in maximum 14bit. 15 & 16bit ADC resolution mode uses only a 14 bit segment of ADC range.

2.6. Analog Output AOUT

The analog output is used for output the analog signal conditioning result and for “End of Line” communication via the ZACwire™ interface (one wire communication interface - OWI). The ZSC31150 supports four different modes of the analog output in combination with OWI behavior:

- OWIENA: analog output is deactivated, OWI communication is enabled
- OWIDIS: analog output is active (~2ms after power on), OWI communication is disabled
- OWIWIN: analog output will be activated after time window,
  OWI communication is enabled in time window of ~500ms in maximum,
  transmission of “START_CM” command has to be finished during time window
- OWIANA: analog output will be activated after ~2ms power on time,
  OWI communication is enabled in time window of ~500ms in maximum,
  transmission of “START_CM” command has to be finished during time window,
  to communicate the internal driven potential at AOUT has to be overwritten
  by the external communication master (AOUT drive capability is current limited)

The analog output potential is driven by a unity gain output buffer, those input signal is generated by a 12.4bit resistor string DAC. The output buffer (BAMP) – a rail-to-rail OPAMP - is offset compensated and current limited. So a short circuit of analog output to ground or power supply does not damage the ZSC31150.

2.7. Serial Digital Interface

The ZSC31150 includes a serial digital interface (SIF), which is used for communication with the circuit to realize calibration of the sensor module. The serial interface is able to communicate with two communication protocols – I²C™ and ZACwire™ (a one wire communication interface – also called OWI). The OWI can be used to realize an “End of Line” calibration via the analog output AOUT of the complete assembled sensor module.

Refer 'ZSC31150 Functional Description' for a detailed description of the serial interfaces and communication protocols.

2.8. Failsafe Features, Watchdog and Error Detection

The ZSC31150 detects various possible errors. A detected error is signalized by changing the internal status in diagnostic mode (DM). In this case the analog output is set to LOW (minimum possible output value = lower diagnostic range – LDR) and the output registers of the digital serial interface are set to a significant error code.

A watchdog oversees the continuous working of the CMC and the running measurement loop. The operation of the internal clock oscillator is verified continuously by oscillator fail detection.

A check of the sensor bridge for broken wires is done permanently by two comparators watching the input voltage of each input (sensor connection and short check). Additionally the common mode voltage of the sensor and sensor input short is watched permanently (sensor aging).

Different functions and blocks in digital part - like RAM-, ROM-, EEPROM- and register content - are watched continuously. Refer 'ZSC31150 Functional Description' for a detailed description of safety features and methods of error messaging.

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2.9. High Voltage, Reverse Polarity and Short Circuit Protection

The ZSC31150 is designed for 5V power supply operation.

The ZSC31150 and the connected sensor are protected from overvoltage and reverse polarity damage by an internal supply voltage limiter. The analog output AOUT can be connected (short circuit, overvoltage and reverse) with all potentials in protection range under all potential conditions at the pins VDDE and VSSE.

All external components – explained in application circuit in chapter 3 – are required to guarantee this operation. The protection is no time limited. Refer 'ZSC31150 High Voltage Protection Description' for a detailed description of protection cases and conditions.

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3 Application Circuit Examples

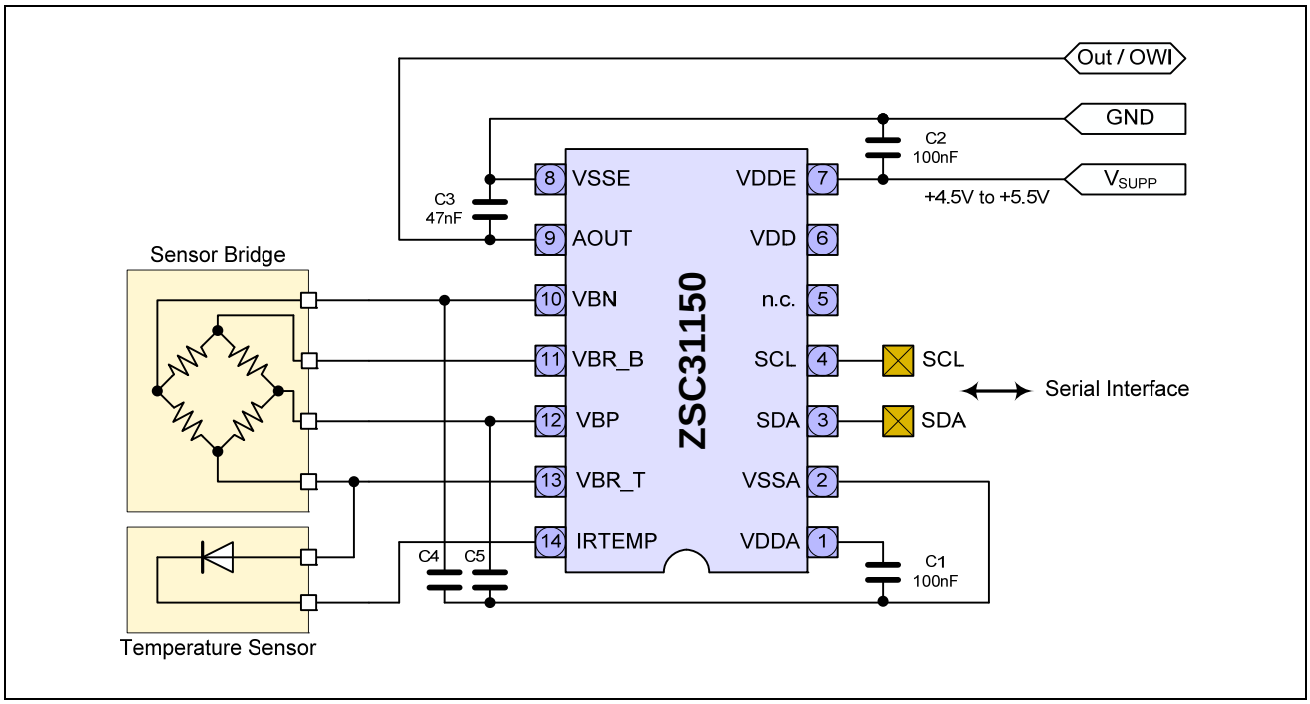
The application circuits contain external components, which are needed for overvoltage, reverse polarity, and short circuit protection.

Note: Check also the available 'ZSC31150 Application Notes' for application examples and board layout.

Table 3.1: Application Circuit Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
C1	C	100		470	nF	
C2	C	100			nF	
C3 [18, 2]	C	4	47	160	nF	The value of C3 is the sum of the load capacitor and the cable capacitance
C4, C5 [19]	C	0		10	nF	Recommended to increase EMC immunity. The value of C4, C5 is the sum of the load capacitor and the cable capacitance
R1			10		kΩ	
R_{IBR}	R	Refer to chapter 1.2			Ω	

Figure 3.1: Bridge in Voltage Mode, External Diode Temperature Sensor



[18] value of C3 summarizes load capacitor and cable capacity
[19] higher values for C3, C4 and C5 increase EMC immunity

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Figure 3.2: Bridge in Voltage Mode, External Thermistor

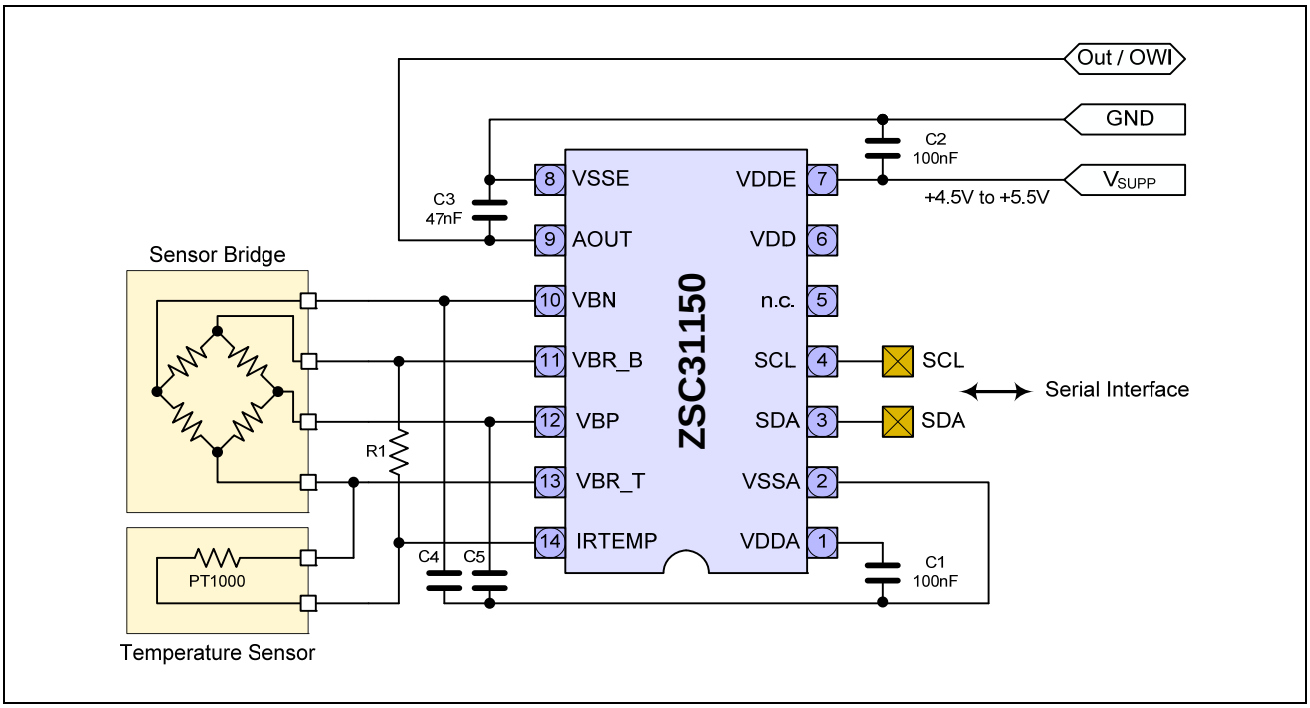
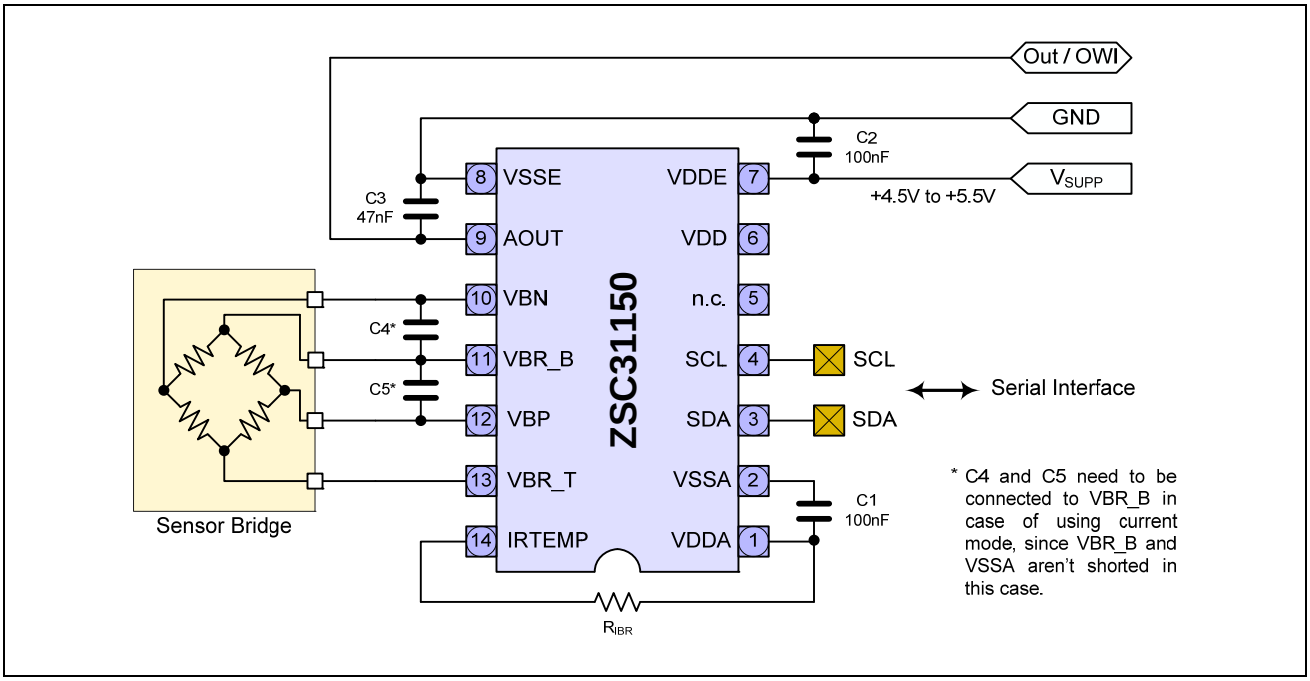


Figure 3.3: Bridge in Current Mode, Temperature Measurement via Bridge TC



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4 Pin Configuration, Latch-Up and ESD Protection

4.1. Pin Configuration and Latch-up Conditions

Table 4.1: Pin Configuration and Latch-Up Conditions

Pin	Name	Description	Remarks	Usage/ Connection [20]	Latch-up Related Application Circuit Restrictions and/or Remarks
1	VDDA	Positive analogue supply voltage	Analog IO	Required/-	
2	VSSA	Negative analogue supply voltage	Analog IO	Required/-	
3	SDA	I²C™ data IO	Digital IO, pull-up	-/VDDA	Trigger Current/Voltage to VDDA/VSSA: +/-100mA or 8/-4V
4	SCL	I²C™ clock	Digital IN, pull-up	-/VDDA	
6	VDD	Positive digital supply voltage	Analog IO	Required or open/-	only capacitor to VSSA is allowed, otherwise no application access
7	VDDE	Positive external supply voltage	Supply	Required/-	Trigger Current/Voltage: -100mA/33V
8	VSSE	Negative external supply voltage	Ground	Required/-	
9	AOUT	Analog output & one wire IF IO	IO	Required/-	Trigger Current/Voltage: -100mA/33V
10	VBN	Negative input sensor bridge	Analog IN	Required/-	
11	VBR_B	Bridge bottom potential	Analog IO	Required/VSSA	Depending on application circuit, short to VDDA/VSSA possible
13	VBR_T	Bridge top potential	Analog IO	Required/VDDA	
12	VBP	Positive input sensor bridge	Analog IN	Required/-	
14	IRTEMP	Temp sensor & current source resistor	Analog IO	-/VDDA, VSSA	Depending on application circuit

4.2. ESD-Protection

All pins have an ESD Protection of >2000V. Additionally the pins VDDE, VSSE and AOUT have an ESD Protection of >4000V.

ESD Protection referred to the human body model is tested with devices in SSOP14 packages during product qualification. The ESD test follows the human body model with 1.5kOhm/100pF based on MIL 883, Method 3015.7.

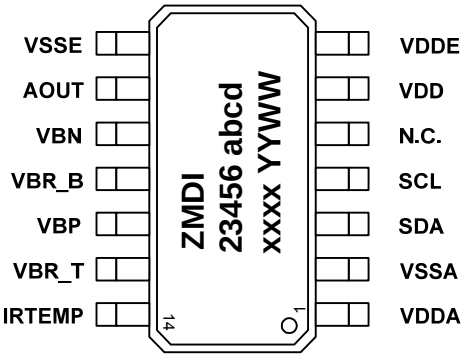
[20] Usage: If “Required” is specified, an electrical connection is necessary – refer to the application circuits
Connection: To be connected to this potential, if not used or no application/configuration related constraints are given

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5 Package

The standard package of the ZSC31150 is an SSOP14 green package (5.3mm body width) with a lead pitch of 0.65 mm.

Figure 5.1: ZSC31150 Pin Diagram



6 Quality and Reliability

The ZSC31150 is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate <5fit (temp=55°C, S=60%) is guaranteed. A typical fit rate of the C7D-technologie, which is used for ZSC31150, is 2.5fit.

7 Customization

For high-volume applications, which require an up- or downgraded functionality compared to the ZSC31150, ZMDI can customize the circuit design by adding or removing certain functional blocks.

For it ZMDI has a considerable library of sensor-dedicated circuitry blocks.

Thus ZMDI can provide a custom solution quickly. Please contact ZMDI for further information.

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8 Ordering Information

Example: **ZSC31150 F A G1 - T**

ZMDI Product Sales Name

Design Revision
The revision level is indicated alphabetically beginning with A for first revision level

Target Application Area/
Normal Operating Temperature Range
A = Automotive (-40°C to +125°C)
E = Extended Automotive (-40°C to +150°C, 1000h@150°C)
L = Long Life Automotive (-40°C to +150°C, 5000h@150°C)

Die/Package Options
B = Tested dice on unsawn wafer
C = Tested dice on frame
D = Tested dice in waffle pack
G1 = Finished parts, RoHS-compliant, in plastic package

Delivery Form *
T = Delivery in tube
R = Delivery in tape on reel

* Only for finished parts in plastic package
Not all possible combinations are available. Please ask ZMDI sales

Product Sales Code	Description	Package
ZSC31150KIT Evaluation Kit V1.0	Modular evaluation and development boards for ZSC31150	KIT boards, IC samples, USB cable, DVD with software and documentation
ZSC31150 Mass Calibration System V1.1	Modular Mass Calibration System (MSC) for ZSC31150	MCS boards, cable, connectors, DVD with software and documentation

9 Additional Documents

Document	File Name
ZSC31150 Feature Sheet	ZSC31150_FeatureSheet_Rev_*.PDF
ZSC31150 Functional Description	ZSC31150_FunctionalDescription_Rev_*.PDF
ZSC31150 High Voltage Protection Description	ZSC31150_HV_PROT_Rev_*.PDF
ZSC31150 Dice Package	ZSC31150_DicePackagePin_Rev_*.PDF
ZSC31150 Bandwidth Calculation Sheet	ZSC31150_Bandwidth_Calculation_Rev*.xls
ZMDI Temperature Profile Calculation Sheet	ZMDI_Temperature_Profile_Rev_*.xls
ZSC31150 Application Kit Description	ZSC31150_APPLKIT_Rev_*.pdf
ZSC31150 Application Notes	ZSC31150_AN*.pdf

Visit ZMDI's website www.zmdi.com or contact your nearest sales office for the latest version of these documents.

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10 Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front End
AOUT	Analog Output
BAMP	Buffer Amplifier
CM	Command Mode
CMC	Calibration Microcontroller
CMV	Common Mode Voltage
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DM	Diagnostic Mode
EEPROM	Electrically Erasable Programmable Read Only Memory
ESD	Electrostatic Device
LDR	Lower Diagnostic Range
MUX	Multiplexer
NOM	Normal Operation Mode
OWI	One Wire Interface
P	Pressure
PGA	Programmable Gain Amplifier
POC	Power on Clear
RAM	Random-Access Memory
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
SCC	Sensor Connection Check
SIF	Serial Interface
SSC+	Positive-biased Sensor Short Check
SSC-	Negative-biased Sensor Short Check
TS	Temperature Sensor
XZC	eXtended Zero Compensation

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11 Document Revision History

Revision	Date	Description
0.46	June 12, 2008	First release after format update
0.47	July 20, 2008	Update after review
1.01	September 20, 2008	“6.” – fit rate added ”1.5.2” – ROM check time revised/corrected ”5.3.4.3” – SSC – no detection limit added
1.02	September 20, 2009	adjust to new ZMDI template
1.03	October 2, 2009	change to ZMDI denotation
1.04	October 22, 2009	formatting and linking issues solved
1.05	February 26, 2010	adjust to new ZMDI template include 'ZSC31150 Feature Sheet' at page 2&3 add ordering codes for ZSC31150 and evaluation kits extend glossary add new phone number for ZMD FAR EAST, Ltd. and ZMDA America Office Madison
1.06	July 29, 2010	correct “Offset shift per step” and “Approx. maximum offset shift” in Table 2.2 for PGA gain = 105 and 52.5 move 1.4.1.6 “Internal pull-up resistor” into chapter 1.4.1 in Table 1.2 redrawing of Sensor Bridge in Figure 3.1, Figure 3.2 and Figure 3.3 add comment for C4 and C5 in Figure 3.3 rename ZMD31150 to ZSC31150
1.07	August 31, 2010	Connection of R_{IBR} in Figure 3.3 corrected
1.08	August 15, 2011	Update ordering information with “Long Life Automotive” (refer Ordering Information and chapter 8)

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