PRELIMINARY

RASTER TO BLOCK CONVERTER

FEATURES

- Real Time Raster to/from Block Conversion
- 1/2 Decimation Processing in the Horizontal Direction
- 30 MHz Maximum Clock Rate
- Only Image in Preset Window is Converted
- Compatable with Zorans ZR36050 JPEG Coder and ZR36011 Color Space Converter
- Supports 1:0:0,4:2:2,and 4:1:1 data formats
- 100-pin plastic quad flat package (PQFP)
- TTL level Input/Output
- Synchronous data and controls
- Low power consumption: 0.45W (Typ.)
- CMOS circuit operating with a single 5V power supply

APPLICATIONS

- Image processing
- Multi-media
- Scanners
- Image Storage
- Image Capture

DESCRIPTION

The ZR36015 performes raster to/from block conversion for image compression and expansion applications, and it can be connected directly to the ZR36050 JPEG coder and the ZR36011 Color Space Converter.

An image compression system can be easily constructed using the ZR36015 with the ZR35060 and ZR36011.

The ZR36015 uses a double buffered external SRAM Strip Buffer to support raster to/from block conversion and block interleave.

The maximum number of pixels that can be processed per line is 8K. The maximum number of lines that can be prcessed per image is 16K. These numbers vary according to the mode of operation.

The ZR36015 supports 4:0:0, 4:1:1, and 4:2:2 data formats, and one half decimation in horizontal direction during compression.

The maximum data transfer rate to the ZR36050 coder is 30 MHz.

[The ZR36015 is fabricated with an advanced low-power CMOS technology, making it suitable for use in low-power, cost sensitive applications. The device is availiable in a 100 pin , Plastic Quad Flat Package (PQFP).]

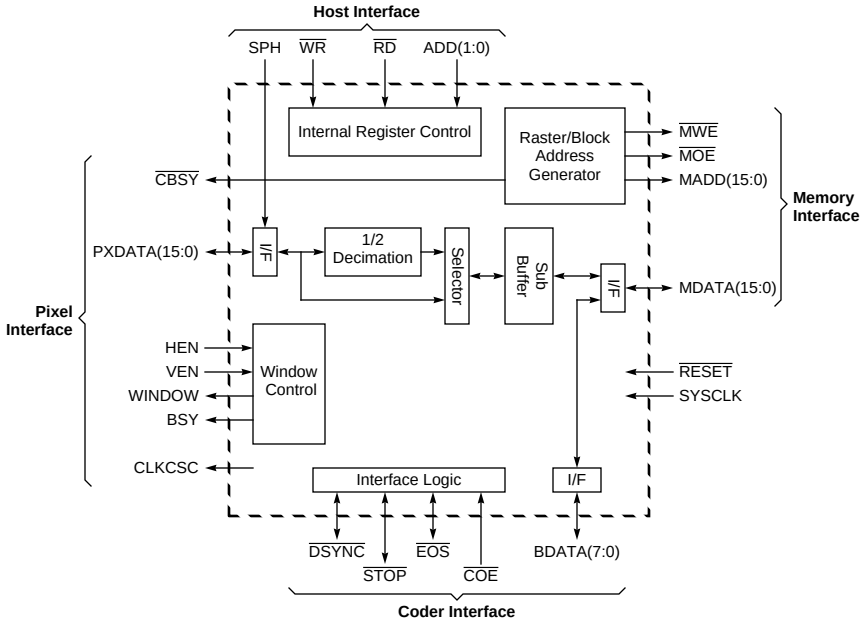


Figure 1. ZR36015 Block Diagram

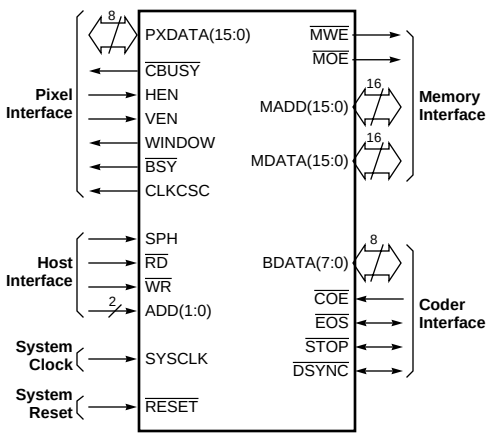


Figure 2. ZR36015 Logical Pinout

This document was created with FrameMaker 4.0.4

SIGNAL DESCRIPTION

Name	Type[1]	Function
PXDATA(15:0)	B	Pixel side data bus. Input for compression and output for expansion. High impedance during RESET or IDLE modes. When SPH is active (High), PXDATA(7:0) is controlled by the Host Interface. It will be high impedance except during a Host read access, in which case it will be driven. The state of PXDATA(15:8) follows that of PXDATA(7:0) in this case but is unused.
HEN	I	Active High Horizontal enable signal (HDelay starts counting from the rise of HEN)
VEN	I	Active High Verticle enable signal (VDelay starts counting from the rise of VEN)
SYSCLK	I	System clock (active on rising edge).
MADD(15:0)	O	Address output for the strip memory. Up to 64K x 16 bits of SRAM is addressable.
MDATA(15:0)	B	Data bus for the strip memory. Memory A is assigned to MDATA(7:0), and Memory B is assigned to MDATA(15:8).
$\overline{\text{MWE}}$	O	Active Low: Write enable for the Strip Memory.
$\overline{\text{MOE}}$	O	Active Low: Output enable for the Strip Memory.
$\overline{\text{DSYNC}}$	B	Active Low: Sync. signal for 64 byte block of data. Output during compression and input during expansion. In compression, $\overline{\text{DSYNC}}$ marks the start of an 8x8 image data block and should appear as an output one SYSCLK cycle before the first image data of a block. During expansion $\overline{\text{DSYNC}}$ is input on SYSCLK before the first image data of a sample block. The width of $\overline{\text{DSYNC}}$ is one SYSCLK. (Connect directly to ZR36050 $\overline{\text{DSYNC}}$ signal).
$\overline{\text{STOP}}$	B	Active Low: Stop sending/receiving. During compression, this signal is an input which indicates that the CODEC is busy, and the ZR36015 should stop sending data. During expansion, this signal is an output indicating the ZR36015 is not ready to receive data, and for the CODEC to stop sending data. (Connect directly to ZR36050 $\overline{\text{STOP}}$ signal).
$\overline{\text{EOS}}$	B	Active Low: Signal indicates the end of each scan. Output during compression and input during expasion. In compression, $\overline{\text{EOS}}$ is output together with the last image data sample of the last block of each scan. In expansion, $\overline{\text{EOS}}$ is input together with the last image data sample of the last block of each scan. (Connect directly to ZR36050 $\overline{\text{EOS}}$ signal).
BDATA(7:0)	B/Z	Data bus interface with the Coder. Output for compression and input for expansion. High impedance during reset. Otherwise, the direction of the bus is determined by the $\overline{\text{COE}}$ input. (Connect directly to ZR36050 PIXEL(11:4) bus.)
ADD(1:0)	I	Address select for Host access to internal registers. Enabled when SPH is high.
$\overline{\text{WR}}$	I	Active Low: Write strobe for Host loading of internal registers and tables. Data is writtern on the rising edge of $\overline{\text{WR}}$. $\overline{\text{WR}}$ is enabled when SPH is high.
$\overline{\text{RD}}$	I	Active Low: Read strobe for Host reading of internal registers and tables. $\overline{\text{RD}}$ is enabled when SPH is high.
$\overline{\text{CBSY}}$	O	Active Low: $\overline{\text{CBSY}}$ indicates that the ZR36015 is not ready for the next strip of data.
$\overline{\text{COE}}$	I	Coder bus output enable signal. HIGH for Compression Mode (enabling the output drivers for the CDATA bus, $\overline{\text{EOS}}$ signal and $\overline{\text{DSYNC}}$ signal. . LOW for Expansion mode (enabling the output drivers for the $\overline{\text{STOP}}$ signal). (Connect directly to ZR36050 COMP signal).
$\overline{\text{BSY}}$	O	Active Low: $\overline{\text{BSY}}$ is active when the ZR36015 is processing an image. Before setting hte $\overline{\text{GO}}$ bit in the Mode Register, $\overline{\text{BSY}}$ should be inactive.
CLKCSC	O	Clock output for ZR36011 Color Space Converter. Used to synchronize data transfers.
SPH	I	Active High: Select host access to the ZR36015 via the PXDATA(7:0) data bus. Enables the $\overline{\text{WR}}$, $\overline{\text{RD}}$ inputs.
WINDOW	O	Active HIGH; Indicates active (windowed) image area.
$\overline{\text{RESET}}$	I	Asynchronous Active LOW reset. All bi-directional signals are tri-stated when this signal is active. After $\overline{\text{RESET}}$, the ZR36015 will be in idle mode (GO bit cleared) and the PXDATA bus will continue to behigh impedance until the GO bit is set .
V_{DD}	—	Power terminal.
V_{SS}	—	Ground terminal.

1. I = Input, O = Output, B = Bidirectional, Z = High Impedance.

FUNCTIONAL DESCRIPTION

The ZR36015 performs conversion between raster and block formatted data, with applications in image compression and expansion. It is designed to work with the ZR36050 JPEG Codec.

Figure 1 is a block diagram of the ZR36015.

The ZR36015 is a programmable device with an asynchronous Host Interface (WR,RD,ADD(1:0) which is enabled by the SPH input . Data is transferred between the Host and the ZR36015 internal Control Registers and configuration tables via the PXDATA(7:0) bus. Because PXDATA(7:0) is used to transfer data to/from the Host, and also for pixel data, an external buffer is required to prevent bus contention.

The internal control registers of the ZR36015 consist of four registers which set the operating mode of the device and control the interface between the host and the configuration tables. The configuration tables are used to specify an active window within the region defined by the VEN and HEN inputs, and to count the actual number of lins that were processed.

The ZR36015 interfaces to a pixel data bus PXDATA(15:0), which transfers 4:0:0, 4:1:1, or 4:2:2 formatted data. Transfer of data on the Pixel Bus is controlled by the Verticle Enable (VEN) and Horizontal Enable (HEN) inputs.

During Compression, Pixel data can be optionally decimated by 2 in the horizontal direction.

When the ZR36015 is interfaced to the ZR36011 “Color Space Converter”, then it is recommended that the Clock for Color Space Converter (CLKCSC) output be connected to the input clock for the ZR36011.

The ZR36015 supports a double buffered Strip Buffer SRAM architecture, with up to 64K 16 bit words. The Strip Buffer stores the image data in interleaved block format. Interleaved block formatted data is transferred between the ZR36015 and the ZR36050 over the BDATA bus.

The ZR36015 can be directly interfaced with the ZR36050 JPEG Codec. Block transfers of data are controlled by the $\overline{\text{DSYNC}}$, $\overline{\text{STOP}}$, $\overline{\text{EOS}}$, $\overline{\text{COE}}$ signals, with data being transferred on the BDATA(7:0) bus. These signals are connected directly to the ZR36050 $\overline{\text{DSYNC}}$, $\overline{\text{STOP}}$, $\overline{\text{EOS}}$, COMP, and PIXEL(11:4) signals respectively.

Overflows or underflows of the double buffered Strip Memroy are indicated by the CBSY output.

System Configuration Example

An example of the ZR36015 system configuration is given in Figure 3. This figure shows an image compression/expansion system which uses the ZR36011 (Color Space Converter) and the ZR36050 (JPEG Codec), in addition to the ZR36015.

The figure shows A/D and D/A conversion devices in between an image source/display and the ZR36011 (Color Space Converter).

The bus between the ZR36011 and the D/A and A/D converterters is in 24 bit RGB format.

In Compression mode the ZR36011 converts the RGB data into YUV (luminance/chrominance) data for more efficient compression.

In Compression mode, the ZR36015 (Raster to Block Converter), converts the raster data into 8x8 blocks for processing by the ZR36050 JPEG Codec. The SRAM strip buffer stores 8 lines of data for conversion into block format.

In Compression mode, the ZR36050 JPEG Codec performes JPEG compression on the block data, and transfers the compressed image over the system bus.

In expansion mode, the process described above is reversed.

The ZR36015 and ZR36050 devices are programmed via the system bus, and require minimal host intervention during the compression/expansion processes.

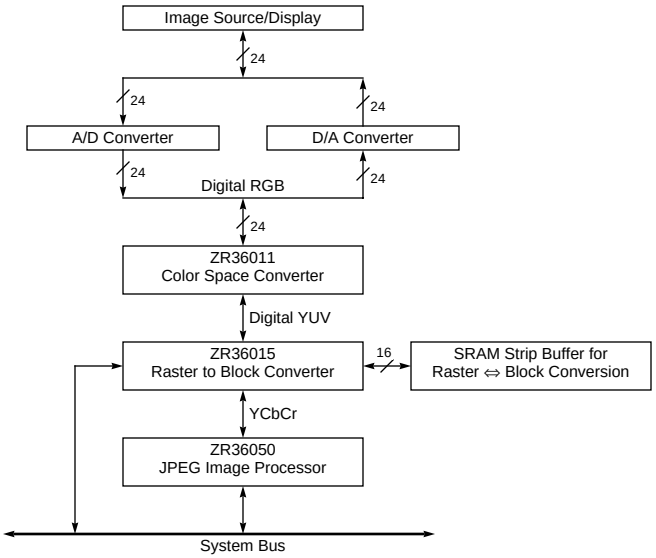


Figure 3. ZR36015 System Configuration Example

Control Registers

The ZR36015 has four Control Registers which allow the Host to set the mode of operation, and to initiate, terminate, and monitor

the status of compression or expansion prcesses. The four control registers are listed and described below.

Table 1: Control Register Map

ADD(1:0)	Contents	Host Access
00	Soft Reset	W
01	Mode Register	R/W
10	Address Pointer Register	R/W
11	Configuration Register Tables	R/W

Soft Reset Register (Write Only):

A Write to the Soft Reset Register will abort the current process, and put the ZR36015 in to the IDLE mode. The Soft Reset does not modify the internal registers of the ZR36015, except for the GO bit in the Mode Register (which is cleared).

After a soft reset, the ZR36015 will be in the IDLE state.

To start a new process, the GO bit in the Mode Register must be set by the Host.

Mode Register (Read/Write):

The table below shows the contents of the Mode Register.

Bit	Name	Description
0	GO	Go: 0: ZR36015 IDLE 1: Set to indicate Encode or Decode process.
1	EDC	0: Decode mode selected 1: Encode mode selected
3:2	MOD(1:0)	Pixel data Mode Select (seeTable 2)
4	DCM	Decimate data (Compression mode only). Active High.
5	CSC	Select ZR36011 Color Space Converter Mode (Active High)
6	-	Not Used
7	BSY	Busy Flag (Active High)

The definition of these bits is given below:

- BSY: Busy Flag (Read Only)

  Active High: Indicates that the ZR36015 is busy performing an encoding or decoding process. The next process should not be started until the current process completes (indicated by the ZR36015 clearing this bit).

  The BSY flag is set to '1' immediately after the GO bit is set. The BSY flag is cleared when the processing for an image is complete and the ZR36015 is ready for the next "GO".

  Before setting the "GO" bit (defined later in this section), the host should check that the Busy Flag is '0', indicating that the previous process has completed.
- CSC: Select ZR36011 Color Space Converter (Write Only)

  Set this bit to a '1' when interfacing the PIXDATA bus to the ZR36011 Color Space Converter, and to a '0' otherwise.

  Setting the CSC bit to a '1', will modifies the pixel data internal delays during compression or expansion to match the delays in the ZR36011 Color Space Converter. A description of the modified pixel data delays is TBD.
- DCM: Select 1/2 Decimation Write Only)

  Set this bit to a '1' when selecting 1/2 decimation mode (for compression only).
- MOD(1:0): Pixel Data Mode Select

  These bits are set to determine the PXDATA bus to/from BDATA bus mode of operation. Table 3 shows the availiable combinations.
- EDC: Enclde/Decode select

  Selects either encode (EDC = '1'), or decode (EDC = '0') mode.
- GO: Process Go Trigger Bit (Write Only)

  Set to '1' to start ZR36015 processing. Prior to setting GO, the host must...

  1) Make sure that the BSY bit is not set.

  2) Set all processing parameters in the tables.

When GO is set, the ZR36015 starts counting pixel elements from the rise of VEN and HEN. When [when is go reset?]

MOD(1:0)	PXDATA Format	BDATA Format
00	1:0:0	1:0:0
01	4:2:2	4:2:2
10	4:2:2	4:1:1
11	4:1:1	4:1:1

Address Pointer Register(R/W):

This register is a pointer to the configuration tables and line count register. A write to the configuration table (ADD(1:0) = "0b11") will write to the table element indicated by the address pointer regstier. A read from the number of lines registers will access the register indicated by the address pointer register. The Address pointer Register is automatically incremented by one after a read or write with ADD(1:0) set to "0b11".

Configuration Register Tables(R/W):

The contents of the Configuration Table are shown in the below. The fields of the Configuration Table are defined below and in Figure 5.

- HDelay(12:0): Horizontal delay in number of pixel elements before active window. The setting range for WDelay(12:0) is 0 to 8191.
- HWidth(14:0): Horizontal width of the active image area. The setting range for Width(14:0) is up to 8191 for.
- VDelay(12:0):Verticle delay in number of pixel elements before active window. The setting range for HDelay(12:0) is 0 to 8191.

- VHeight(12:0):Verticle height of the active image area. The maximum setting for Height(12:0) is 8191. Setting Height(12:0) to '0' in encode mode, lets the Height of the active image area be determined by the non-active point of VEN.

Address Pointer Value	Window Setting Value
0	HDelay(7:0)
1	HDelay(12:8)[1]
2	HWidth(7:0)
3	HWidth(14:0)[1]
4	VDelay(7:0)
5	VDelay(12:8)[1]
6	VWidth(7:0)
7	VWidth(13:8)[1]
8	Number of Lines(7:0)
9	Number of Lines(13:8)[1]

1. Assigned to LSB's of PIXDATA(7:0)

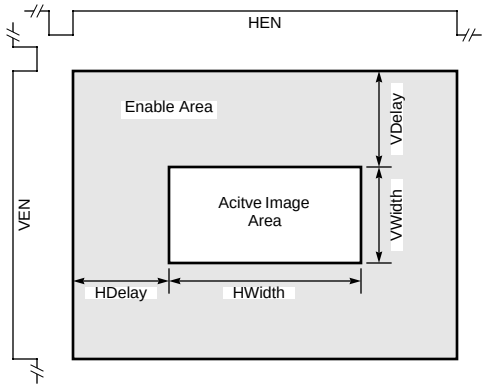


Figure 4. Active Image Area

Number of Lines Table:

The Number of Lines Table holds the number of lines processed in encoding by the ZR36015.

Operating States

The ZR36015 has four Operating States; Reset, Idle, Compression and Expansion.

Reset State

While the RESET input is asserted, the ZR36015 is in the Reset State. In this state the PXDATA and BDATA busses are high impedance, and the $\overline{\text{DSYNC}}$, $\overline{\text{STOP}}$, $\overline{\text{EOS}}$ signals are high impedance.

After a RESET, the ZR36015 will be in the IDLE state.

Idle State

After a Soft RESET, or after the RESET input signal has been applied, or at the end of a compression or expansion process, the ZR36015 will be in the IDLE state. In the IDLE state, no active processing is taking place, and the PXDATA bus is high impedance (the bus drivers for the Coder Interface are controlled by the COE signal).

While in the IDLE state, the ZR36015 Configuration Register Tables can be loaded with the values to select the desired active image area. Also, the Mode Register is loaded with the desired Mode of operation, and the number of lines table can be read

To leave the IDLE state and enter one of the processing states (compression or expansion), the GO bit in the Mode registe is set.

Compression

When the GO bit is set to "1", and the EDC bit equals "1", then the ZR36015 enters the Compression State.

Setting the GO bit results in the BSY bit in the mode register being set.

Once the GO bit is set, then on the falling edge of the Verticle Sync Signal (VEN), the BSY output signal will be set. The BSY bit (and output signal) will stay set until the end of the Compression process. The hardware can monitor the BSY signal, to determine when the Compression process has completed. Note that the GO bit must be set at least three SYSCLK cycles before the VEN goes from High to Low (see figure ???).

Following the above, the ZR36015 monitors the VEN input to detect the transiton of VEN from low to high. This indicates the beginning of the image to be processed The next VDelay lines of data are ignored in order to reach the "active image area". Then the next VWidth lines of data are processed.

The HEN input synchronizes the line by line transfers of data into the ZR36015. On the rise of HEN, the next HDelay pixels are ignored in order to reach the "active image area". Then the next HWidth pixels are procesed.

The MOD(1:0) bits in the Mode Register determine the format of the data on the PXDATA bus, and the DCM bit determines if decimation is performed.

After the last of the data in the “Active Image Area” has been converted to Block format and transferred to the Coder (as indicated by the EOS output), the GO bit and the BSY bit (and BSY signal) are cleared and the ZR36015 enters the IDLE state.

In order to compress a sequene of images, the GO bit must be set for each image. However, the table values do not have to be re-initialized for each image.

Expansion

When the GO bit is set to “1”, and the EDC bit equals “0”, then the ZR36015 enters the Expansion State.

Setting the GO bit results in the BSY bit in the mode register being set.

Once the GO bit is set, then on the falling edge of the Verticle Sync Signal (VEN), the BSY output signal will be set. The BSY bit (and output signl) will stay set until the end of the Expansion process. The, to determine when the Expansion process has completed. Note that the GO bit must be set at least three SYSCLK cycles before the VEN goes from High to Low (see figure ???).

Following the above, the ZR36015 monitores the VEN input to detect the transition of VEN from low to high. This indicates the beginning of the time interval when the image is to be output to the PIXEL bus. The ZR36015 waits VDelay lines before putting the first line of decoded data out to the PIXDATA bus.

The HEN input synchronized the line by line transfers of data to the PXDATA bus. On the rise of HEN, the ZR36015 waits HDelay SYSCLKs until outputting the decoded line of pixels (HWIDTH of them) on the PXDATA bus.

The MOD(1:0) bits in the Mode Register and the data in the Configuretino Tables, must match the format and size fo the data being decodced by the ZR36050.

The DCM bit is not used in expansion.

After the last of the data in the “Active Image Area” has been transmitted to the PXDATA bus, the GO bit and the BSY bit (and BSY signal) are cleared, and the ZR36015 enters the IDLE state.

In order to expand a sequence of images, the GO bit must be set for each image. However, the table values do not have to be re-initialized for each image.

System Interface

The SPH input is used to select host access to the ZR36015, (set SPH to ‘1’). Host access for read/write of the ZR36015’s control registers is carried out using the system interface pins (RD,WR, and ADD(1:0)), in addition to the lower 8-bits of PXDATA bus. Once host access is selected, the WE and RD signals initiate the writing and reading of data (using the PXDATA bus), to locations specified by the ADD(1:0) inputs.

Since the Host and image source share PXDATA(7:0), an external bidirectional buffer is required on PXDATA(7:0) in order to avoid bus contention. The ADD(1:0), RD, and WR inputs are ignored when Host Access is not selected by SPH. The table below shows the addressing of the internal control registers by the ADD(1:0) address inputs.

Pixel Bus Formats

The Pixel Bus “PXDATA(15:0), is divided into two bytes. PXDATA(15:8) is always used to represent the Y data, while PXDATA(7:0) is always used to represent the UV data.

The data formats of PXDATA are according to the setting of the MOD(1:0) bits in the Mode Register.

Table 2 and 3 show the format of PXDATA bus for each mode.

Table 2: Pixel Bus Data Format (Mode 3)

PXDATA	1st	2nd	3rd	4th
PXDATA (15:8)	Y1 (7:0)	Y1 (7:0)	Y1 (7:0)	Y1 (7:)
PXDATA (7)	U1 (7)	U1 (5)	U1 (3)	U1 (1)
PXDATA (6)	U1 (6)	U1 (4)	U1 (2)	U1 (0)
PXDATA (5)	V1 (7)	V1 (5)	V1 (3)	V1 (1)
PXDATA (4)	V1 (6)	V1 (4)	V1 (2)	V1 (0)
PXDATA (3:0)	–	–	–	–

Table 3: Pixel Bus Data Format (Modes 0, 1, 3)

PXDATA	Format							
	(1:0:0)		(4:2:2)		(4:1:1)			
	1st	2nd	1st	2nd	1st	2nd	3rd	4th
PXDATA (15:8) (Y)	Y0	Y1	Y0	Y1	Y0	Y1	Y2	Y3
PXDATA (7:0) (UV)	–	–	U0	V0	U0 (7:6) V0 (7:6)	U0 (5:4) V0 (5:4)	U0 (3:2) V0 (3:2)	U0 (1:0) V0 (1:0)

PXDATA Syncronization Clock Frequency:

The input and output of data on PXDATA(15:0) are carried out in synchronization with the clock signal of SYSCLK for mode 0, or SYSCLK/2 for modes 1, 2 and 3. Table 4 shows the PXDATA bus sync clock frequency for each of the modes of operation.

Table 4: PXDATA Bus Sync Clock Frequency

MOD (1:0)	Pixel Side Format	Coder Side Format	PXDATA Bus Sync Clock Freq.[1]
0 (00)	(1:0:0)	(1:0:0)	SYSCLK
1 (01)	(4:2:2)	(4:2:2)	SYSCLK÷2
2 (10)	(4:2:2)	(4:1:1)	SYSCLK÷2
3 (11)	(4:1:1)	(4:1:1)	SYSCLK÷2

1. The sync clock freq. of the coder bus side is SYSCLK in all modes.

The data seen on the Pixel Bus during Compressoin is shown in Figure 5.

PIXEL PROCESSING TIMING

The leading edge of the frame is identified by the fall of VEN (after the GO bit is set). Tge VDelay is counted from the following rise of the VEN input. The HDelay is counted from the rise of the HEN input. The HEN and VEN signals must remain high at least until the end of the active image area (as defined by the Configuration Register table).

HEN must conform to either A or B in Figure 8.

Within the image area defined by the VEN and HEN signals, is the “Active Image Area”, which is determined by the HDelay, HWidth, VDelay, and VWidth values in the configuration table. Pixel processing is performed only on those pixels which lie in the active image area defined in Figure 4. The width and height of the active image area are determined by the “HWidth” and “VHeight” values in the configuration register table.

If VWidth is set to zero (a special case), then lines will continue to be processed for as long as VEN remains high (maximum of 8K lines). This feature allows processing of frames with an unknown number of lines. At the end of processing, the “Number of Lines” register will contain the number of lines that have been processed. Figure 7 illustrates the “active image area” for this special case.

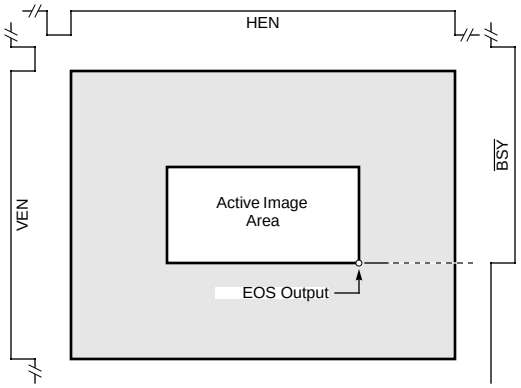


Figure 6. Pixel Processing Image Area

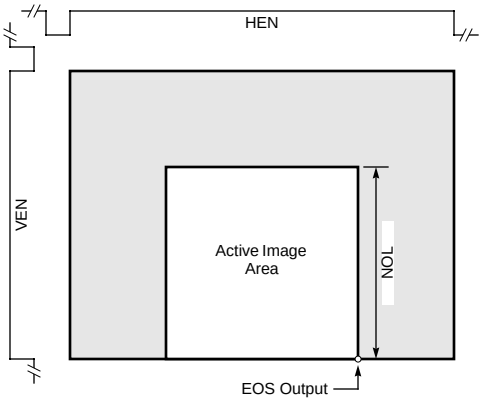


Figure 7. EOS Asertion

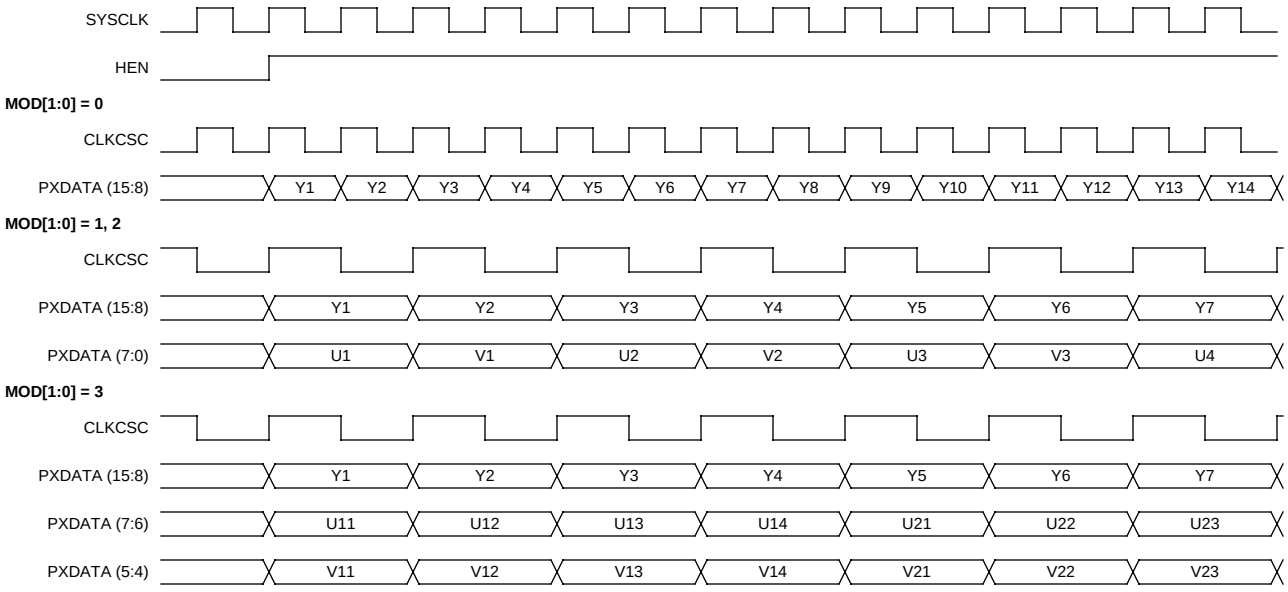


Figure 5. Functional Timing Chart - Pixel Bus Side

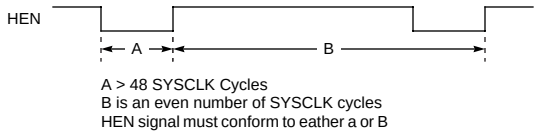


Figure 8. Setting of HEN Timing

Window Output Signal

The WINDOW output (active high) is aligned with the PDATA bus, identifying the pixels which correspond to the active image area. Figure 5 shows the functional timing for the window signal for the case where Mode=0, and HDelay = 0 or HDelay = 3.

The Window signal is set “HDelay” pixels after the rise of HEN, and goes inactive “HWidth” pixels later. The timing for the WINDOW signal is identical for both compression and expansion modes.

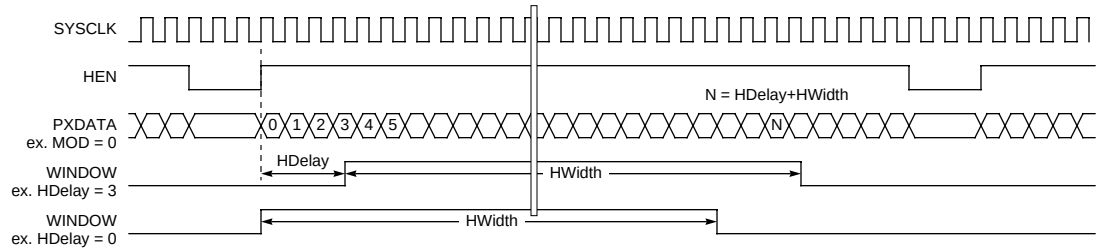


Figure 9. Example of Window Output Timing

Line Counting

The ZR36015 counts the number of lines that were processed during encoding mode, and stores this number in the “number of lines” registers defined in Table 5.

When “VHeight” is set to zero, the number of lines processed is dependent on the duration of the VEN signal. If the duration of the VEN signal does not correspond to an active image area with a number of lines that is a multiple of 8 (for modes 0,1,3) or a multiple of 16 (mode 2) then the number of lines is rounded up to the nearest multiple of 8(16). This feature ensures blocks of data that are compatible with JPEG image compression algorithms.

If the number of lines being processed exceeds 8192, then the ZR36015 terminates the processing after processing 8192 lines.

“BUSY” Bit and Busy Signal Timing

The BSY (Busy) bit in the Mode Register is set to ‘1’ (active) when the Go bit is aserted. When the ZR365015 finishes processing the data in the active image area, it clears the BSY and GO bits and the $\overline{BSY}$ signal. The $\overline{BSY}$ signal follows the BSY bit when VEN falls.

Setting GO

The GO bit in the Mode Register is set in order to begin processing of an image. Before setting the GO bit, the ZR36015‘s Mode Register and Table values should be configured for the desired operation, and the BSY bit (in the Mode Register) should be checked to insure that it is not set. If the BSY bit is set, this indicates that the previous process has not completed, and so the ZR36015 is not ready to start a new process. If the BSY bit is not set, then the ZR36015 is free to begin a new process. The $\overline{BSY}$ signal can be monitored to determine when the previous process is complete.

When the GO bit is set, then the ZR36015 will respond to the next VEN that is sees. The GO bit must be set at lease 3 SYSCLK cycles before the trailing edge of VEN in order to respond to the next active high pulse of VEN. If the GO bit is not set at least 3

SYSCLKs before the trailing edge of VEN, then the following VEN signal (active high) will be ignored, and the VEN pulse after that will be processed.

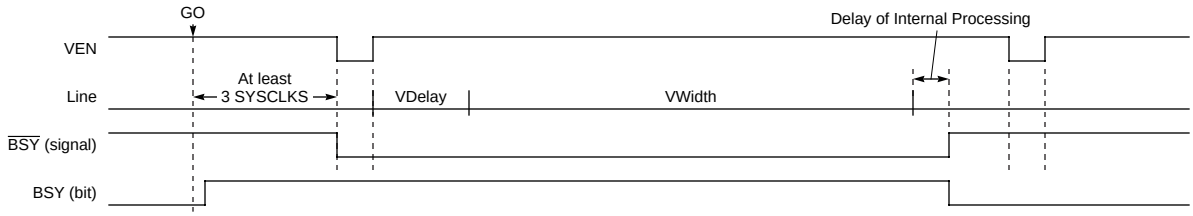


Figure 10. Relationship of BSY Terminal and BSY Flag and GO Bit

DECIMATION

Horizontal Decimation of data by a factor of 2 is supported for the ZR36015. This allows for the reduction of the volume of data being stored in the Strip Buffer (and sent out over the BDATA bus) by half.

The tables below shows how data is decimated for each mode.

Decimation	Pixel Elements							
Mode 0 (4:0:0)	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Mode 1 (4:2:2)	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
	U0	V0	U2	V2	U4	V4	U6	V6
Mode 3 (4:1:1)	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
	U0/V0				U4/V4			

During expansion there is no interpolation mode for the data (except as described below for mode 2).

In mode 2, the data is decimated horizontally as shown above for mode 1. But in addition, the UV data for every other line (starting with the second line) is dropped. The figure below shows this case.

Decimation	Pixel Elements							
Mode 2 (1st line)	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
	U0	V0	U2	V2	U4	V4	U6	V6
Mode 2 (2nd line)	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
	U0	V0	U2	V2	U4	V4	U6	V6

During Expansion in mode 2, the UV data for the 1st line is replicated to replace to corresponding UV data for the second line.

Note that the MCU for mode 2 will be H=2, V=2.

Sub-Buffer and Strip Buffer Interface

Figure 12 shows the Sub-Buffer Interfaces between the Pixel Data, the Coder Data, and the double buffered Strip Memory.

The Strip Memory Interface can perform a 16-bit read or write on every SYSCLK cycle. In order to keep up with the required data throughput, the Pixel Data and Coder Data Sub-Buffers each must be able to perform a 16-bit read or write to the Strip Memory on every other SYSCLK cycle. Therefore the Strip Memory Interface is shared between the Pixel Data, and Coder Data Sub-Buffers, with each Sub-Buffer accessing the Strip Memory on alternate SYSCLK cycles. Figure TBD shows the timing for alternate read and writes to the Strip Memory.

The Pixel Data Sub-Buffer performs conversion of the data between the PXDATA Bus and the Strip Memories. (The A Memory stores the data for all the even pixels, and the B Memory stores the data for all the odd pixels; (see the section on Strip Memory Format).

The Coder Data Sub-Buffer performs the conversion of the data between the Strip Memories and the Coder Data Bus.

During Compression, pixel data is transferred from the PXDATA Bus to the Strip Memories, and data from the Strip Memories is transferred to the Coder Data Bus. During Expansion, Coder data is transferred to the Strip Memories, and data from the Strip Memories is transferred to the Pixel Data Bus.

Figure TBDX7 shows the timing for the data and the control signals for the Strip Buffer Interface.

Note that reads and writes to the Strip Memory are asynchronous to one another, in that either can continue to occur (on alternate SYSCLK cycles) independently of whether or not the other side is ready to transfer data. The only restriction is that a strip buffer must be emptied (filled) before its time to switch sides (or else the CBSY signal becomes active (see section TBD)

Strip Buffer

In Compression, the raster format data is read into the Strip Buffer and stored in interlaced JPEG Block format in the Strip Buffer. This data is then read out to the Coder Data Bus in interlaced Block format for compression by the JPEG CODEC (ZR36050). In Expansion, the operation is reversed.

For modes 0,1 and 3,the Strip Buffer is filled with the data from 8 lines. For mode 2, data from 16 lines is stored in a Strip Buffer.

The Strip Buffers are composes of an A and B side. The A side stores the even pixel data and the B side stores the odd pixel data. Figure 12 shows the A and B sides to the Strip Buffers.

In order to provide double buffering (two strip buffers), the A and B memories are separated into high and low address spaces. The high address space of the A and B Memories is indicated by the A' and B' shown in the figure below. The starting address of A' and B' is determined by the mode of operation for the ZR36015 and whether decimation is being performed (see the section on Strip buffer Capacity).

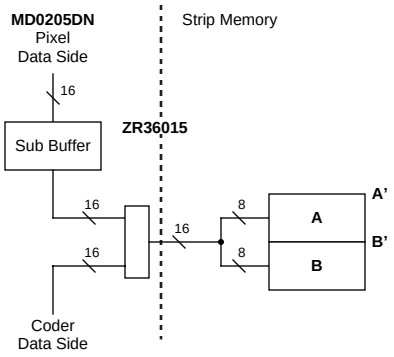


Figure 11. Double-Buffer Configuration

CODER BUSY SIGNAL (CBSY)

Before changing over from the A/B face to the A'/B' face of from the A'/B' face to the A/B face the CBSY signal must not be active. The CBSY signal is active under the following conditions.

1. In compression, when all of the pixel data for the active window have been written to the Strip Memory, then CBSY will be asserted if the Coder has not yet read out all data from the other side of the Strip Memory Buffer.
2. In expansion, when all of the pixel data for the current frame has been read out of one face of the double buffered Strip Memory, and the Coder has not yot filled the other side of the buffer with data for the next frame.

In either Compression or Expansion, if CBSY is set, then the first HEN signal (for the next strip) should not be asserter until the CBSY signal becomes inactive.

Factors which can alleviate system problems which are caused by CBSY, are the use of decimation and/or the reduction of the "active image area".

CONDITIONS FOR CBSY IN ENCODING MODE

The following sections describe the CBSY signal in relation to the timing for loading and unloading the strip memory. Examples are given for the encoding and for the decoding modes.

The Strip Memory is double buffered, with one buffer being represented by the A,B memories, and the othre buffer represented by the A',B' memories (see figure TBD). For the purpose of the following discussions, we assume that we start loading to the AB side of the Strip Buffer, and then load the A'B' side of the strip buffer (see references to AB,A'B' in figures TBD-TBD).

Encoding Examples of CBSY Timing

Example #1 : No $\overline{\text{CBSY}}$

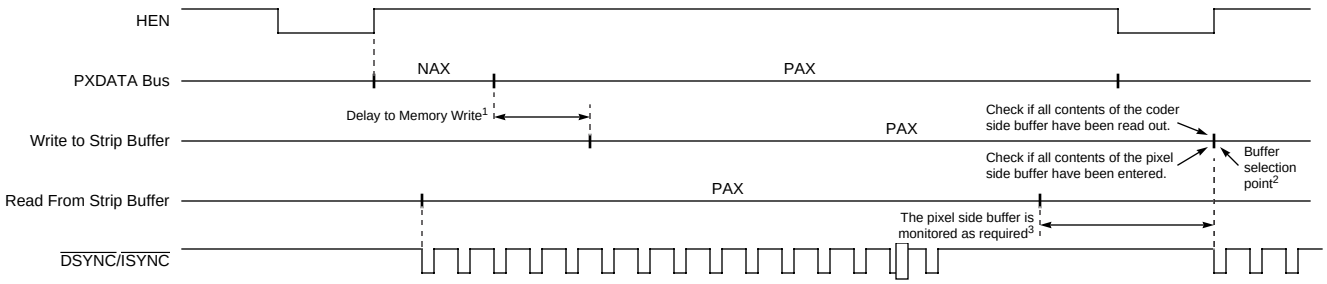
Figure 12 shows an example in encoding mode, where the CBSY is not issues.

Referring to Figure 12, following sequence of events occur...

1. HEN goes HIGH, (indicating the start of the last line of a strip. The ZR36015 begins to count HDelay in order to ingnore the first HDelay pixels of the line.
2. DSYNC active indicates that data for Strip Buffer AB (previously loaded) is being unloaded to the Coder Bus.
3. The ZR36015 finishes counting HDelay; data for Strip Buffer A'B' continues to be loaded from the Pixel bus.
4. Readout of data from the A'B' side of the strip buffer is complete. The ZR36015 checks to make sure that the AB side of the Strip Buffer is full before switching sides to begin reading data from the AB side to the Code Buffer. In Example 1, The first DSYNC for the next strip is not issues immediately because the A'B' side of the Strip Buffer is still being loaded.
5. The writing of a strip to the A'B' side of the Strip Buffer is complete. At this time the Coder side switches, and data from the A'B' side of the strip buffer starts to be read out to the Coder interface, as indicated by the active DSYNC signal.

In Example 1, no CBSY was generated because when the strip being loaded into the A'B' side of the Strip Buffer was completed, the AB side of the code buffer was already empty and the Pixel Side was able to switch to the AB side immediately in order to begin writing the next strip.

We assummed in Example 1 that $\overline{\text{STOP}}$ was not active, otherwise new $\overline{\text{DSYNC}}$s would not be issued (i.e. the ZR36015 would not write data to the ZR36050 Codec) until the $\overline{\text{STOP}}$ signal became inactive.



1. See table TBD for “Delay to Memory Write”.
2. The “Buffer Selection Point” happens at the completion of writing a strip (???? line), and indicates when the ZR36015 switches strip buffer sides to read this new strip.
3. When a complete strip has been written, then the 1st DSYNC for this strip will be asserted (assuming that STOP is not active).

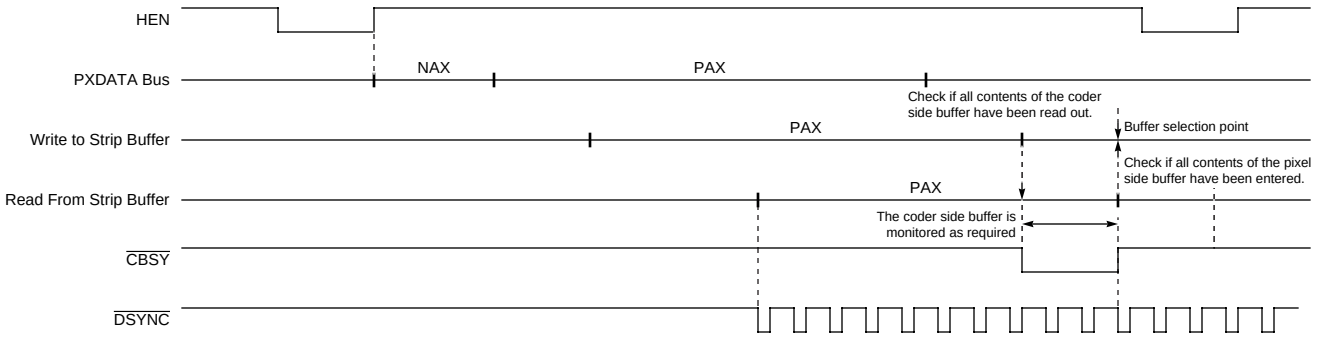
Figure 12. Example of Double-Sided Buffer Selection Timing - In Encoding (No $\overline{\text{CBSY}}$)

Example #2: Short $\overline{\text{CBSY}}$

Figure 13 shows an example in encoding mode, where the CBSY is issued for a short period (i.e., CBSY becomes inactive before the beginning of input for the next strip).

1. HEN goes HIGH, indicating the start of the last line of a strip. The ZR36015 begins to count HDelay in order to ingnore the first HDelay pixels of the line.
2. The ZR36015 finishes counting HDelay; data for Strip Buffer A’B’ starts to be loaded from the Pixel bus.
3. DSYNC active indicates that data for Strip Buffer AB (previously loaded) continues to be unloaded to the Coder Bus.
4. The writing of a strip to the A’B’ side of the Strip Buffer is complete. At this time the ZR36015 checks to see if the datat from AB has been unloaded. In example 2, AB is still in the process of being unloaded, so the CBSY signal is asserted to indicate the the ZR36015 is not ready to accept more input data from the Pixel side.

Readout of data from the AB side of the strip buffer is complete. Now two things happen. First, the ZR36015 detects that data is already availiable in the A’B’ side of the Strip Buffer, and so it continues to assert DSYNCs, indicataing that the A’B’ side is now being unloaded to the Coder Bus. Second, the CBSY signal becomes inactive, indicating that the AB side of the strip buffer is now empty and that data from the Pixel Bus can be loaded into the AB side.



1. When CBSY is outputted at the timing as shown above (completed within one line), the following oine is not ignored.
2. The timing of CBSY when the line is ignored is as shown below.

Figure 13. Example of Double-Sided Buffer Selection Timing - In Encoding (Short $\overline{\text{CBSY}}$)

Example #3: CBSY active when HDelay + HWidth is set to the maximum period of HEN

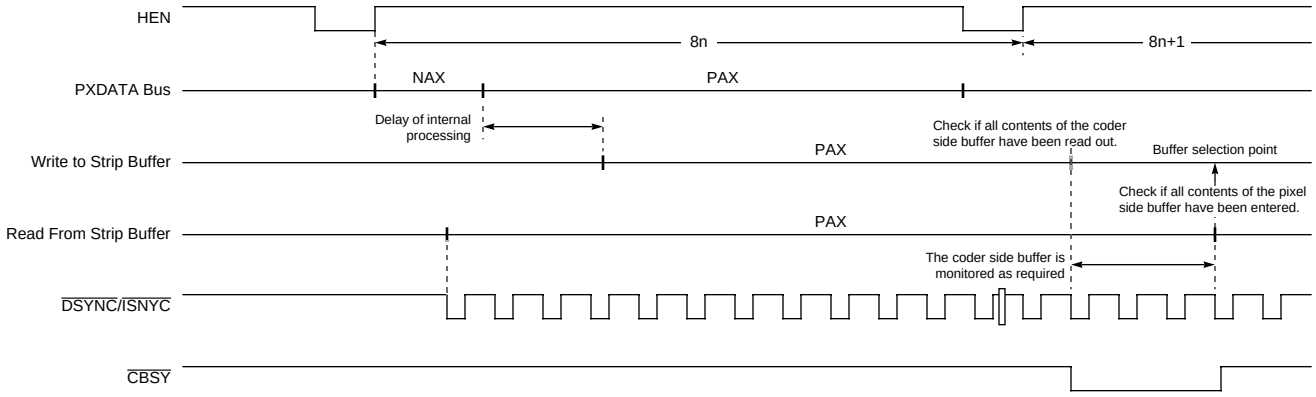
Figure 14 shows an example in encoding mode, where the HDelay + HWidth is set to the maximum perion of HEN. Because of this, the CBSY can become active after the HEN for the 1st line of the next strip becomes active.

1. HEN goes HIGH, (indicating the start of the last line of a strip. The ZR36015 begins to count HDelay in order to ingnore the first HDelay pixels of the line.

2. DSYNC active indicates that data for Strip Buffer AB (previously loaded) continues to be unloaded to the Coder Bus.
3. The ZR36015 finishes counting HDelay; then data for Strip Buffer A'B' continues to be loaded from the Pixel bus.
4. The writing of a strip to the A'B' side of the Strip Buffer is complete. At this time the ZR36015 checks to see if the datat from AB has been unloaded. In example 3, AB is still in the process of being unloaded, so the CBSY signal is asserted to indicate the the ZR36015 is not ready to accept more input data from the Pixel side. But before CBSY is asserted, the next HEN signal (for the first line of the next strip) becomes active.

   HEN has become active because the CBSY signal was not asserted in time to stop it. This is due to the HDelay+HWidth values being the maximum (length of HEN). Also, we've assumed that the low period between HENs is minimal.

In example 3, line 8n+1 will be ignored (lost) due to the CBSY signal. The ZR36015 will begin processing the next new input line after CBSY is de-asserted.



1. If PAX + NAX is set to the maximum effective period of HEN as shown above, $\overline{CBSY}$ may be active on a line following the 8n line (16n line depending on the mode) for the reason of internal delay. In this case, the processing of the line is started in MD0205, and finished when $\overline{CBSY}$ is active. In case of the above timing chart, MD0205 ignores the 8n+1 line, waits until $\overline{CBSY}$ becomes non-active and resumes processing from the rise of next HEN (8n+2 line).

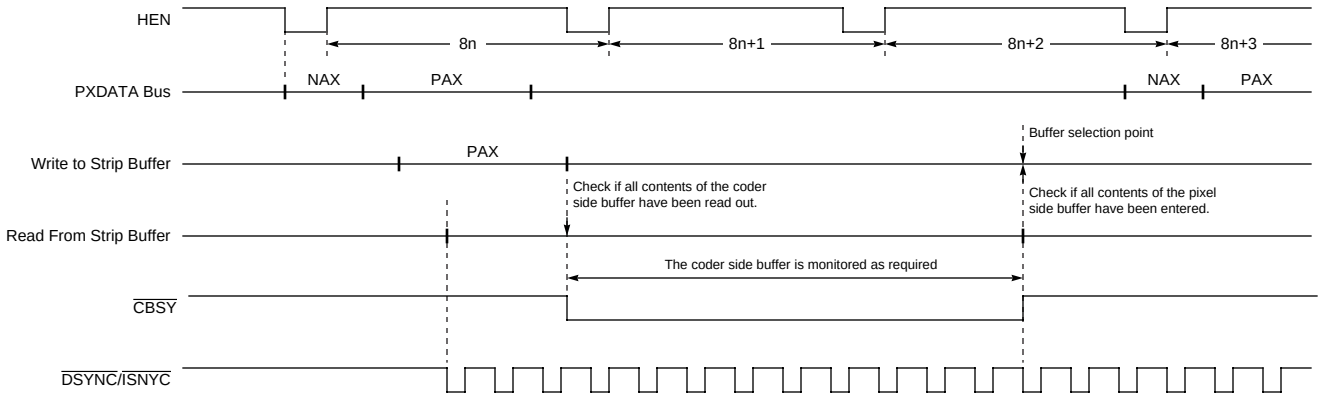
Figure 14. Example of CBSY Timing - In Encoding (HDelay + HWidth = Width of HEN)

Example #4: Long CBSY, New lines continue to come in

Figure 15 shows an example in enoding mode, where the CBSY signal is active for a long period (this could be the result of the STOP signal being active for a long period). Also in this example, new lines continue to be input into the ZR36015 (as indicated by the HEN signal).

In example #4, lines 8n+1 and 8n+2 will be ignored (lost), and processing will continue with line 8n+3.

For system which must not loose lines of data, the new lines of data must be held up and only input after CBSY becomes inactive.



1. If the processing at the coder side is substantially delayed and $\overline{CBSY}$ is outputted for a long period of time as shown above, all lines which cover $\overline{CBSY}$ are ignored. Accordingly, in case of the above timing chart, the 8n+1 line and the 8n+2 line are ignored and the processing is started from the 8n+3 line.

Figure 15. Example of CBSY Timing

Decoding Examples of CBSY Timing

Example #5

BUSY in Decoding Mode. Three examples for Decoding, Figure 24, E2, E3.

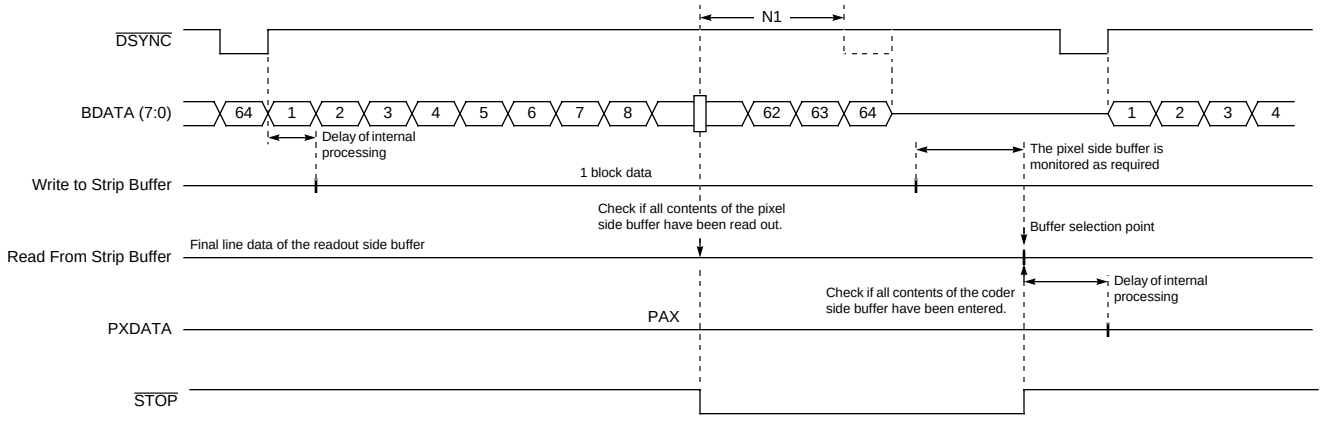


Figure 16. Example of Double-Sided Buffer Selection Timing - In Decoding

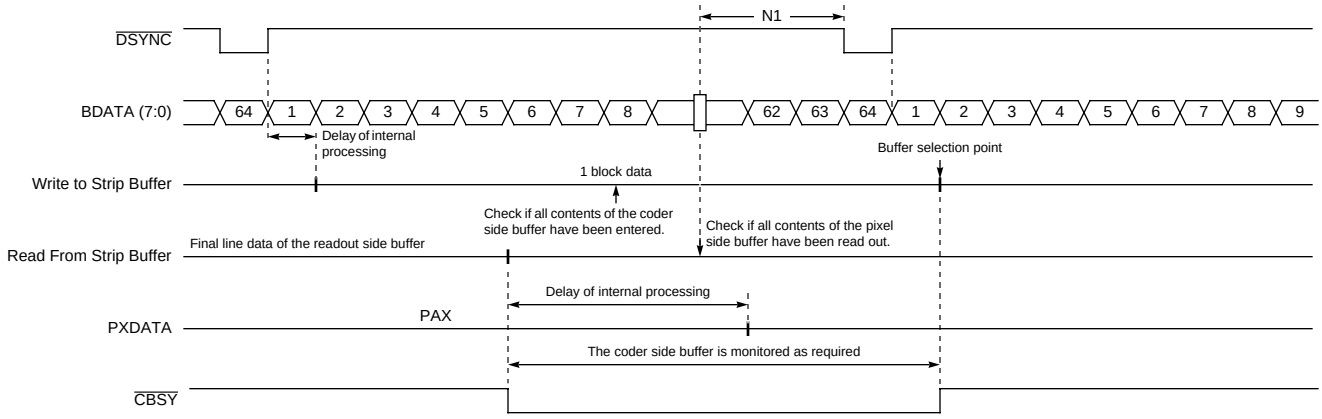


Figure 17. Example of Double-Sided Buffer Selection Timing - In Decoding

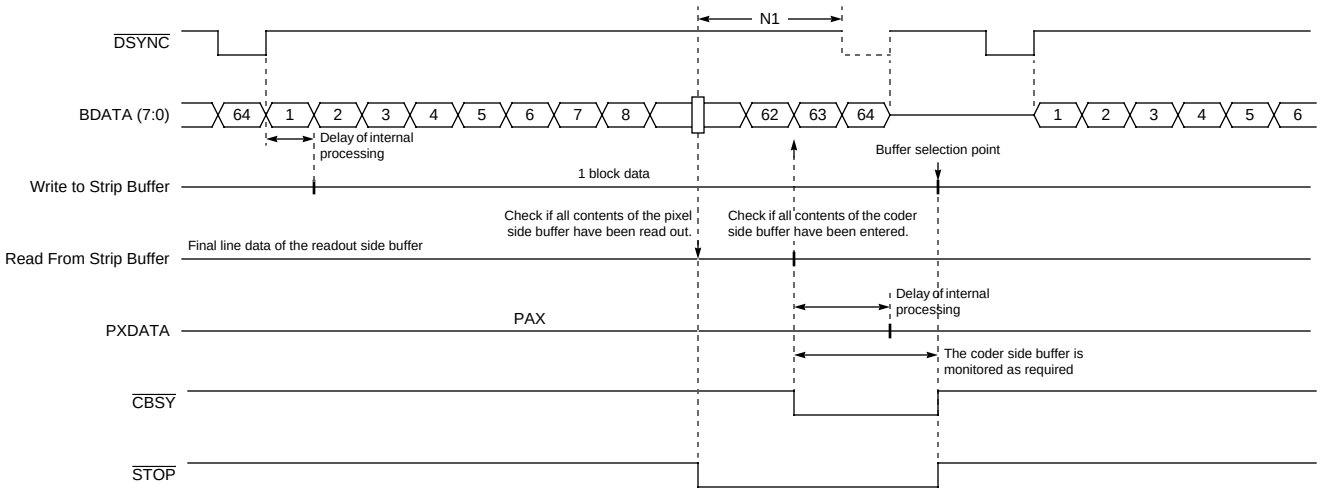


Figure 18. Example of Double-Sided Buffer Selection Timing - In Decoding

Strip Buffer Memory Format

Two SRAMs form a strip buffer. The 16-bit wide strip buffer is divided into 2 areas at point α * HWidth. Where:

$$\alpha = K * L * HWidth * D$$

	Low Memory	High Memory
Memory A (lower 8 bits)	Write Area (RD Area)	Read Area (Write Area)
Memory B (Upper 8 bits)	Write Area (RD Area)	Read Area (Write Area)

Address 0 Address = α * HWidth

An example of the amount of data stored in the strip buffer for each component of an active region of 704 x 240 is given in Figure 16.

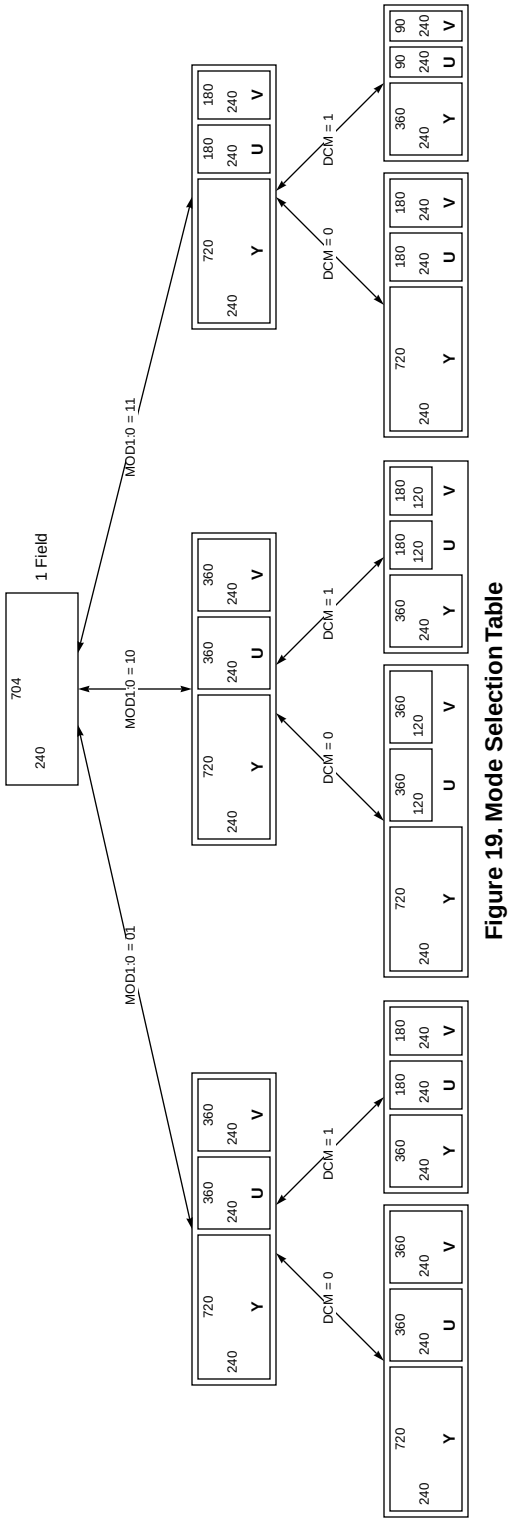
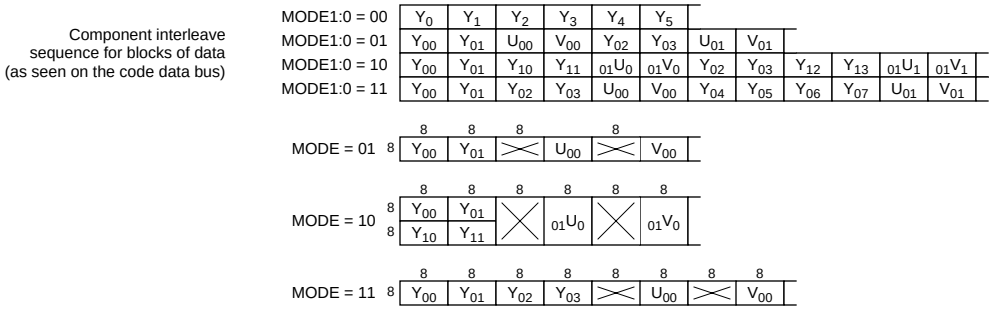
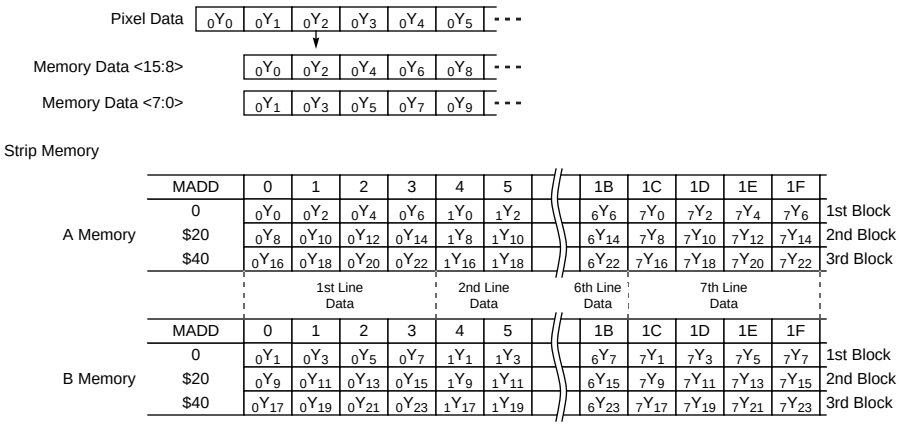


Figure 19. Mode Selection Table



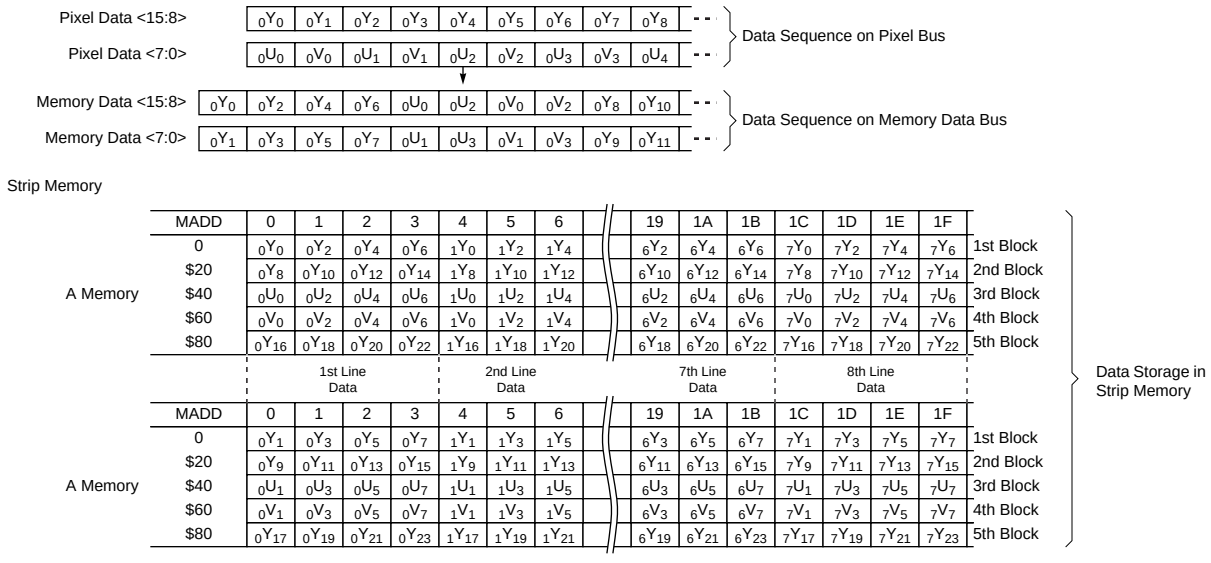
Note: Y_X notation indicates the "xth block of data for component Y

Figure 20. Memory Format - Write Area



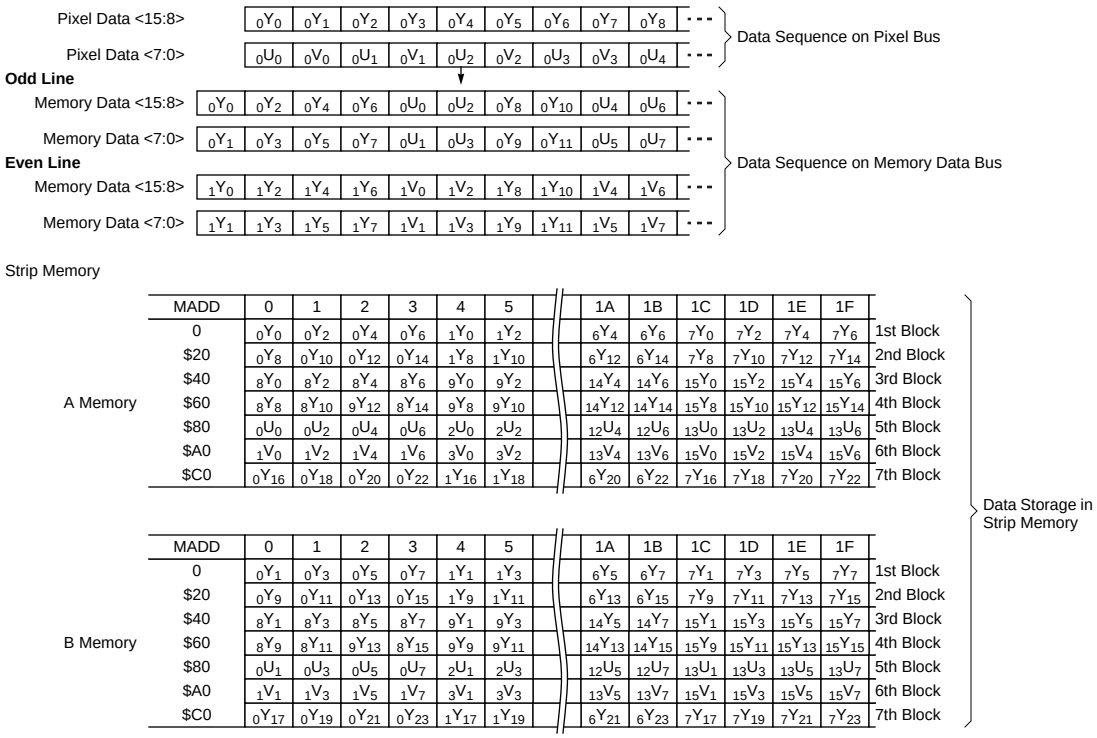
Note: $_aY_b$ notation indicates the Y component of the pixel element in row "a" and column "b".

Figure 21. Memory Format - MODE 1:0 = 00



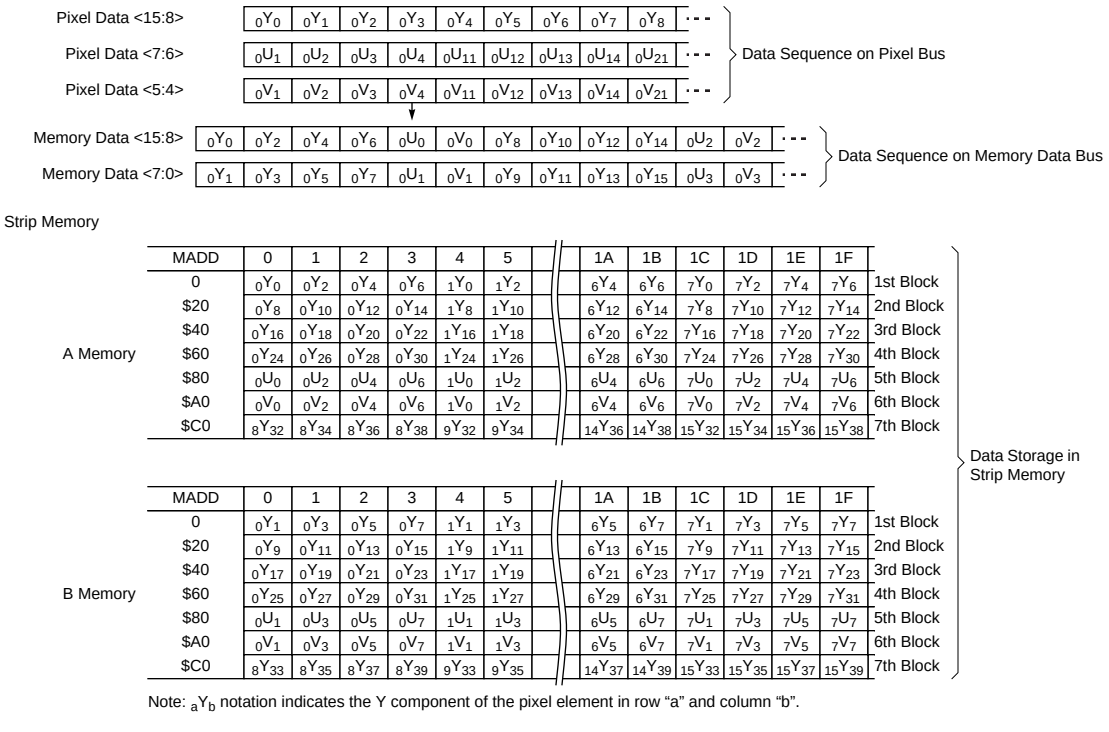
Note: $_aY_b$ notation indicates the Y component of the pixel element in row "a" and column "b".

Figure 22. Memory Format - MODE 1:0 = 01



Note: ${}_aY_b$ notation indicates the Y component of the pixel element in row "a" and column "b".

Figure 23. Memory Format - MODE 1:0 = 10



Note: ${}_aY_b$ notation indicates the Y component of the pixel element in row "a" and column "b".

Figure 24. Memory Format - MODE 1:0 = 11

Strip Buffer Capacity

The address range for the strip buffer is 64K (limited by the number of address bits for the strip buffer memory). Given that the strip buffer is 16 bits wide, this gives a maximum memory capacity of 128K bytes that can be accessed.

The raster to block process stores even blocks for each element in the A strip buffer memory, and the odd blocks for each element in the B strip bufer memory (see figure TBD). This divides the storage capacity required for the total strip evenly between the A and B sides of the memory.

The table below is used to calculate the required total strip buffer memory capacity (evenly distributed between the A and B memories) of the strip buffer.

$$\text{Capacity} = 2 \times K \times L \times \text{HWidth} \times D$$

Where...

- "2" is required because the strip buffer is double buffered
- K indicates the number of bytes of data required for each pixel
- L indicates the number of lines of data required to form a strip
- D is equal to "1" for no decimation delected, and is equal to "1/2" if decimation is selected.

The maximum number of pixels per line that can be entered for each mode is given in the table below. This number for the maximum number of pixels per line is determined by the maximum addressable strip buffer capacity. When less strip memory is used (i.e., less than 64K x 16-bits), then the numbers in the table below must be scaled accordingly.

The limitations for the VHeight values are given in the table below. These limitations are imposed so that the image size corresponds to a complete Minimum Configurable Unit (as defined in the JPEG specification)

MOD (1:0)	0 (1:0:0)	1 4:2:2)	2 (4:1:1)	3 (4:1:1)
k	1	2	1.5	1.5
1	8	8	16	8

HWidth is limited as shown below:

	MOD (1:0)	0 (1:0:0)	1 (4:2:2)	2 (4:1:1)	3 (4:1:1)
DCM = 0	HWidth maximum value (Maximum number of pixels in horizontal direction)	8192	4096	2720	5440
	HWidth minimum value (Minimum number of pixels in horizontal dirction)	8	16	16	32
	Setting value of HWidth	Multiple of 8	Multiple of 16	Multiple of 16	Multiple of 32

	MOD (1:0)	0 (1:0:0)	1 (4:2:2)	2 (4:1:1)	3 (4:1:1)
DCM = 1	HWidth maximum value (Maximum number of pixels in horizontal direction)	16384	8192	5440	10880
	HWidth minimum value (Minimum number of pixels in horizontal dirction)	16	32	32	64
	Setting value of HWidth	Multiple of 16	Mulitple of 32	Multiple of 32	Multiple of 64

The limitations to PAY are such that the maximum value is 8192 lines and the minimum value for each format is as shown below:

MOD (1:0)	0 (1:0:0)	1 4:2:2)	2 (4:1:1)	3 (4:1:1)
VWIdth minimum value (Minimum number of lines in vertical direction)	8	8	16	8
Setting value of VWIdth	Multiple of 8	Multiple of 8	Multiple of 16	Multiple of 8

Coder Bus Interface

The ZR36015 Raster to Block Converter interfaces directely to the ZR36050 JPEG Codec.

The Coder Bus Interface consists of the $\overline{\text{DSYNC}}$, BDATA(7:0), $\overline{\text{STOP}}$, $\overline{\text{EOS}}$, and $\overline{\text{COE}}$ signals (see figure 2).

The Direction of these interface for each mode of operation is given in the table below.

Table 5: Coder Bus Interface

Signal	Compression Mode (EDC = 0)	Expansion Mode (EDC = 1)
$\overline{\text{DSYNC}}$	Output	Input
BDATA (7:0)	Output	Input
$\overline{\text{STOP}}$	Input	Output
$\overline{\text{EOS}}$	Output	Input
$\overline{\text{COE}}$	Input	Input

The data transfer rate on BDATA(7:0) is equal to the SYSCLK rate for all formats.

The mode of operation is determined by the "EDC" bit in the Mode Register when the GO bit is asserted.

Bidirectional signals are availiable as inputs immediately after a hard reset, and as outputs after the GO bit in the Mode Register has been set.

The COE signal enables the outputs of the bidirectional signals of the Code Bus Interface. When COE is High, the outputs for Compression Mode are enabled, when COE is Low, the output for Expansion mode are enabled. When the ZR36015 is used

with the ZR36050, the COE signal is connected to the ZR36050's "COMP" output.

The DSYNC signal synchronized 64 byte block transfers between the ZR36015 and the ZR36050.

The STOP signal indicates to the sending device that the receiving device is not ready for more data. New blocks of data will not be sent to the receiving device until the STOP signal becomes inactive.

The EOS signal indicates the end of each component of a scan. This active low signal is an output in encoding modes. EOS indicates the last image data sample of the last block of each scan leaving the ZR36015. In encoding modes, EOS is output regardless of the STOP signal.

EOS is an input signal in the decoding mode. It is input together with the last image data sample of the last block of each scan entering the ZR36015.

The width of EOS is one SYSCLK cycle in encoding mode, and must be on SYSCLK cycle in decoding mode.

Figure 22 shows the functional timing for the DSYNC and EOS signals relative to the BDATA(7:0) data and SYSCLK.

The functional timing relationship for the STOP (when used as an input during compression mode) is given in Figure 23.

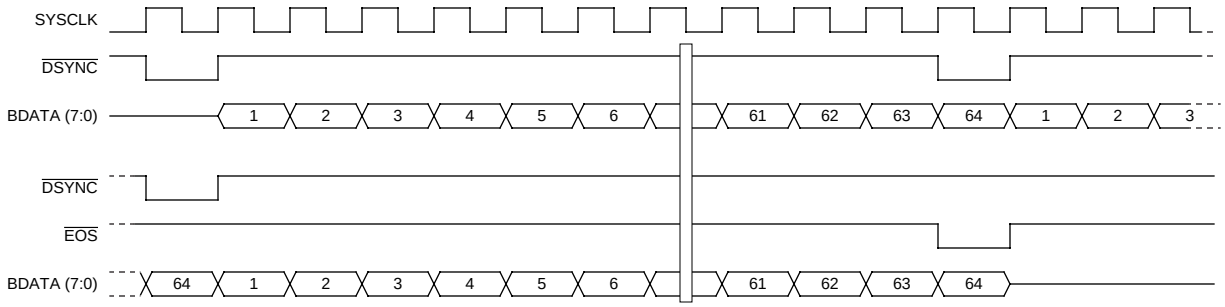


Figure 25. Functional Timing for DSYNC and EOS Relative to BDATA(7:0)

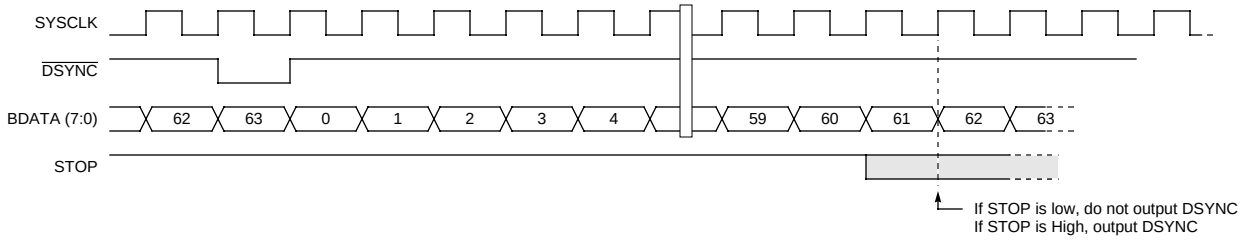


Figure 26. Functional Timing for STOP When Used as an Input

The "delay to memory write" indicates the number of clock cycles it takes for the pixel data to propagate through the ZR36015 to the strip buffer memory. This value is shown in the table below.

Table 6: Delay to Memory Write

Mode	Delay (in number of SYSCLKS)
0	2 or 3
1	10 or 11
2	10 or 11
3	10 or 11

In the table above, the smaller value corresponds to the even clock PXDATA element, and the larger value corresponds to the odd PXDATA element (the ZR36015 writes 16 bits to the strip memroy at a time).

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -40°C to +125°C
Supply Voltage to Ground Potential Continuous ..... -0.5V to V_{CC}+0.5V
DC Voltage Applied to Outputs for High Impedance Output State ..... -0.3V to V_{CC}+0.3V
DC Input Voltage ..... -0.5V to V_{CC}+0.5V

DC Output Current, into or out of Outputs (not to exceed 200mA total) 20mA/output
DC Input Current ..... ±10mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGE

Commercial Devices

Temperature ..... $0°C \le T_A \le +70°C$
Supply Voltage ..... $4.75V \le V_{CC} \le 5.25V$

DC CHARACTERISTICS

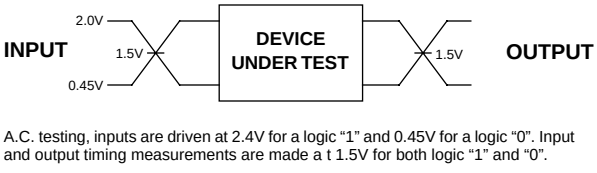
Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	–	0.8	V	
V_{IH}	Input High Voltage	2.0	–	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8mA
			V_{SS} + 0.05	V	I_{OL} = 1A
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -8mA
		V_{DD} - 0.05		V	I_{OH} = -1A
I_{CC}	Power Supply Current		TBD	mA	V_{DD} = 5V, f=30 MHz, C_L=20pf, T_A=25°C
I_{LI}	Input Leakage Current	-TBD	TBD	µA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage Current	-TBD	TBD	µA	$V_{OUT} = V_{SS}$
I_{OZ}	Output Disable Current	-TBD	TBD	µA	$V_{OUT} = V_{DD}$ or V_{SS}
C_{IN}	Input Capacitance		TBD	pF	
C_B	Bidirectional Capacitance		TBD	pF	
V_{II}	Hysteresis Voltage	TBD		V	

AC CHARACTERISTICS

Signal Number	Description	Min	Max	Units	Test Conditions
1	CLK Period	33		ns	
2	CLK High	15		ns	2.0V
3	Clock Low Width	15		ns	
4	Clock Rise Time	3		ns	
5	Clock Fall Time	3		ns	
6	Input Hold Time[1]	5		ns	
7	Input Setup Time[1]	5		ns	
8	Data Propagation Delay for PIXDATA[2]	4	33	ns	tbd
9	Data Propagation Delay for $\overline{\text{CBUSY}}$, WINDOW, $\overline{\text{BSY}}$	2	24	ns	
	Data Propagation Delay for CLKCSC	5	16		
10	Data Propagation Delay for $\overline{\text{DSYNC}}$, $\overline{\text{STOP}}$, $\overline{\text{EOS}}$, $\overline{\text{COE}}$, BDATA	2	17	ns	
11	RESET Pulse Width	tbd		ns	
12	Data Propagation Delay for WINDOW	2	24	ns	
13	Data Propagation Delay for PIXDATA[3]	4	33	ns	
18	Memory Write Address Set-up	tbd		ns	
19	Memory Write Address Hold[4]	1		ns	
21	Memory Write Pulse[5]	21		ns	
22	Memory Output Disable to End of Write	tbd		ns	
23	Memory Write Data Valid[6]	tbd		ns	
24	Memory Write Data Hold[4]	5		ns	
27	Memory Data High-Z Time	tbd		ns	
28	Memory Data Enable Time	tbd		nd	
30	Memory Read Cycle	tbd		ns	
33	Memory Output Enable Pulse Width (Low)	tbd		ns	
34	Memory Read Data Setup	tbd		ns	
35	Memory Read Data Hold	tbd		ns	
36	Memory Read Address Valid	tbd		ns	
37	Memory Read Address Hold	tbd		ns	
40	Propagation Delay for $\overline{\text{MWE}}$	2	23	ns	
41	Propagation Delay for $\overline{\text{MOE}}$	2	23	ns	
50	Time before Trailing SPH that $\overline{\text{RD}}$, $\overline{\text{WR}}$ Should be High	tbd		ns	
51	Minimum Host Write Pulse Width	tbd		ns	
52	Minimum Host Read Pulse Width	tbd		ns	

Signal Number	Description	Min	Max	Units	Test Conditions
53	Host Address Setup	tbd		ns	
54	Host Address Hold	tbd		ns	
55	Minimum Non-Active Time Between Host Read or Write	tbd		ns	
56	Minimum Time After Fall of SPH to 1st Read or Write	tbd		ns	
58	Host Read Address Hold Time	tbd		ns	
59	Host Write Data Valid	tbd		ns	
60	Host Write Data Hold	tbd		ns	
61	Host Read Data Enable	tbd		ns	
62	Host Read Data Valid	tbd		ns	
63	Host Read Data Hold	tbd		ns	
64	Host Read Data Disable	tbd		ns	
70	Propagation Delay for CSCCLK	tbd		ns	

1. T_{IH} and T_{IS} are for the following input signals: PXDATA (15:0), HEN, VEN, $\overline{DSYNC}$, $\overline{STOP}$, $\overline{EOS}$, BDATA
2. Assumes WINDOW signal is high.
3. Measured during clock cycle when WINDOW goes high.
4. Measured from either rise of $\overline{MWE}$, or fall of $\overline{MOE}$.
5. Time during which $\overline{MWE}$ = low, and $\overline{MOE}$ = high.
6. Measured from start of time when $\overline{MWE}$ = low, and $\overline{MOE}$ = High.



A.C. testing, inputs are driven at 2.4V for a logic “1” and 0.45V for a logic “0”. Input and output timing measurements are made a t 1.5V for both logic “1” and “0”.

Figure 1. AC TESTING INPUT, OUTPUT

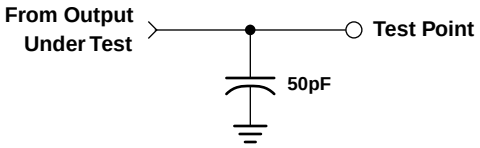


Figure 1. NORMAL AC TEST LOAD

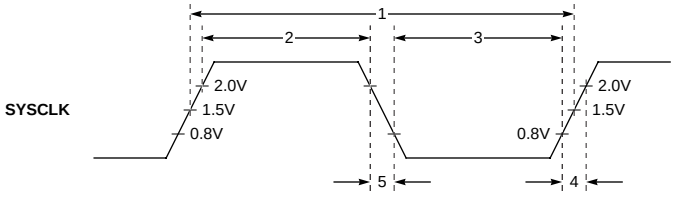


Figure 1. System Clock Timing

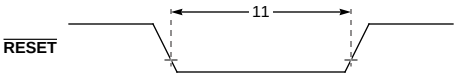


Figure 1. $\overline{RESET}$ Pulse Width

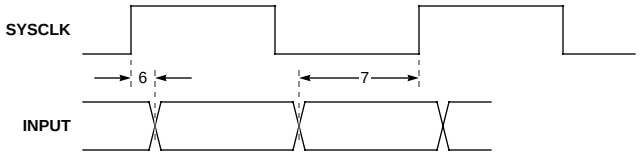


Figure 1. Synchronous Input Setup & Hold Times

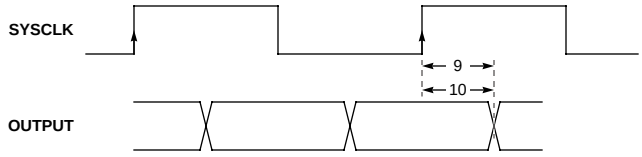


Figure 1. Output Propogation Delay

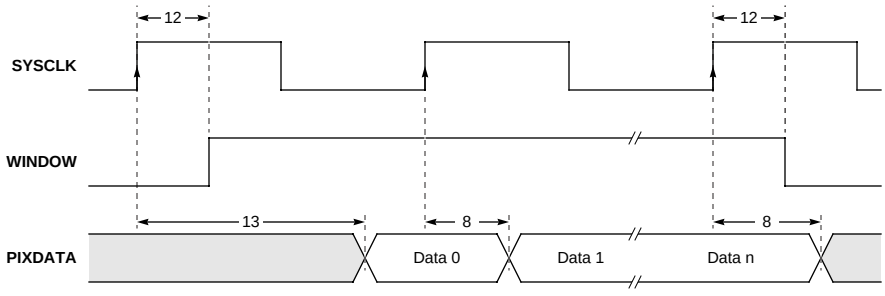


Figure 1. X4

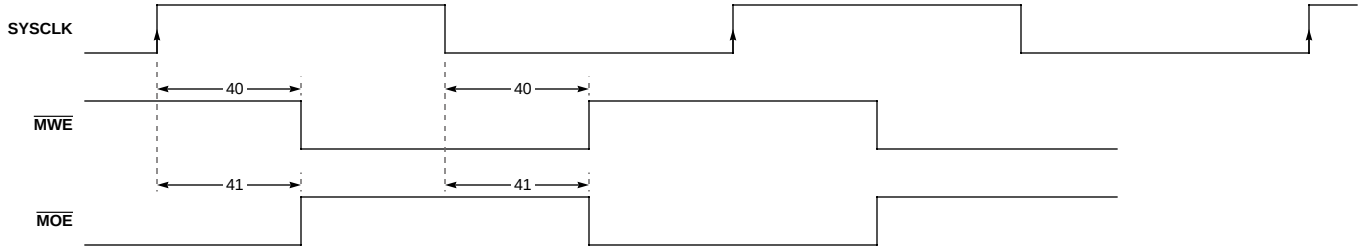


Figure 1. Memory Interface Synchronous Timing

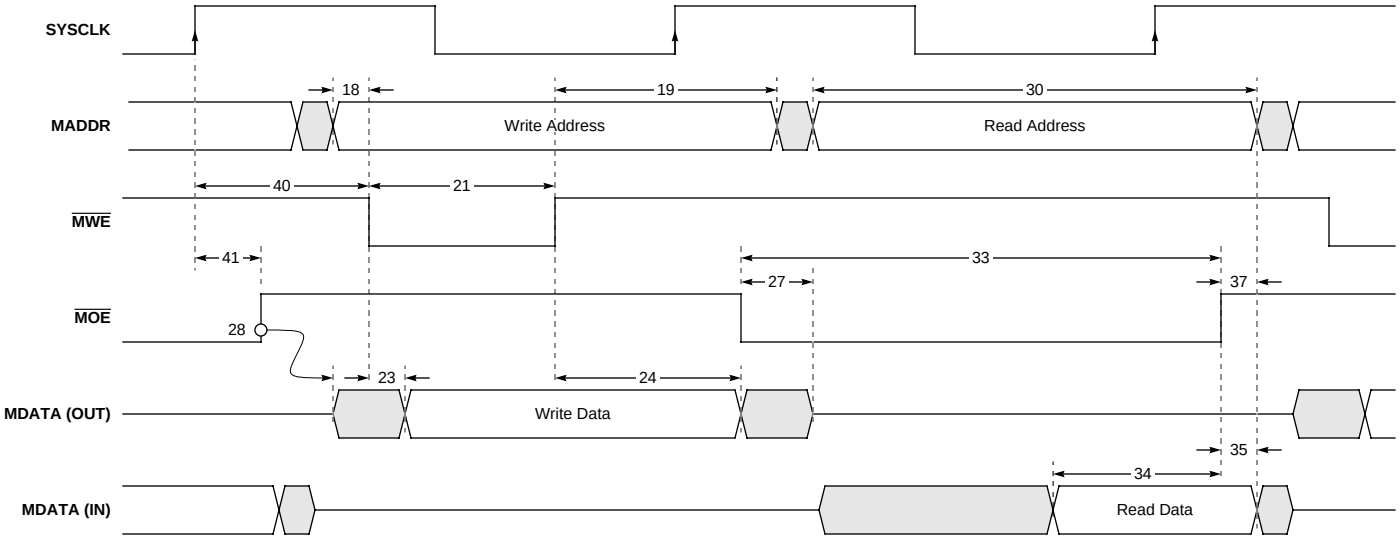


Figure 1. Memory Interface R/W Asynchronous Timing

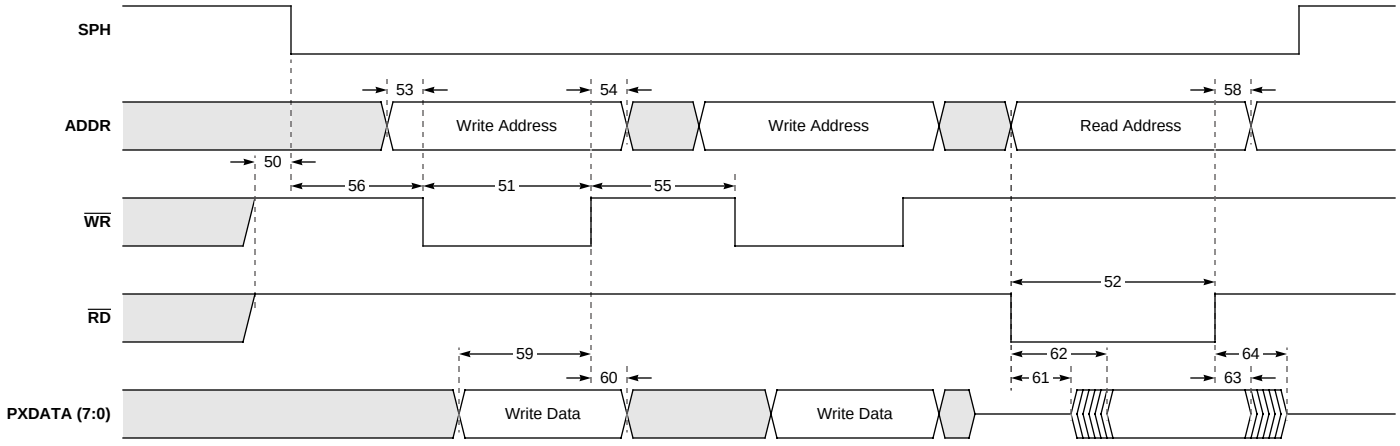


Figure 1. System Interface Timing

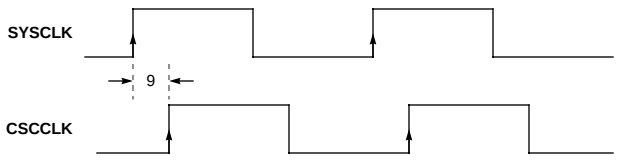


Figure 1. 203CLK Timing - Mode = 0

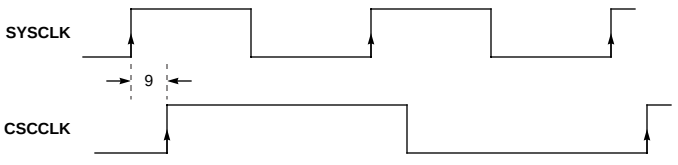
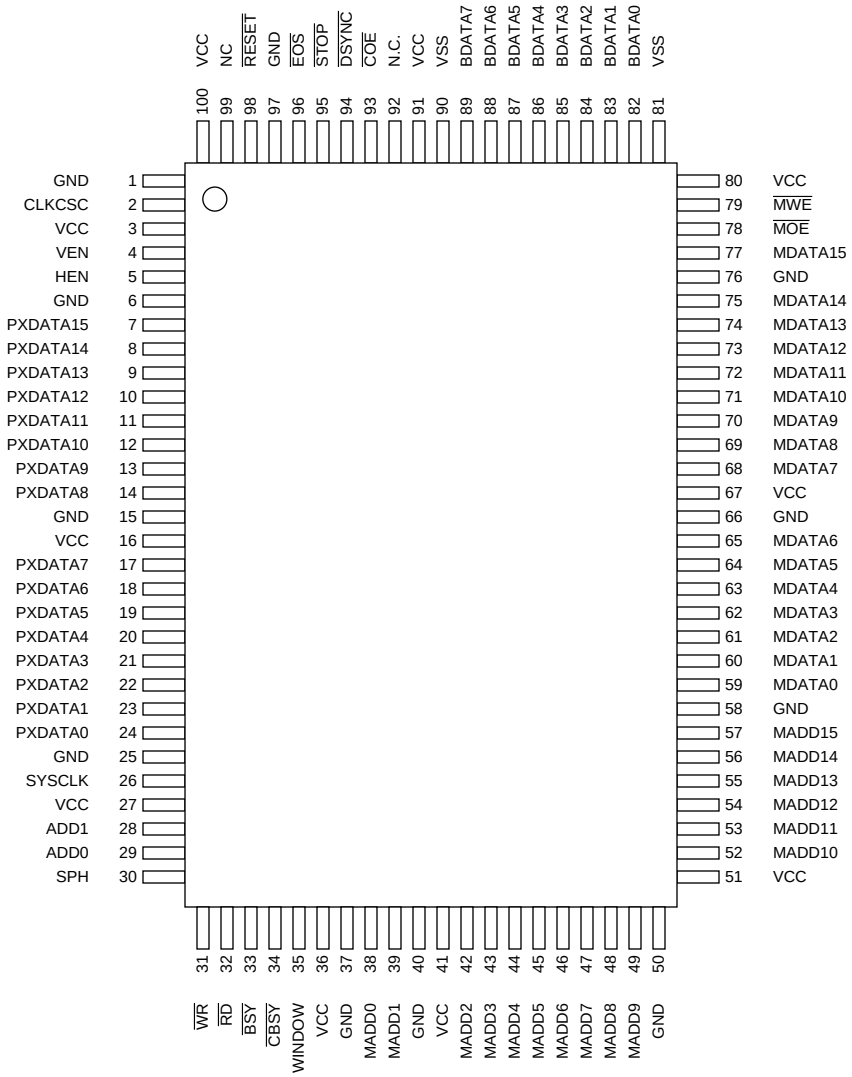


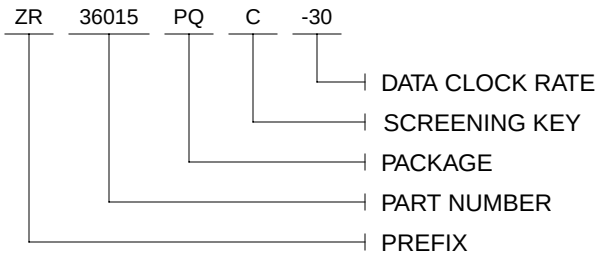
Figure 1. 203CLK Timing - Mode = 1, 2, 3

100-Pin Flat Pack Pin Assignment

Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type
1	GND	–	21	PXDATA3	B	41	VCC	–	61	MDATA2	O	81	GND	-
2	CLKCSC	O	22	PXDATA2	B	42	MADD2	O	62	MDATA3	O	82	BDATA0	B
3	VCC	–	23	PXDATA1	B	43	MADD3	O	63	MDATA4	O	83	BDATA1	B
4	VEN	I	24	PXDATA0	B	44	MADD4	O	64	MDATA5	O	84	BDATA2	B
5	HEN	I	25	GND	–	45	MADD5	O	65	MDATA6	O	85	BDATA3	B
6	GND	-	26	SYSCLK	I	46	MADD6	O	66	GND	–	86	BDATA4	B
7	PXDATA15	B	27	VCC	–	47	MADD7	O	67	VCC	–	87	BDATA5	B
8	PXDATA14	B	28	ADD1	I	48	MADD8	O	68	MDATA7	O	88	BDATA6	B
9	PXDATA13	B	29	ADD0	I	49	MADD9	O	69	MDATA8	O	89	BDATA7	B
10	PXDATA12	B	30	SPH	I	50	GND	–	70	MDATA9	O	90	GND	–
11	PXDATA11	B	31	$\overline{WR}$	I	51	VCC	–	71	MDATA10	O	91	VCC	–
12	PXDATA10	B	32	$\overline{RD}$	I	52	MADD10	O	72	MDATA11	O	92	NC	-
13	PXDATA9	B	33	$\overline{BSY}$	O	53	MADD11	O	73	MDATA12	O	93	$\overline{COE}$	O
14	PXDATA8	B	34	$\overline{CBSY}$	O	54	MADD12	O	74	MDATA13	O	94	$\overline{DSYNC}$	B
15	GND	-	35	WINDOW	O	55	MADD13	O	75	MDATA14	O	95	$\overline{STOP}$	B
16	VCC	-	36	VCC	-	56	MADD14	O	76	GND	–	96	$\overline{EOS}$	B
17	PXDATA7	B	37	GND	-	57	MADD15	O	77	MDATA15	O	97	GND	-
18	PXDATA6	B	38	MADD0	O	58	GND	-	78	$\overline{MOE}$	O	98	$\overline{RESET}$	I
19	PXDATA5	B	39	MADD1	O	59	MDATA0	O	79	$\overline{MWE}$	O	99	NC	–
20	PXDATA4	B	40	GND	–	60	MDATA1	O	80	VCC	–	100	VCC	-



ORDERING INFORMATION



PACKAGE
PQ - Plastic Quad Flat Pack (EIAJ)

DATA CLOCK RATE
30.0 MHz

SCREENING KEY
C - 0°C to +70°C (V_{CC} = 4.75V to 5.25V)

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