Z89313

DIGITAL TELEVISION CONTROLLER

FEATURES

Part Number	ROM (Word)	RAM (Word)	Speed (MHz)
Z89313	32K x 16	1K x 16	12
- 52-Pin Shrink DIP Package
- 4.5- to 5.5-Volt Operating Range
- Z89C00 RISC Processor Core
- 0°C to +70°C Temperature Range
- Direct Closed Caption Decoding
- TV Tuner Serial Interface
- Customized Character Set
- Character Control Mode
- Directly Controlled Receiver Functions

GENERAL DESCRIPTION

The Z89313 is a member of Zilog's family of Digital Television Controllers designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities.

The Z89313 features a powerful Z89C00 RISC processor core that controls on-board peripheral functions and registers using the standard processor instruction set.

In closed caption mode, text can be decoded directly from the composite video signal and displayed on the screen with assistance from the processor's digital signal processing capabilities. The character representation in this mode allows for a simple attribute control through the insertion of control characters.

The character control mode provides access to the full set of attribute controls. The modification of attributes is allowed on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

Display attributes, including underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency, are made possible through a fully customized 512 character set, formatted in two 256 character banks.

Serial interfacing with the television tuner is provided through the tuner serial port. Digital channel tuning adjustments may be accessed through the industry-standard I^2C port.

Additional hardware provides the capability to display two to three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Special circuitry can be activated to improve the visibiity of text by adding a right-sided shadow effect to the characters.

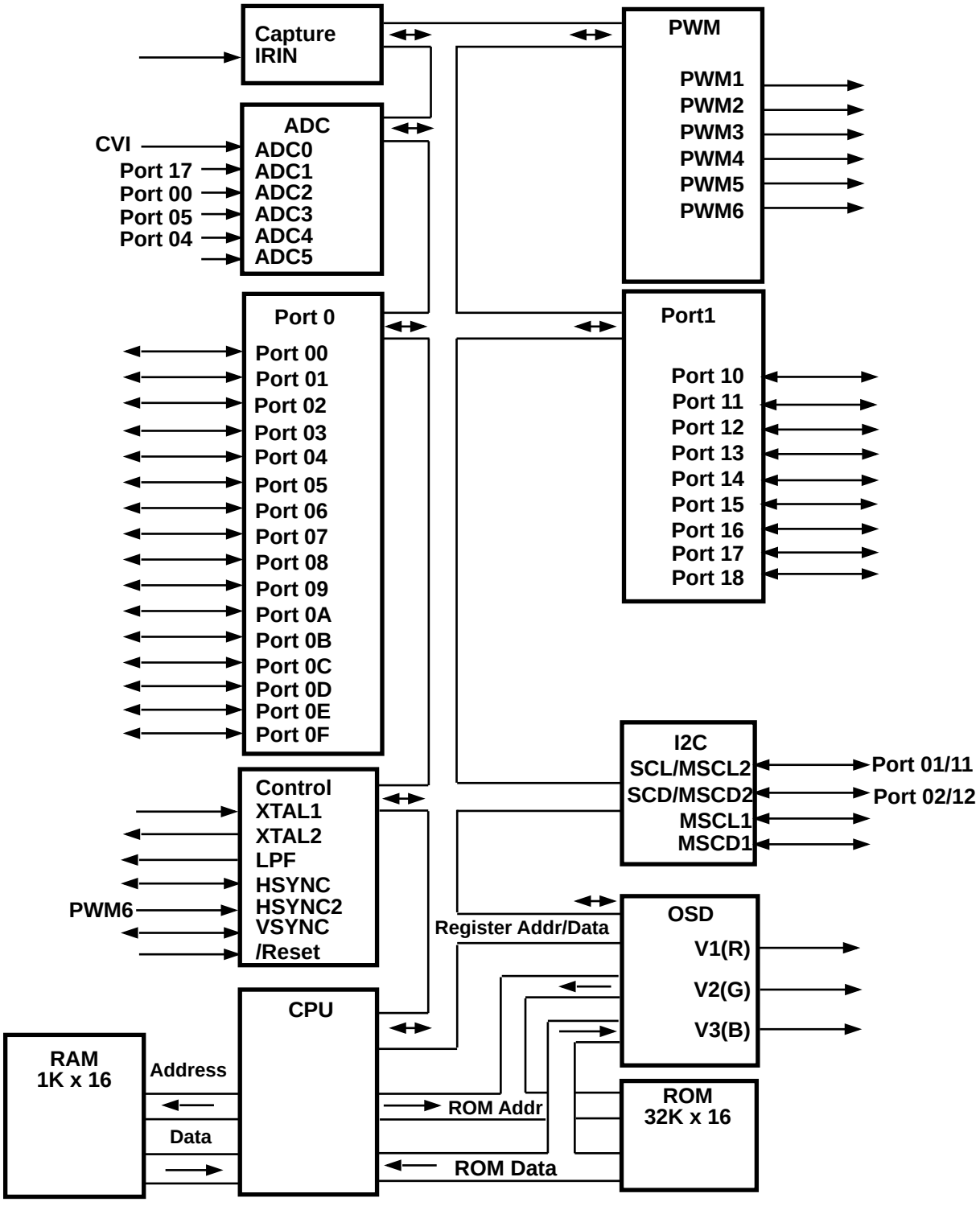
Receiver functions such as color and volume can be directly controlled by six 8-bit pulse width modulated ports.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

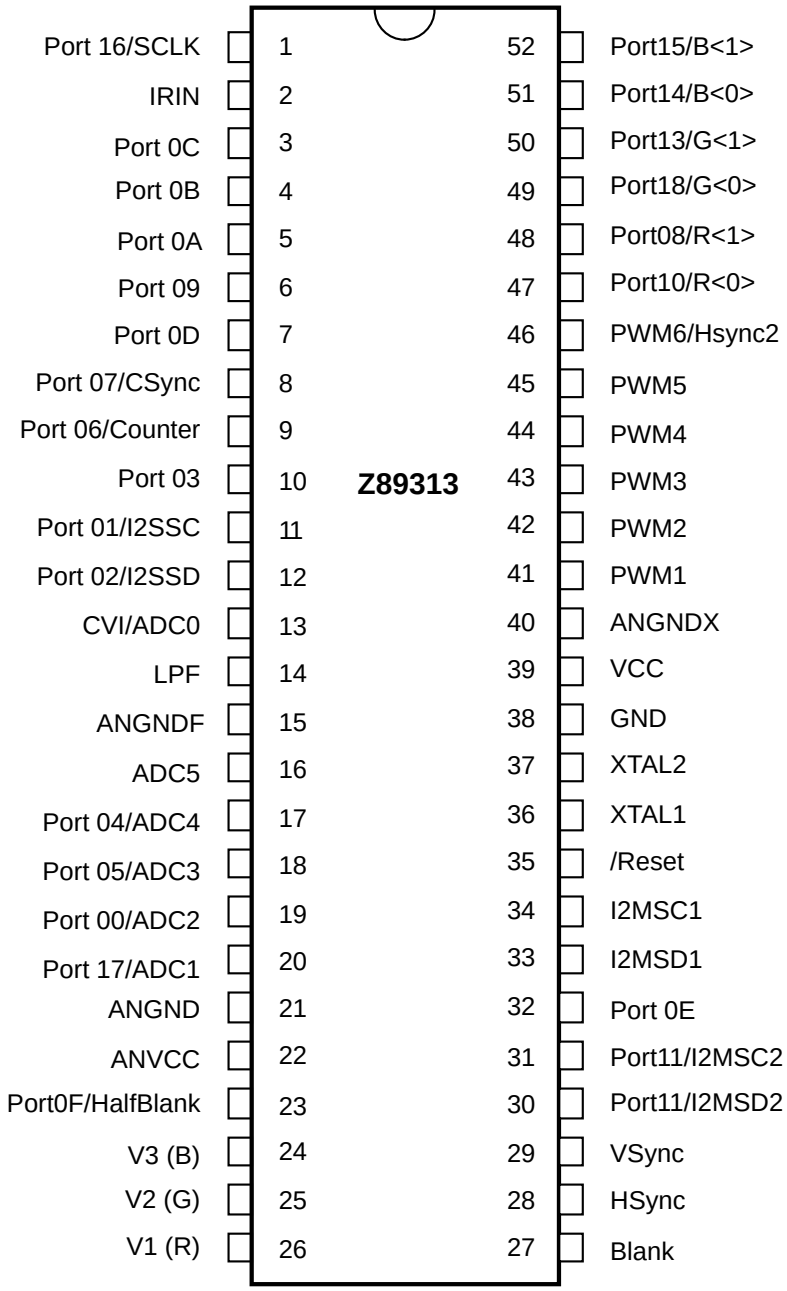
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

PIN DESCRIPTION



52-Pin Shrink DIP Configuration

PIN DESCRIPTION

Z89313

Pin Name	Function	Z89313 52-Pin	Configuration Direction	Configuration Reset
V_{CC}, ANV_{CC}[a]	+5 V	39,22	PWR	–
GND, ANGND, ANGNDF, ANGNDX[b]	0 V	38,21,15,40	PWR	–
IRIN	Infrared Remote Capture Input	2	I	I
ADC[5:1]	4-Bit Analog-to-Digital Converter Input	16,17,18,19,20	AI	I
PWM[6:1]	8-Bit Pulse Width Modulator Output	46,45,44,43,42,41	O	O
Port0[F:0]	Bit Programmable Input/Output Ports	23,32,7,3,4,5,6,48,8,9,18, 17,10,12,11,19	B	I
Port1[8:0]	Bit Programmable Input/Output Ports	49,20,1,52,51,50,30, 31,47	B	I
SCL	I^2C Clock I/O	11,31,34	BOD	
SCD	I^2C Data I/O	12,30,33	BOD	
XTAL1	Crystal Oscillator Input	36	AI	I
XTAL2	Crystal Oscillator Output	37	AO	O
LPF	Loop Filter	14	AB	O
HSYNC	H_Sync	28,46	B	I
VSYNC	V_Sync	29	B	I
/RESET	Device Reset	35	I	I
V[3:1]	OSD Video Output (Typically Drive B, G, and R Outputs)	24,25,26	O	O
Blank	OSD Blank Output	27	O	O
Half Blank	OSD Half Blank Output	23	O	
SCLK	Internal Processor SCLK	–	O	

Notes:

Please refer to pin-out diagram for shared pin numbers.

a) AN_{VCC} is for the reference voltage of the ADC input.

b) ANGND is for the reference ground of the ADC input.
ANGNDF is for LPF ground, and ANGNDX is for XTAL circuit ground.

V1, V2, V3 ANALOG OUTPUT

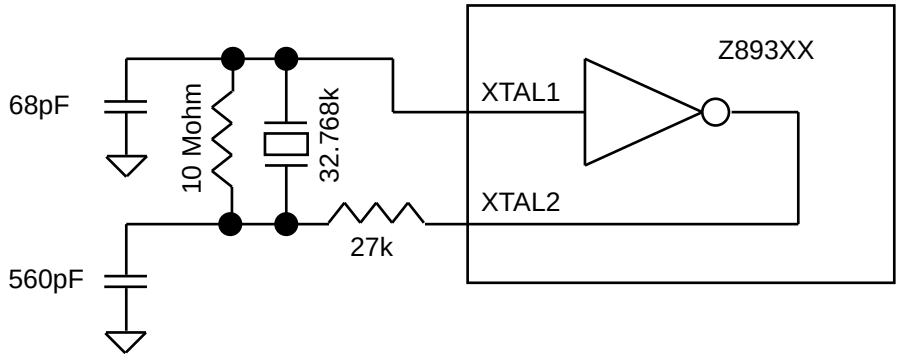
Specifications V_{CC} = 5.25 V

V_{cc} = 5.25 V	Condition	Limit
Output Voltage	Bit = 11	4.30 V ± 0.3 V
	Bit = 10	3.10 V ± 0.25 V
	Bit = 01	1.90 V ± 0.20 V
	Bit = 00	0 V ± 0.75 V
Setting Time	70% of DC Level, 10pf Load	< 50 ns

V1, V2, V3 ANALOG OUTPUT

Specifications V_{CC} = 4.75 V

V_{cc} = 4.75 V	Condition	Limit
Output Voltage	Bit = 11	3.90 V ± 0.30 V
	Bit = 10	2.80 V ± 0.25 V
	Bit = 01	1.70 V ± 0.20 V
	Bit = 00	0 V ± 0.65 V
Setting Time	70% of DC Level, 10pf Load	< 50 ns



32K Oscillator Recommended Circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Power Supply Voltage	0	7	V	
V_{ID}	Input Voltage	–0.3	V_{CC} +0.3	V	Digital Inputs
V_{IA}	Input Voltage	–0.3	V_{CC} +0.3	V	Analog Inputs (A/D0...A/D4)
V_O	Output Voltage	–0.3	V_{CC} +0.3	V	All Push-Pull Digital Output
I_{OH}	Output Current High		–10/–1[a]	mA	One Pin
I_{OH}	Output Current High		–100	mA	All Pins
I_{OL}	Output Current Low		20/1[b]	mA	One Pin
I_{OL}	Output Current Low		200	mA	All Pins
T_A	Operating Temperature	0	70	°C	
T_A	Storage Temperature	–65	150	°C	

Notes:
a) 1 mA max. when output pad impedance is 600 Ω.
b) 1 mA max. when output pad impedance is 600 Ω.

DC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to + 5.5 V; F_{OSC} = 32.768 KHz

Symbol	Parameter	Min	Max	Typical	Units	Conditions
V_{IL}	Input Voltage Low	0	0.2 V_{CC}	0.4	V	
V_{IH}	Input Voltage High	0.6 V_{CC}	V_{CC}	3.6	V	
V_{OL}	Output Voltage Low		0.4	0.16	V	@ I_{OL} = 1 mA
V_{OH}	Output Voltage High	V_{CC} –0.9		4.75	V	@ I_{OL} = 0.75 mA
V_{XL}	Input Voltage XTAL1 Low		0.3 V_{CC}	1.0	V	External Clock
V_{XH}	Input Voltage XTAL1 High	V_{CC} –2.0		3.5	V	Generator Driven
V_{HY}	Schmitt Hysteresis	3.0	0.75	0.5	V	On XTAL1 Input Pin
I_{IR}	Reset Input Current		150	90	µA	V_{RL} = 0 V
I_{IL}	Input Leakage	–3.0	3.0	0.01	µA	@ 0 V and V_{CC}
I_{CC}	Supply Current		100	60	mA	
I_{CC1}	Supply Current		300	100	µA	Sleep Mode @ 32 KHz
I_{CC2}	Supply Current		40	5	µA	Stop Mode

AC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to 5.5 V; F_{OSC} = 32.768 KHz

Symbol	Parameter	Min	Max	Typical	Units	Note
T_PC	Input Clock Period	16	100	32	µS	
T_RC,T_FC	Clock Input Rise and Fall			12	µS	
T_DPOR	Power On Reset Delay	0.8		1.2	s	Depends on Crystal

AC CHARACTERISTICS*

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to 5.5 V; F_{OSC} = 32.768 KHz

Symbol	Parameter	Min	Max	Typical	Units
T_WRES	Power-On Reset Min. Width		5TPC		µS
T_DH_S	H_Sync Incoming Signal Width	5.5	12.5	11	µS
T_DV_S	V_Sync Incoming Signal Width	0.15	1.5	1.0	mS
T_DE_S	Time Delay Between Leading Edge of V_Sync and H_Sync in Even Field	–12	+12	0	µS
T_DO_S	Time Delay Between Leading Edge of H_Sync in Odd Field	20	44	32	µS
T_WHV_S	H_Sync/V_Sync Edge Width		2.0	0.5	µS

Notes:
All timing of the I^2C bus interface are defined by related specifications of the I^2C bus interface.

Pre-Characterization Product:
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