Z0103/07/09 series

Triacs

Rev. 02 — 12 September 2002 **Product data**

1. Product profile

1.1 Description

Passivated triacs in conventional and surface mounting packages. Intended for use in applications requiring high bidirectional transient and blocking voltage capability. Available in a range of gate current sensitivities for optimum performance.

Product availability:

Z0103MA; Z0103NA; Z0107MA; Z0107NA; Z0109MA; Z0109NA in SOT54B

Z0103MN; Z0103NN; Z0107MN; Z0107NN; Z0109MN; Z0109NN in SOT223.

1.2 Features

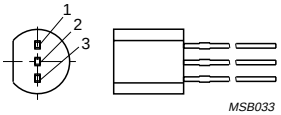
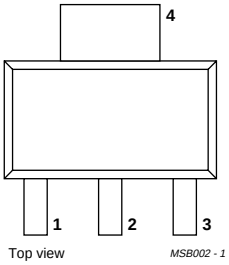
- Blocking voltage to 800 V (NA and NN types)
- 1 A on-state RMS current.

1.3 Applications

- Home appliances
- Fan controllers
- Small motor control
- Small loads in industrial process control.

2. Pinning information

Table 1: Pinning - SOT54B (TO-92), SOT223, simplified outline and symbol

Pin	Description		Simplified outline	Symbol
1	terminal 2 (T2)	SOT54B (TO-92)		 MBL300
2	gate (G)			
3	terminal 1 (T1)			
1	terminal 1 (T1)	SOT223		
2	terminal 2 (T2)			
3	gate (G)			
4	terminal 2 (T2)			

SOT54B (TO-92) **SOT223**

3. Ordering information

3.1 Ordering options

Table 2: Ordering information

Part Number	Voltage (V_{DRM})	Gate Sensitivity (I_{GT})	Package
Z0103MA	600 V	3 mA	SOT54B (TO-92)
Z0103NA	800 V	3 mA	SOT54B (TO-92)
Z0107MA	600 V	5 mA	SOT54B (TO-92)
Z0107NA	800 V	5 mA	SOT54B (TO-92)
Z0109MA	600 V	10 mA	SOT54B (TO-92)
Z0109NA	800 V	10 mA	SOT54B (TO-92)
Z0103MN	600 V	3 mA	SOT223
Z0103NN	800 V	3 mA	SOT223
Z0107MN	600 V	5 mA	SOT223
Z0107NN	800 V	5 mA	SOT223
Z0109MN	600 V	10 mA	SOT223
Z0109NN	800 V	10 mA	SOT223

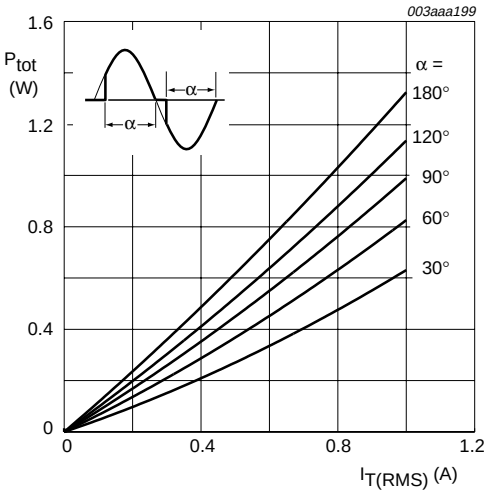
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

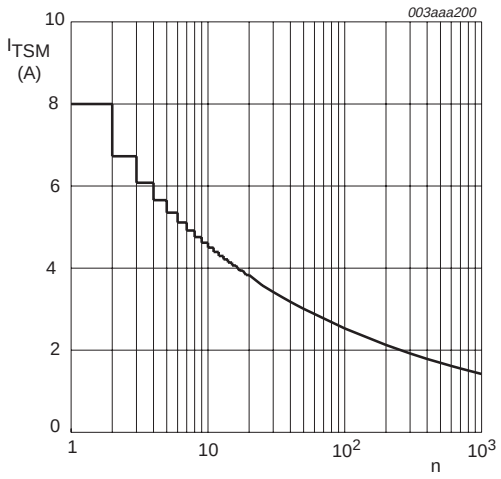
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage	25 °C ≤ T_j ≤ 125 °C			
	Z0103/07/09MA; Z0103/07/09MN		-	600	V
	Z0103/07/09NA; Z0103/07/09NN		-	800	V
V_{RRM}	repetitive peak reverse voltage	25 °C ≤ T_j ≤ 125 °C			
	Z0103/07/09MA; Z0103/07/09MN		-	600	V
	Z0103/07/09NA; Z0103/07/09NN		-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; T_j = 25 °C prior to surge; Figure 2 and Figure 3			
		t = 20 ms	-	8	A
		t = 16.7 ms	-	8.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles; Figure 4			
	SOT223	T_{sp} = 90 °C	-	1	A
	SOT54B (TO-92)	T_{lead} = 50 °C	-	1	A
I^2t	I^2t for fusing	t = 10 ms	-	0.35	A^2s
dI_T/dt	rate of rise of on-state current	I_{TM} = 1.0 A; I_G = 2 x I_{GT}; dI_G/dt = 100 mA/µs	-	20	A/µs
I_{GM}	peak gate current	t_p = 20 µs	-	1.0	A
P_{GM}	peak gate power		-	2.0	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		–40	+150	°C
T_j	junction temperature		–40	+125	°C

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α = conduction angle

Fig 1. Maximum on-state power dissipation as a function of RMS on-state current; typical values.



n = number of cycles at f = 50 Hz

Fig 2. Maximum permissible non-repetitive peak on-state current as a function of number of cycles for sinusoidal currents; typical values.

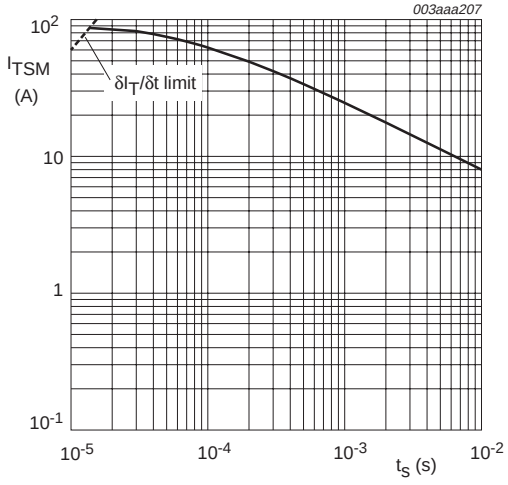


Fig 3. Maximum permissible non-repetitive peak on-state current as a function of surge duration for sinusoidal currents; typical values.

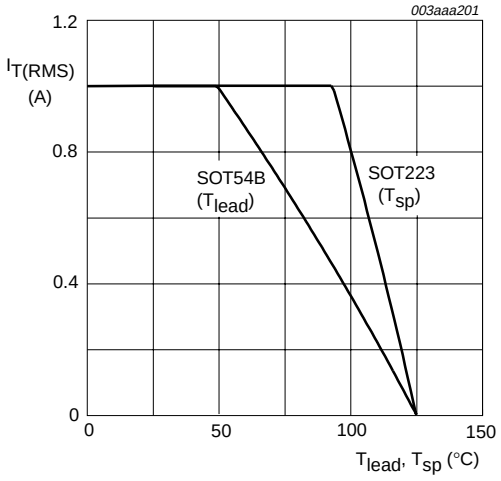


Fig 4. Maximum permissible RMS on-state current as a function of lead temperature and solder point temperature; typical values.

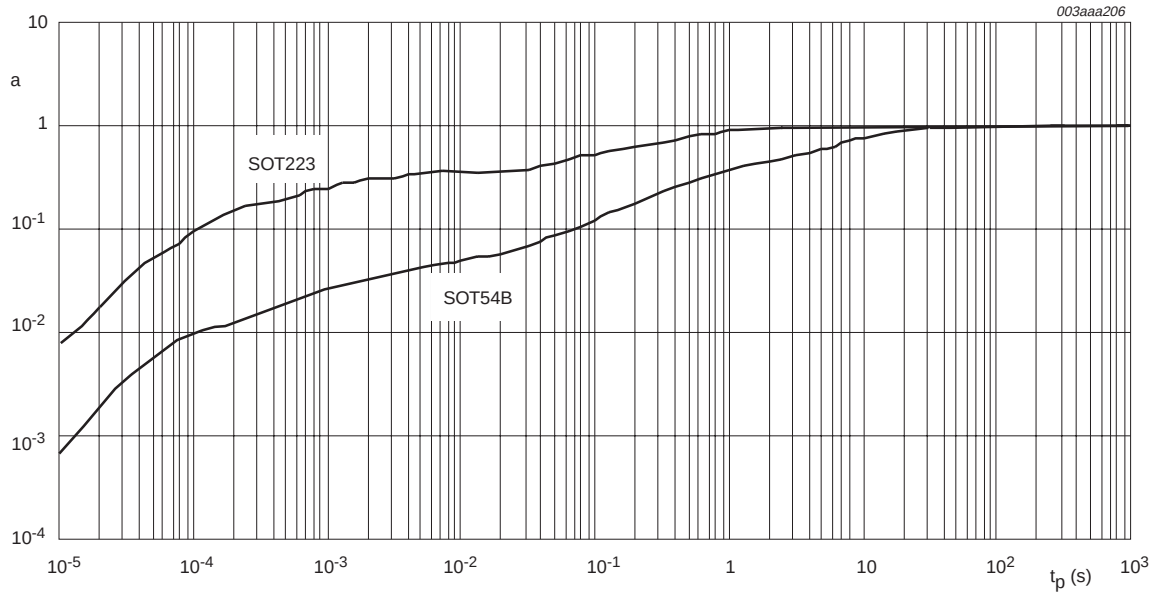
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5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point for SOT223	Figure 5	-	-	25	K/W
$R_{th(j-lead)}$	thermal resistance from junction to lead for SOT54B (TO-92)	Figure 5	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT223	minimum footprint; mounted on a PCB	-	60	-	K/W
	SOT54B (TO-92)	vertical in free air	-	150	-	K/W

5.1 Transient thermal impedance



$$a = \frac{Z_{th(j-lead)}}{R_{th(j-lead)}}$$ for SOT54B (TO-92)

$$a = \frac{Z_{th(j-sp)}}{R_{th(j-sp)}}$$ for SOT223

Fig 5. Transient thermal impedance from junction to lead and junction to solder point as a function of pulse duration.

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6. Characteristics

Table 5: Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; R_L = 30 Ω; T2+ G+; T2+ G–; T2– G–; Figure 9				
	Z0103MA/MN/NA/NN		-	-	3	mA
	Z0107MA/MN/NA/NN		-	-	5	mA
	Z0109MA/MN/NA/NN		-	-	10	mA
	Z0103MA/MN/NA/NN	V_D = 12 V; R_L = 30 Ω; T2– G+; Figure 9	-	-	5	mA
	Z0107MA/MN/NA/NN		-	-	7	mA
	Z0109MA/MN/NA/NN		-	-	10	mA
I_L	latching current	V_D = 12 V; R_L = 30 Ω; T2+ G+; T2– G–; T2– G+; Figure 7				
	Z0103MA/MN/NA/NN		-	-	7	mA
	Z0107MA/MN/NA/NN		-	-	10	mA
	Z0109MA/MN/NA/NN		-	-	15	mA
	Z0103MA/MN/NA/NN	V_D = 12 V; R_L = 30 Ω; T2+ G–; Figure 7	-	-	15	mA
	Z0107MA/MN/NA/NN		-	-	20	mA
	Z0109MA/MN/NA/NN		-	-	25	mA
I_H	holding current	I_T = 50 mA; Figure 8				
	Z0103MA/MN/NA/NN		-	-	7	mA
	Z0107MA/MN/NA/NN		-	-	10	mA
	Z0109MA/MN/NA/NN		-	-	10	mA
V_T	on-state voltage	Figure 6	-	1.3	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; R_L = 30 Ω; T_j = 25 °C; Figure 11	-	-	1.3	V
		$V_D = V_{DRM}$; R_L = 3.3 kΩ; T_j = 125 °C; Figure 11	0.2	-	-	V
I_D	off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 °C	-	-	500	µA
Dynamic characteristics						
dV_D/dt	critical rate of rise of off-state voltage	V_D = 0.67 $V_{DRM(max)}$; T_j = 110 °C; exponential waveform; gate open; Figure 10				
	Z0103MA/MN/NA/NN		10	-	-	V/µs
	Z0107MA/MN/NA/NN		20	-	-	V/µs
	Z0109MA/MN/NA/NN		50	-	-	V/µs
dV_{com}/dt	critical rate of change of commutating voltage	V_D = 400 V; I_T = 1 A; T_j = 110 °C; dI_{com}/dt = 0.44 A/ms; gate open				
	Z0103MA/MN/NA/NN		0.5	-	-	V/µs
	Z0107MA/MN/NA/NN		1	-	-	V/µs
	Z0109MA/MN/NA/NN		2	-	-	V/µs

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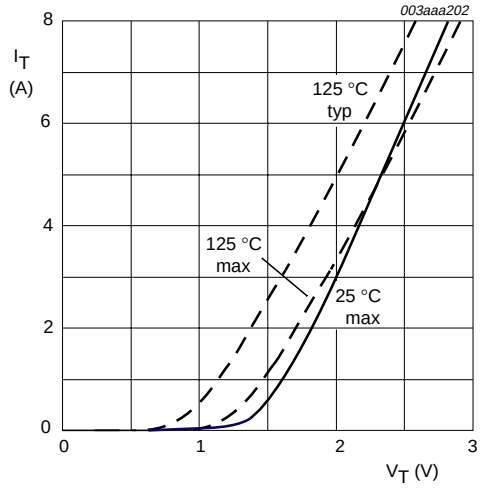
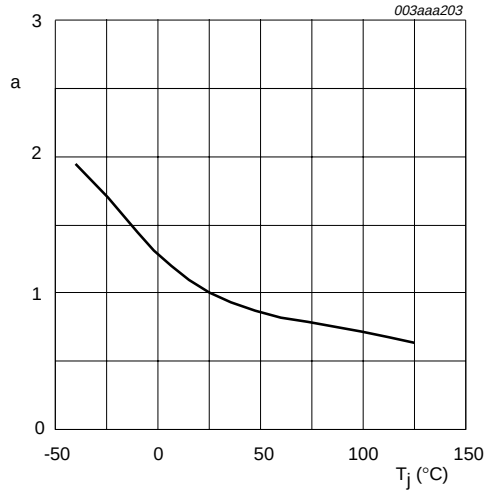
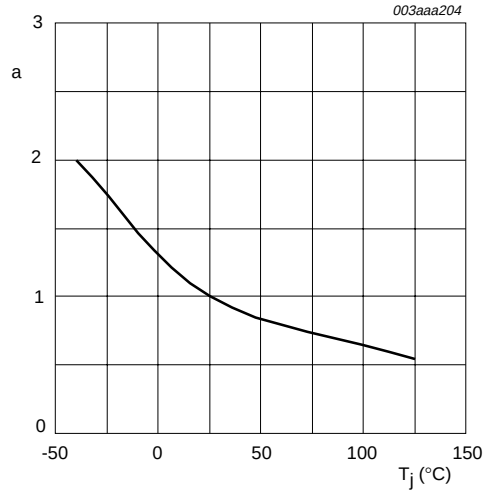


Fig 6. On-state current as a function of on-state voltage; typical and maximum values.



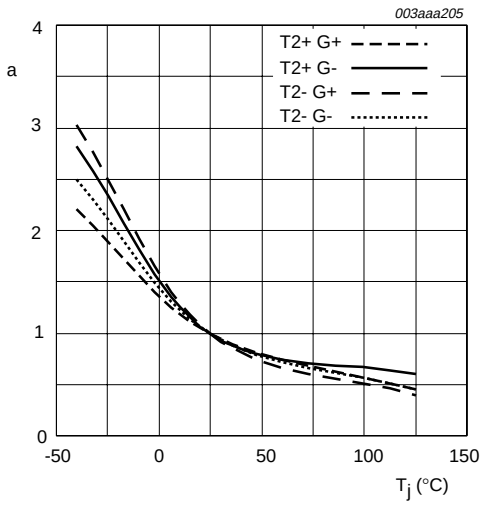
$$a = \frac{I_L}{I_{L(25^\circ C)}}$$

Fig 7. Normalized latching current as a function of junction temperature; typical values.



$$a = \frac{I_H}{I_{H(25^\circ C)}}$$

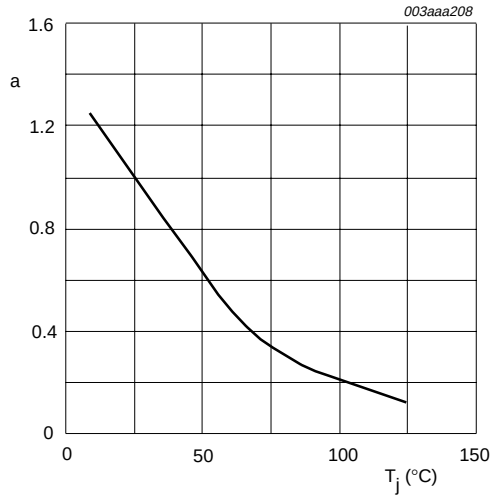
Fig 8. Normalized holding current as a function of junction temperature; typical values.



$$a = \frac{I_{GT}}{I_{GT(25^\circ C)}}$$

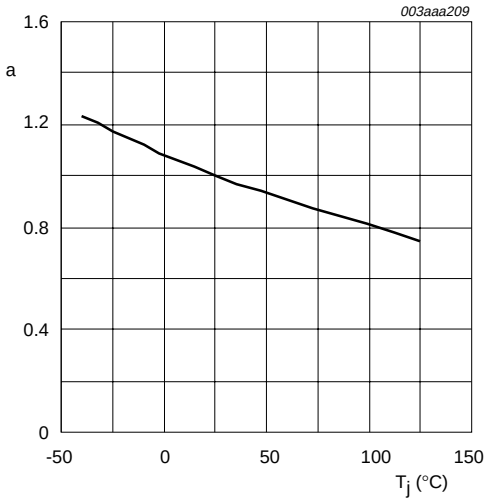
Fig 9. Normalized gate trigger current as a function of junction temperature; typical values.

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$$a = \frac{dV_D/dt}{dV_{D(25°C)}/dt}$$

Fig 10. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values.



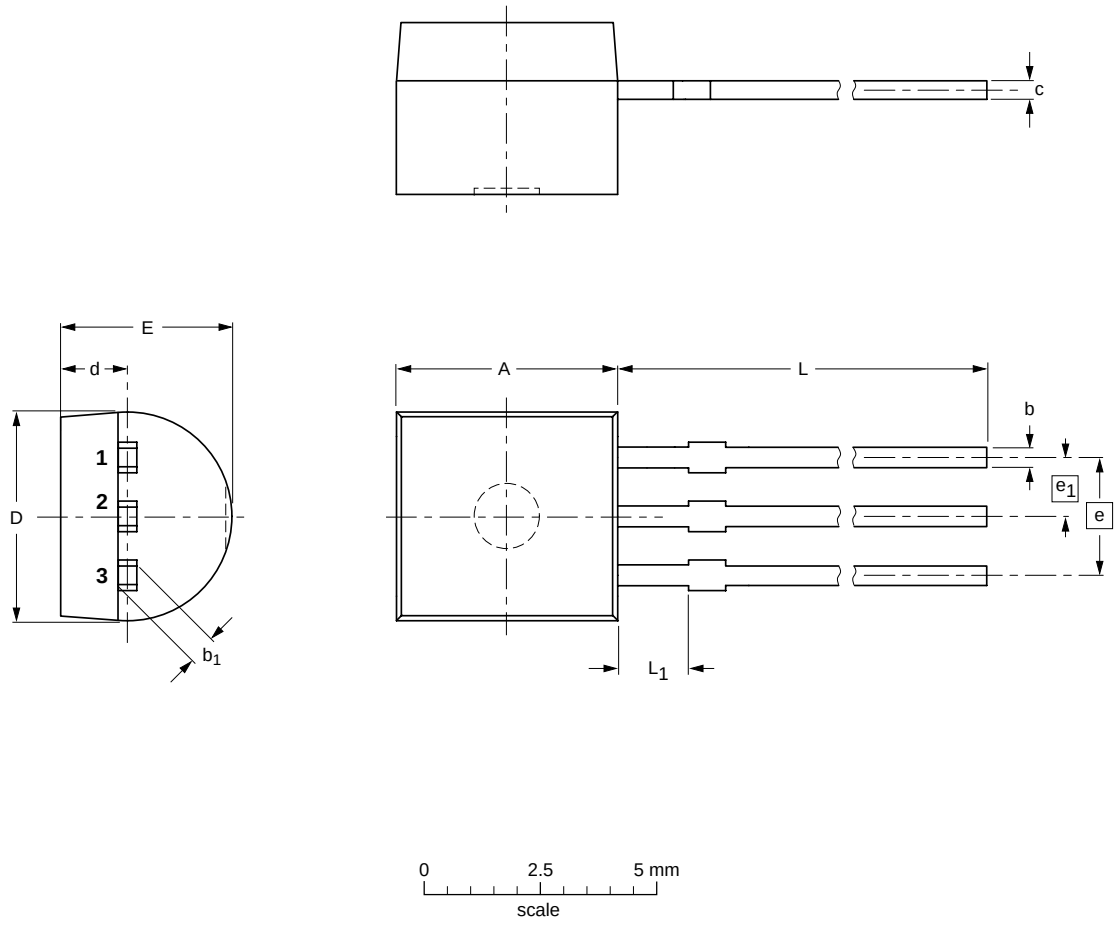
$$a = \frac{V_{GT}}{V_{GT(25^{\circ}C)}}$$

Fig 11. Normalized gate trigger voltage as a function of junction temperature; typical values.

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7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54B**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1 max	c	D	d	E	e	e_1	L	L_1 (1)
mm	4.8 4.4	0.45 0.36	0.48	0.43 0.33	4.7 4.5	1.7 1.4	3.7 3.4	2.54	1.27	15.2 12.7	1.55 1.45

Note

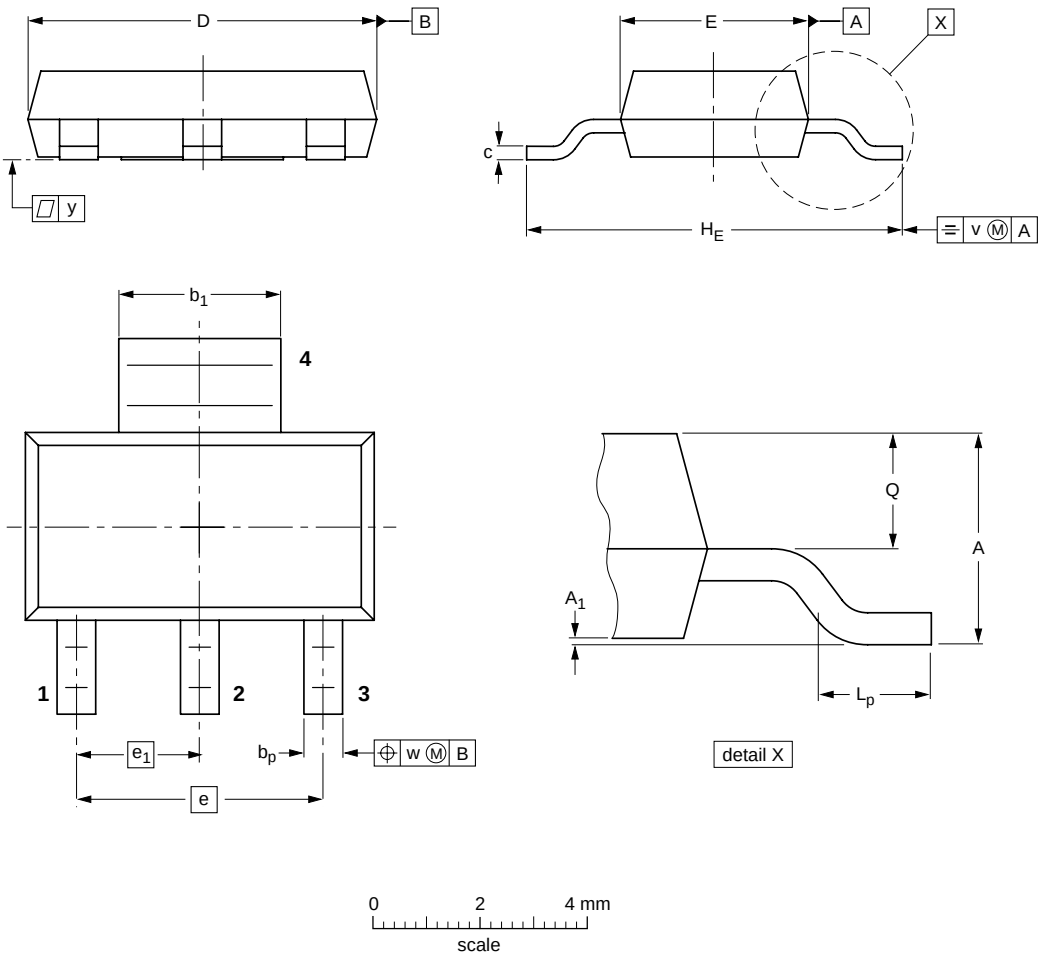
1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54B		TO-92				02-01-29

Fig 12. SOT54B (TO-92).

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Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223			SC-73			~~97-02-28~~ 99-09-13

Fig 13. SOT223.

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8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20020912		**Product data; supersedes data of 11 April 2002**
			Table 5 “Characteristics” Addition of dV_{com}/dt data. Correction to dV_D/dt data
01	20020411	-	**Product data; initial version (9397 750 09419)**

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9. Data sheet status

Data sheet status[1]	Product status[2]	Definition
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Contents

1	**Product profile**	**1**
1.1	Description	1
1.2	Features	1
1.3	Applications	1
2	**Pinning information**	**1**
3	**Ordering information**	**2**
3.1	Ordering options	2
4	**Limiting values**	**2**
5	**Thermal characteristics**	**4**
5.1	Transient thermal impedance	4
6	**Characteristics**	**5**
7	**Package outline**	**8**
8	**Revision history**	**10**
9	**Data sheet status**	**11**
10	**Definitions**	**11**
11	**Disclaimers**	**11**

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