YMZ263B

Multimedia Audio & Game Interface Controller (MMA)

■ OVERVIEW

The YMZ263B (MMA) was developed to meet the multimedia needs of personal computers. We have successfully packaged in a single chip features like PCM/ADPCM record and playback, MIDI communications, and a general purpose game port. It is now possible to create a compact, personal computer based sound system by combining the YMZ263B (MMA) with the YM3812 (OPL2) and the YMF262 (OPL3).

■ FEATURES

(1) PCM/ADPCM section

- Selectable PCM/ADPCM modes.
- Two built-in recording and playback channels.
- Each channel can select among sampling frequencies:
  In ADPCM mode, 22.05 kHz, 11.025 kHz, 7.35 kHz, and 5.5125 kHz.
  In PCM mode, 44.1 kHz, 22.05 kHz, 11.025 kHz and 7.35 kHz.
- PCM has 8-bit or 12-bit resolution, ADPCM compresses 12-bit data into 4 bits.
- Built-in 12-bit floating A/D and D/A converters for record and playback.
- 2-channel and double over-sampling A/D conversion.
- 4-channel and double over-sampling D/A conversion.
- For voice data I/O with the CPU, channel 1 and channel 2 both provide built-in 128-byte FIFO buffers. Selectable CPU (polling/interrupt) mode and DMA mode.

(2) MIDI section

- UART for sending and receiving data that meets MIDI standards.
- Separate built-in 16-byte FIFO buffers for sending and for receiving.

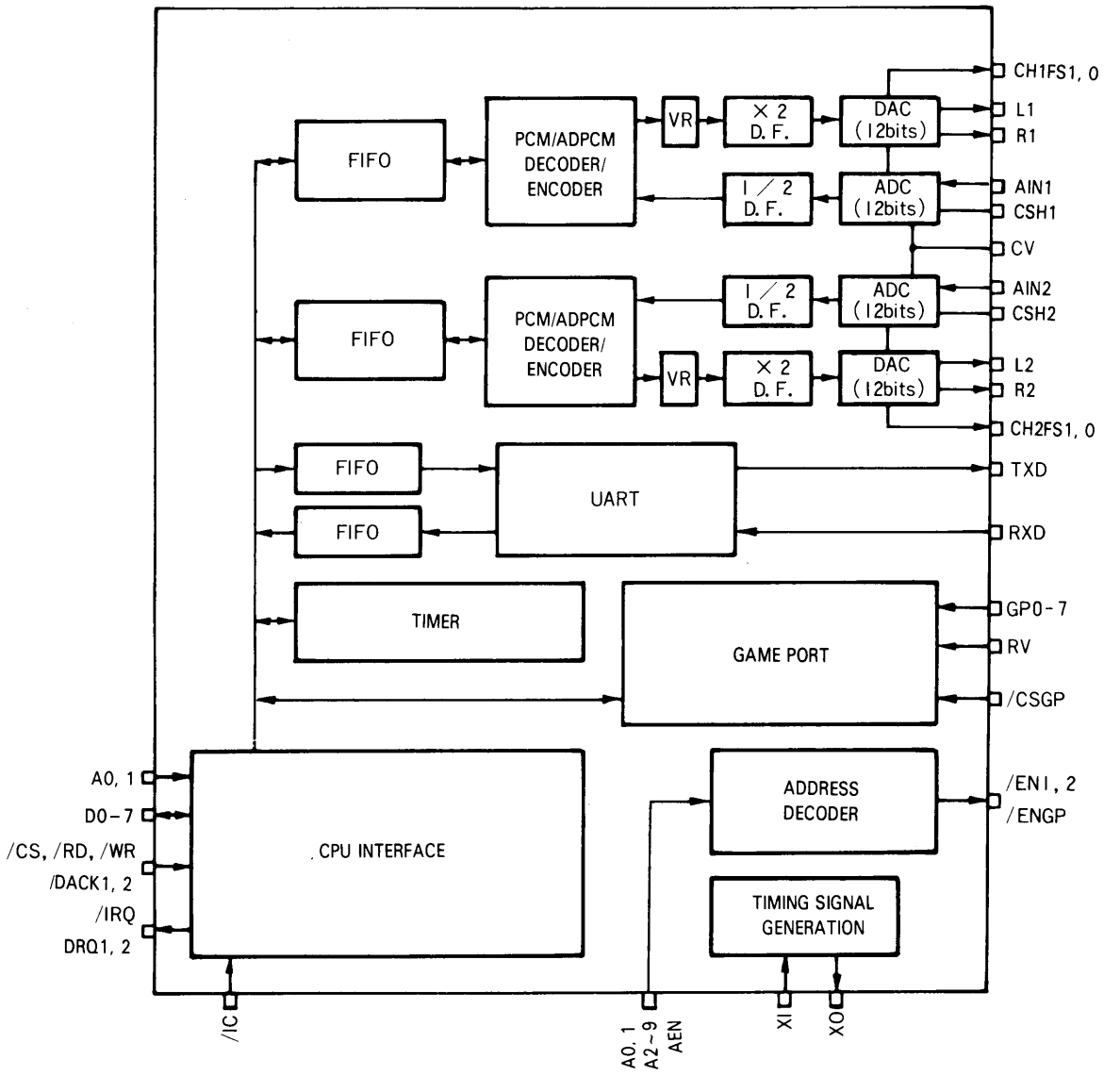
(3) Game Port section

- Eight input ports for interfacing joysticks, etc.

(4) Miscellaneous

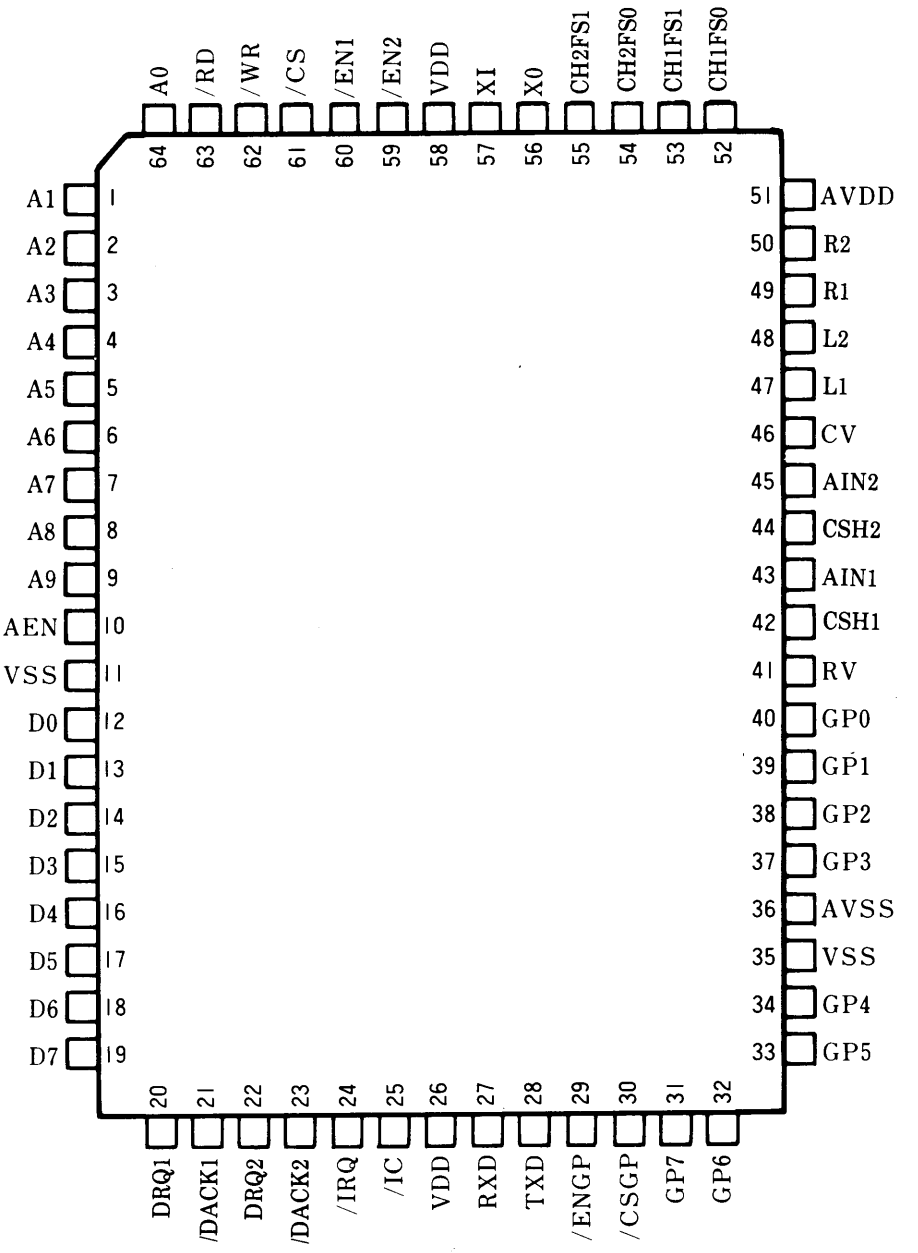
- Three built-in timers.
- Built-in address decoder.
- 5V battery, silicon gate CMOS process.
- 64 pin QFP package.

■ BLOCK DIAGRAM



■ PIN OUT DIAGRAM

- YMZ263B-F



<64QFP Top View>

■ PIN CONFIGURATION

No.	Name	I/O	Function	
1	A1	I	CPU interface	Address bus
2	A2	I		Address bus
3	A3	I		Address bus
4	A4	I		Address bus
5	A5	I		Address bus
6	A6	I		Address bus
7	A7	I		Address bus
8	A8	I		Address bus
9	A9	I		Address bus
10	AEN	I		Address enable
11	VSS	—	Ground (digital)	
12	D0	I/O	CPU interface	Data bus
13	D1	I/O		Data bus
14	D2	I/O		Data bus
15	D3	I/O		Data bus
16	D4	I/O		Data bus
17	D5	I/O		Data bus
18	D6	I/O		Data bus
19	D7	I/O		Data bus
20	DRQ1	O		DMA request signal 1
21	/DACK1	I		DMA acknowledge signal 1
22	DRQ2	O		DMA request signal 2
23	/DACK2	I		DMA acknowledge signal 2
24	/IRQ	OD		Interrupt signal
25	/IC	I+	Initial clear input	
26	VDD	—	+5V power supply (digital)	
27	RXD	I	MIDI UART	Data input
28	TXD	O	MIDI UART	Data output
29	/ENGP	O	Address decoder output for game port (201H)	
30	/CSGP	I+	Game port	Chip select
31	GP7	I+		Input port
32	GP6	I+		Input port
33	GP5	I+		Input port
34	GP4	I+		Input port
35	VSS	—	Ground (digital)	
36	AVSS	—A	Ground (analog)	
37	GP3	IA*	Game port	Input port
38	GP2	IA*		Input port
39	GP1	IA*		Input port
40	GP0	IA*		Input port
41	RV	IA	Voltage input pin for game port	
42	CSH1	—A	PCM/ADPCM channel 1	ADC sample hold capacitor connection pin
43	AIN1	IA		ADC input pin
44	CSH2	—A	PCM/ADPCM channel 2	ADC sample hold capacitor connection pin
45	AIN2	IA		ADC input pin
46	CV	—A	ADC center voltage pin	
47	L1	OA	PCM/ADPCM Channel 1 (left)	DAC output pin
48	L2	OA	PCM/ADPCM Channel 2 (left)	DAC output pin
49	R1	OA	PCM/ADPCM Channel 1 (right)	DAC output pin
50	R2	OA	PCM/ADPCM Channel 2 (right)	DAC output pin

No.	Name	I/O	Function
51	AVDD	−A	+5V power supply (analog)
52	CH1FS0	O	PCM/ADPCM Channel 1 Sampling frequency information output 0
53	CH1FS1	O	Sampling frequency information output 1
54	CH2FS0	O	PCM/ADPCM Channel 2 Sampling frequency information output 0
55	CH2FS1	O	Sampling frequency information output 1
56	XO	O	Quartz oscillator connection pin
57	XI	I	Quartz oscillator connection pin or master clock input (16.9344 MHz)
58	VDD	—	+5V power supply (digital)
59	/EN2	O	Address decoder output 2 (388H ~ 38BH)
60	/EN1	O	1 (38CH ~ 38FH)
61	/CS	I+	CPU interface Chip select
62	/WR	I	Write enable
63	/RD	I	Read enable
64	A0	I	Address bus

Notes: I/O notation:

A:	Analog pin
OD:	Open drain output pin
I+:	Input pin with built-in pull-up resistor
IA*	short-circuited to AVSS.

■ FUNCTIONS

1. Clock XI, XO

Pins XI and XO make up the quartz oscillator circuit. The oscillation frequency is 16.9344 MHz. An external clock may be connected to the XI input pin.

2. CPU Interface A0, A1, D0 ~ 7, /CS, /RD, /WR, /IRQ

An 8 bit parallel interface is used to control the components of this LSI. Data bus controls, such as register data Read/Write and Status Read, are performed using the /CS, /RD, /WR, A0, and A1 signals. The combination of these signals determines the mode:

/CS	/RD	/WR	A0	A1	CPU access mode
H	×	×	×	×	Inactive mode
L	H	L	L	×	Address Write mode
L	H	L	H	L/H	Data Write mode
L	L	H	L	L	Status Read mode
L	L	H	H	L/H	Data Read mode

Note: × means "Don't care"

(a) Inactive mode

When /CS is "H", the data bus D0 ~ D7 is in a high impedance state.

(b) Address Write mode

Use this mode to specify the address for read/write operations. Address data should be loaded on the data bus.

(c) Data Write mode

Use this mode to write data to the address specified in Address Write mode. The data on the data bus will be written to the specified register.

(d) Status Read mode

Use this mode to read the status. The status information will be output on the data bus.

(e) Data Read mode

Use this mode to read data from the address specified in Address Write mode. The data from the register will be output on the data bus.

When an interrupt signal is generated by any section of this LSI, the /IRQ pin is set to "L" and the CPU is notified.

Note) YMZ263B requires the following wait time before next operation of data/address writing or before that of data/address reading.

WAIT TIME .... Over 8 cycles (Master clock)

3. FIFO Buffer DRQ1, DRQ2, /DACK1, /DACK2

Data input/output between the PCM/ADPCM section and the CPU is carried out through 128 byte FIFO buffers for each channel. This can be connected with the DMA controller for DMA transfer in the DMA mode.

4. PCM/ADPCM CH1FS0, CH1FS1, CH2FS0, CH2FS1, L1, R1, L2, R2, AIN1, CSH1, AIN2, CSH2, CV

PCM/ADPCM decoder output is performed in several steps. First, the digital volume controls in both channel 1 and channel 2 adjust the output level. Double over-sampling processing is performed on this output. D/A conversion is performed at twice the specified sampling frequency. Finally, the voltage output is sent to the L1, R1, L2 and R2 pins. (Over-sampling processing is not performed in the 44.1 kHz PCM mode.)

The analog signals input from AIN1 and AIN2 are processed as follows: The signal is A/D converted at twice the specified sampling frequency. One half under-sampling processing is performed on this signal. Finally, the input is fed into the PCM/ADPCM encoder. For A/D conversion, a sample hold capacitor is attached externally to the CSH1 and CSH2 pins. The CV pin is a center voltage pin for the A/D converter. (Under-sampling processing is not performed in the 44.1 kHz PCM mode.)

PCM/ADPCM sampling frequency information for each channel 1 and channel 2 is output for external LPF switching through CH1FS0, CH1FS1, CH2FS0, and CH2FS1.

PCM	ADPCM	CH1FS1, CH2FS1	CH1FS0, CH2FS0
44.1 kHz	—	L	L
22.05 kHz	22.05 kHz	L	H
11.025 kHz	11.025 kHz	H	L
7.35 kHz	7.35 or 5.5125 kHz	H	H

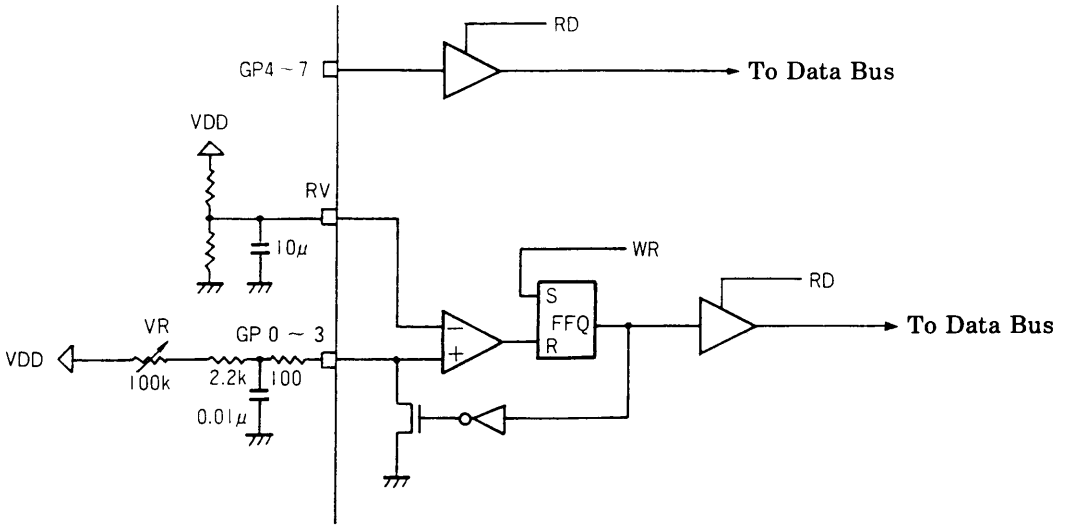
5. MIDI TXD, RXD

Output data is buffered in a 16-byte FIFO buffer, and then synchronized output is transmitted by the UART through the TXD pin. Synchronized input from the RXD pin is received by the UART and buffered in a 16-byte FIFO buffer.

6. Game Port /CSGP, GP0~7, RV

Pins GP4~7 are used for a general purpose input port. When/GSGP='L' and /RD='L', the data from pins GP4~7 is output on D4~7 of the data bus. Pins GP0~3 can be read from the data bus, and are compared with the RV voltage internally so that these pins can be used for a joystick connection. If the pin voltage is lower than the RV voltage, "1" is assigned. Apply the voltage to be compared on the RV pin. (The voltage to be compared: 0.63*VDD~0.70*VDD)

Note that pins GP0~3 are connected internally to the AVSS pin. When /CSGP="L" and /WR="L", Pins GP0~3 are cut off from the AVSS pin, and comparison with the RV voltage is started. Thus, by adding a constant, "1" period width of the data to be read varies with respect to the resistance value.



〈Example of Pins GP0 ~ 7 Input Equivalent Circuit and External Circuit〉

7. **Address Decoder** **AEN, A0 ~ 9, /EN1, /EN2, /ENGP**

In order to minimize external connections, an address decoder with fixed parameters is built in. /EN1, /EN2, and /ENGP are decorder output for YMZ263B (except GAME PORT), sound generator the YMF262 and the like, and GAME PORT.
/EN1, /EN2, and /ENGP will become "L" when decoder output address is valid.

AEN is the chip select for the address decoder. If AEN="H", then/EN1, /EN2, and /ENGP will not become "L" regardless of the values of A0 ~ 9.

8. **Initial Clear** **/IC**

Initial clear must be performed at LSI power-up.

■ REGISTERS

1. Register Map

CH	CHANNEL 1 (A1='L')										CHANNEL 2 (A1='H')									
ADDR	R/W	D7	D6	D5	D4	D3	D2	D1	D0		R/W	D7	D6	D5	D4	D3	D2	D1	D0	
$00	R/W								SELT		—									
$01	—	LSI TEST									—									
$02	W	TIMER 0 (L)									—									
$03	W	TIMER 0 (H)									—									
$04	W	BASE COUNTER (L)									—									
$05	W	TIMER 1					BASE COUNTER(H)				—									
$06	R/W	TIMER 2 (L)									—									
$07	R/W	TIMER 2 (H)									—									
$08	W	*1	T2 MSK	T1 MSK	T0 MSK	ST BC	ST2	ST1	ST0		—									
$09	W	ADP RST	R	L	FS1	FS0	PCM	PLY / REC	ADP ST		W	ADP RST	R	L	FS1	FS0	PCM	PLY / REC	ADP ST	
$0A	W	VOLUME CONTROL									W	VOLUME CONTROL								
$0B	R/W	PCM DATA									R/W	PCM DATA								
$0C	W	DMA MOD	FMT 1	FMT 0	SEL F2	SEL F1	SEL F0	MSK FIF	DMA ENB		W		FMT 1	FMT 0	SEL F2	SEL F1	SEL F0	MSK FIF	DMA ENB	
$0D	W			MSK POV	MSK MOV	MDI TRS RST	MSK TRQ	MDI RCV RST	MSK RRQ		—									
$0E	R/W	MIDI DATA									—									

Note: Sections with diagonal lines are "Don't care",
All of the register values are set to "0" except for SELT, ADPRST, MDI TRSRST, MDI RCVRST by initial clear.

*1: Be sure to set to '0'.

2. Description of Registers

Use pin A1 to select channel 1 or channel 2 of the PCM/ADPCM. Use Data Read mode to read the R/W registers that can be read.

Address	Name	Function
$00	SELT	Selects 2's complement or offset binary.
$01	LSI TEST	This register is used for testing the LSI.
$02 ~ 03	TIMER0	TIMER0 is a 16-bit programmable down counter.
$04 ~ 05	BASE COUNTER	BASE COUNTER is a 12-bit programmable counter that supplies clock functions for TIMER1 and TIMER2.
$05	TIMER1	TIMER1 is a 4-bit programmable down counter that is controlled by the base counter clock.
$06 ~ 07	TIMER2	TIMER2 is a 16-bit programmable down counter that is controlled by the base counter clock.
$08	T0MSK,T1MSK,T2MSK	Masks the interrupt signal generated by the corresponding timer.
$08	ST0,ST1,ST2,STBC	Control the start and stop of TIMER0, TIMER1, TIMER2 and BASE COUNTER.
$09	ADPRST	Resets PCM/ADPCM.
$09	L,R	Enables output from the corresponding channel.
$09	FS0,FS1	Selects PCM/ADPCM sampling frequency.
$09	PCM	Selects PCM mode or ADPCM mode.
$09	PLY/REC	Selects recording or playback.
$09	ADPST	Controls the start and stop of recording and playback.
$0A	VOLUME CONTROL	Sets the output attenuation value.
$0B	PCM DATA	This register is used for writing data into the FIFO buffer and reading data from the FIFO buffer.
$0C	DMAMOD	Sets the mode for transfer of data between channel1 and channel2 using one channel of the controller.
$0C	FMT0,FMT1	Specifies the PCM data format.
$0C	SELF0,SELF1,SELF2	Specifies the 128-byte FIF0 data valume point for interrupt signal generation.
$0C	MSKFIF	Masks the interrupt signal generated by FIFO.
$0C	DMAENB	Selects DMA mode or CPU mode.
$0D	MSKPOV	Masks interrupt signals due to overrun errors during PCM/ADPCM recording.
$0D	MSKMOV	Masks interrupt signals due to overrun error during MIDI receiving.
$0D	MDITRSRST	Reset the MIDI transmit circuit.
$0D	MSKTRQ	Masks interrupt signals for the MIDI transmit FIFO.
$0D	MDIRCVRST	Resets the MIDI receive circuit.
$0D	MSKRRQ	Masks interrupt signals for the MIDI receive FIFO.
$0E	MIDI DATA	This register is used for writing data into the MIDI FIFO buffer and reading data from the MIDI FIFO buffer.

3. Status Bits

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Status	OV	T2	T1	T0	TRQ	RRQ	FIF 2	FIF 1

4. Description of Status

When any block generates an interrupt signal, the bit of the corresponding status register becomes "1", and at the same time /IRQ becomes "L" and the CPU is notified.

Name	Function
0V	Becomes "1" when a MIDI receive overrun error or a PCM/ADPCM record overrun error occurs.
T0,T1,T2	Becomes "1" when the specified time elapses in the corresponding timer.
TRQ	Becomes "1" when the MIDI transmit FIFO buffer is empty.
RRQ	Becomes "1" when the MIDI receive FIFO buffer has data in it.
FIF1,FIF2	Becomes "1" after the PCM/ADPCM FIFO passes the point that was specified in SELF2, F1, F0.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	−0.3 ~ V_{DD}+0.5	V
Operating temperature	T_{op}	0 ~ 70	°C
Storage temperature	T_{stg}	−50 ~ 125	°C

2. Recommended Operating Conditions

Item	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{op}	0	25	70	°C

3. DC Characteristics (Conditions; Ta=0 ~ 70°C, V_{DD}=5.0 ± 0.25 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power consumption	P_D	V_{DD}=5.0V f_M=16.9344MHz			200	mW
Input highlevel voltage 1	V_{IH1}	*1	2.2			V
Input lowlevel voltage 1	V_{IL1}	*1			0.8	V
Input highlevel voltage 2	V_{IH2}	*2	3.5			V
Input lowlevel voltage 2	V_{IL2}	*2			1.0	V
Input leakage current	I_{LI}	V_I=0 ~ 5V, *3	−10		10	μA
Input capacity	C_I				10	pF
Output highlevel voltage	V_{OH}	I_{OH}=−80μA	V_{DD} −1.0			V
Output lowlevel voltage	V_{OL}	I_{OL}=2.0mA			V_{SS}+0.4	V
Output capacity	C_O				10	pF
Output leakage current	I_{LO}	V_I=0 ~ 5V, *4	−10		10	μA
Pull up registance	R_U		80		400	kΩ

Note) *1: Applied to /WR, /RD, /CS, A0 ~ A9, AEN, D0 ~ D7, RXD, /CSGD, GP4 ~ GP7, /DACK1, /DACK2 (when used as input pins)

*2: Applied to XI, /IC

*3: Applied to /WR, /RD, A0 ~ A7, AEN, D0 ~ D7, RXD, /CSGP, GP4 ~ GP7 (When used as input pins)

*4: When D0 ~ D7 are in high impedance

4. AC Characteristics (Conditions; Ta=0~70°C, VDD=5.0±0.25 V)

Item	Symbol	Figure	Min.	Typ.	Max.	Unit
Master clock frequency	fM	Fig A-1		16.9344		MHz
Master clock duty	D		45	50	55	%
Reset pulse width	NICW	Fig A-2	80			cycle *1
Address setup time	tAS	Fig A-3, 4	10			ns
Address hold time	tAH	Fig A-3, 4	10			ns
Chip select write width	tCSW	Fig A-3	50			ns
Chip select read width	tCSR	Fig A-4	100			ns
Write pulse width	tWW	Fig A-3	50			ns
Write data setup time	tWDS	Fig A-3	10			ns
Write data hold time	tWDH	Fig A-3	20			ns
Read pulse width	tRW	Fig A-4	100			ns
Read data access time	tACC	Fig A-4			100	ns
Read data hold time	tRDH	Fig A-4	10			ns
DRQ hold time	tDRQH	Fig A-5			50	ns
DMA read setup time	tDRS	Fig A-5	50			ns
DMA read hold time	tDRH	Fig A-5	20			ns
DMA read data access time	tDRAC	Fig A-5			100	ns
DMA read data hold time	tDRDH	Fig A-5	10			ns
DMA write setup time	tDWS	Fig A-6	50			ns
DMA write hold time	tDWH	Fig A-6	20			ns
DMA write data setup time	tDWDS	Fig A-6	10			ns
DMA write data hold time	tDWDH	Fig A-6	20			ns

Note) *1: Master clock cycle

5. Analog Characteristics (Conditions; Ta=0~70°C, VDD=5.0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	VIA	*1			4.8	V
Output voltage	VOA	*2			4.8	V
DC offset voltage	CV	*3		2.5		V
Offset voltage	VOFF	*2			0.1	V
Linearity error		*2			±30	mV
Step error		*2			±1.0	LSB

Note) *1: Applied to AIN1, AIN2
*2: Applied to L1, R1, L2, R2
*3: Applied to CV

6. Timing Diagram

(1) Clock timing

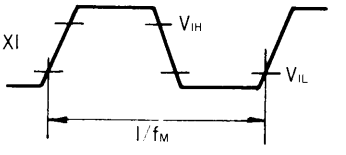


Fig A-1

(2) Reset pulse

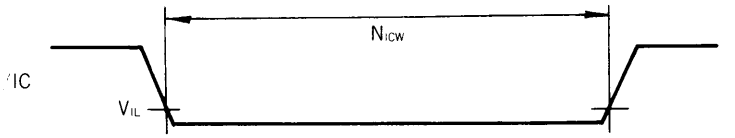


Fig A-2

(3) Address/Data write timing

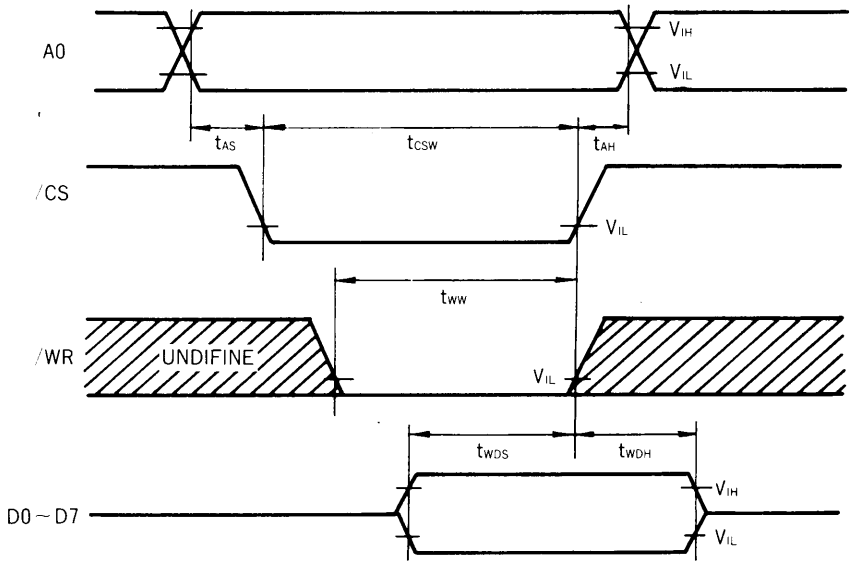


Fig A-3

Note: tCSW, tWW, and tWDH are based on either /CS or /WR being driven to high level.

(4) Status/Data read timing

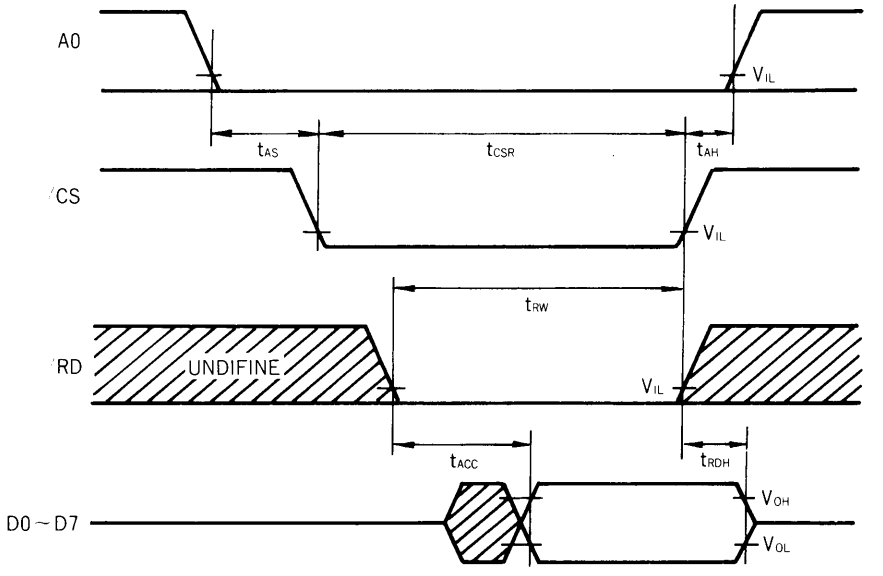


Fig A-4

Note: tACC is based on whichever of /CS or /RD goes to the low level last.

tCSW, tRW, and tWDH are based on either /CS or /WR being driven to high level.

(5) DMA read timing

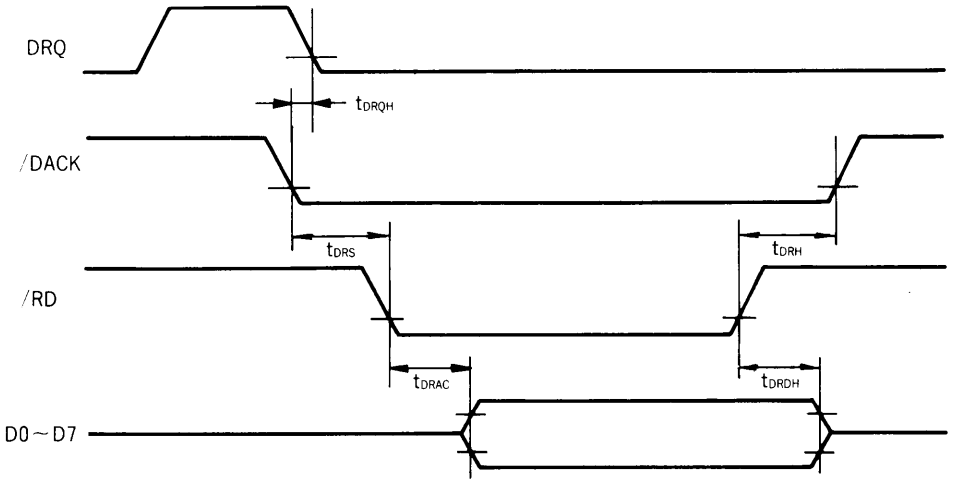


Fig A-5

(6) DMA write timing

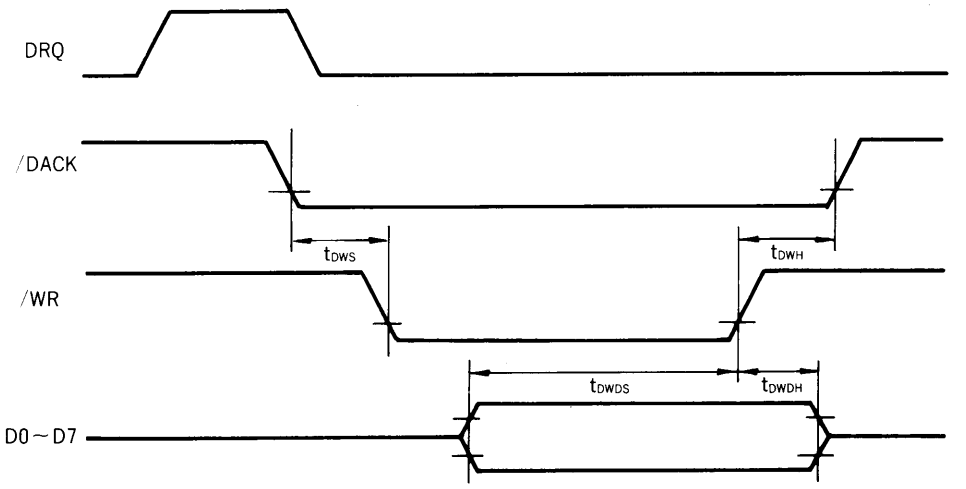
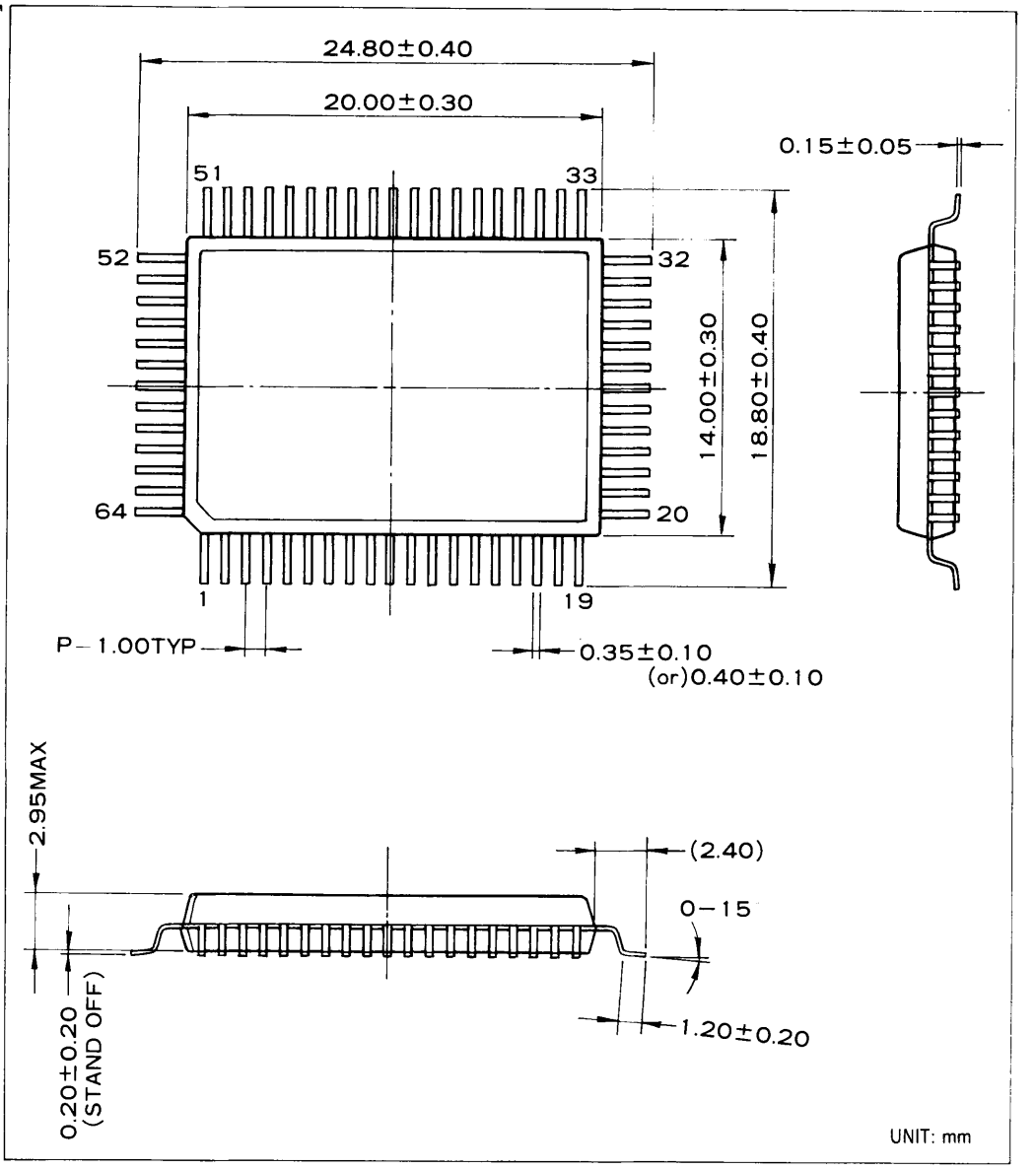


Fig A-6

■ EXTERNAL VIEWS

● YMZ263B-F



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