YAMAHA LSI

YMF754

Preliminary

DS-1E

■ OVERVIEW

YMF754 (DS-1E) is a high performance audio controller for the PCI Bus. DS-1E consists of two separated functional blocks. One is the PCI Audio block and the other is the Legacy Audio block.

PCI Audio block provides 64-voice XG wavetable synthesizer with reverb and variation by using the software driver from YAMAHA. It also supports DirectSound hardware accelerator, Downloadable Sound (DLS) and DirectMusic accelerator.

Legacy Audio block supports FM synthesizer, Sound Blaster Pro, MPU401 UART mode and Joystick function in order to provide hardware compatibility for numerous PC games on real DOS without any software driver.

DS-1E supports the connection to AC'97 which provides high quality DAC, ADC and analog mixer, and it can connect two AC'97s. In addition, it supports consumer IEC958, Digital Audio Interface (SPDIF In/Out), to connect external audio equipment by digital.

In addition to support the same functions of YMF744B (DS-1S), DS-1E adds direct recording function for SPDIF In, and realizes to use SPDIF In and Zoomed Video Port at the same time. And, DS-1E is featured with the capability of dramatically reducing power consumption at normal operation.

■ FEATURES

- PCI 2.2 Compliant
- PC98 / PC99 specification Compliant
- PCI Bus Power Management rev. 1.0 Compliant (Support D0, D2 and D3 state)
- Supports clock run
- PCI Bus Master for PCI Audio
  - True Full Duplex Playback and Capture with different Sampling Rate
  - Maximum 64-voice XG capital Wavetable Synthesizer including GM compatibility
  - DirectSound Hardware Acceleration
  - DirectMusic Hardware Acceleration
  - Downloadable Sound (DLS) level-1
- Legacy Audio compatibility
  - FM Synthesizer
  - Hardware Sound Blaster Pro compatibility
  - MPU401 UART mode MIDI interface
  - Joystick
- Supports PC/PCI and Distributed DMA for legacy DMAC (8237) emulation
- Supports Serialized IRQ
- Supports I^2S serial input for Zoomed Video Port
- Supports Consumer IEC958 Port (SPDIF In/Out)
- Supports direct recording function for SPDIF In
- Capability for using SPDIF In and Zoomed Video Port at the same time.
- Supports AC'97 Interface (AC-Link) Revision 2.1
- AC'97 Digital Docking
- Supports 4-Channel Speaker
- Hardware Volume Control
- EEPROM Interface
- Single Crystal operation (24.576MHz)
- Power supply: 3.3V for I/O (5V tolerant), 2.5V for Internal core logic
- 128-pin LQFP YMF754-V : 0.5mm pin pitch
  YMF754-R : 0.4mm pin pitch

GENERAL MIDI SONDIUS-XG™
XG Sensaura™

The contents of this catalog are target specifications and are subject to change without prior notice. When using this device, please recheck the specifications.

YAMAHA CORPORATION

YMF754 CATALOG
CATALOG No.:LSI-4MF754A00
June 28, 1999

■ LOGOS

GENERAL MIDI logo is a trademark of Association of Musical Electronics Industry (AMEI), and indicates GM system level 1 Compliant.

XG logo is a trademark of YAMAHA Corporation.

SONDIUS-XG logo is a trademark that Stanford University in the United States and YAMAHA Corporation hold jointly.

Sensaura logo is a trademark of Central Research Laboratories Limited.

1. GM system level 1

GM system level 1 is a world standard format about MIDI synthesizer which provides voice arrangements and MIDI functions.

2. XG

XG is a format about MIDI synthesizer that is proposed by YAMAHA, and keeps the upper compatibility of GM system level 1. The good points are the voice arrangements kept extensively, a large number of the voices, modification of the voices, 3 kinds of effects, and so on.

3. SONDIUS-XG

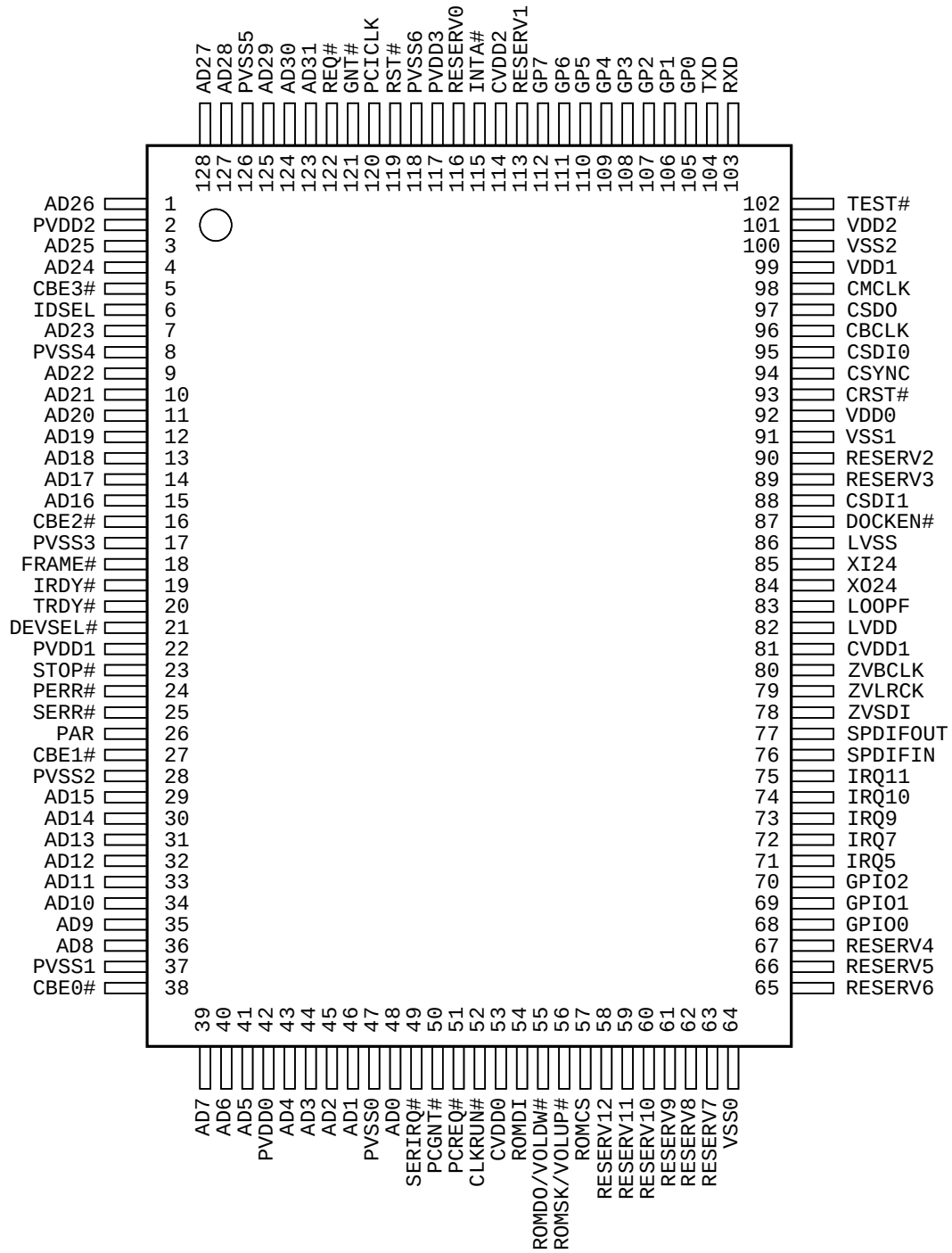
Products bearing the SONDIUS-XG logo are licensed under patents of Stanford University and YAMAHA Corporation as listed on <http://www.sondius-xg.com>. The SONDIUS-XG produces acoustic sound outputs by running a virtual simulation of the actual acoustic instrument operation. Therefore, it provides much more real-world acoustic sound outputs fundamentally different from the Wavetable sound generator that simply processes the recorded acoustic sound sources only. The SONDIUS-XG adds the technology of virtual acoustic sound to the XG format.

4. Sensaura

Sensaura is a technology which provides 3D positional audio and moving effect by HRTF (Head Related Transfer Function) with 2 speakers or headphone. This feature makes it possible to enjoy invariable and unchangeable sound feelings in all-positional area covering as wide as 360 degrees.

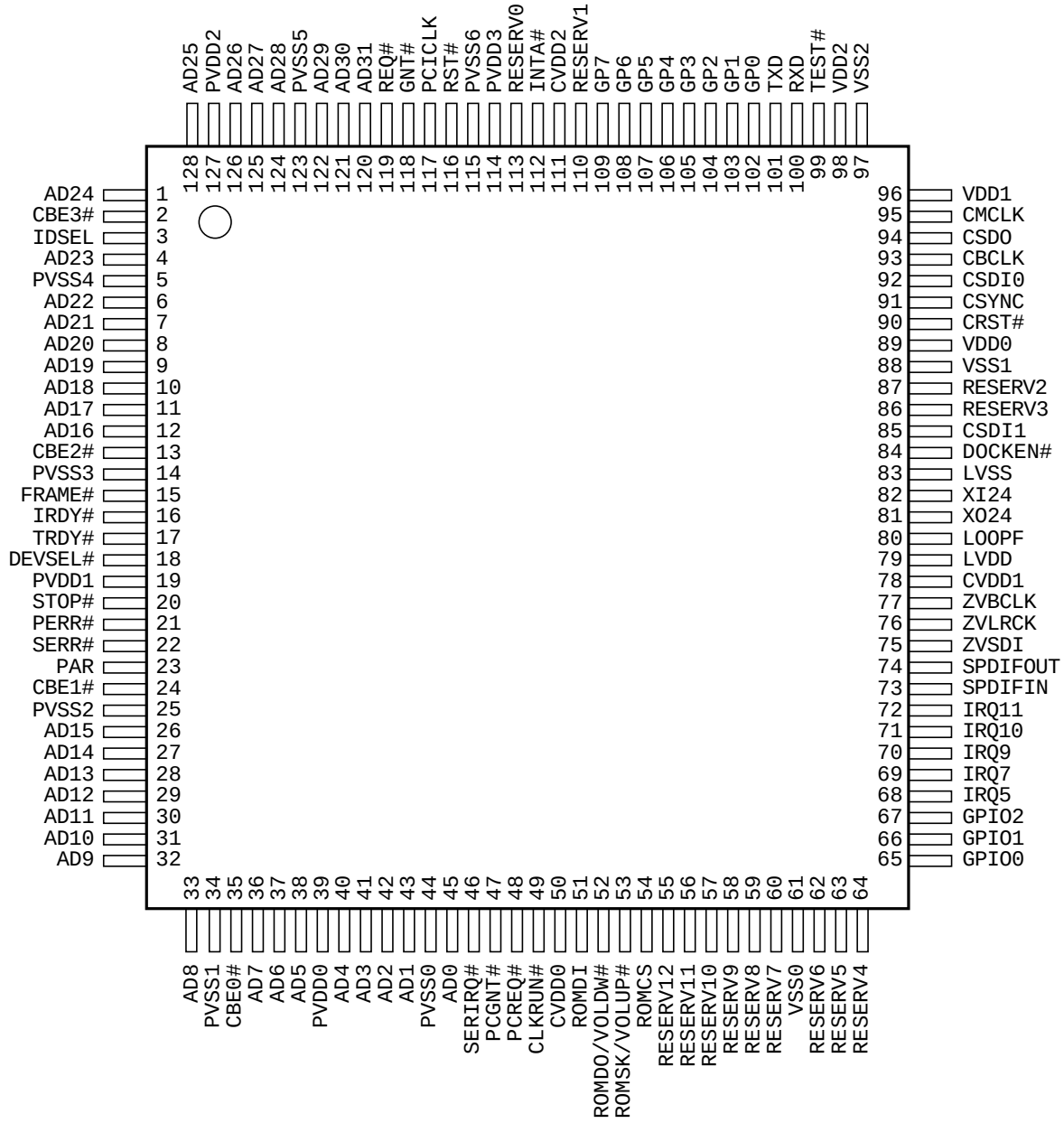
■ PIN CONFIGURATION

YMF754-V (0.5mm pin pitch)



128 Pin LQFP Top View

YMF754-R (0.4mm pin pitch)



128 Pin LQFP Top View

■ PIN DESCRIPTION

1. PCI Bus Interface (54-pin)

Name	I/O	Type	Size	Function
PCICLK	I	P	-	PCI Clock
RST#	I	P	-	Reset
AD[31:0]	IO	Ptr	-	Address / Data
C/BE[3:0]#	IO	Ptr	-	Command / Byte Enable
PAR	IO	Ptr	-	Parity
FRAME#	IO	Pstr	-	Frame
IRDY#	IO	Pstr	-	Initiator Ready
TRDY#	IO	Pstr	-	Target Ready
STOP#	IO	Pstr	-	Stop
IDSEL	I	P	-	ID Select
DEVSEL#	IO	Pstr	-	Device Select
REQ#	O	P	-	PCI Bus Master Request
GNT#	I	P	-	PCI Bus Master Grant
PCREQ#	O	Ptr	-	PC/PCI Request
PCGNT#	I	Ptr	-	PC/PCI Grant
PERR#	IO	Pstr	-	Parity Error
SERR#	O	Pod	-	System Error
INTA#	O	Pod	-	Interrupt signal output for PCI Bus
SERIRQ#	IO	Ptr	-	Serialized IRQ
CLKRUN#	IO	Ptr	-	Clock Run

2. AC'97 Interface (8-pin)

Name	I/O	Type	Size	Function
CRST#	O	T	6mA	Reset signal for AC'97
CMCLK	O	C	-	Master Clock for AC'97 (24.576MHz)
CBCLK	I	T	-	AC-link: Bit Clock for AC'97 audio data
CSDO	O	T	6mA	AC-link: AC'97 Serial audio output data
CSYNC	O	T	6mA	AC-link: AC'97 Synchronized signal
CSDI0	I	T	-	AC-link: AC'97 Serial audio input data (Primary)
CSDI1	I	Tup	-	AC-link: AC'97 Serial audio input data (Secondary)
DOCKEN#	I	Tup	-	Secondary AC'97 Enable

3. External Audio Interface (5-pin)

Name	I/O	Type	Size	Function
SPDIFOUT	O	T	2mA	Digital Audio Interface output
SPDIFIN	I	Tup	-	Digital Audio Interface input
ZVBCLK	I	Tup	-	Zoomed Video Port Bit Clock
ZVLRCK	I	Tup	-	Zoomed Video Port L/R Clock
ZVSDI	I	Tup	-	Zoomed Video Port Serial Data

4. Legacy Device Interface (15-pin)

Name	I/O	Type	Size	Function
IRQ5	O	Ttr	6mA	Interrupt 5 of Legacy Audio It is directly connected to the interrupt signal of System I/O chip.
IRQ7	O	Ttr	6mA	Interrupt 7 of Legacy Audio
IRQ9	O	Ttr	6mA	Interrupt 9 of Legacy Audio
IRQ10	O	Ttr	6mA	Interrupt 10 of Legacy Audio
IRQ11	O	Ttr	6mA	Interrupt 11 of Legacy Audio.
GP[3:0]	I	A	-	Joystick Port
GP[7:4]	I	Tup	-	Joystick Port
RXD	I	Tup	-	MIDI Data Receive
TXD	O	T	2mA	MIDI Data Transfer

5. Miscellaneous (11-pin)

Name	I/O	Type	Size	Function
ROMCS	O	T	2mA	Chip select for external EEPROM
ROMSK / VOLUP#	IO	Tup	2mA	Serial clock for external EEPROM or Hardware Volume (Up)
ROMDO / VOLDW#	IO	Tup	2mA	Serial data output for external EEPROM or Hardware Volume (Down)
ROMDI	I	Tup	-	Serial data input for external EEPROM
XI24	I	C	-	24.576 MHz Crystal
XO24	O	C	-	24.576 MHz Crystal
LOOPF	I	A	-	Capacitor for PLL
GPIO[2:0]	IO	Tup	6mA	General purpose Input / Output GPIO2 can use for a reset pin of Secondary AC'97.
TEST#	I	Tup	-	LSI Test pin (Do not connect externally.)

6. Power Supply (22-pin)

Name	I/O	Type	Size	Function
PVDD[3:0]	-	-	-	3.3V Power supply for PCI Bus Interface
PVSS[6:0]	-	-	-	Ground for PCI Bus Interface
CVDD[2:0]	-	-	-	2.5V Power supply for Core logic
VDD[2:0]	-	-	-	3.3V Power supply
VSS[2:0]	-	-	-	Ground
LVDD	-	-	-	2.5V Power supply for PLL Filter
LVSS	-	-	-	Ground for PLL Filter

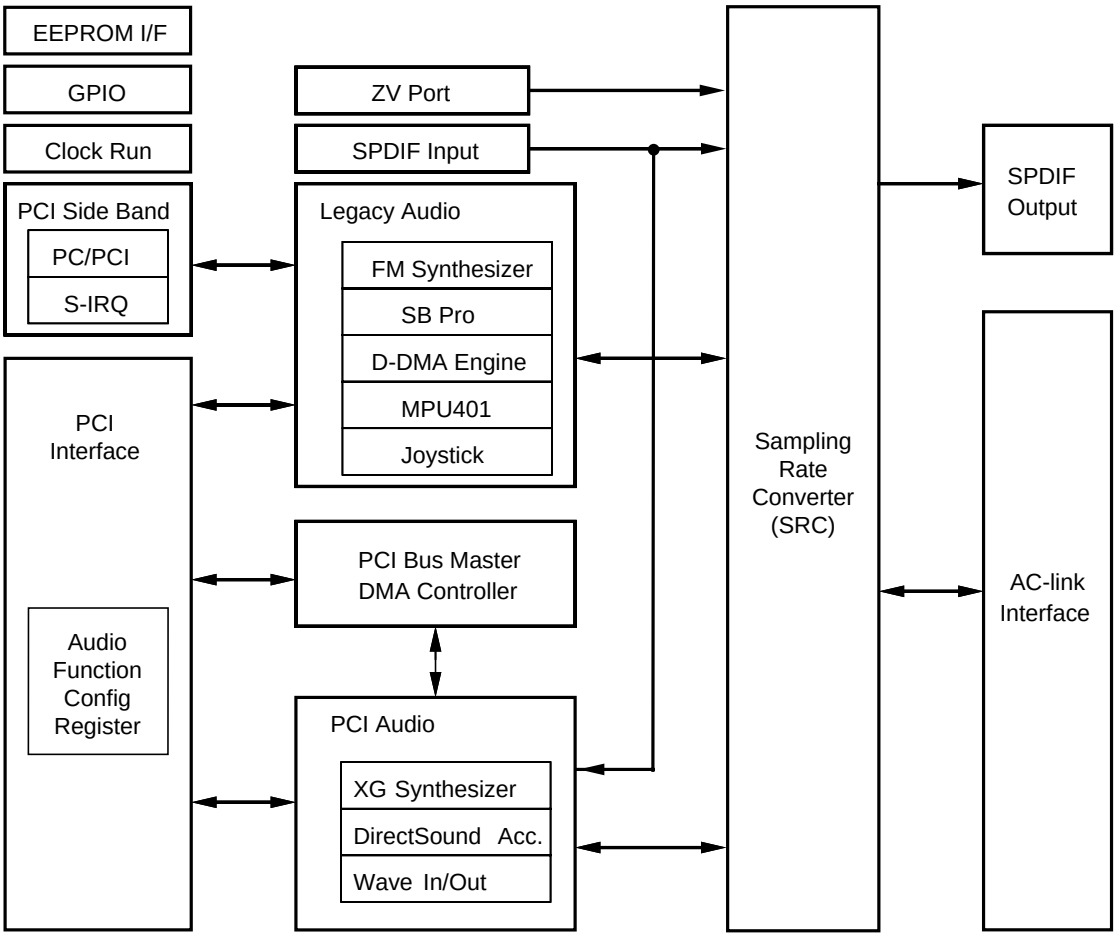
7. Reserve Pin (13-pin)

Name	I/O	Type	Size	Function
RESERV[12:0]	-	-	-	Reserve pins (Do not connect externally.)

TYPE

T : TTL	A : Analog	Ptr : Tri-State PCI
Ttr : Tri-State TTL	C : CMOS	Pstr : Sustained Tri-Sate PCI
Tup : Pull up (Max. 300kohm) TTL	P : PCI	Pod : Open Drain PCI

■ BLOCK DIAGRAM



■ FUNCTION OVERVIEW

1. PCI INTERFACE

DS-1E supports the PCI bus interface and complies to PCI revision 2.2.

1-1. PCI Bus Command

DS-1E supports the following PCI Bus commands.

1-1-1. Target Device Mode

C/BE[3:0]#				Command
0	0	0	0	Interrupt Acknowledge (not support)
0	0	0	1	Special Cycle (not support)
0	0	1	0	I/O Read
0	0	1	1	I/O Write
0	1	0	0	reserved
0	1	0	1	reserved
0	1	1	0	Memory Read
0	1	1	1	Memory Write
1	0	0	0	reserved
1	0	0	1	reserved
1	0	1	0	Configuration Read
1	0	1	1	Configuration Write
1	1	0	0	Memory Read Multiple (alias to memory read)
1	1	0	1	Dual Address Cycle (not support)
1	1	1	0	Memory Read Line (alias to memory read)
1	1	1	1	Memory Write and Invalidate (alias to memory write)

DS-1E does not assert DEVSEL# when accessed with commands that are indicated as (not supported) or reserved.

1-1-2. Master Device Mode

C/BE[3:0]#				Command
0	1	1	0	Memory Read
0	1	1	1	Memory Write

When DS-1E becomes a Master Device, it generates only memory write and read cycle commands.

1-2. PCI Configuration Register

In addition to the Configuration Register defined by PCI Revision 2.2, DS-1E provides proprietary PCI Configuration Registers in order to control legacy audio function, such as FM Synthesizer, Sound Blaster Pro, MPU401 and Joystick. These additional registers are configured by BIOS or the configuration software from YAMAHA Corporation.

The following shows the overview of the PCI Configuration Register.

Offset	b[31..24]	b[23..16]	b[15..8]	b[7..0]
00-03h	Device ID		Vendor ID	
04-07h	Status		Command	
08-0Bh	Base Class Code	Sub Class Code	Programming IF	Revision ID
0C-0Fh	Reserved	Header Type	Latency Timer	Reserved
10-13h	PCI Audio Memory Base Address			
14-17h	Legacy Audio I/O Base Address (Dummy for SB, FM, MPU, D-DMA)			
18-1Bh	Legacy Audio I/O Base Address (Dummy for Joystick)			
1C-2Bh	Reserved			
2C-2Fh	Subsystem ID		Subsystem Vendor ID	
30-33h	Reserved			
34-37h	Reserved			Cap Pointer
38-3Bh	Reserved			
3C-3Fh	Maximum Latency	Minimum Grant	Interrupt Pin	Interrupt Line
40-43h	Extended Legacy Audio Control		Legacy Audio Control	
44-47h	Subsystem ID Write		Subsystem Vendor ID Write	
48-4Bh	DS-1E Power Control 1		DS-1E Control	
4C-4Fh	DS-1E Power Control 2		D-DMA Slave Configuration	
50-53h	Power Management Capabilities		Next Item Pointer	Capability ID
54-57h	Reserved		Power Management Control / Status	
58-5Bh	DS-1E Secondary AC'97 Power Control		ACPI Mode	
5C-5Fh	Reserved			
60-63h	Sound Blaster Base Address		FM Synthesizer Base Address	
64-67h	Joystick Base Address		MPU401 Base Address	
68-FFh	Reserved			

Reserved registers are hardwired to "0". All data written to these registers are discarded. The values read from these registers are all zero.

DS-1E can be accessed by using any bus width, 8-bit, 16-bit or 32-bit.

00-01h: Vendor ID

Read Only
Default: 1073h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Vendor ID															

b[15:0] .....Vendor ID

This register contains the YAMAHA Vendor ID registered in Revision 2.2. This register is hardwired to **1073h**.

02-03h: Device ID

Read Only
Default: 0012h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Device ID															

b[15:0] .....Device ID

This register contains the Device ID of DS-1E. This register is hardwired to **0012h**.

04-05h: Command

Read / Write
Default: 0000h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	SER	-	PER	-	-	-	BME	MS	IOS

b0.....IOS: I/O Space

This bit is a dummy one that is capable of writing. This bit indicates for BIOS or OS that DS-1E includes I/O devices.

b1.....MS: Memory Space

This bit enables DS-1E to response to Memory Space Access.
"0": DS-1E ignores Memory Space Access. (default)
"1": DS-1E responds to Memory Space Access.

b2.....BME: Bus Master Enable

This bit enables DS-1E to act as a master device on the PCI bus.
"0": Do not set DS-1E to be the master device. (default)
"1": Set DS-1E to be the master device.

b6.....PER: Parity Error Response

This bit enables DS-1E responses to Parity Error.

"0": DS-1E ignores all parity errors. (default)

"1": DS-1E performs error operation when DS-1E detects a parity error.

b8.....SER: SERR# Enable

This bit enables DS-1E to drive SERR#.

"0": Do not drive SERR#. (default)

"1": Drives SERR# when DS-1E detects an Address Parity Error on normal target cycle or a Data Parity Error on special cycle.

06-07h: Status

Read / Write Clear
Default: 0210h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
DPE	SSE	RMA	RTA	STA	DEVT		DPD	-	-	-	CAP	-	-	-	-

b4.....CAP: Capability (Read Only)

This bit indicates that DS-1E supports the capability register. This bit is read only. When 58-59h : ACPI Mode register, ACPI bit is "0", the bit is "1". When ACPI bit is "1", the bit is "0".

b8.....DPD: Data Parity Error Detected

This bit indicates that DS-1E detects a Data Parity Error during a PCI master cycle.

b[10:9].....DEVT: DEVSEL Timing (Read Only)

This bit indicates that the decoding speed of DS-1E is Medium.

b11.....STA: Signaled Target Abort

This bit indicates that DS-1E terminates a transaction with Target Abort during a target cycle.

b12.....RTA: Received Target Abort

This bit indicates that a transaction is terminated with Target Abort while DS-1E is in the master memory cycle.

b13.....RMA: Received Master Abort

This bit indicates that a transaction is terminated with Master Abort while DS-1E is in the master memory cycle.

b14.....SSE: Signaled System Error

This bit indicates that DS-1E asserts SERR#.

b15.....DPE: Detected Parity Error

This bit indicates that DS-1E detects Address Parity Error or Data Parity Error during a transaction.

08h: Revision ID

Read Only
Default: 00h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Revision ID							

b[7:0] .....Revision ID

This register contains the revision number of DS-1E. This register is hardwired to **00h**.

09h: Programming Interface

Read Only
Default: 00h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Programming Interface							

b[7:0] .....Programming Interface

This register indicates the programming interface of DS-1E. This register is hardwired to **00h**.

0Ah: Sub-class Code

Read Only
Default: 01h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Sub-class Code							

b[7:0] .....Sub-class Code

This register indicates the sub-class of DS-1E. This register is hardwired to **01h**. DS-1E belongs to the **Audio** Sub-class.

0Bh: Base Class Code

Read Only
Default: 04h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Base Class Code							

b[7:0] .....Base Class Code

This register indicates the base class of DS-1E. This register is hardwired to **04h**. DS-1E belongs to the **Multimedia** Base Class.

0Dh: Latency Timer

Read / Write
Default: 00h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Latency Timer							

b[7:0] .....Latency Timer

When DS-1E becomes a Bus Master device, this register indicates the initial value of the Master Latency Timer.

0Eh: Header Type

Read Only
Default: 00h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Header Type							

b[7:0] .....Header Type

This register indicates the device type of DS-1E. This is hardwired to **00h**.

10-13h: PCI Audio Memory Base Address

Read / Write
Default: 00000000h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MBA	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
MBA (higher)															

b[31:15] .....MBA: Memory Base Address

This register indicates the physical Memory Base address of the PCI Audio registers in DS-1E. The base address can be located anywhere in the 32-bit address space. Data in the DS-1E register is not prefetchable.

Size of the register to be mapped into the memory space is 32,768 bytes.

14-17h: Legacy Audio I/O Base Address (Dummy for SB, FM, MPU, D-DMA)

Read / Write
Default: 00000001h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IOBASE0										-	-	-	-	-	I/O
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b0.....IO (Read Only)

This bit indicates that the base address is assigned to I/O. This bit is hardwired to "1".

b[15:6].....IOBASE0

This register is used so that the OS may secure I/O resources for Sound Blaster Pro, FM Synthesizer, MPU401 and D-DMA controller. Because this register is a dummy one, each for the I/O addresses of the above blocks is assigned with the I/O addresses set to 4C-4Dh and 60-65h respectively by the software driver.

18-1Bh: Legacy Audio I/O Base Address (Dummy for Joystick)

Read / Write
Default: 00000001h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IOBASE1														-	I/O
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

b0.....IO (Read Only)

This bit indicates that the base address is assigned to I/O. This bit is hardwired to "1".

b[15:2].....IOBASE1

This register is used so that the OS may secure I/O resource for the joystick port. Because this register is a dummy one, the joystick I/O address is assigned with the I/O address set to 66-67h by the software driver.

2C-2Dh: Subsystem Vendor ID

Read Only
Default: 1073h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Subsystem Vendor ID															

b[15:0] .....Subsystem Vendor ID

This register contains the Subsystem Vendor ID. In general, this ID is used to distinguish adapters or systems made by different IHVs using the same chip by the same vendor. This register is read only. To write the IHV's Vendor ID, use 44-45h (Subsystem Vendor ID Write Register). IHVs must change this ID to their Vendor ID in the BIOS POST routine.

In case of the system such as Sound Card which BIOS can not control, this ID can be changed by connecting EEPROM externally. Then, Subsystem Vendor ID Write Register is invalid.

In case EEPROM is not externally, the default value is the YAMAHA's Vendor ID, **1073h**.

2E-2Fh: Subsystem ID

Read Only
Default: 0012h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Subsystem ID															

b[15:0] .....Subsystem ID

This register contains the Subsystem ID. In general, this ID is used to distinguish adapters or systems made by different IHVs using the same chip by the same vendor. This register is read only. To write the IHV's Device ID, use 46-47h (Subsystem ID Write Register). IHVs must change this ID to their ID in the BIOS POST routine.

In case of the system such as Sound Card which BIOS can not control, this ID can be changed by connecting EEPROM externally. Then, Subsystem ID Write Register is invalid.

In case EEPROM is not externally, the default value is the YAMAHA's Device ID, **0012h**.

34h: Capability Register Pointer

Read Only
Default: 50h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Capability Register Pointer							

b[7:0] .....Capability Register Pointer

This register indicates the offset address of the Capabilities register in the PCI Configuration register when 58-59h: ACPI Mode register, ACPI bit is "0". DS-1E provides PCI Bus Power Management registers as the capabilities. The Power Management registers are mapped to 50h - 55h in the PCI Configuration register, and this register indicates "50h".

When ACPI bit is "1", this register indicates "00h".

3Ch: Interrupt Line

Read / Write
Default: 00h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Interrupt Line							

b[7:0] .....Interrupt Line

This register indicates the interrupt channel that INTA# is assigned to.

3Dh: Interrupt Pin

Read Only
Default: 01h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Interrupt Pin							

b[7:0] .....Interrupt Pin

DS-1E supports INTA# only. This register is hardwired to 01h.

3Eh: Minimum Grant

Read Only
Default: 05h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Minimum Grant							

b[7:0] .....Minimum Grant

This register indicates the length of the burst period required by DS-1E.

This register is hardwired to **05h**.

3Fh: Maximum Latency

Read Only
Default: 19h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Maximum Latency							

b[7:0] .....Maximum Latency

This register indicates how often DS-1E generates the Bus Master Request.

This register is hardwired to **19h**.

40-41h: Legacy Audio Control

Read / Write
Default: 907Fh
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
LAD	SIEN	MPUIRQ			SBIRQ			SDMA		I/O	MIEN	MEN	JPEN	FMEN	SBEN

b0.....SBEN: Sound Blaster Enable

This bit enables the mapping of the Sound Blaster Pro block in the I/O space specified by 62-63h: Sound Blaster Base Address register, when LAD is set to "0".

"0": Disable the mapping of the SB block to the I/O space

"1": Enable the mapping of the SB block to the I/O space (default)

b1.....FMEN: FM Synthesizer Enable

This bit enables the mapping of the FM Synthesizer block in the I/O space specified by 60-61h: FM Synthesizer Base Address register when LAD is set to "0". FM Synthesizer registers can be accessed via SB I/O space, while the SB block is enabled, even if FMEN is set to "0".

"0": Disable the mapping of the FM Synthesizer block to the FMIO space

"1": Enable the mapping of the FM Synthesizer block to the FMIO space (default)

After setting FMEN to "1", about 100 msec is necessary before accessing these I/O space.

b2.....JPEN: Joystick Port Enable

This bit enables the mapping of the Joystick block in the I/O space specified by 66-67h: Joystick Base Address register, when LAD is set to "0".

"0": Disable the mapping of the Joystick block

"1": Enable the mapping of the Joystick block (default)

b3.....MEN: MPU401 Enable

This bit enables the mapping of the MPU401 block in the I/O space specified by 64-65h: MPU401 Base Address register, when LAD is set to "0".

"0": Disable the mapping of the MPU401 block

"1": Enable the mapping of the MPU401 block (default)

b4.....MIEN: MPU401 IRQ Enable

This bit enables the interrupt service of MPU401, when LAD is set to "0" and MEN is set to "1". MPU401 generates an interrupt signal when it receives any kind of MIDI data from the RXD pin.

"0": The MPU401 block can not use the interrupt service.

"1": The MPU401 block can use interrupt signals determined by the MPUIRQ bits. (default)

b5.....I/O: I/O Address Aliasing Control

This bit selects the number of bits to decode for the I/O address of each block.

"0": 16-bit address decode

"1": 10-bit address decode (default)

b[7:6] .....SDMA: Sound Blaster DMA-8 Channel Select

These bits select the DMA channel for the Sound Blaster Pro block.

"0": DMA ch0
"1": DMA ch1 (default)
"2": reserved
"3": DMA ch3

b[10:8] .....SBIRQ: Sound Blaster IRQ Channel Select

These bits select the interrupt channel for the Sound Blaster Pro block.

"0": IRQ5 (default)
"1": IRQ7
"2": IRQ9
"3": IRQ10
"4": IRQ11
"5" - "7": reserved.

b[13:11] .....MPUIRQ: MPU401 IRQ Channel Select

When MIEN is set to "1", these bits select the interrupt channel for the MPU401 block.

"0": IRQ5
"1": IRQ7
"2": IRQ9 (default)
"3": IRQ10
"4": IRQ11
"5" - "7": reserved

Same interrupt channels can be assigned to SBIRQ and MPUIRQ.

b14.....SIEN: Serialized IRQ enable

DS-1E supports 3 types of interrupt protocols: PCI interrupt (INTA#), Legacy interrupt (IRQs) and Serialized IRQ. The interrupt protocol is selected with IMOD and SIEN as follows.

The interrupt channels for IRQs and Serialized IRQ are determined by SBIRQ and MPUIRQ,. Only one protocol can be used at once.

SIEN	IMOD	Interrupt protocol	
0	0	Legacy interrupt (IRQs)	(default)
0	1	PCI interrupt (INTA#)	
1	0	Serialized IRQ	
1	1	reserved	

b15.....LAD: Legacy Audio Disable

This bit disables the Legacy Audio block.

"0": Enables the Legacy Audio block

"1": Disables the Legacy Audio block (default)

When this bit is set to "1", DS-1E does not respond to the I/O Target transaction for legacy I/O address on the PCI bus.

42-43h: Extended Legacy Audio Control

Read / Write
Default: 0000h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IMOD	SBVER		SMOD		-	-	MAIM	-	-	-	-	-	-	-	-

b8.....MAIM: MPU401 Acknowledge Interrupt Mask

This bit determine whether interrupt is asserted when the acknowledge, which is occurred by changing MPU401 mode form default to UART, is returned.

"0": Interrupt is asserted when the acknowledge is returned. (default)

"1": Interrupt is masked when the acknowledge is returned.

b[12:11].....SMOD: SB DMA mode

These bits determine the protocol to achieve the DMAC(8237) function on the PCI bus.

"0": PC/PCI (default)

"1": reserved

"2": Distributed DMA (D-DMA)

"3" reserved

b[14:13].....SBVER: SB Version Select

These bits set the version of the SB Pro DSP. The value set in these bits is returned by sending the E1h DSP command.

"0": ver 3.01 (default)

"1": ver 2.01

"2": ver 1.05

"3": reserved

b15.....IMOD: Legacy IRQ mode

The legacy interrupt protocol is selected with IMOD and SIEN. Refer to the explanation of SIEN bit.

44-45h: Subsystem Vendor ID Write

Read / Write
Default: 1073h
Access Bus Width: 16-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Subsystem Vendor ID Write															

b[15:0] .....Subsystem Vendor ID Write

This register sets the Subsystem Vendor ID that is read from 2C-2Dh (Subsystem Vendor ID register). The default value is the YAMAHA Vendor ID, **1073h**. IHVs must change this ID to their Vendor ID in the BIOS POST routine.

In case EEPROM connects externally, this register is invalid, and do not reflect to Subsystem Vendor ID.

46-47h: Subsystem ID Write

Read / Write
Default: 0012h
Access Bus Width: 16-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Subsystem ID Write															

b[15:0] .....Subsystem ID Write

This register sets the Subsystem ID that is read from 2E-2Fh (Subsystem ID register). The default value is the DS-1E Device ID, **0012h**. IHVs must change this ID to their ID in the BIOS POST routine.

In case EEPROM connects externally, this register is invalid, and do not reflect to Subsystem ID.

48-49h: DS-1E Control

Read / Write
Default: 0001h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	ACLS	WRST	-	CRST

b0.....CRST: AC'97 Software Reset Signal Control

This bit controls the CRST# signal.

"0": Inactive (CRST#=High)

"1": Active (CRST#=Low) (default)

b2.....WRST: AC'97 Warm Reset

This bit places the AC'97 in warm reset condition when the BIT_CLK signal on the AC'97 remains in inactive state. If this bit is set to "1", it will automatically return to "0" after 1.3µs time duration. This bit is valid only while the ACLS bit is set to "0". Except in this case, even if this bit is attempted to be set to "1", no warm reset will be generated (write operation of "1" remains disabled).

"0": Normal (default)

"1": AC'97 Warm Reset

b3.....ACLS: AC-Link Status (Read Only)

This bit indicates whether or not the AC-link is active. This bit is "1" when the AC-link remains in active state (the BIT_CLK signal is active).

"0": AC'97 Inactive (default)

"1": AC'97 Active

4A-4Bh: DS-1E Power Control 1

Read / Write
Default: 0000h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	-	JSR	-	-	-	DPLL	-	DMC

b0.....DMC: Disable Master Clock Oscillation

Setting this bit to "1" disables the oscillation of the Master Clock (24.576 MHz).

"0": Normal (default)

"1": Disable

b2.....DPLL: Disable PLL Clock Oscillation

Setting this bit to "1" disables the oscillation of PLL.

"0": Normal (default)

"1": Disable

b6.....JSR: Joystick Reset

This bit controls reset of the flip-flop circuit following the analog comparator stage on the joystick port. The Initial value is set to "0" immediately after power on reset or hardware reset.

"0": Normal (default)

"1": Resets the flip-flop circuit following the analog comparator stage on the joystick port

b8.....PR0: AC'97 Power Down Control 0

This bit controls the power state of the **ADC and Input Mux** in the Primary AC'97.

"0": Normal (default)

"1": Power down

b9.....PR1: AC'97 Power Down Control 1

This bit controls the power state of the **DAC** in the Primary AC'97.

"0": Normal (default)

"1": Power down

b10.....PR2: AC'97 Power Down Control 2

This bit controls the power state of the **Analog Mixer (Vref still on)** in the Primary AC'97. This power state retains the Reference Voltage of the AC'97.

"0": Normal (default)

"1": Power down

b11.....PR3: AC'97 Power Down Control 3

This bit controls the power state of the **Analog Mixer (Vref off)** in the Primary AC'97. This power state removes Reference Voltage of the AC'97.

"0": Normal (default)

"1": Power down

b12.....PR4: AC'97 Power Down Control 4

This bit controls the power state of the **AC-link** in the Primary AC'97.

"0": Normal (default)

"1": Power down

b13.....PR5: AC'97 Power Down Control 5

Setting this bit to "1" disables the internal clock of the Primary AC'97. In case the AC'97 is used with DS-1E, the master clock is supplied from DS-1E. Therefore, when the clock is stopped completely, set PR5 bits to "1" firstly, then the CMCD bit should be set to "1" after duration of 1ms or longer.

"0": Normal (default)

"1": Disable

b14.....PR6: AC'97 Power Down Control 6

This bit controls PR6 bit status of the power control register in the Primary AC'97.

b15.....PR7: AC'97 Power Down Control 7

This bit controls PR7 bit status of the power control register in the Primary AC'97.

Respective data set to b[15:8] are correspondingly set into the "Power down Ctrl/Stat" register in the Primary AC'97 via the AC-Link. These are not set into the "Power down Ctrl/Stat" register in the Secondary AC'97.

4C-4Dh: D-DMA Slave Configuration

Read / Write
Default: 0000h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Base Address												EA	TS		CE

b0.....CE: Channel Enable

This bit enables the Distributed DMA function.

"0": Disable Distributed DMA (default)

"1": Enable Distributed DMA

b[2:1].....TS: Transfer Size (Read Only)

These bits indicate the size of the DMA transfer. Since DS-1E supports only 8-bit DMA transfer, the bits are hardwired to 00b.

b3.....EA: Extended Address (Read Only)

DS-1E does not support extended address mode. This bit is hardwired to 0b.

b[15:4].....Base Address : D-DMA Slave Base Address

These bits indicate the D-DMA slave base address.

4E-4Fh: DS-1E Power Control 2

Read / Write
Default: 0000h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	PSHWV	PSIO	PSACL	PSDIR	PSDIT	PSZV	PSSRC	PSPCA	PSJOY	PSMPU	PSSB	PSFM	CMCD

b0.....CMCD: CODEC Master Clock Disable

Setting this bit to "1" disables the oscillation of the CMCLK. To stop a clock, when the CMCLK is supplied to the AC'97, it is required that b13:PR5 bit of 4A-4Bh register is set to "1". (If the Secondary AC'97 is used, it is also necessary that b5:SPR5 bit of 5A-5Bh register is set to "1".)

"0": Normal (default)

"1": Disable

b1.....PSFM: Power Save FM Synthesizer

Setting this bit to "1" stops a clock supplied to the FM synthesizer block.

"0": Normal (default)

"1": Disable

b2.....PSSB: Power Save Sound Blaster

Setting this bit to "1" stops a clock supplied to the Sound Blaster block.

"0": Normal (default)

"1": Disable

b3.....PSMPU: Power Save MPU401

Setting this bit to “1” stops a clock supplied to the MPU401 block.

“0”: Normal (default)

“1”: Disable

b4.....PSJOY: Power Save Joystick

Setting this bit to “1” disables the comparator of the Joystick block.

“0”: Normal (default)

“1”: Disable

b5.....PSPCA: Power Save PCI Audio

Setting this bit to “1” stops a clock supplied to the PCI Audio block.

“0”: Normal (default)

“1”: Disable

b6.....PSSRC: Power Save SRC

Setting this bit to “1” stops a clock supplied to the SRC block.

“0”: Normal (default)

“1”: Disable

b7.....PSZV: Power Save Zoomed Video port

Setting this bit to “1” stops a clock supplied to the Zoomed Video port block.

“0”: Normal (default)

“1”: Disable

b8.....PSDIT: Power Save Digital Audio Interface Transmitter

Setting this bit to “1” stops a clock supplied to the DIT (SPDIF OUT) block.

“0”: Normal (default)

“1”: Disable

b9.....PSDIR: Power Save Digital Audio Interface Receiver

Setting this bit to “1” stops a clock supplied to the DIR (SPDIF IN) block.

“0”: Normal (default)

“1”: Disable

b10.....PSACL: Power Save AC-Link

Setting this bit to “1” stops a clock supplied to the AC-Link block.

“0”: Normal (default)

“1”: Disable

b11.....PSIO: Power Save I/O Pad

Setting this bit to “1” cuts the pull up resistor of the input pins except for the PCI interface and AC-Link. The input signals keep the level before PSIO bit is set from “0” to “1”. In case the input level is only “low”, the pull up resistor is cut.

“0”: Normal (default)

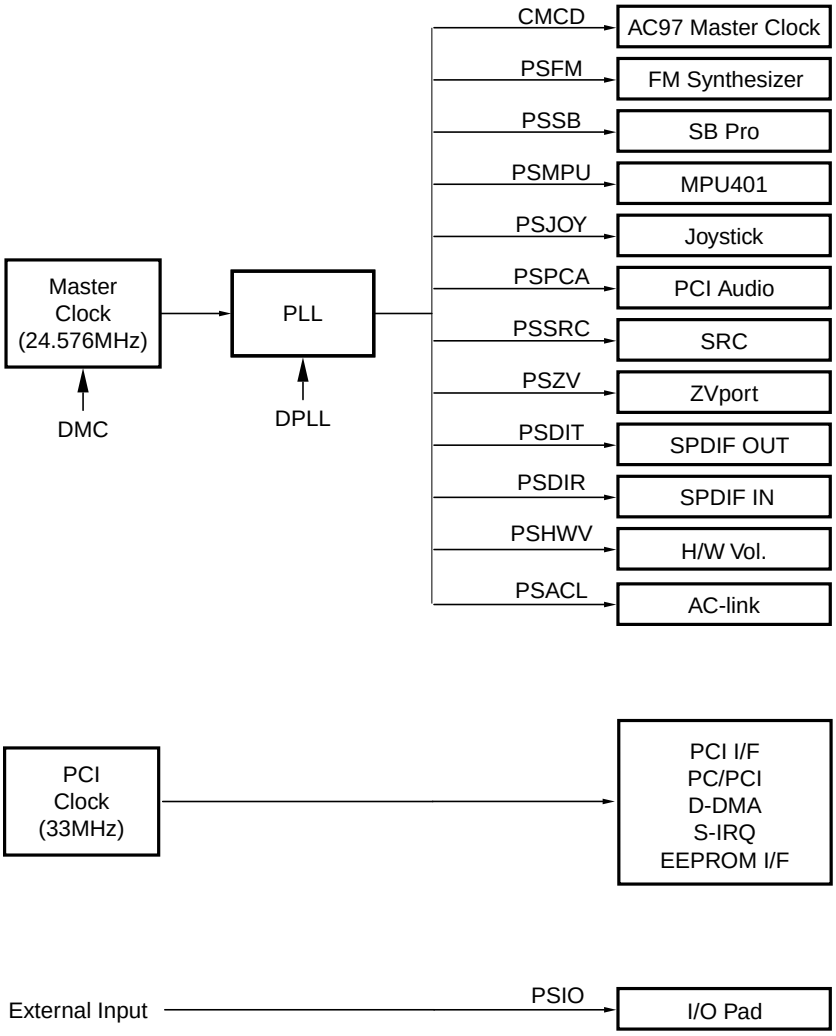
“1”: Cuts the pull up resistor

b12.....PSHWV: Power Save Hardware Volume

Setting this bit to “1” stops a clock supplied to the Hardware Volume block.

“0”: Normal (default)

“1”: Disable



Power Management Block

50h: Capability ID

Read Only
Default: 01h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Capability ID							

b[7:0] .....Capability ID: Capability Identifier

This register indicates that the new capability register is for Power Management control. This register is hardwired to **01h**.

51h: Next Item Pointer

Read Only
Default: 00h
Access Bus Width: 8, 16, 32-bit

b7	b6	b5	b4	b3	b2	b1	b0
Next Item Pointer							

b[7:0] .....Next Item Pointer

DS-1E does not provide other new capability besides Power Management. This register is hardwired to **00h**.

52-53h: Power Management Capabilities

Read Only
Default: 0401h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	D2S	-	-	-	-	-	-	-	Version		

b[2:0] .....Version

These bits contain the revision number of the Power Management Interface Specification. They are hardwired to **001b**.

b10.....D2S: D2 Support

This bit indicates that DS-1E support “D2” of the power state. It is hardwired to “1”.

54-55h: Power Management Control / Status

Read / Write
Default: 0000h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	PS	

b[1:0].....PS: Power State

These bits determine the power state of DS-1E. DS-1E supports the following power states:

"0": D0

"1": D1 (not supported)

"2": D2

"3": $D3_{hot}$

When the power state is changed from $D3_{hot}$ to D0, DS-1E resets the PCI Configuration register 00-3Fh. DS-1E transits to D0 Uninitialized state.

Though the power state of this register is changed, the power consumption of DS-1E is not changed. To support low power, Windows driver controls DS-1E Power Control 1 / DS-1E Power Control 2 / DS-1E Control / DS-1E Secondary AC'97 Power Control registers.

DS-1E can support the power state of D0, D1, D2 and D3 with ACPI. In this case, set ACPI bit (58-59h: ACPI Mode Register) to "1" to disable Capabilities of PCI Bus Power Management.

58-59h: ACPI Mode

Read / Write
Default: 0000h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ACPI

b0.....ACPI: ACPI Mode Select

This bit select either PCI Bus Power Management or ACPI Mode for power management of DS-1E.

"0": PCI Bus Power Management is used. CAP bit (06-07h: Status Register) and Capabilities Pointer (34h) are enabled. (default)

"1": ACPI Mode is used. CAP bit and Capabilities Pointer are hardwired "0", and disabled.

5A-5Bh: DS-1E Secondary AC'97 Power Control

Read / Write
Default: 0000h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	-	SPR7	SPR6	SPR5	SPR4	SPR3	SPR2	SPR1	SPR0

b0.....SPR0: Secondary AC'97 Power Down Control 0

This bit controls the power state of the **ADC and Input Mux** in the Secondary AC'97.

"0": Normal (default)

"1": Power down

b1.....SPR1: Secondary AC'97 Power Down Control 1

This bit controls the power state of the **DAC** in the Secondary AC'97.

"0": Normal (default)

"1": Power down

b2.....SPR2: Secondary AC'97 Power Down Control 2

This bit controls the power state of the **Analog Mixer (Vref still on)** in the Secondary AC'97. This power state retains the Reference Voltage of the AC'97.

"0": Normal (default)

"1": Power down

b3.....SPR3: Secondary AC'97 Power Down Control 3

This bit controls the power state of the **Analog Mixer (Vref off)** in the Secondary AC'97. This power state removes Reference Voltage of the AC'97.

"0": Normal (default)

"1": Power down

b4.....SPR4: Secondary AC'97 Power Down Control 4

This bit controls the power state of the **AC-link** in the Secondary AC'97.

"0": Normal (default)

"1": Power down

b5.....SPR5: Secondary AC'97 Power Down Control 5

Setting this bit to "1" disables the internal clock of the Secondary AC'97. In case the AC'97 is used with DS-1E, the master clock is supplied from DS-1E. Therefore, when the clock is stopped completely, set SPR5 bits to "1" firstly, then the CMCD bit should be set to "1" after duration of 1ms or longer.

"0": Normal (default)

"1": Disable

b6.....SPR6: Secondary AC'97 Power Down Control 6

This bit controls PR6 bit status of the power control register in the Secondary AC'97.

b7.....SPR7: Secondary AC'97 Power Down Control 7

This bit controls PR7 bit status of the power control register in the Secondary AC'97.

Respective data set to b[7:0] are correspondingly set into the "Power down Ctrl/Stat" register in the Secondary AC'97 via the AC-Link. These are not set into the "Power down Ctrl/Stat" register in the Primary AC'97.

60-61h: FM Synthesizer Base Address

Read / Write
Default: 0388h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FM Synthesizer Base Address														-	-

b[15:2] .....FM Synthesizer Base Address

This register sets the base address of the FM synthesizer. If b5:I/O bit of 40h register is set to "1", b[9:2] bits are decoded by ignoring b[15:10] bits.

62-63h: Sound Blaster Base Address

Read / Write
Default: 0220h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Sound Blaster Base Address												-	-	-	-

b[15:4] .....Sound Blaster Base Address

This register sets the base address of the Sound Blaster. If b5:I/O bit of 40h register is set to "1", b[9:4] bits are decoded by ignoring b[15:10] bits.

64-65h: MPU401 Base Address

Read / Write
Default: 0330h
Access Bus Width: 8, 16, 32-bit

b15	b14	B13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MPU401 Base Address															-

b[15:1] .....MPU401 Base Address

This register sets the base address of the MPU401. If b5:I/O bit of 40h register is set to "1", b[9:1] bits are decoded by ignoring b[15:10] bits.

66-67h: Joystick Base Address

Read / Write
Default: 0201h
Access Bus Width: 8, 16, 32-bit

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Joystick Base Address															

b[15:0] .....Joystick Base Address

This register sets the base address of the Joystick. If b5:I/O bit of 40h register is set to "1", b[9:0] bits are decoded by ignoring b[15:10] bits.

2. ISA Compatible Device

DS-1E contains the following functions to maintain the compatibility with the past ISA Sound Devices. These devices are considered Legacy devices and the functions are referred to as Legacy Audio.
Legacy Audio is independent from PCI Audio and can be used simultaneously.
The configuration is set in the Legacy Audio Control Register in the PCI Configuration Register space.
Basically, these registers are configured by the BIOS.
Also, logical device IDs are assigned to the devices to support Plug and Play. Yamaha defines the following logical IDs.
To control the device with the BIOS, the logical device IDs must be defined in the PnP BIOS extended ROM space. The logical IDs are determined by how it is configured. IDs and configuration are as follows.

Logical Device ID	Functions used (Block)			
	FM(*)	MPU401	SB Pro (*)	Joystick
YMH0100	O	O	O	
YMH0101				O
YMH0102	O			
YMH0103		O		
YMH010A	O	O		

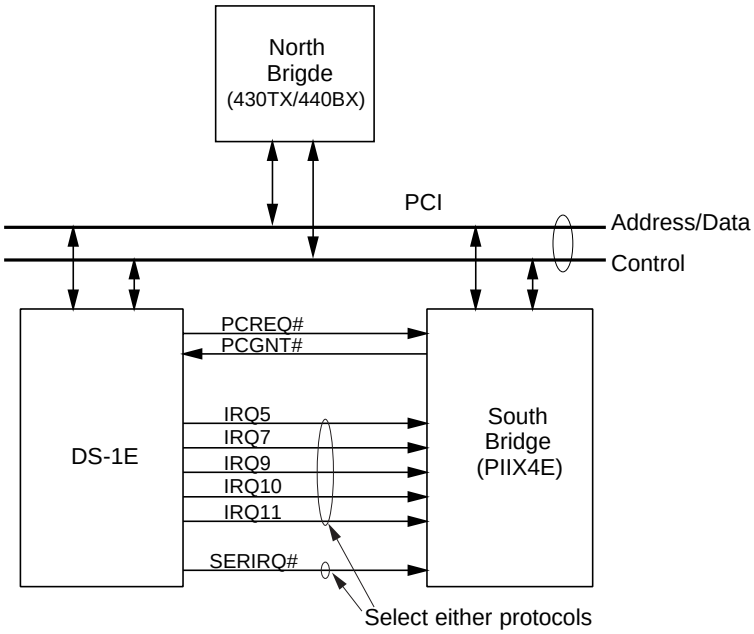
* The blocks pertain to the following.
FM: Points to the FM synthesizer mapped to AdLibBase (0x0388).
SB Pro: Points to the Voice Playback section only.

These devices are independent from each other, and can be Enabled/Disabled individually. However, both AdLib and Sound Blaster must be disabled to disable the internal FM Synthesizer. Disabling just AdLib only masks the access.

The driver by Yamaha supports logical device ID, YMH0100, YMH0102, YMH0103 and YMH010A.
For YMH0101, use the driver provided by Microsoft.

DS-1E supports PC/PCI and D-DMA protocols to emulate the DMA of SB Pro on the PCI. In addition, DS-1E supports the old type of interrupts used by ISA and the Serialized IRQ protocol.

The combination of PC/PCI and Serialized IRQ is recommended for DS-1E.
The system block diagram when using Intel chip set is shown below.



The PCI-to-ISA bridge needs to support PC/PCI. IRQ is directly connected to the IRQ input pins on the PCI-to-ISA bridge.

2-1. FM Synthesizer Block

FM Synthesizer Block is register compatible with YMF289B. However, Power Management register has been deleted because it is now controlled by the PCI Configuration Register.

The following shows the FMBase I/O map of FM Synthesizer.

FMBase	(R)	Status Register port
FMBase	(W)	Address port for Register Array 0
FMBase+1	(R/W)	Data port
FMBase+2	(W)	Address port for Register Array 1
FMBase+3	(R/W)	Data port

The following shows the FM Synthesizer Block registers.

2-1-1. Status Register

FM Synthesizer Status Register (RO):

Address	D7	D6	D5	D4	D3	D2	D1	D0
xxh	IRQ	FT1	FT2	-	-	BUSY	-	BUSY

2-1-2. FM Synthesizer Data Register

FM Synthesizer Data Register Array 0 (R/W):

Address	D7	D6	D5	D4	D3	D2	D1	D0
00-01h	LSI TEST							
02h	TIMER 1							
03h	TIMER 2							
04h	RST	MT1	MT2	-	-	-	ST2	ST1
08h	-	NTS	-	-	-	-	-	-
20-35h(*1)	AM	VIB	EGT	KSR	MULT			
40-55h(*2)	KSL		TL					
60-75h(*3)	AR				DR			
80-95h(*4)	SL				RR			
A0-A8h	F-NUM (L)							
B0-B8h	-	-	KON	BLOCK			F-NUM (H)	
BDh	DAM	DVB	RHY	BD	SD	TOM	TC	HH
C0-C8h	(*6)	(*6)	CHR	CHL	FB			CNT
E0-F5h(*5)	-	-	-	-	-	WS		

FM Synthesizer Data Register Array 1 (R/W)

Address	D7	D6	D5	D4	D3	D2	D1	D0
00-01h	LSI TEST							
04h	-	-	CONNECTION SEL					
05h	-	-	-	-	-	(*6)	(*6)	NEW
20-35h(*1)	AM	VIB	EGT	KSR	MULT			
40-55h(*2)	KSL		TL					
60-75h(*3)	AR				DR			
80-95h(*4)	SL				RR			
A0-A8h	F-NUM (L)							
B0-B8h	-	-	KON	BLOCK			F-NUM (H)	
C0-C8h	(*6)	(*6)	CHR	CHL	FB			CNT
E0-F5h(*5)	-	-	-	-	-	WS		

*1 : 26h, 27h, 2Eh and 2Fh do not exist.

*2 : 46h, 47h, 4Eh and 4Fh do not exist.

*3 : 66h, 67h, 6Eh and 6Fh do not exist.

*4 : 86h, 87h, 8Eh and 8Fh do not exist.

*5 : E6h, E7h, EEh and EFh do not exist.

*6 : The bits exist, but do not function.

2-2. Sound Blaster Pro Block

Sound Blaster Pro block emulates the DSP commands of Sound Blaster and Sound Blaster Pro. Only playback functions are supported (record functions are not supported). However, to maintain compatibility for games, it is designed so that every DSP command receives a correct response.
The DMA transfer of this block uses PC/PCI or D-DMA protocol.

The following shows the SBBase I/O map of SB Pro.

SBBase	(R)	FM Synthesizer Status port
SBBase	(W)	FM Synthesizer Address port for Register Array 0
SBBase+1h	(R/W)	FM Synthesizer Data register
SBBase+2h	(W)	FM Synthesizer Address port for Register Array 1
SBBase+3h	(R/W)	FM Synthesizer Data port
SBBase+4h	(R/W)	SB Mixer Address port
SBBase+5h	(R/W)	SB Mixer Data port
SBBase+6h	(W)	SB DSP Reset port
SBBase+8h	(R)	FM Synthesizer Status port
SBBase+8h	(W)	FM Synthesizer Address port for Register Array 0
SBBase+9h	(R/W)	FM Synthesizer Data port
SBBase+Ah	(R)	DSP Read Data port
SBBase+Ch	(R)	DSP Write-buffer status port
SBBase+Ch	(W)	DSP Write Command/Data port
SBBase+Eh	(R)	DSP Read-buffer status port

2-2-1. DSP Command

The following shows the list of DSP Commands that are supported by the SB Pro engine. Both SB and SB Pro commands are supported.

CMD	Support	Function
10h	o	8bit direct mode single byte digitized sound output
14h	o	8bit single-cycle DMA mode digitized sound output
16h		8bit to 2bit ADPCM single-cycle DMA mode digitized sound output
17h		8bit to 2bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
1Ch	o	8bit auto-init DMA mode digitized sound output
1Fh		8bit to 2bit ADPCM auto-init DMA mode digitized sound output with ref. byte
20h(*1)	o	8bit direct mode single byte digitized sound input
24h(*1)	o	8bit single-cycle DMA mode digitized sound input
2Ch(*1)	o	8bit auto-init DMA mode digitized sound input
30h	o	Polling mode MIDI input
31h	o	Interrupt mode MIDI input
34h	o	UART polling mode MIDI I/O
35h	o	UART interrupt mode MIDI I/O
36h(*2)	o	UART polling mode MIDI I/O with time stamping
37h(*2)	o	UART interrupt mode MIDI I/O with time stamping
38h	o	MIDI output
40h	o	Set digitized sound transfer Time Constant
48h	o	Set DSP block transfer size
74h	o	8bit to 4bit ADPCM single-cycle DMA mode digitized sound output
75h	o	8bit to 4bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
76h		8bit to 3bit ADPCM single-cycle DMA mode digitized sound output
77h		8bit to 3bit ADPCM single-cycle DMA mode digitized sound output with ref. byte
7Dh	o	8bit to 4bit ADPCM auto-init DMA mode digitized sound output with ref. byte
7Fh		8bit to 3bit ADPCM auto-init DMA mode digitized sound output with ref. byte
80h	o	Pause DAC for a duration
90h	o	8bit high-speed auto-init DMA mode digitized sound output
91h	o	8bit high-speed single-cycle DMA mode digitized sound output
98h(*1)	o	8bit high-speed auto-init DMA mode digitized sound input
99h(*1)	o	8bit high-speed single-cycle DMA mode digitized sound input
A0h(*1)	o	Set input mode to mono
A8h(*1)	o	Set input mode to stereo
D0h	o	Pause 8bit DMA mode digitized sound I/O
D1h(*3)	o	Turn on speaker
D3h(*3)	o	Turn off speaker
D4h	o	Continue 8bit DMA mode digitized sound I/O
D8h	o	Get speaker status
DAh	o	Exit 8bit auto-init DMA mode digitized sound I/O
E1h	o	Get DSP version number

Note:

(*1) The SB Block responds correctly to the commands for recording and also executes the DMA transfer. 80h is always transferred.

(*2) Only output is supported for this command.

(*3) This command only changes Speaker Status (D8h).

Undocumented commands other than the ones listed above are also supported.

2-2-2. Sound Blaster Pro Mixer

The following shows the register map of the Mixer section of Sound Blaster Pro.

Address	b7	b6	b5	b4	b3	b2	b1	b0	Remark
00h	Reset								
04h	Voice Volume L			"1"	Voice Volume R			"1"	SB Pro Mixer
0Ah	-	-	-	"1"	-	MIC Volume*			
0Ch	-	-	Ifilter*	"1"	Input Source*			"1"	
0Eh	-	-	Ofilter*	"1"	-	-	St. SW	"1"	
22h	Master Volume L			"1"	Master Volume R			"1"	
26h	MIDI Volume L			"1"	MIDI Volume R			"1"	
28h	CD Volume L*			"1"	CD Volume R*			"1"	
2Eh	Line Volume L*			"1"	Line Volume R*			"1"	
F0h	SBPDA	-	-	-	SS	SM	SE	SBPDR	Suspend / Resume
F1h	SCAN DATA								
F2h	Current FM Synthesizer Index								
F3h	-	-	-	-	-	-	-	CFA	
F4h	FFEMP	FFFUL	-	-	-	-	-	MPUS	
F8h	-	-	-	-	-	-	-	SBI	IRQ Status

The registers marked with * exist, but do not function.

DS-1E does not have the circuit that corresponds to the SB Mixer. Therefore, the volume settings on the SB Mixer are converted to the DSP coefficients of DS-1E or to AC'97 register values.
The conversion for each case is described below.

(1) SB Mixer → DSP

The volume of master, MIDI and Voice, are applied to this case.
When the SB register is set, a 14-bit coefficient value is determined from the following conversion table and used as the DSP coefficient. The attenuation value of Master Volume, MIDI, and voice are summed together to obtain the coefficient.
These volumes cannot be controlled from PCI Audio block.

(1) Volume for MIDI

		MIDI Vol. (26h)							
		0	1	2	3	4	5	6	7
Master Vol. (22h)	0	mute	mute	mute	mute	mute	mute	mute	mute
		0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
	1	mute	-52dB	-42dB	-36dB	-32dB	-30dB	-28dB	-26dB
		0000h	0029h	0082h	0103h	019Bh	0206h	028Ch	0335h
	2	mute	-42dB	-32dB	-26dB	-22dB	-20dB	-18dB	-16dB
		0000h	0082h	019Bh	0335h	0515h	0666h	080Eh	0A24h
	3	mute	-36dB	-26dB	-20dB	-16dB	-14dB	-12dB	-10dB
		0000h	0103h	0335h	0666h	0A24h	0CC5h	1013h	143Dh
	4	mute	-32dB	-22dB	-16dB	-12dB	-10dB	-8dB	-6dB
		0000h	019Bh	0515h	0A24h	1013h	143Dh	197Ah	2013h
	5	mute	-30dB	-20dB	-14dB	-10dB	-8dB	-6dB	-4dB
		0000h	0206h	0666h	0CC5h	143Dh	197Ah	2013h	2861h
	6	mute	-28dB	-18dB	-12dB	-8dB	-6dB	-4dB	-2dB
		0000h	028Ch	080Eh	1013h	197Ah	2013h	2861h	32D6h
	7	mute	-26dB	-16dB	-10dB	-6dB	-4dB	-2dB	0dB
		0000h	0335h	0A24h	143Dh	2013h	2861h	32D6h	3FFFh

The default is Master = 4, MIDI = 4 (-12dB).

(2) Volume for Voice

		Voice Vol. (04h)							
		0	1	2	3	4	5	6	7
Master Vol. (22h)	0	mute	mute	mute	mute	mute	mute	mute	mute
		0000h	0000h	0000h	0000h	0000h	0000h	0000h	0000h
	1	mute	-56dB	-46dB	-40dB	-36dB	-34dB	-32dB	-30dB
		0000h	0019h	0052h	00A3h	0103h	0146h	019Bh	0206h
	2	mute	-46dB	-36dB	-30dB	-26dB	-24dB	-22dB	-20dB
		0000h	0052h	0103h	0206h	0335h	0409h	0515h	0666Eh
	3	mute	-40dB	-30dB	-24dB	-20dB	-18dB	-16dB	-14dB
		0000h	00A3h	0206h	0409h	0666h	080Eh	0A24h	0CC5h
	4	mute	-36dB	-26dB	-20dB	-16dB	-14dB	-12dB	-10dB
		0000h	0103h	0335h	0666h	0A24h	0CC5h	1013h	143Dh
	5	mute	-34dB	-24dB	-18dB	-14dB	-12dB	-10dB	-8dB
		0000h	0146h	0409h	080Eh	0CC5h	1013h	143Dh	197Ah
	6	mute	-32dB	-22dB	-16dB	-12dB	-10dB	-8dB	-6dB
		0000h	019Bh	0515h	0A24h	1013h	143Dh	197Ah	2013h
	7	mute	-30dB	-20dB	-14dB	-10dB	-8dB	-6dB	-4dB
		0000h	0206h	0666h	0CC5h	143Dh	187Ah	2013h	2861h

The default is Master = 4, Voice = 4 (-16dB).

(2) SB Mixer → AC'97

The volume of CD, Line and MIC are applied to this case. AC'97 volume are not updated automatically when these values are changed. Thus, the SB Mixer values need to be written to the AC'97 register with the software.

2-2-3. SB Suspend / Resume

The SB block can read the internal state as to support Suspend and Resume functions. The internal state is made up of 268 flip flops. To read the state, these states are shifted in order and read 8 bits at a time from the SCAN DATA register.

These registers are mapped to the SB Mixer space (see SB Mixer Register map). The registers have the following functions.

F0h: Scan In/ Out Control

Read / Write
Default: 00h

b7	b6	b5	b4	b3	b2	b1	b0
SBPDA	-	-	-	SS	SM	SE	SBPDR

b0.....SBPDR: Sound Blaster Power Down Request

This bit stops the internal state of the Sound Blaster block.

"0": Normal (default)

"1": Stop

b1.....SE: Scan Enable

This bit Shifts the internal state by 1 bit. Setting a "1" followed by a "0" shifts the internal state.

b2.....SM: Scan Mode

This bit sets whether to read or write the state.

"0": Write (default)

"1": Read

b3.....SS: Scan Select

This bit gives permission to read or write the internal data to the SCAN DATA register.

"0": Normal operation (Do not allow read or write). (default)

"1": Allow read and write.

b7.....SBPDA: Sound Blaster Power Down Acknowledgement

This bit indicates that the SB Block is ready to read or write to the internal state after setting SBPDR. This bit is read only.

"0": Read/Write not possible

"1": Read/ Write possible

F1h: Scan In/ Out Data

Read / Write
Default: 00h

b7	b6	b5	b4	b3	b2	b1	b0
SCAN DATA							

b[7:0].....SCAN DATA

This is the data port for reading and writing the internal state.

F2h: Current FM Synthesizer Index

Read Only
Default: 00h

b7	b6	b5	b4	b3	b2	b1	b0
Current FM Synthesizer Index							

b[7:0].....Current FM Synthesizer Index

This register indicates current index of the FM Synthesizer.

F3h: Current FM Synthesizer Array

Read Only
Default: 00h

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	CFA

b0.....CFA: Current FM Synthesizer Arary

This bit indicates that the FM Synthesizer array is being currently set to Array 0 or 1.

"0": Array 0 (default)

"1": Array 1

F4h: FM Synthesizer / MPU401 Status

Read Only
Default: 80h

b7	b6	b5	b4	b3	b2	b1	b0
FFEMP	FFFUL	-	-	-	-	-	MPUS

b0.....MPUS: MPU401 Status

This bit indicates current MPU401 status.

"0": Default mode (Intelligent mode) (default)

"1": UART mode

b6.....FFFUL: FM Synthesizer FIFO Full

This bit indicates whether or not FIFO followed by the FM Synthesizer is full.

"0": not Full (default)

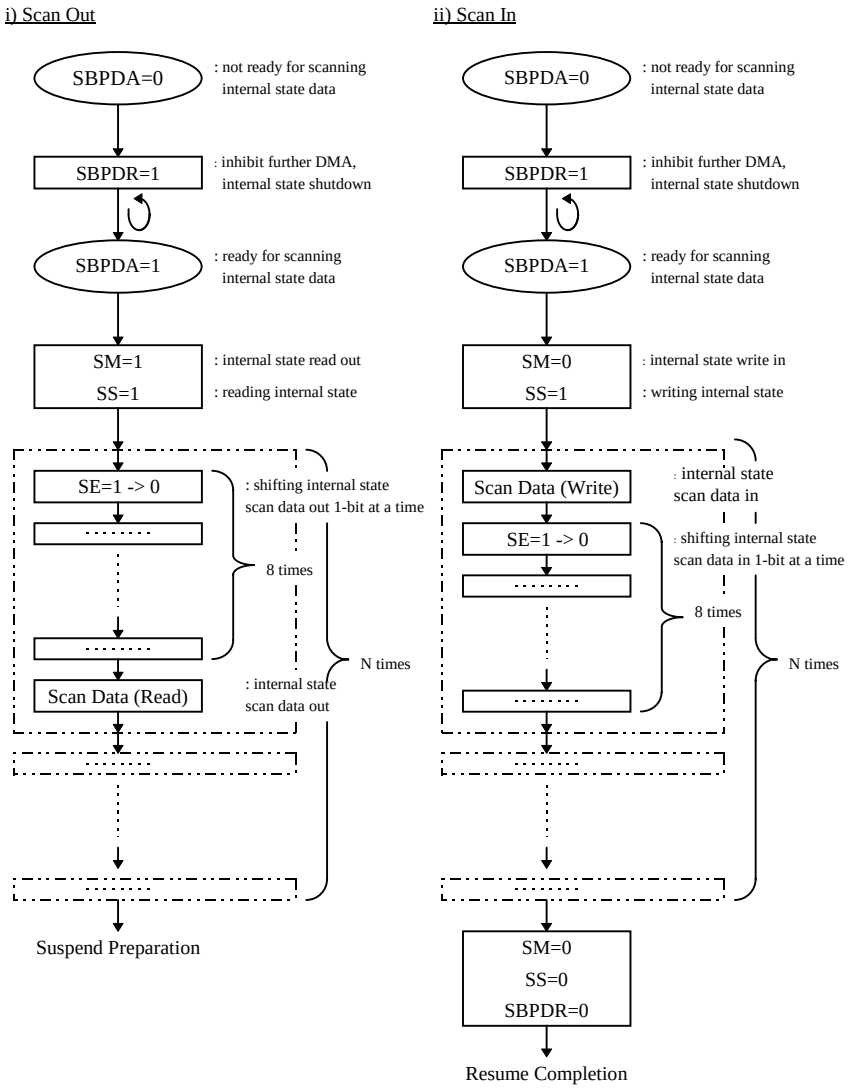
"1": Full

b7.....FFEMP: FM Synthesizer Empty

This bit indicates whether or not FIFO followed by the FM Synthesizer is empty.

"0": not Empty

"1": Empty (default)



N = 34 byte (Total Scan Data = 268 bit (33 byte x 8 + 4 bit))

2-2-4. SB IRQ Status

F8h: Interrupt Flag Register

Read Only
Default: 00h

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	SBI

b0.....SBI: SB Interrupt Flag

This bit indicates that the SB DSP occurs the interrupt. This bit is read only. Thus, read the SB DSP read port to clearing the interrupt and this bit. Then, the value of the read port is invalid.

2-3. MPU401

MPU401 block is for transmitting and receiving MIDI data. It is compatible with UART mode of "MPU401". Full duplex operation is possible using the 16-byte FIFO for each direction, transmitting and receiving.

The following shows the MPUBase I/O map for MPU401.

MPUBase	(R/W)	MIDI Data port
MPUBase + 1h	(R)	Status Register port
MPUBase + 1h	(W)	Command Register port

port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	Data							
+1h (W)	Command							
+1h (R)	/DSR	/DRR	-	-	-	-	-	-

2-4. Joystick

Joystick Block is the port for connecting IBM compatible analog joystick.

The following shows the JSBase I/O map for Joystick.

JSBase (R/W)

Port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	JBB2	JBB1	JAB2	JAB1	JBCY	JBCX	JACY	JACX

JACX... Joystick A, Coordinate X
JACY... Joystick A, Coordinate Y
JBCX... Joystick B, Coordinate X
JBCY... Joystick B, Coordinate Y
JAB1... Joystick A, Button 1
JAB2... Joystick A, Button 2
JBB1... Joystick B, Button 1
JBB2... Joystick B, Button 2

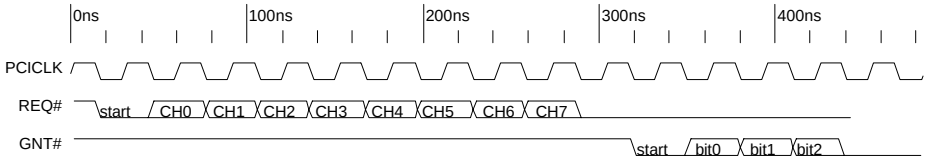
3. DMA Emulation Protocol

The former synthesizer LSI for the ISA bus such as the Sound Blaster used the DMA controller (8237: ISA DMAC) on the system to transfer the sound data from/to the host.
For DS-1E, however, ISA DMAC must be used to transfer the sound data to the Sound Blaster Pro Block of the Legacy Audio Block.
Because signals to connect to the ISA DMAC are generally not available on the PCI bus, there are two ways proposed from the industry to emulate the ISA DMAC on the PCI bus. One is PC/PCI and the other is D-DMA.
DS-1E supports both protocols for transferring SB Pro sound data on the PCI bus.

3-1. PC/PCI

DS-1E provides two signals, PCREQ# and PCGNT# to realize the PC/PCI. The format of the signals is shown below. DS-1E asserts PCREQ# and sets PCREQ# to "HIGH" using the PCICLK corresponding to the DMA channel it is going to use.

In addition, DS-1E determines whether the next PCI I/O cycle is its own from the channel information that is encoded in PCGNT#.



PCGNT# is encoded as follows.

GNT# Encoding			
bit2	**bit1**	**bit0**	GNT# Bits
0	**0**	**0**	DMA Channel 0
0	**0**	**1**	DMA Channel 1
0	**1**	**0**	DMA Channel 2
0	**1**	**1**	DMA Channel 3
1	**0**	**0**	Reserved
1	**0**	**1**	DMA Channel 5
1	**1**	**0**	DMA Channel 6
1	**1**	**1**	DMA Channel 7

DS-1E supports only 8-bit DMA channels (DMA Channel 0-3). It also only supports Single DMA transfer.

3-2. D-DMA

DS-1E provides the following registers to support D-DMA. D-DMA Slave Configuration Register (4C-4Dh) of the PCI Configuration register is used to set the Base address of the Slave Address.

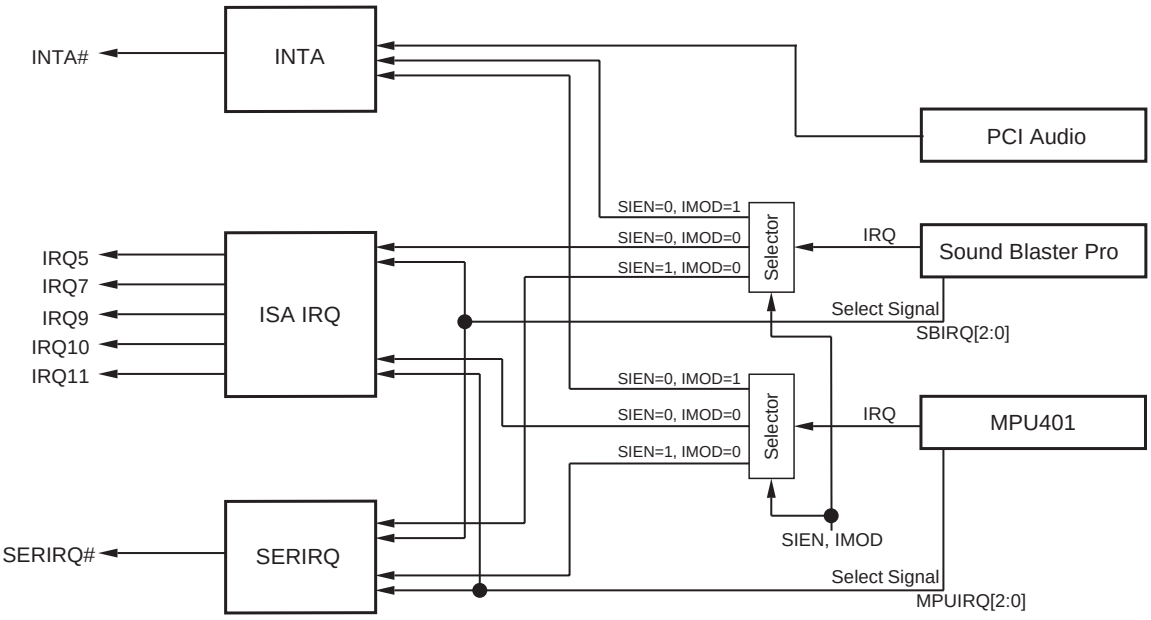
Slave Address	R/W	Register Name
Base + 0h	W	Base Address 0-7
Base + 0h	R	Current Address 0-7
Base + 1h	W	Base Address 8-15
Base + 1h	R	Current Address 8-15
Base + 2h	W	Base Address 16-23
Base + 2h	R	Current Address 16-23
Base + 3h	W	Base Address 24-31
Base + 3h	R	Current Address 24-31
Base + 4h	W	Base Word Count 0-7
Base + 4h	R	Current Word Count 0-7
Base + 5h	W	Base Word Count 8-15
Base + 5h	R	Current Word Count 8-15
Base + 6h	W	Base Word Count 16-23
Base + 6h	R	Current Word Count 16-23
Base + 7h	N/A	Reserved
Base + 8h	W	Command
Base + 8h	R	Status
Base + 9h	W	Request
Base + Ah	N/A	Reserved
Base + Bh	W	Mode
Base + Ch	W	Reserved
Base + Dh	W	Master Clear
Base + Eh	N/A	Reserved
Base + Fh	R/W	Multi-Channel Mask

These registers can be accessed by 8-bit or 16-bit bus width.

DS-1E supports 8-bit DMA transfer only.

4. Interrupt Routing

DS-1E supports three types of interrupts, interrupt signal on the PCI bus (INTA#), interrupt signal on the ISA bus (IRQ[5,7,9,10,11]), and Serialized IRQ.
The IRQs on DS-1E are routed as shown below.



PCI Audio can only use INTA#, but the Sound Blaster Pro and MPU401 blocks of the Legacy Audio Block can use any of the three protocols.
The protocol can be switched using 40-43h (Legacy Audio Control Register) of the PCI Configuration Register.

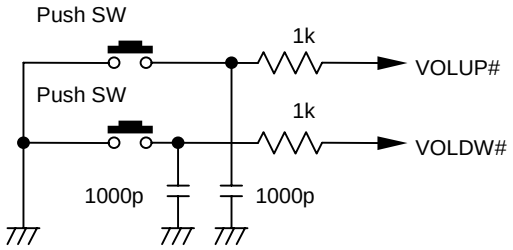
4-1. Serialized IRQ

Serialized IRQ is a method to encode IRQs of 15 channels into one signal.

DS-1E provides the SERIRQ# pin to support Serialized IRQ.
Only one channel out of the 5 channels, IRQ5, IRQ7, IRQ9, IRQ10, and IRQ11, can be encoded into the IRQ/Data frame of Serialized IRQ.
The IRQ channel is selected using 40h-43h (Legacy Audio Control Register) of the PCI Configuration Register.

5. Hardware Volume Control

The hardware volume control determines the AC'97 master volume without using any software control using the external circuit listed below.
Two pins, VOLUP# for increasing the volume and VOLDW# for decreasing the volume, are used.



DS-1E provides a shadow register for the AC'97 master volume. When the software accesses the AC'97 master volume, it is always reflected in the shadow register.
Bringing the VOLUP# pin LOW level increments the left and right-channel shadow register by +1.5dB respectively. If either one of channel shadow registers have been already set to maximum value (00000b), the corresponding channel shadow register remains in the same value, and the other channel shadow register will only be incremented. If both of channel shadow registers have been already set to maximum values, they remain in the same values.
Bringing the VOLDW# pin LOW level decrements the left and right-channel shadow register by -1.5dB respectively. If either one of channel shadow registers have been already set to minimum value (11111b), the corresponding channel shadow register remains in the same value, and the other channel shadow register will only be decremented. If both of channel shadow registers have been already set to minimum values, they remain in the same values.
The master volume for the AC'97 is updated automatically via the AC-Link by setting corresponding values to the shadow registers.
When both of the VOLUP# and VOLDW# pins are at LOW level at the same time, the MUTE bit of the shadow register is enabled to automatically set the MUTE bit of the AC'97 master volume via the AC-Link.
When either one of the VOLUP# or VOLDW# pins is at LOW level, mute condition of the AC'97 is deactivated via the AC-Link. At this point of time, the master volume is set to the value before the mute.
When the AC-Link is busy (in case the register is controlled by the AC'97 Control Register), shadow register values will be set to the AC'97 on the next frame. At this time, BUSY is set at the AC'97 control register.

When the master volume is changed or muted depending on the logic level transition status of the VOLUP# and VOLDW# pins, an interrupt is generated at the host. The interrupt is used to notify the driver that the master volume has been changed.

When the AC'97 is not connected or it is placed in power down mode, the shadow register values will remain in the same even if the VOLDW# and VOLUP# pins are at LOW level.

6. Digital Audio Interface

DS-1E supports each system of the SPDIF input/output port compliant with the IEC958 specification.

6-1. SPDIF IN

SPDIF input sampling frequency is 32.0kHz, 44.1kHz or 48.0kHz.
In DS-1E, sampling rate of the SPDIF signal incoming from the SPDIFIN pin is converted to 48.0kHz in the frequency rate conversion stage in order to process all the signals at 48.0kHz frequency. If input sampling frequency is 48.0kHz, however, this is resampled at 96.0kHz, then decimated into 48.0kHz frequency.
DS-1E supports a direct recording function which records by input sampling rate of the SPDIFIN pin without converting to 48kHz.
The input signal applied to the SPDIFIN pin can be also provided as outputs to the SPDIFOUT pin.

The SPDIF input is used to be selected between Zoomed Video Port on YMF744B (DS-1S). However, on DS-1E, the both functions can be used at the same time.

6-2. SPDIF OUT

SPDIF output is selected from three types of data indicated below:

A : Dolby digital (AC-3) encoded data
B : Output data (to be provided to the DAC slot on the AC-link) after digital mixing
C : Input data applied to the SPDIFIN pin

When the above A and B data are supplied as outputs, output sampling frequency is fixed at 48 kHz, and when the above C data is supplied as an output, output sampling frequency is dependent on the frequency available from the SPDIFIN input pin.

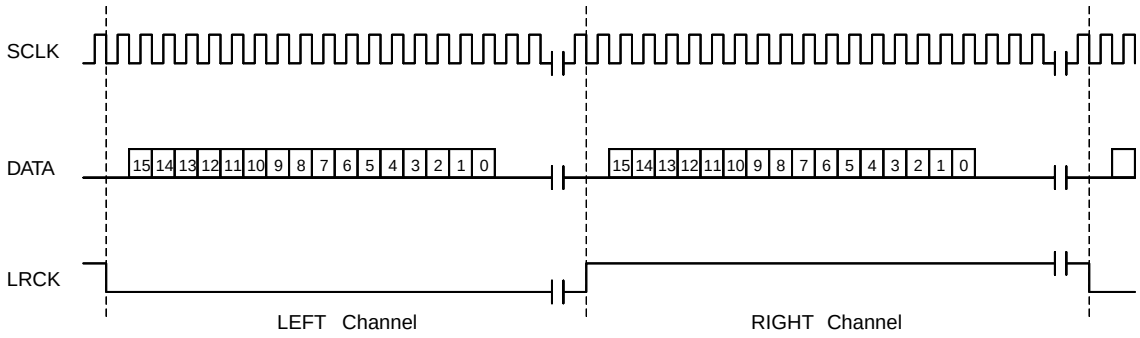
Control and category codes of the channel status are provided as sampling rate converter, copyright protection available and commercially available recorded software in accordance with the serial copy management system. Such a code arrangement allows output data to be digitally copied only to the next generation ones. When input signal to the SPDIFIN pin is provided as output, no modification is made for the channel status, etc., and output data is code-dependent available from the SPDIFIN pin.

7. Zoomed Video Port

Zoomed Video Port is defined in the PC Card Standard (PCMCIA) applicable to the notebook PC or other systems. This port is used to directly output video and/or audio signals onto the PCMCIA bus for D/A conversion process, and connect them directly to the video and/or audio signal processing chips on the PC system. Its major applications include MPEG decoder card and video capture card, etc.

Because the video and/or audio signals on the Zoomed Video Port have been output in synchronized condition, DS-1E mixes it with the other audio signals, and outputs to AC'97 or SPDIF.

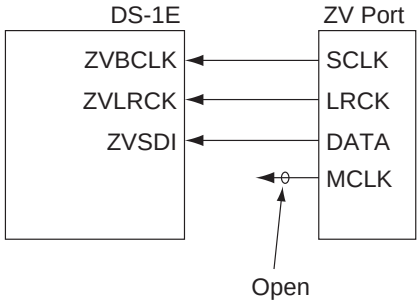
Audio signals to be transferred on the Zoomed Video Port include bit clock (SCLK), L/R clock (LRCK) and serial data (DATA), and they are provided as outputs in the format defined below. This is generally called I^2S format.



In the Zoomed Video Port, synchronization with a master clock supplied from the bus is inherently required. However, DS-1E can asynchronously process audio signal input via the Zoomed Video Port, eliminating the need for master clock.

Sampling rate of the audio signals input via the Zoomed Video Port is resampled to 96.0kHz sampling frequency at the stage followed by the SRC block, then converted to 48.0kHz sampling rate in the SRC block stage. Sampling rates to be supported on the Zoomed Video Port include 22.05kHz, 32.0kHz, 44.1kHz and 48.0kHz.

Interface connection arrangement between the DS-1E and the Zoomed Video Port is as illustrated below.



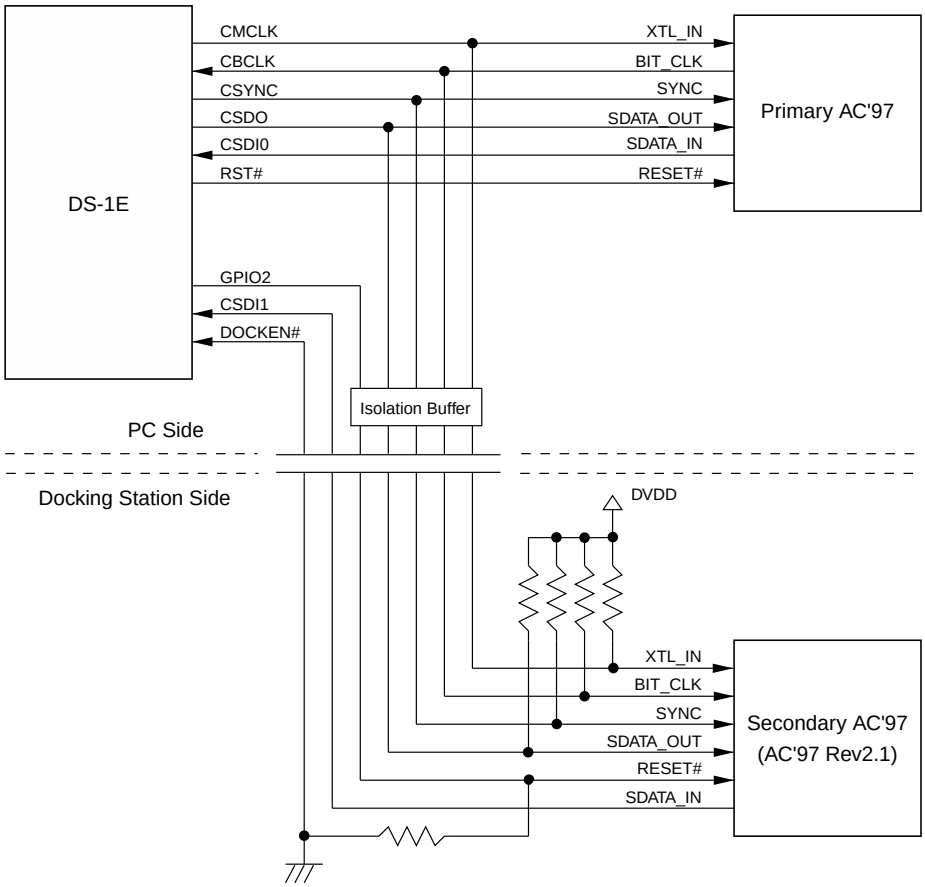
The Zoomed Video Port is used to be selected between SPDIF input on YMF744B (DS-1S). However, on DS-1E, the both functions can be used at the same time.

8. Multiple AC'97 & Multi-Channel

DS-1E allows connection with up to two AC'97s, and plays back up to 4-channel PCM data. Therefore, the following applications can be realized.

8-1. AC'97 Digital Docking

AC'97 digital docking can be realized by mounting the secondary AC'97 on the docking station side. Typical example of digital docking connection between DS-1E and AC'97s is represented in the diagram below.



When digital docking interface is made with the main side (PC side) powered on, but docking station side powered off, it may be not desirable for the secondary AC'97 that each output signal from the AC-Link is applied to the secondary AC'97 that remains in powered off state. In order to avoid such a situation, it is necessary to place an additional isolation buffer on the PC side (or docking station side).

8-2. 4-Channel Speaker System

4-channel speaker system can be realized by the connection of DS-1E with two 2-channel AC'97s as described at "8-1. AC'97 Digital Docking" or using the AC'97 that includes 4-channel D/A converters. Then, 4-channel PCM data can be played back at one time.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Power Supply Voltage (PVDD, VDD)	V_{DD3}	-0.3	4.6	V
Power Supply Voltage (CVDD, LVDD)	V_{DD2}	-0.3	3.6	V
Input Voltage	V_{IN}	-0.3	5.75	V
Operating Ambient Temperature	T_{OP}	0	70	°C
Storage Temperature	T_{STG}	-50	125	°C

Note : PVSS=VSS=LVSS=0[V]

2. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (PVDD, VDD)	V_{DD3}	3.00	3.30	3.60	V
Power Supply Voltage (CVDD, LVDD)	V_{DD2}	2.30	2.50	2.70	V
Operating Ambient Temperature	T_{OP}	0	25	70	°C

Note : PVSS=VSS=LVSS=0[V]

3. DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level Input Voltage 1	V_{IN}		-0.5	-	5.75	V
High Level Input Voltage 1	V_{IH1}	*1	$0.5V_{DD3}$	-	-	V
Low Level Input Voltage 1	V_{IL1}	*1	-	-	$0.3V_{DD3}$	V
High Level Input Voltage 2	V_{IH2}	*2	$0.7V_{DD3}$	-	-	V
Low Level Input Voltage 2	V_{IL2}	*2	-	-	$0.3V_{DD3}$	V
High Level Input Voltage 3	V_{IH3}	*3	$0.65V_{DD3}$	-	-	V
Low Level Input Voltage 3	V_{IL3}	*3	-	-	$0.35V_{DD3}$	V
High Level Input Voltage 4	V_{IH4}	*4	2.0	-	-	V
Low Level Input Voltage 4	V_{IL4}	*4	-	-	0.8	V
Input Leakage Current	I_{IL}	$0< V_{IN} < V_{DD5}$	-10	-	10	µA
High Level Output Voltage 1	V_{OH1}	*5, I_{OH1} = -0.5mA	$0.9V_{DD3}$	-	-	V
Low Level Output Voltage 1	V_{OL1}	*5, I_{OL1} = 1.5mA	-	-	$0.1V_{DD3}$	V
High Level Output Voltage 2	V_{OH2}	*6, I_{OH2} = -100µA	$0.8V_{DD3}$	-	-	V
Low Level Output Voltage 2	V_{OL2}	*6, I_{OL2} = 300µA	-	-	$0.2V_{DD3}$	V
High Level Output Voltage 3	V_{OH3}	*7, I_{OH3} = -2.0mA	$0.9V_{DD3}$	-	-	V
Low Level Output Voltage 3	V_{OL3}	*7, I_{OL3} = 6.0mA	-	-	$0.1V_{DD3}$	V
High Level Output Voltage 4	V_{OH4}	*8, I_{OH4} = -0.5mA	2.4	-	-	V
Low Level Output Voltage 4	V_{OL4}	*8, I_{OL4} = 1.5mA	-	-	0.4	V
High Level Output Voltage 5	V_{OH5}	*9, I_{OH5} = -1.5mA	2.4	-	-	V
Low Level Output Voltage 5	V_{OL5}	*9, I_{OL5} = 4.5mA	-	-	0.4	V
Input Pin Capacitance	C_{IN}		5	-	15	pF
Clock Pin Capacitance	C_{CLK}		5	-	15	pF
IDSEL Pin Capacitance	C_{IDSEL}		5	-	15	pF
Output Leakage Current	I_{OL}		-10	-	10	µA
Power Supply Current		Normal	-	75	100	mA
		Power Save (*10)	-	TBD	TBD	mA

Note : Top = 0~70°C, PVDD=3.3±0.3[V], VDD=3.3±0.3[V], CVDD=2.5±0.2[V], LVDD=2.5±0.2[V]

*1: Applicable to all PCI Iuput/Output pins and Iunput pins.

*2: Applicable to XI24 pin.

*3: Applicable to CBCLK, CSDI0 and CSDI1 pins.

*4: Applicable to ZVBCLK, ZVLRCK, ZVSDI, GP[7:4], RXD, VOLUP#, VOLDW#, GPIO[2:0], DOCKEN#, ROMDI, SPDIFIN and TEST# pins.

*5: Applicable to all PCI Input/Output pins and output pins.

*6: Applicable to XO24 pin.

*7: Applicable to CRST#, CSYNC, CSDO and CMCLK pins.

*8: Applicable to SPDIFOUT, ROMSK, ROMDO, ROMCS, GPIO[2:0] and TXD pins.

*9: Applicable to IRQ5, IRQ7, IRQ9, IRQ10 and IRQ11 pins.

*10: All DS-1E Power Control bits are set to “1”.

4. AC Characteristics

4-1. Master Clock (Fig.1)

Item	Symbol	Min.	Typ.	Max.	Unit
XI24 Cycle Time	t_{XICYC}	-	40.69	-	ns
XI24 High Time	t_{XIHIGH}	13	-	24	ns
XI24 Low Time	t_{XILOW}	13	-	24	ns

Note : Top = 0-70°C, PVDD=3.3±0.3 V, VDD=3.3±0.3 V, CVDD=2.5±0.2 V, LVDD=2.5±0.2 V

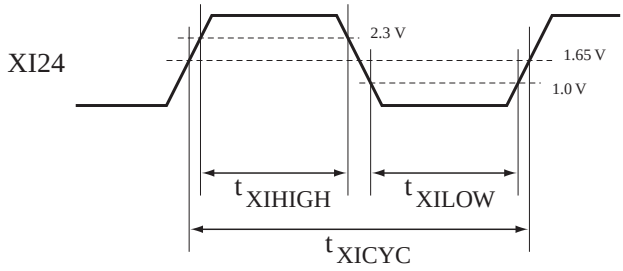


Fig.1: XI24 Master Clock timing

4-2. Reset (Fig.2)

Item	Symbol	Min.	Typ.	Max.	Unit
Reset Active Time after Power Stable	t_{RST}	1	-	-	ms
Power Stable to Reset Rising Edge	t_{RSTOFF}	10	-	-	ms
Reset Slew Rate	-	50	-	-	mV/ns

Note : Top = 0-70°C, PVDD=3.3±0.3 V, VDD=3.3±0.3 V, CVDD=2.5±0.2 V, LVDD=2.5±0.2 V, C_L=50 pF

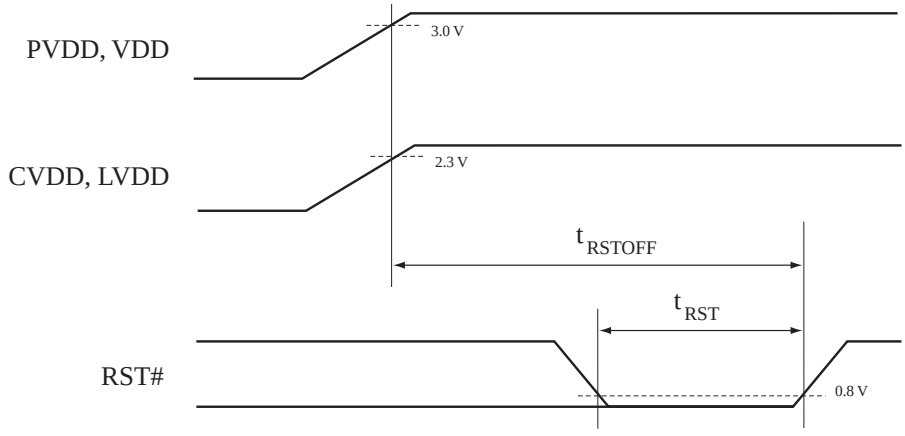


Fig.2: PCI Reset timing

4-3. PCI Interface (Fig.3, 4)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
PCICLK Cycle Time	t_{PCYC}		30	-	-	ns
PCICLK High Time	t_{PHIGH}		11	-	-	ns
PCICLK Low Time	t_{PLOW}		11	-	-	ns
PCICLK Slew Rate	-		1	-	4	V/ns
PCICLK to Signal Valid Delay	t_{PVAL}	(Bused signal)	2	-	11	ns
	$t_{PVAL(PTP)}$	(Point to Point)	2	-	12	ns
Float to Active Delay	t_{PON}		2	-	-	ns
Active to Float Delay	t_{POFF}		-	-	28	ns
Input Setup Time to PCICLK	t_{PSU}	(Bused signal)	7	-	-	ns
	$t_{PSU(PTP)}$	*11 (Point to Point)	10	-	-	ns
		*12 (Point to Point)	12	-	-	ns
Input Hold Time for PCICLK	t_{PH}		0	-	-	ns

Note : Top = 0-70°C, PVDD=3.3±0.3 V, VDD=3.3±0.3 V, CVDD=2.5±0.2 V, LVDD=2.5±0.2 V, C_L=10 pF

*11: This characteristic is applicable to REQ# and PCREQ# signal.

*12: This characteristic is applicable to GNT# and PCGNT# signal.

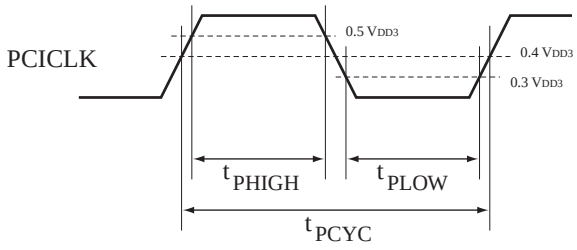


Fig.3: PCI Clock timing

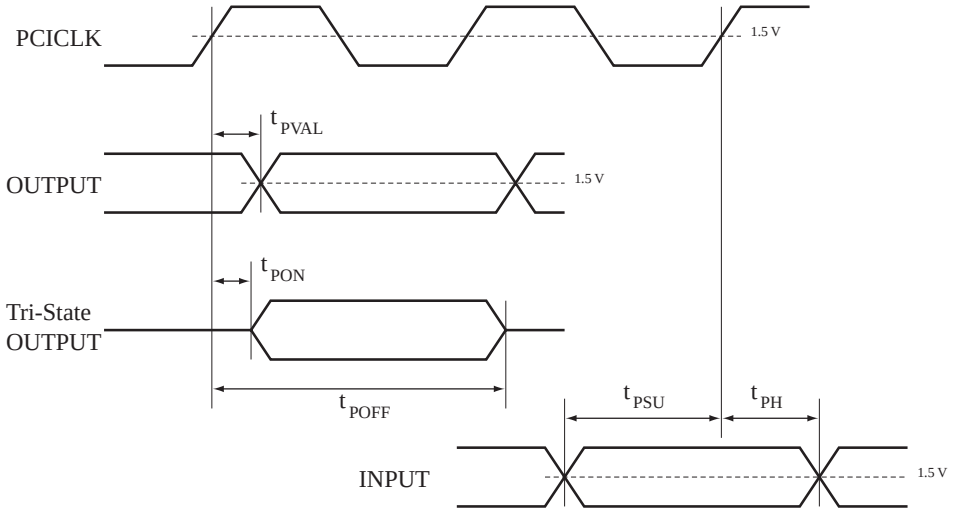


Fig.4: PCI Bus Signals timing

4-4. AC'97 Master Clock (Fig.5)

Item	Symbol	Min.	Typ.	Max.	Unit
CMCLK Cycle Time	t_{CMCYC}	-	40.69	-	ns
CMCLK High Time	t_{CMHIGH}	8	-	-	ns
CMCLK Low Time	t_{CMLOW}	8		-	ns
CMCLK Rising Time	t_{CMR}	-	4.6	-	ns
CMCLK Falling Time	t_{CMF}	-	2.1	-	ns

Note : Top = 0-70°C, PVDD=3.3±0.3 V, VDD=3.3±0.3 V, CVDD=2.5±0.2 V, LVDD=2.5±0.2 V, C_L=50 pF

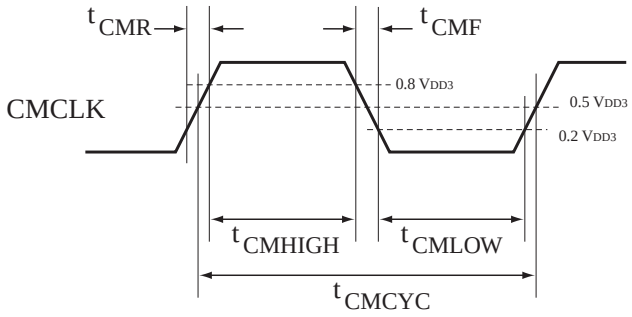


Fig.5: Master Clock timing for AC'97

4-5. AC-link (Fig.6)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CBCLK Cycle Time	t_{CBICYC}		-	81.4	-	ns
CBCLK High Time	$t_{CBIHIGH}$		35	40.7	45	ns
CBCLK Low Time	t_{CBILOW}		35	40.7	45	ns
CSYNC Cycle Time	t_{CSYCYC}		-	20.8	-	µs
CSYNC High Time	$t_{CSYHIGH}$		-	1.3	-	µs
CSYNC Low Time	t_{CSYLOW}		-	19.5	-	µs
CBCLK to Signal Valid Delay	t_{CVAL}	*13	-	-	20	ns
Output Hold Time for CBCLK	t_{COH}	*13	0	-	-	ns
Input Setup Time to CBCLK	t_{CISU}	*14	15	-	-	ns
Input Hold Time for CBCLK	t_{CIH}	*14	5	-	-	ns
Warm Reset Width			-	1.3	-	µs

Note) Top = 0-70°C, PVDD=3.3±0.3 V, VDD=3.3±0.3 V, CVDD=2.5±0.2 V, LVDD=2.5±0.2 V, C_L=50 pF

*13: This characteristic is applicable to CSYNC and CSDO signal.

*14: This characteristic is applicable to CSDI signal.

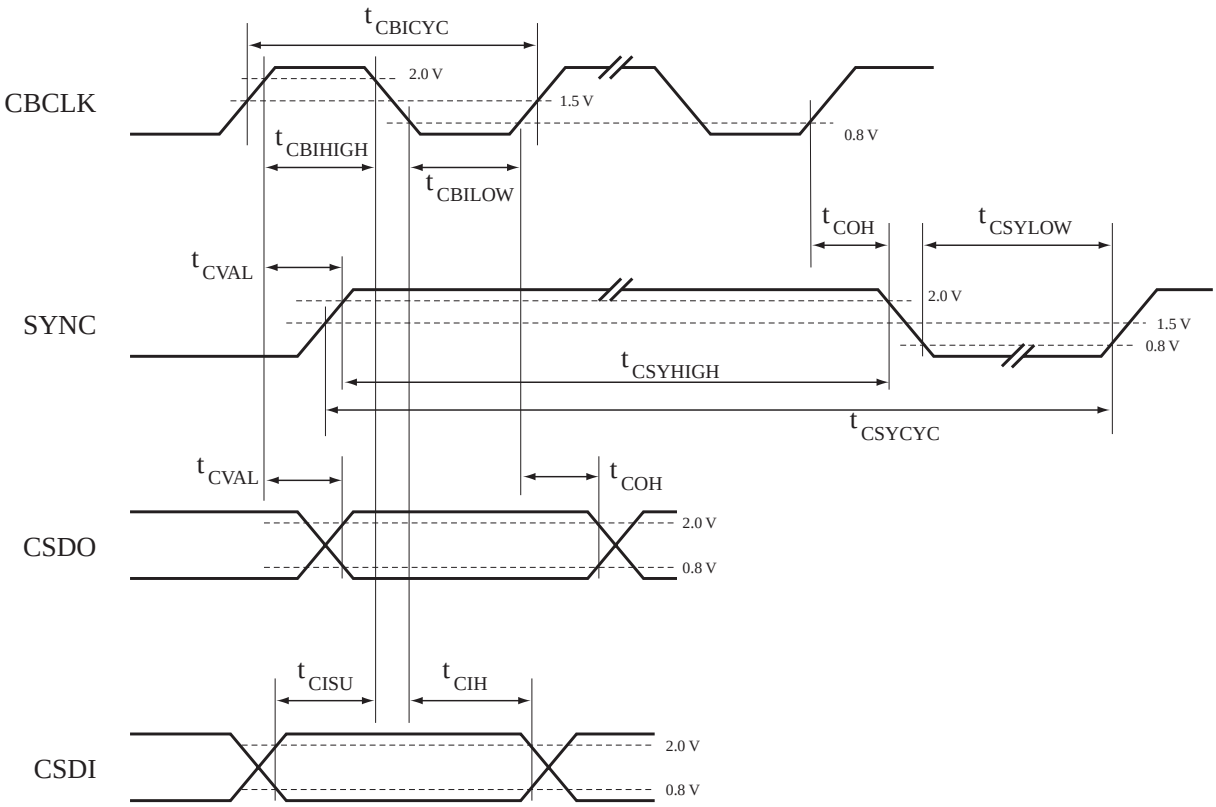


Fig.6: AC-link timing

4-6. Zoomed Video Port (Fig.7)

Item	Symbol	Min.	Typ.	Max.	Unit
ZVLRCK Delay Time	t_{SLRD}	2	-	-	ns
ZVLRCK Setup Time	t_{SLRS}	32	-	-	ns
ZVBCLK Low Time	t_{SCLKL}	22	-	-	ns
ZVBCLK High Time	t_{SCLKH}	22	-	-	ns
ZVSDI Setup Time	t_{SDS}	32	-	-	ns
ZVSDI Hold Time	t_{SDH}	2	-	-	ns

Note : Top = 0-70°C, PVDD=3.3±0.3 V, VDD=3.3±0.3 V, CVDD=2.5±0.2 V, LVDD=2.5±0.2 V, C_L=50 pF

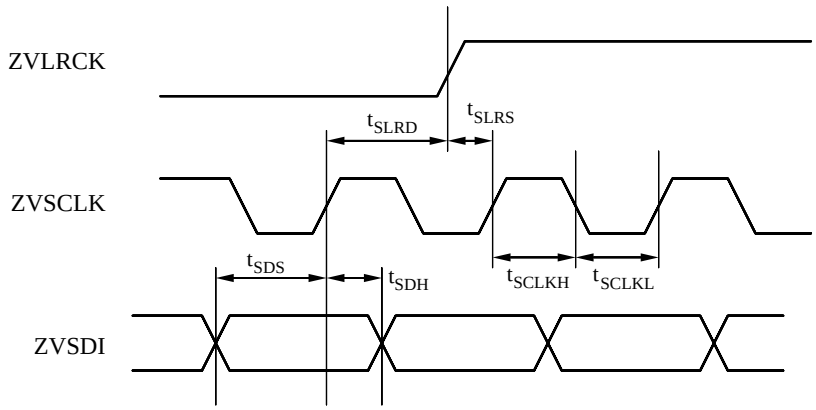
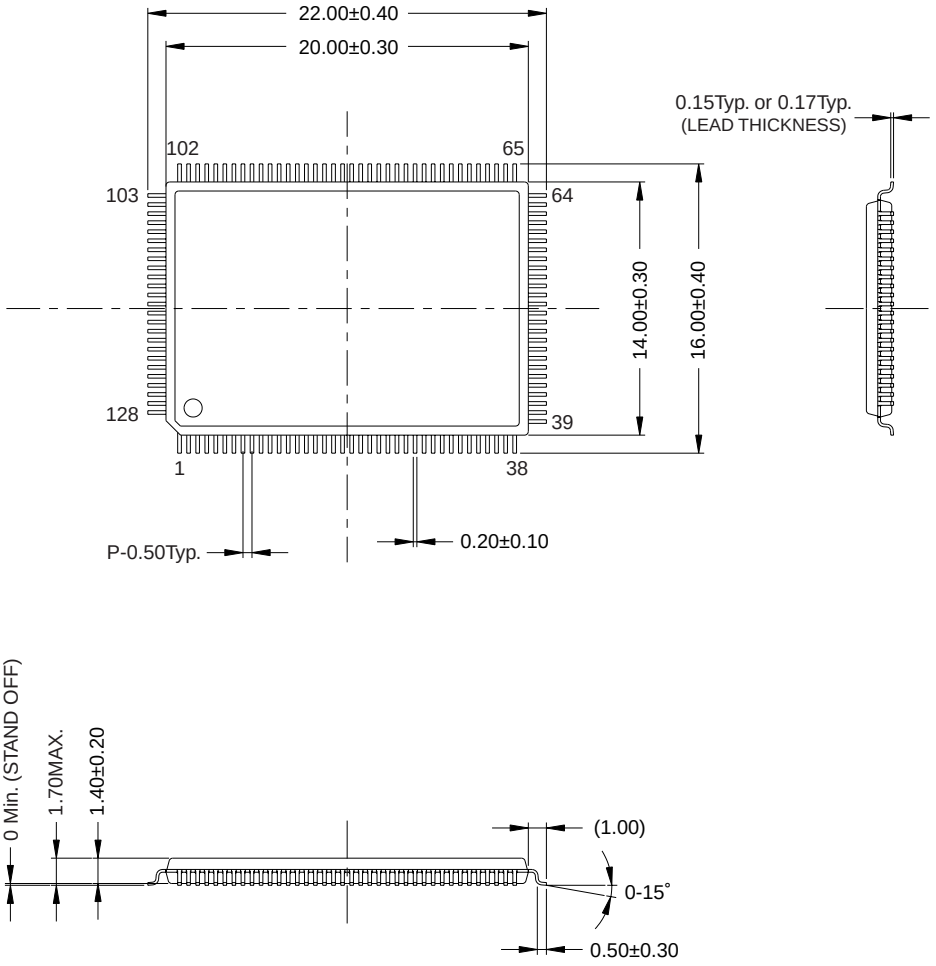


Fig.7: Zoomed Video Port timing

■ EXTERNAL DIMENSIONS

YMF754-V

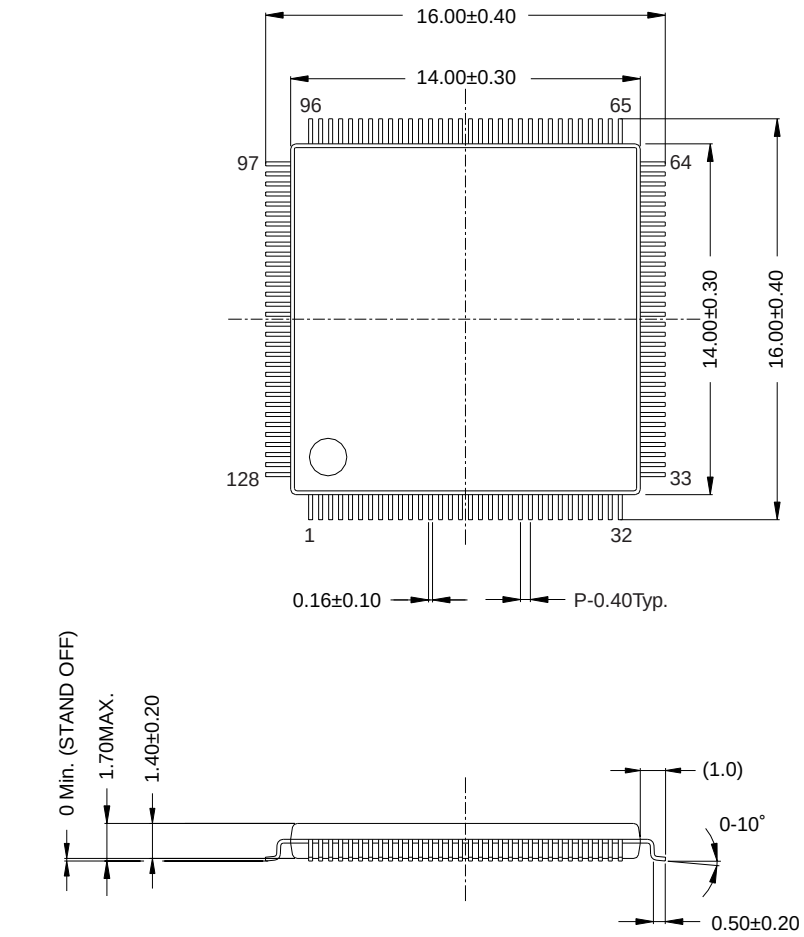


Unit : mm

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT : mm

Note : The LSIs for surface mount need especial consideration on storage and soldering conditions.
For detailed information, please contact your nearest agent of Yamaha.

YMF754-R



Unit : mm

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT : mm

Note : The LSIs for surface mount need especial consideration on storage and soldering conditions.
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