XU1004-BD

Transmitter
32.0-45.0 GHz

Rev. V1
Mimix Broadband

Features

- Sub-harmonic Transmitter
- Integrated Mixer, LO Doubler/Buffer & Output Amplifier
- +14.0 dBm Output Third Order Intercept (OIP3)
- +4.0 dBm LO Drive Level
- 5.0 dB Conversion Gain
- 100% On-Wafer RF and DC Testing
- 100% Commercial-Level Visual Inspection Using Mil-Std-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

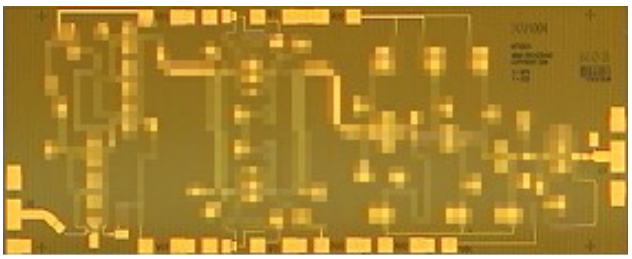
Description

M/A-COM Tech's 32.0-45.0 GHz GaAs MMIC transmitter has a +14.0 dBm output third order intercept across the band. This device is a balanced, resistive pHEMT mixer followed by a distributed output amplifier and includes an integrated LO doubler and LO buffer amplifier. The use of integrated LO doubler and LO buffer amplifier makes the provision of the LO easier than for fundamental mixers at these frequencies. IF and IF mixer inputs are provided and an external 180 degree hybrid is required to select the desired sideband. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Ordering Information

Part Number	Package
XU1004-BD-000V	Where "V" is RoHS compliant die packed in vacuum released gel paks
XU1004-BD-EV1	evaluation module

Chip Device Layout



Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage (Vd)	+6.0 VDC
Supply Current (Id1,2)	200,180 mA
Gate Bias Voltage (Vg)	+0.3 VDC
Input Power (IF Pin)	0.0 dBm
Storage Temperature (Tstg)	-65 ºC to +165 ºC
Operating Temperature (Ta)	-55 ºC to Table[1]
Channel Temperature (Tch)	MTTF Table[1]

(1) Channel temperature affects a device's MTTF. It is recommended to keep channel temperature as low as possible for maximum life.

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Electrical Specifications: 35-45 GHz (RF/Upper Side Band) (Ambient Temperature T=25°C)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (RF) Lower Side Band	GHz	32.0	-	42.0
Frequency Range (LO)	GHz	16.0	-	25.0
Frequency Range (IF)	GHz	DC	-	4.0
Input Return Loss RF (S22)	dB	-	10.0	-
Small Signal Conversion Gain RF/IF (S21)[2]	dB	-	5.0	-
LO Input Drive (P_{LO})	dBm	-	+4.0	-
Isolation LO/RF @ LOx1	dB	-	TBD	-
Isolation LO/RF @ LOx2	dB	-	TBD	-
Output Third Order Intercept (OIP3)[1,2]	dBm	-	+14.0	-
Drain Bias Voltage (Vd1,2)	VDC	-	+4.0	+5.5
Gate Bias Voltage (Vg1,2)	VDC	-1.2	-0.3	+0.1
Gate Bias Voltage (Vg3,4) Mixer, Doubler	VDC	-1.2	-0.5	+0.1
Supply Current (Id1) (Vd1=4.0 V, Vg=-0.3 V Typical)	mA	-	160	180
Supply Current (Id2) (Vd2=4.0 V, Vg=-0.3 V Typical)	mA	-	145	165

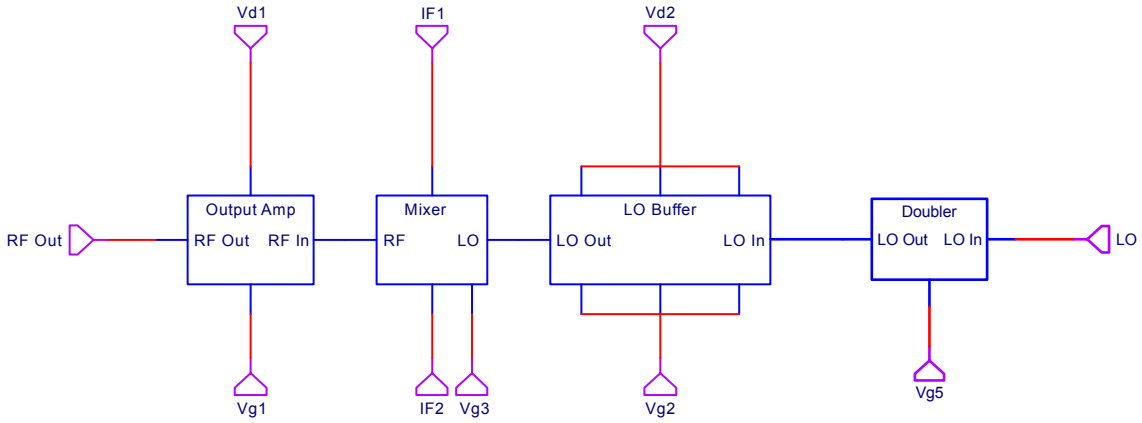
(1) Measured using constant current.
(2) Measured using LO Input drive level of 0.0.

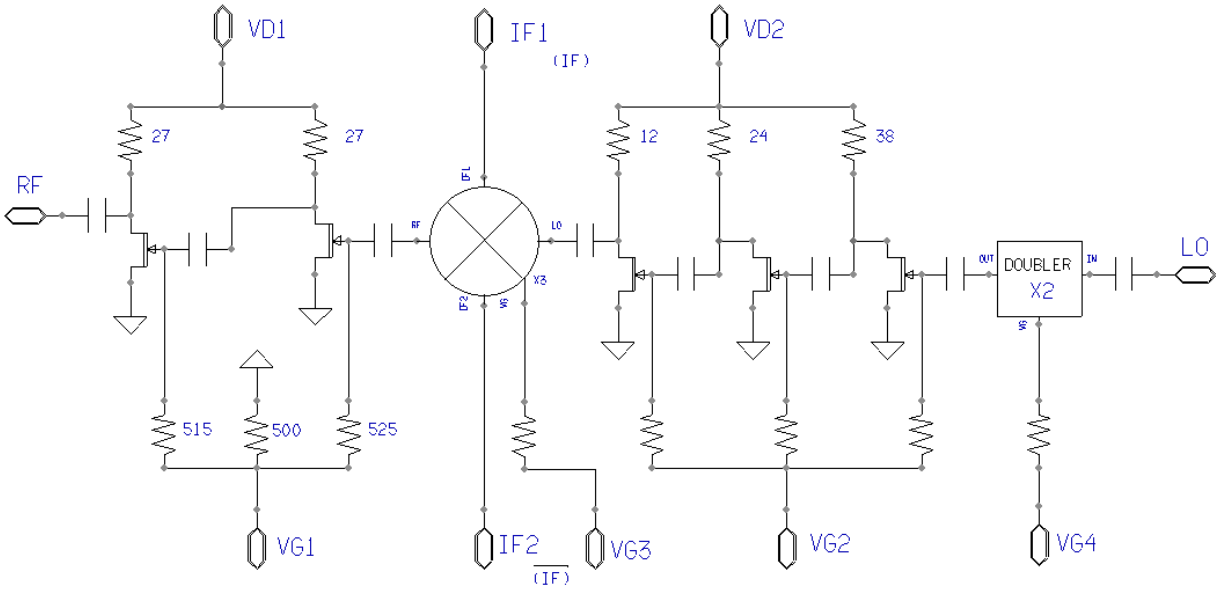
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Block Diagram & Schematics





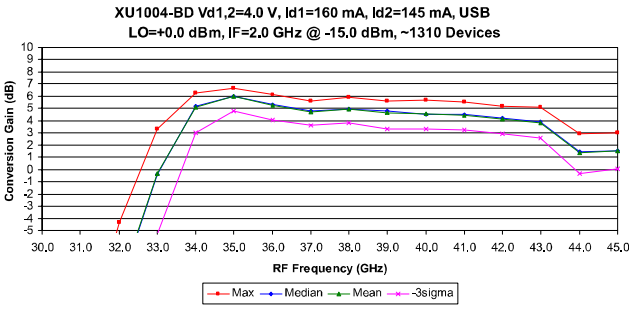
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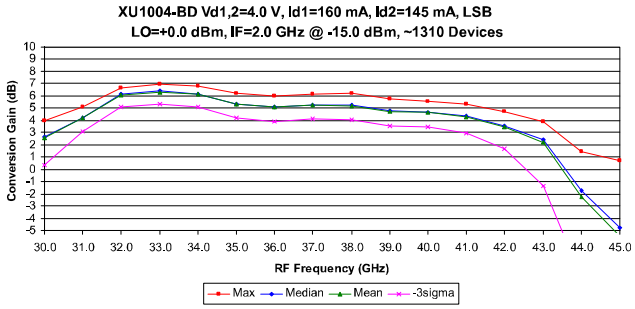
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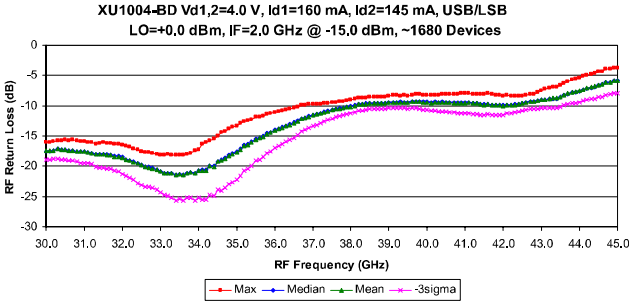
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Typical Performance Curves







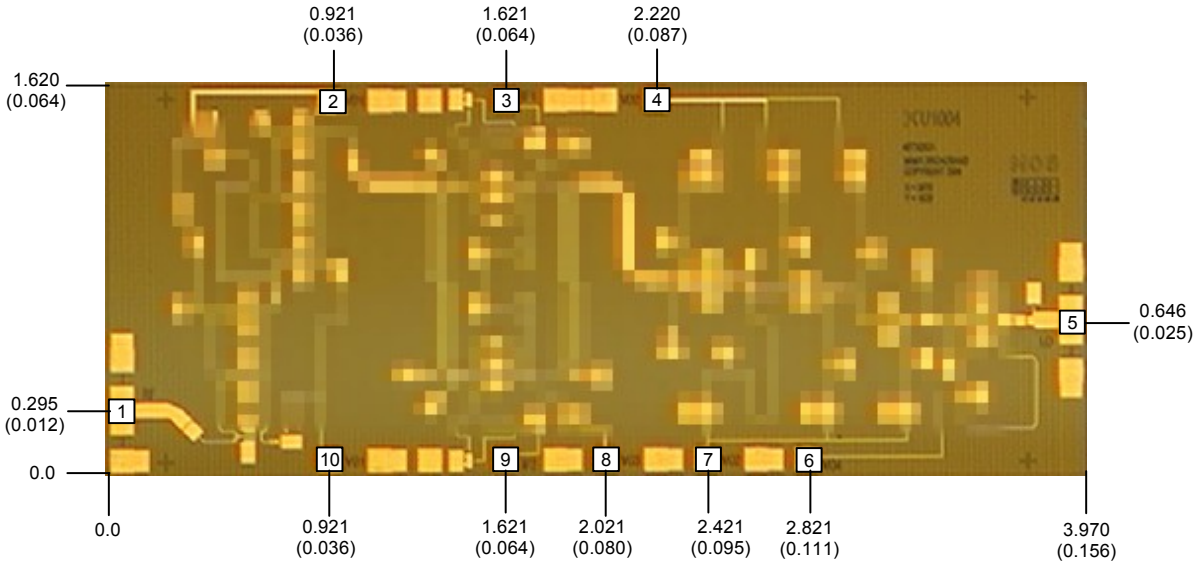
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Mechanical Drawing

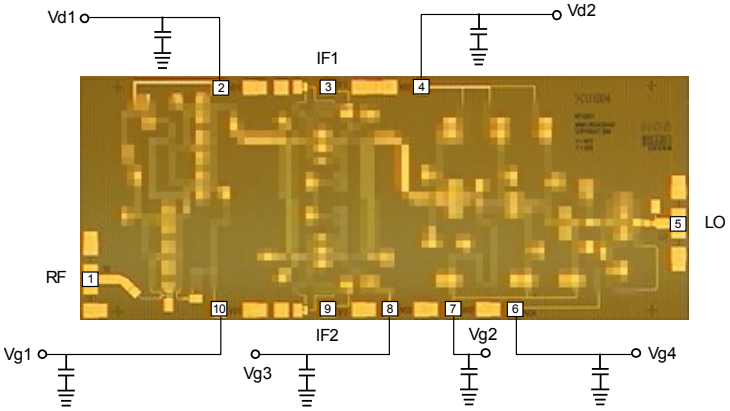


(Note: Engineering designator is 40TX0531)

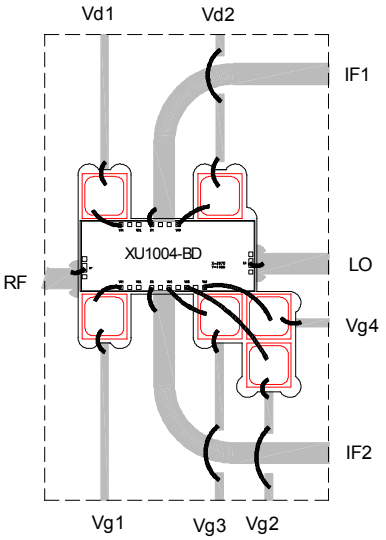
Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.013 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
All DC/IF Bond Pads are 0.100 x 0.100 (0.004 x 0.004). All RF Bond Pads are 0.100 x 0.200 (0.004 x 0.008)
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 3.987 mg.

Bond Pad #1 (RF Out)	Bond Pad #3 (IF1)	Bond Pad #5 (LO)	Bond Pad #7 (Vg2)	Bond Pad #7 (IF2)
Bond Pad #2 (Vd1)	Bond Pad #4 (Vd2)	Bond Pad #6 (Vg4)	Bond Pad #8 (Vg3)	Bond Pad #8 (Vg1)

Bias Arrangement



Bypass Capacitors - See App Note [2]



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MTTF Table (TBD)

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.

Backplate Temperature	Channel Temperature	Rth	MTTF Hours	FITs
55 deg Celsius	deg Celsius	C/W	E+	E+
75 deg Celsius	deg Celsius	C/W	E+	E+
95 deg Celsius	deg Celsius	C/W	E+	E+

Bias Conditions: Vd1=Vd2=4.0V, Id1=160 mA, Id2=145 mA

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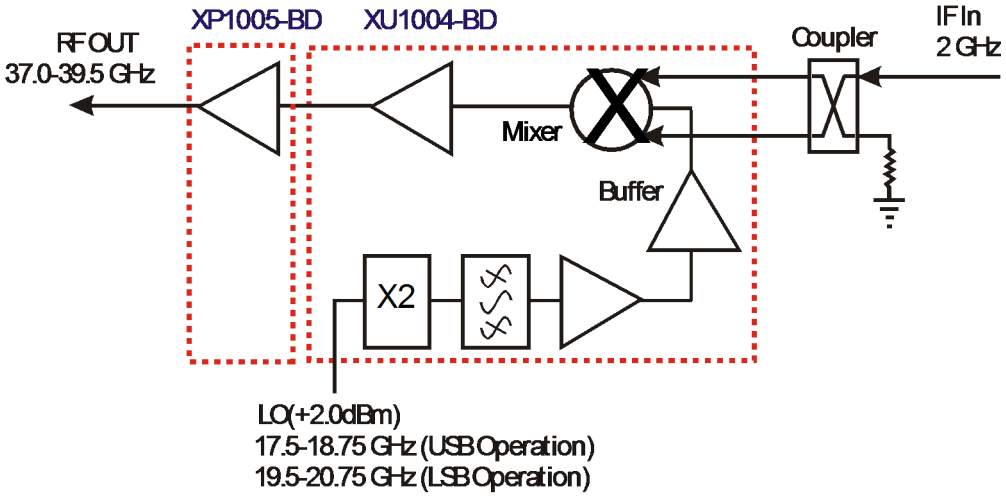
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App Note [1] Biasing - As shown in the bonding diagram, this device is operated by separately biasing Vd1 and Vd2 with Vd(1,2)=4.0V, Id1=160mA and Id2=145mA. Additionally, a mixer and doubler bias are also required with Vg3=Vg4=-0.5V. Adjusting Vg3 and Vg4 above or below this value can adversely affect conversion gain, LO/RF isolation and intercept point performance. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.3V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement -
For Parallel Stage Bias (Recommended for general applications) - The same as Individual Stage Bias but all the drain or gate pad DC bypass capacitors (~100-200 pF) can be combined. Additional DC bypass capacitance (~0.01 uF) is also recommended to all DC or combination (if gate or drains are tied together) of DC bias pads.

For Individual Stage Bias - Each DC pad (Vd1,2 and Vg1,2,3,4) needs to have DC bypass capacitance (~100-200 pF) as close to the device as possible. Additional DC bypass capacitance (~0.01 uF) is also recommended.

Typical Application



M/A-COM Tech MMIC-based 32.0-45.0 GHz Receiver Block Diagram
(Changing LO and IF frequencies as required allows design to operate as high as 45 GHz)

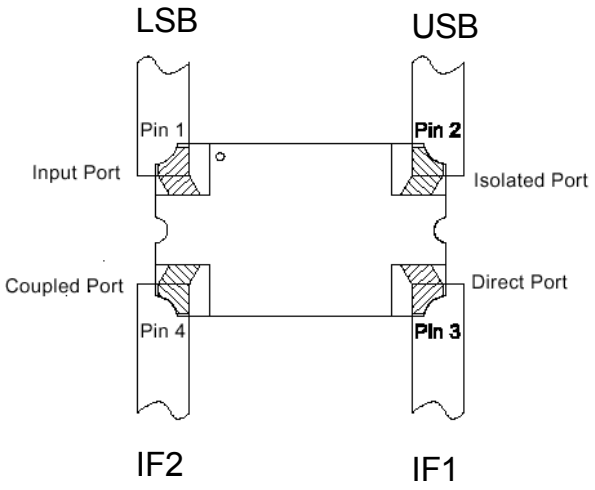
M/A-COM Tech's 32.0-45.0 GHz XU1004 GaAs MMIC Transmitter can be used in saturated radio applications and linear modulation schemes up to 128 QAM. The receiver can be used in upper and lower sideband applications from 32.0-45.0 GHz.

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App Note [3] USB/LSB Selection -



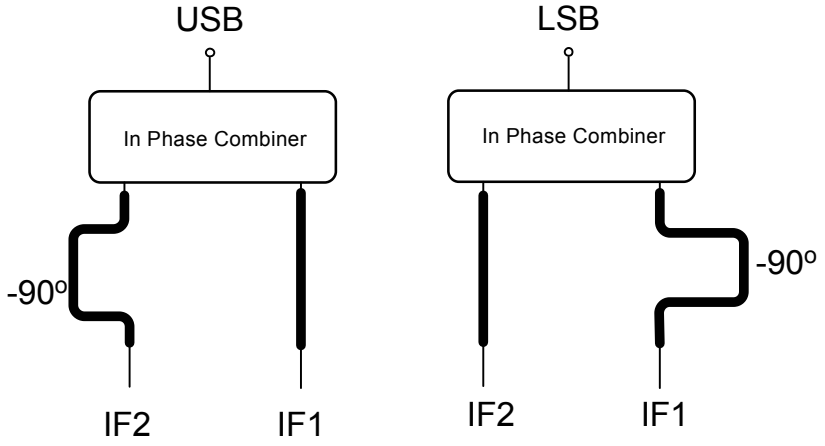
For Upper Side Band operation (USB):

With IF1 and IF2 connected to the direct port (0º) and coupled port (90º) respectively as shown in the diagram, the USB signal will reside on the isolated port. The input port must be loaded with 50 ohms.

For Lower Side Band operation (LSB):

With IF1 and IF2 connected to the direct port (0º) and coupled port (90º) respectively as shown in the diagram, the LSB signal will reside on the input port. The isolated port must be loaded with 50 ohms.

An alternate method of Selection of USB or LSB:



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Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.

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