E3/DS3/STS-1 JITTER ATTENUATOR,STS-1 TO DS3 DESYNCHRONIZER

JULY 2000 *REV. 1.01*

GENERAL DESCRIPTION

The XRT71D00 is a single channel, single chip Jitter Attenuator, that meets the Jitter requirements specified in the ETSI TBR-24, Bellcore GR-499 and GR-253 standards.

In addition, the XRT71D00 also meets the Jitter and Wander specifications described in the ANSI T1.105.03b 1997, Bellcore GR-253 and GR-499 standards for Desynchronizing and Pointer adjustments in the DS3 to STS-SPE mapping applications.

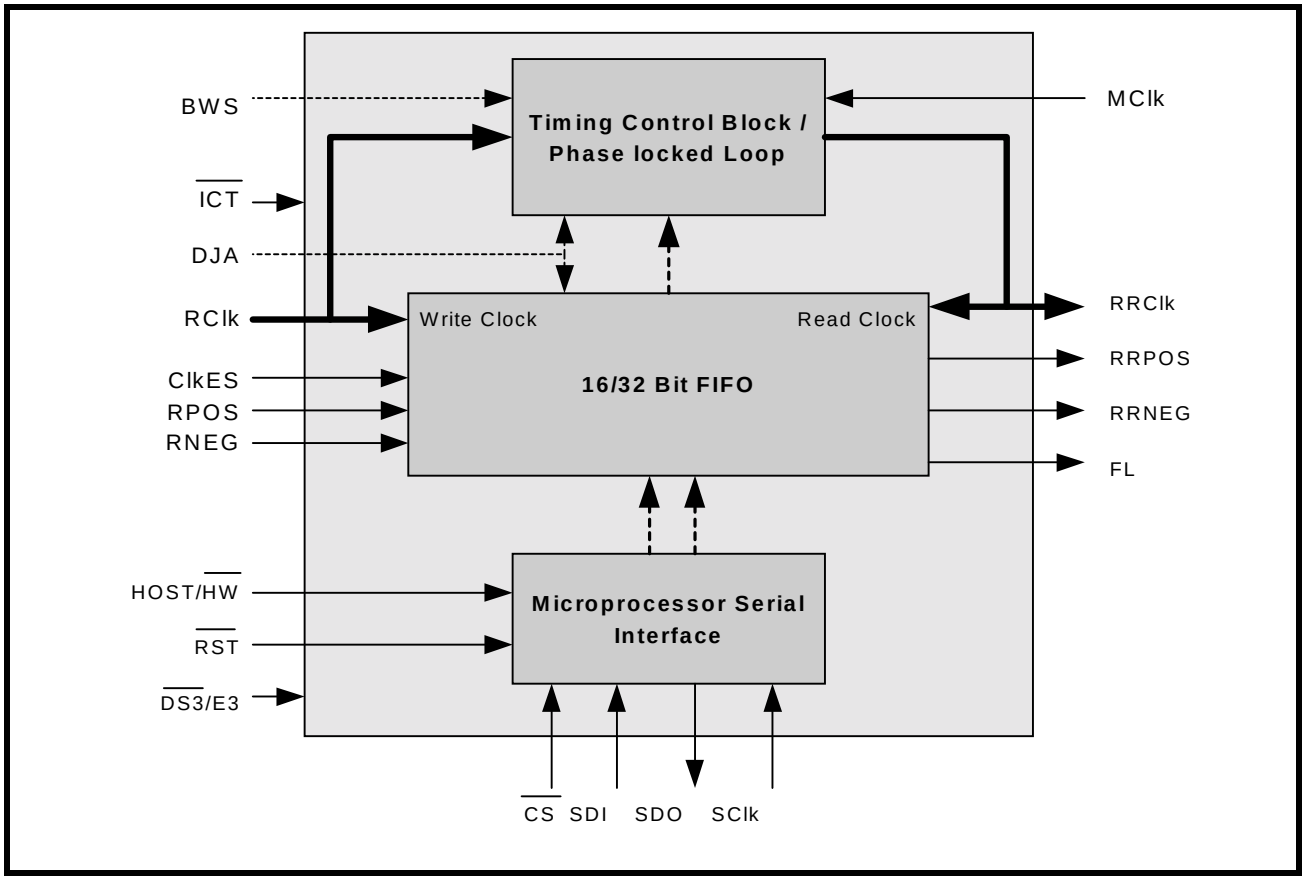
FEATURES

- Meets the E3/DS3/STS-1 jitter requirements
- No external components required
- Compliance with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- Meets output jitter requirement as specified by ETSI TBR24
- Meets the Jitter and Wander specifications described in T1.105.03b,GR-253 and GR-499 standards.
- Selectable buffer size of 16 and 32 bits
- Jitter attenuator can be disabled
- Available in a 32 pin TQFP package.
- Single 3.3V or 5.0V supply.
- Operates over - 40^0 C to 85^0 C temperature range.

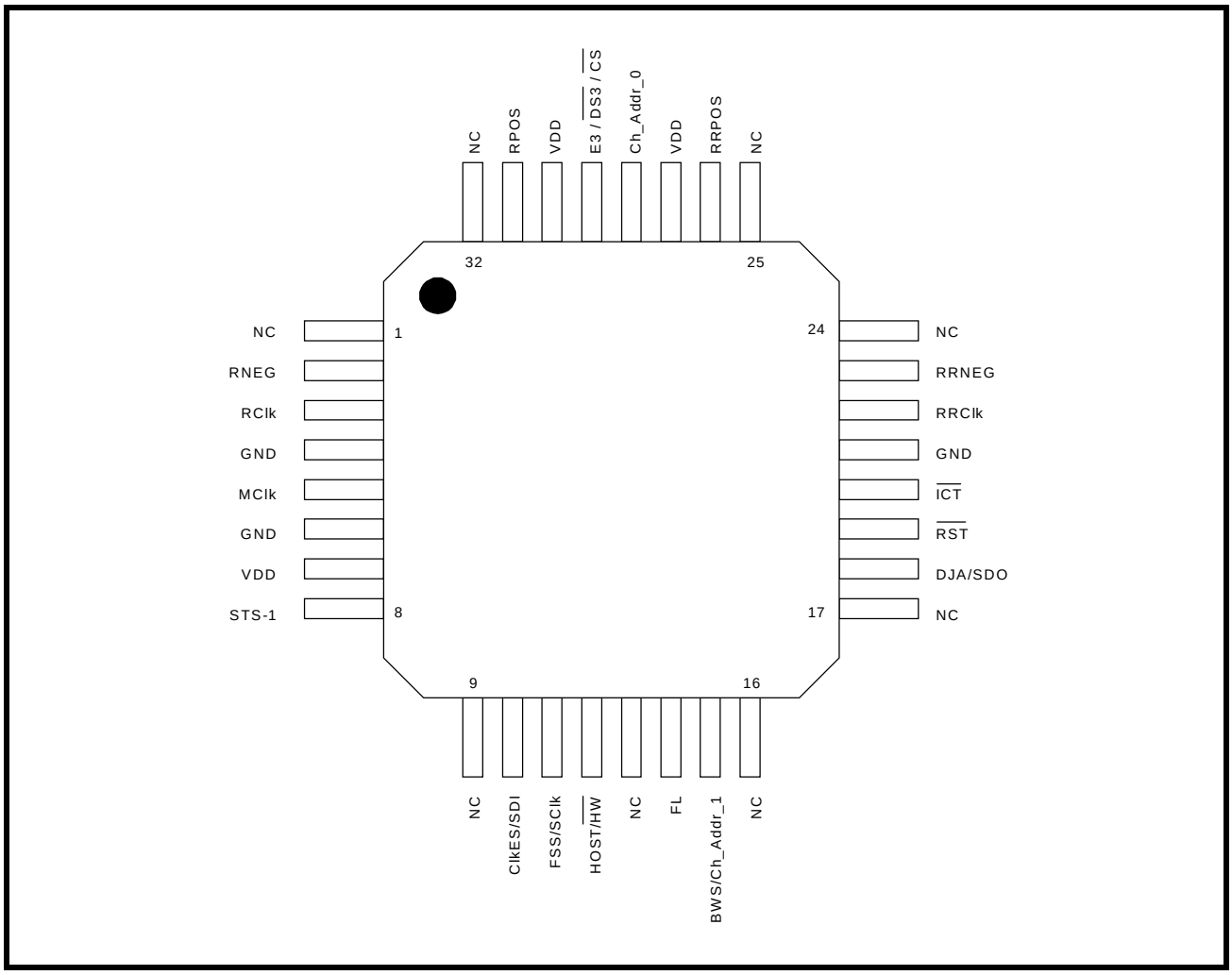
APPLICATIONS

- E3/DS3 Access Equipment.
- STS-SPE to DS3 Mapper
- DSLAMs

BLOCK DIAGRAM OF THE XRT71D00



PIN OUT OF THE XRT71D00 (32 LEAD TFQP PACKAGE)



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT71D00IQ	32 Lead TQFP	-40^0C to $+85^0$C

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PIN DESCRIPTIONS

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
1	NC	***	**This pin is not connected internally**
2	RNEG	I	**Receive Negative Data (Jittery)** The input jittery negative data is sampled either on the rising or falling edge of RClk depending on the setting of ClkES (pin 10). If ClkES is "high", then RNEG will be sampled on the falling edge of RClk. If ClkES is "low", then RPOS will be sampled on the rising edge of RClk. This pin is typically tied to the "RNEG" output pin of the LIU.
3	RClk	I	**Receive Clock (Jittery)** Clock input RClk should be connected to the recovered clock.
4	GND	***	Digital Ground
5	MClk	I	**Master Clock Input.** Reference clock for internal PLL. 44.736MHz+/-20ppm or 34.368MHz+/-20ppm. This clock must be continuous and jitter free with duty cycle between 30 to 70%. ***NOTE:*** *It is permissible to use the EXClk signal orSTS-1 clock.*
6	GND	***	Analog Ground
7	VDD	***	**Analog Positive Supply**: 3.3V or 5.0V ± 5%
8	STS-1	I	**SONET STS-1 Mode Select:** This pin along with the E3/DS3* select pin (pin 29) configures the XRT71D00 either in E3, DS3 or STS-1 mode. A table relating to the setting of the pins is given below: **STS-1 / E3/DS3* / XRT71D00 Operating Mode** 0 / 0 / DS3 (44.736 MHz) 0 / 1 / E3 (34.368 MHz) 1 / 0 / STS-1 (51.84 MHz) 1 / 1 / E3 (34.368 MHz) ***NOTES:*** *1. This input pin is active only in the Hardware Mode* *2. Internal 50 K Ohm pull-up resistor.*
9	NC	***	**This pin is not connected internally**
10	ClkES/(SDI)	I	**Clock Edge Select Input/Serial Data Input Pin.** The function of this pin depends on whether XRT71D00 is configured in Harware or Host Mode. **Hardware Mode—**Clock Edge Select Input The status of this pin determines the sampling edge on RClk to RPOS/ RNEG and RRPOS/RRNEG data update on RRClk edge. When high: **RPOS/RNEG** is sampled on falling edge of **RClk** and **RRPOS/RRNEG** is updated on rising edge of **RRClk**. When low: **RPOS/RNEG** is sampled on rising edge of **RClk** and **RRPOS/RRNEG** is updated on falling edge of **RRClk**. **Host Mode—**Serial Data Input The address value (of the command registers) or the data value is either Read or Written through this pin. The input data will be sampled on the rising edge of the SClk pin (pin 11).

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
11	FSS/(SClk)	I	**FIFO Size Select Input/Serial Clock Input.** The function of this depends on whether XRT71D00 is configured in Hardware or Host mode. **Hardware Mode—FIFO Size Select Input** When high: Selects 32 bits FIFO. When low: Selects 16 bits FIFO. **Host Mode—Microprocessor Serial Interface Clock Signal** This signal will be used to (1) sample the data, on the SDI pin, on the rising edge of this signal. Additionally, during "Read" operations, the Microprocessor Serial Interface will update the SDO output on the falling edge of this signal.
12	HOST/$\overline{HW}$	I	**Host/Hardware Mode Select:** An active-high input enables the Host mode. Data is written to the command registers to configure the XRT71D00. In the Host mode, the states of discrete input pins are inactive. An active-low input enables the Hardware Mode.In this mode, the discrete inputs are active.
13	NC	***	**This pin is not connected internally.**
14	FL	O	**FIFO Limit.** This output pin is driven high whenever the internal FIFO comes within two-bits of being completely full.
15	BWS/ Ch_Addr_1	I	**Bandwidth Select Input/Channel Addr_1 Assignment Input.** The function of this input pin depends on whether XRT71D00 is configured in Host or Hardware mode. **Hardware Mode—Bandwidth Select Input:** Connect this pin high to select wide jitter transfer bandwidth, and connect low to select narrow jitter transfer bandwidth. **Host Mode—Channel_Addr_1 Assignment Input:** This input pin, along with pin 28 permits the user to assign a "Channel Address" to the XRT71D00 device.
16	NC	***	**This pin is not connected internally.**
17	NC	***	**This pin is not connected internally.**
18	DJA/ (SDO)	I/(O)	**Disable Jitter Attenuator Input/Serial Data Output pin:** The function of this pin depends on whether XRT71D00 is configured in Host or Hardware mode. **Hardware Mode—Disable Jitter Attenuator:** An active-high disables the Jitter Attenuator.The RPOS/RNEG and RClk will be passed through without jitter attenuation. **Host Mode—Serial Data Output:** This pin will serially output the contents of the specified Command Register, during "Read" Operations. The data, on this pin, will be updated on the falling edge of the SClk input signal. This pin will be tri-stated upon completion of data transfer. ***NOTE:*** *The user is advised to tie this pin to GND, if the XRT71D00 has been configured to operate in the "HOST" Mode.*
19	$\overline{RST}$	I	**Reset Input.** (Active-Low) A high-low transition will re-center the internal FIFO, and will clear the Command Registers (for Host Mode operation). Resetting this pin may corrupt data within the device. For normal operation, pull this pin to VDD.

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
20	$\overline{ICT}$	I	**In Circuit Testing Input.** Active low. With this pin tied to ground, all output pins will be in high impedance mode for in-circuit-testing. For normal operation this input pin should be tied to VDD.
21	GND	***	Digital Ground:
22	RRClk	O	**Receive Output (De-jittered) Clock.** Output the de-jittered or smoothed clock if the jitter attenuator is enabled. The de-jittered data, RRPOS/RRNEG are clocked to this signal. If ClkES is "low", RRPOS/RRNEG will be updated at the falling edge of RRClk. If ClkES is "high", RRPOS/RRNEG will be updated at the rising edge of RRClk.
23	RRNEG	O	**Receive Negative Data (De-Jittered) Output.** De-jittered negative data output. Updated on the rising or falling edge of RRClk, depending upon the state of the ClkES input pin (or bit-field setting).
24	NC	***	**This pin is not connected internally.**
25	NC	***	**This pin is not connected internally.**
26	RRPOS	O	**Receive Positive Data (De-Jittered) Output.** De-jittered positive data output. Updated on the rising or falling edge of RRClk (see pin 9), depending upon the state of the ClkES input pin (or bit-field setting).
27	VDD	***	**Digital Positive Supply Voltage**: 3.3V or 5.0V ± 5%
28	Ch_Addr_0	I	**Channel Addr_0 Assignment Input.** This input pin, along with pin 15 permits the user to assign a "Channel Address" to the XRT71D00.
29	E3/$\overline{DS3}$ ($\overline{CS}$)	I	**E3/DS3 Select Input/Chip Select Input:** The function of this pin depends on whether the XRT71D00 is configured in Host or Hardware mode. **Hardware Mode—E3/DS3* Select Input**: This pin along with the STS-1 mode select pin (pin 8) selects the operating mode. The following table provides the configuration: **STS-1** **E3/DS3*** **XRT71D00 Operating Mode** 0 0 DS3 (44.736 MHz) 0 1 E3 (34.368 MHz) 1 0 STS-1 (51.84 MHz) 1 1 E3 (34.368 MHz) **HOST Mode—Chip Select Input:** An active-low input enables the serial interface. (Note: This pin is internally pulled "high".)
30	VDD	***	**Digital Positive Supply Voltage**: 3.3V or 5.0V ± 5%
31	RPOS	I	**Receive Positive Data (Jittery) Input.** Data that is input on this pin is sampled on either the rising or falling edge of RClk depending on the setting of the ClkES pin (pin 10). If ClkES is "high", then RPOS will be sampled on the falling edge of RClk. If ClkES is "low", then RPOS will be sampled on the rising edge of RClk.
32	NC	***	**This pin is not connected internally.**

ELECTRICAL CHARACTERISTICS

AC Electrical Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS.
MClk	Duty Cycle	30	50	70	%
MClk	Frequency E3		34.368		MHz
MClk	Frequency DS3		44.736		MHz
MClk	Frequency STS-1		51.84		MHz
RClk	Duty Cycle	30	50	70	%
RClk	Frequency (E3,DS3 or STS-1)	-400	0	400	ppm
RClk	Rise Time				ns
RClk	Fall Time				ns
tsu	RPOS/RNEG to RClk rise time setup	5			ns
th	RPOS/RNEG to RClk rising hold time	5			ns
td	RRPOS/RRNEG delay from RRClk rising	5			ns
te	RRPOS/RRNEG delay from RRClk falling	5			ns

Microprocessor Serial Interface Timing (see Figure 6)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS.
t21	CSB Low to Rising Edge of SClk Setup Time	50			ns
t22	SClk to CSB Hold Time	20			ns
t23	SDI to Rising Edge of SClk Setup Time	50			ns
t24	SDI to Rising Edge of SClk Hold Time	50			ns
t25	SClk “Low” Time	240			ns
t26	SClk “High” Time	240			ns
t27	SClk Period	500			ns
t28	SClk to CSB Hold Time	50			ns
t29	CSB “Inactive” Time	250			ns
t30	Falling Edge of SClk to SDO Valid Time			200	ns
t31	Falling Edge of SClk to SDO Invalid Time			100	ns
t32	Falling Edge of SClk, or rising edge of CSB to High Z		100		ns

DC Electrical Characteristics (TA = 25 0C, VDD = 3.3 V ± 5 % unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	VDD	3.135	3.3	3.465	V
Input High Voltage	VIH	2.0		5.25	V
Input Low Voltage	V_{IL}	-0.5		0.8	V
Output High Voltage @ IOH=-5mA	VOH	2.4			V
Output Low Voltage @ IOL=5mA	VOL			0.4	V
Supply Current (E3)	Icc	36	40	52	mA
Supply Current (DS3)	Icc	40	41	43	mA
Supply Current (STS-1)	Icc		TBD		
Input Leakage Current(except Input pins with Pull-up resistor.	IL			± 10	µA
Input Capacitance	CI		5.0		pF
Output Load Capacitance	C_L			25	pF

DC Electrical Characteristics (TA = 25 0C, VDD = 5.0 V ± 5 % unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	VDD	4.75	5.0	5.25	V
Input High Voltage	VIH	2.0		5.25	V
Input Low Voltage	V_{IL}	-0.5		0.8	V
Output High Voltage @ IOH=-5mA	VOH	2.4			V
Output Low Voltage @ IOL=5mA	VOL			0.4	V
Supply Current (E3)	Icc	36	40	52	mA
Supply Current (DS3)	Icc	40	41	43	mA
Supply Current (STS-1)	Icc		TBD		
Input Leakage Current(except Input pins with Pull-up resistor.	IL			± 10	µA
Input Capacitance	CI		5.0		pF
Output Load Capacitance	C_L			25	pF

ABSOLUTE MAXIMUM RATINGS:

Supply Range	-0.5 V to + 6.0 V
ESD Rating	> 2000 V on all pins
Operating Temperature	-40^0C to $+85^0$C
Storage Temperature	-65°C to + 150°C

SYSTEM DESCRIPTION

The XRT71D00 is an integrated E3/DS3/STS-1 jitter attenuator that attenuates the jitter from the input clock and data.The jitter attenuation performance meets the latest specifications such as Bellcore GR-499 CORE,GR-253 CORE, ETSI TBR24,ITU-T G.751,ITU-T G.752 and ITU-T G.755 standards.

In addition, the XRT71D00 also meets both the “mapping” and “pointer adjustment” jitter generation criteria for both Category I and Category II interfaces as specified in Bellcore GR-253.

The XRT71D00 also meets the DS3 wander specification that apply to SONET and asynchronous interfaces as specified in the ANSI T1.105.03b 1997 standard.

Additionally, to support loop-timing applications, the XRT71D00 device can also be used to reduce and limit the amount of jitter in the recovered line clock signal.

Figure 1 presents a simple block diagram of the XRT71D00 device, when it is configured to operate in the “Hardware” Mode and Figure 2 presents a simple block diagram of the XRT71D00 device, when it is configured to operate in the “Host” Mode.

FIGURE 1. ILLUSTRATION OF THE XRT71D00 (CONFIGURED TO OPERATE IN THE “HARDWARE” MODE)

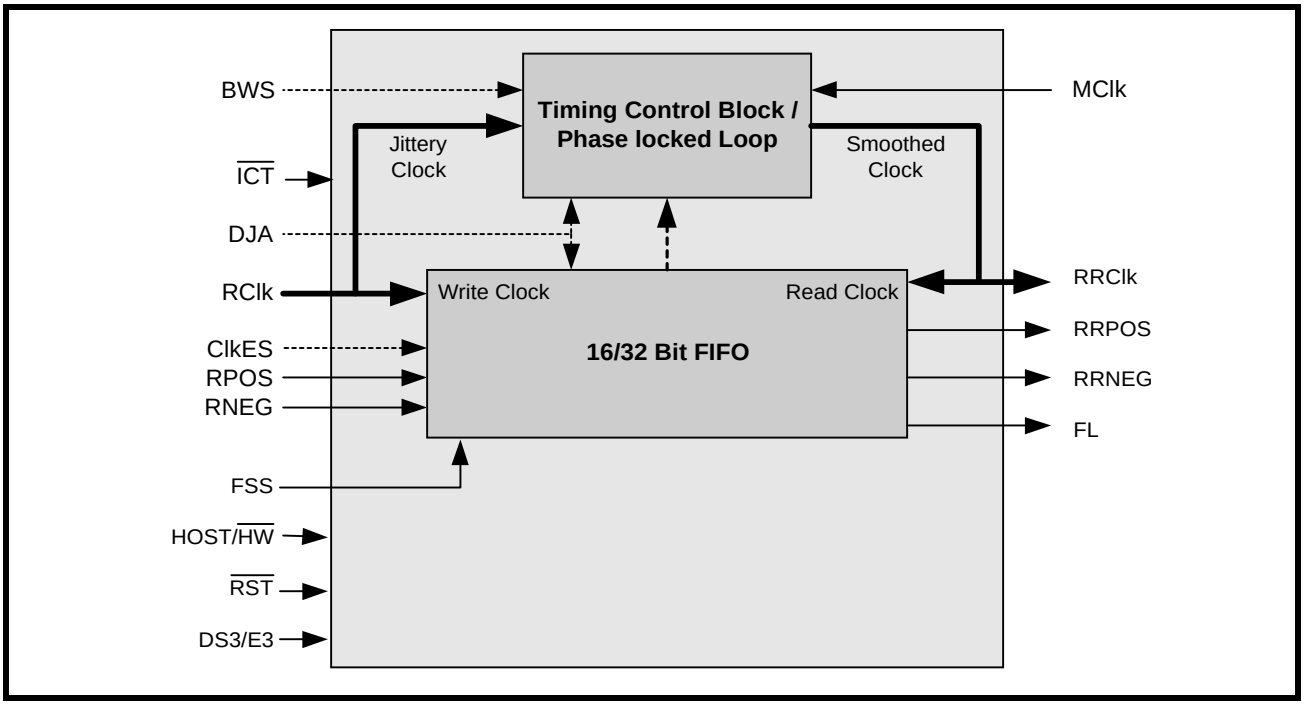
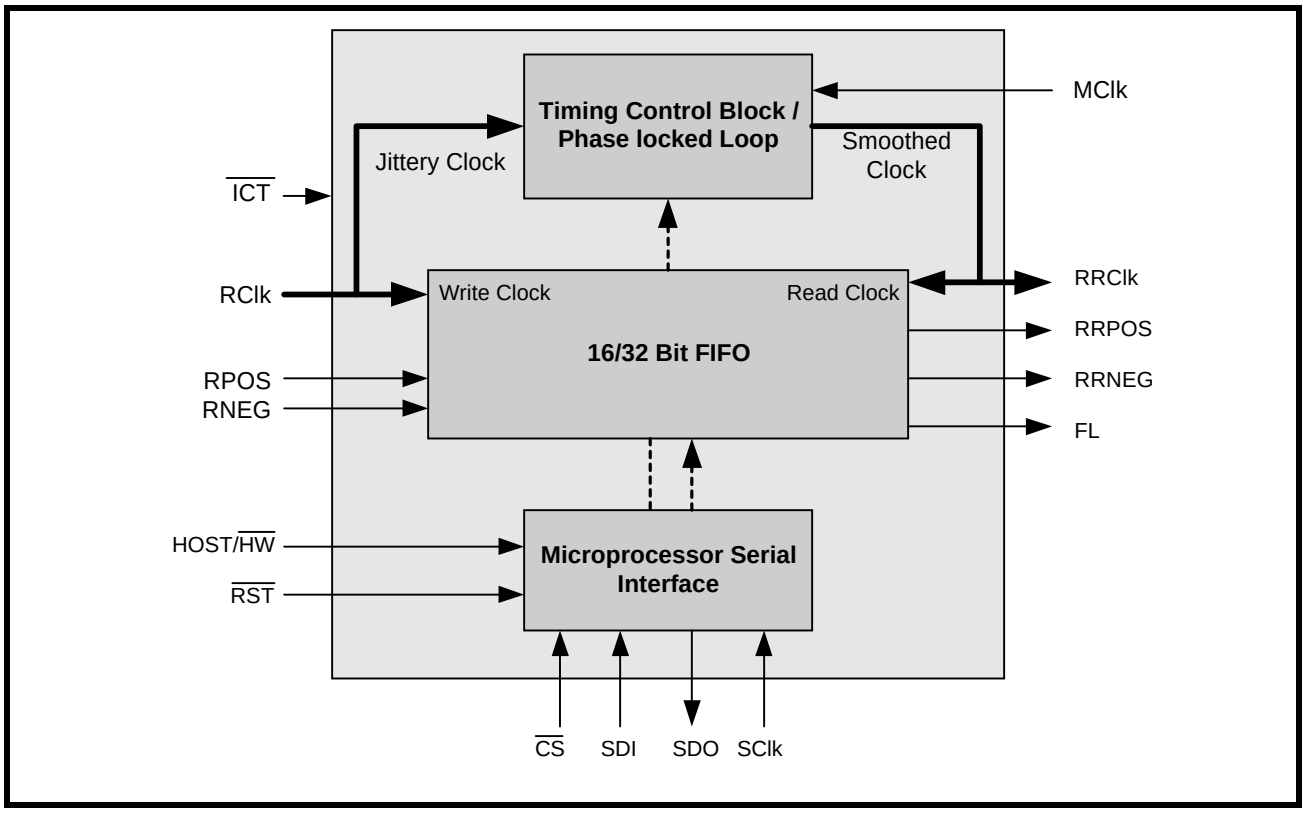


FIGURE 2. ILLUSTRATION OF THE XRT71D00(CONFIGURED TO OPERATE IN THE "HOST" MODE)



The XRT71D00 DS3/E3 Jitter Attenuator IC consists of the following functional blocks:

- Timing Control Block
- The "Jitter-Attenuator" PLL
- The "2-Channel 16/32 Bit FIFO".

BACKGROUND INFORMATION:

DEFINITION OF JITTER

One of the most important and least understood measures of clock performance is jitter. The International Telecommunication Union defines jitter as "short term variations of the significant instants of a digita signal from their ideal positions in time". Jitter can occur due to any of the following:

1) Imperfect timing recovery circuit in the system
2) Cross-talk noise
3) Inter-symbol interference/Signal Distortion

SONET STS-1 to DS3 MAPPING

SONET equipment jitter criteria are specified as:

i) Jitter Transfer

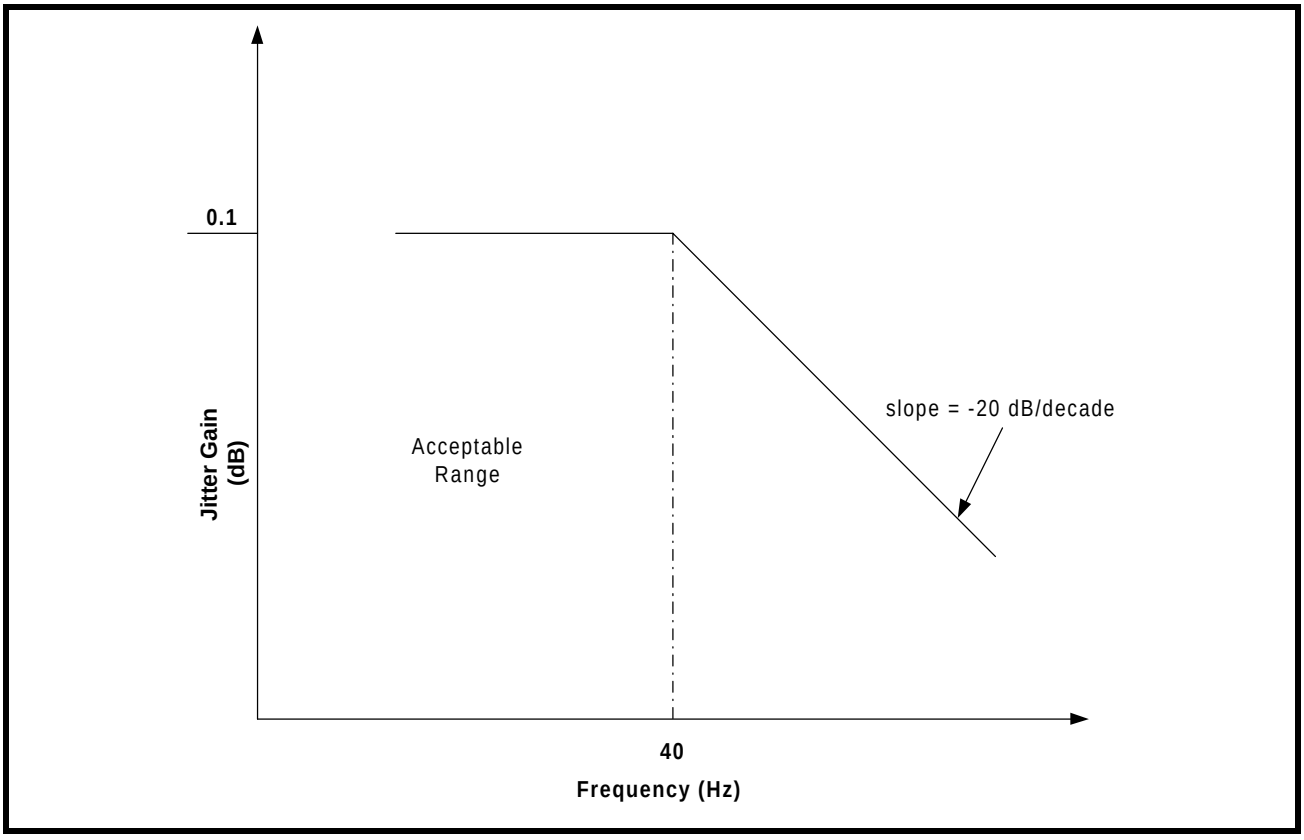
ii) Jitter Tolerance

iii) Jitter Generation

JITTER TRANSFER CHARACTERISTICS:

The primary purpose of jitter transfer requirements is to prevent performance degradations by limiting the accummulation of jitter through the system such that it does not exceed the network interface jitter requirements. Thus, it is more important that a system meet the jitter transfer criteria for relatively high input jitter amplitudes. The jitter transferred through the system must be under the jitter mask for any input jitter amplitude within the range as shown in Figure 3

FIGURE 3. CATEGORY 1 DS3 JITTER TRANSFER MASK



JITTER TOLERANCE:

The jitter tolerance in the network element is defined as the maximum amount of jitter in the incoming signal that it can receive in an “error-free”manner.

JITTER GENERATION:

Jitter generation is defined in Section 7.3.3 of GR-499-CORE. Jitter generation criteria exists for both Category I and II interfaces, which consist of “mapping” and “pointer adjustment” jitter generation.

Mapping jitter is the sum of the intrinsic payload mapping jitter and the jitter that is generated as a result of the bit stuffing mechnisms used in all of the asynchronous DSn mapping into STS SPE.

JITTER ATTENUATION:

A digital Jitter Attenuation loop combined with the FIFO provides Jitter attenuation. The Jitter Attenuator requires no external components except for the reference clock.

Data is clocked into the FIFO with the associated clock signal (TClk or RClk) and clocked out of the FIFO with the dejittered clock and data. When the FIFO is within 2 bits of being completely full, the FIFO Limit (FL) will be set.

In Figure 1 and Figure 2, this “de-jittered” clock is labeled “Smoothed Clock”. This “Smoothed Clock” is now used to “Read Out” the “Recovered Data” from the 16/32 bit FIFO. This “Smoothed Clock” will also be output to the Terminal Equipment via the “RRClk” output pin. Likewise, the “Smoothed Recovered Data” will output to the Terminal Equipment via the RRPOS and RRNEG output pins.

The XRT71D00 device is designed to work as a companion device with XRT7300 (STS-1/DS3/E3) Line Interface Unit.

.ETSI TBR24 specifies the maximum output jitter in loop timing must be no more than 0.4UIpp when measured between 100Hz to 800KHzwith upto 1.5UI input jitter at 100Hz.. This means a jitter attenuator with bandwidth less than 100Hz is required to be compliant with the standard. ITU G.751 is another application where low bandwidth jitter attenuator is needed to smooth the gapped clock output in the de-multiplexer system.

SONET STS-1 DS3 MAPPING:

Bellcore GR-253 section 3.4.2 and the ANSI T1.105-199 describes the asynchronous mapping for DS3 into STS-1 SPE.

An asynchronous mapping for DS3 into STS-1 SPE is defined for clear-channel transport of DS3 signals that meet the DSX-3 requirements in the GR-499-CORE.

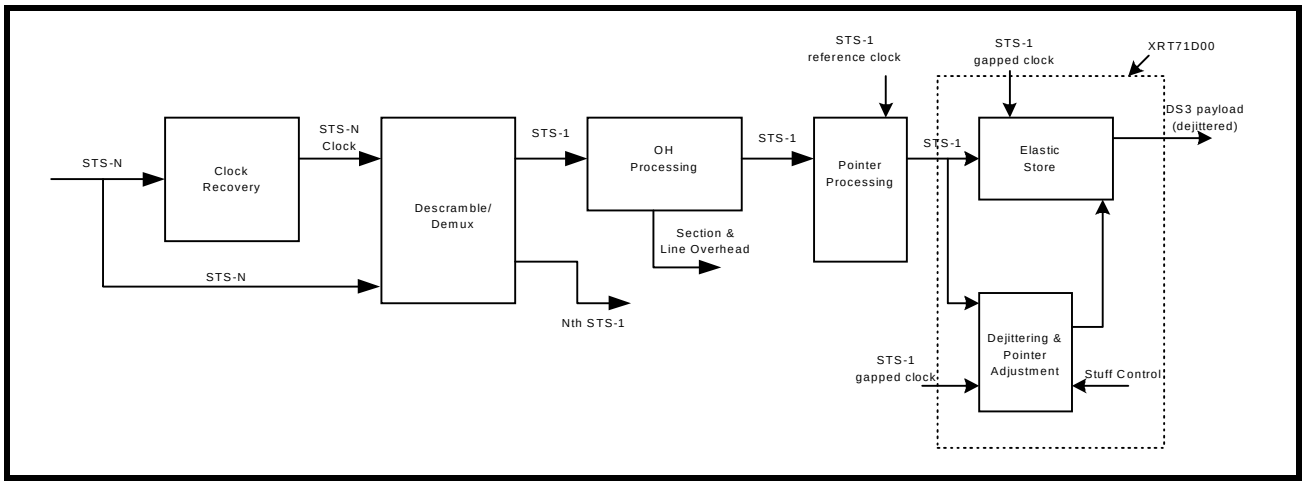
When the input data has a rate lower than the output data rate, the positive stuffing will occur. The stuffing mechanism that generates the C-bits is implemented in a desynchronizer that has the jitter output less than 0.4 UIpp assuming no jitter or wander at the input of the synchronizer and no pointer adjustments. A block diagram of the Desynchronizer is shown in Figure 4.

The elastic store accepts the STS-1 data stream and a gapped clock. The gaps in the input clock inhibit the elastic store from writing all but DS3 payload data.

The bit leaking circuit stores incoming STS-1 pointer adjustments into a queue and leaks them out of the desynchronizer one bit at a time.

STS-Nc signal is used to transport higher rate signals. However,the digital signals that SONET carries do not fit in the SPE perfectly.

FIGURE 4. XRT71D00 DESYNCHRONIZER BLOCK DIAGRAM



Hardware Mode

The Host/$\overline{HW}$ pin (pin 12) is used to select the operating mode of the XRT71D00. In Hardware mode (connect this pin to ground), the serial processor interface is disabled and hardwired pins are used to control configuration and report status..

TABLE 1: FUNCTIONS OF DUAL MODE PINS IN "HARDWARE" MODE CONFIGURATION

PIN #	PIN NAME	FUNCTION, WHILE IN THE HARDWARE MODE
10	ClkES (SDI)	ClkES
11	FSS (SClk)	FSS
15	BWS/Ch_Addr_1	BWS
18	DJA/(SDO)	DJA
28	Ch_Addr_0	None
29	E3/$\overline{DS3}$/($\overline{CS}$)	E3/$\overline{DS3}$

HOST MODE:

In Host mode (connect this pin to VDD), the serial port interface pins are used to control configuration and status report. In this mode, serial interface pins : SDI, SDO,SClk and CS are used.

A listing of these Command Registers, their Addresses, and their bit-formats are listed below in Table 2.

TABLE 2: ADDRESS AND BIT FORMATS OF THE COMMAND REGISTERS

ADDR	COMMAND REGISTER	CH_ADDR_1	CH_ADDR_0	TYPE	D6	D5	D4	D3	D2	D1	D0
0X06	CR6	0	0	R/W	STS-1	0	E3/DS3*	DJA	BWS	ClkES	FSS
0x07	CR7	0	0	RO	***	***	***	***	***	***	FL
0x0E	CR14	0	1	R/W	STS-1	0	E3/DS3*	DJA	BWS	ClkES	FSS
0x0F	CR15	0	1	RO	***	***	***	***	***	***	FL
0x16	CR22	1	0	R/W	STS-1	0	E3/DS3*	DJA	BWS	ClkES	FSS
0x17	CR22	1	0	RO	***	***	***	***	***	***	FL

- The serial interface for both the XRT71D00 and the XRT7300, XRT7302 and XRT7303, E3/DS3/STS-1 LIU which makes it easy to configure both the XRT71D00 and the LIU with a single CS, SDI, SDO and SClk input and output pins.

SERIAL INTERFACE OPERATION.

Serial interface data structure and timings are provided in Figure 5 and 6 respectively..

The clock signal is provided to the SClk and the CS is asserted for 50 ns prior to the first rising edge of the SClk.

BIT 1—"R/W" (READ/WRITE) BIT

This bit will be clocked into the SDI input, on the first rising edge of SClk (after $\overline{CS}$ has been asserted). This bit indicates whether the current operation is a "Read" or "Write" operation. A "1" in this bit specifies a "Read" operation; whereas, a "0" in this bit specifies a "Write" operation.

Bits 2 through 5: The five (5) bit Address Values (labeled A0, A1, A2 ,A3,and A4)

The next four rising edges of the SClk signal will clock in the 5-bit address value for this particular Read (or Write) operation. The address selects the Command Register for reading data from, or writing data to. The address bits to the SDI input pin is applied in ascending order with the LSB (least significant bit) first.

BIT 7:

A5 must be set to "0", as shown in Figure 5.

BIT 8—A6

The value of "A6" is a "don't care".

Once these first 8 bits have been written into the Serial Interface, the subsequent action depends upon whether the current operation is a "Read" or "Write" operation.

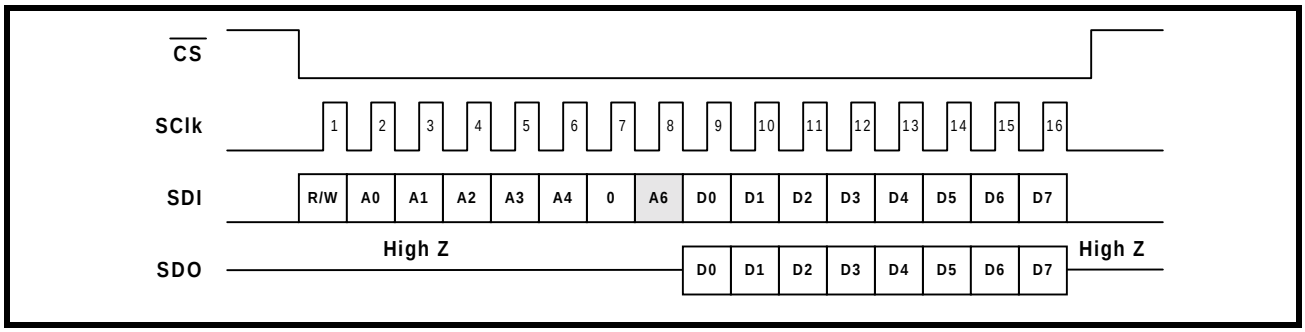
READ OPERATION

Once the last address bit (A4) has been clocked into the SDI input, the "Read" operation will proceed through an idle period, lasting three SClk periods. On the falling edge of SClk Cycle #8 (see Figure 5) the serial data output signal (SDO) becomes active. At this point the user can begin reading the data contents of the addressed Command Register (at Address [A4,A3, A2, A1, A0]) via the SDO output pin. The Serial Interface will output this seven bit data word (D0 through D6) in ascending order (with the LSB first), on the falling edges of the SClk . The data (on the SDO output pin) is stable for reading on the very next rising edge of the SClk .

WRITE OPERATION

Once the last address bit (A4) has been clocked into the SDI input, the "Write" operation will proceed through an idle period, lasting three SClk periods. Prior to the rising edge of SClk Cycle #9 , eight bit data word is applied to SDI input. Data on SDI is latched on the rising edge of SClk.

FIGURE 5. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



NOTES:

1. *A5 is always "0".*
2. *R/W = "1" for "Read" Operations*
3. *R/W = "0" for "Write" Operations*
4. *Denotes a "don't care" value (shaded areas)*

SIMPLIFIED INTERFACE OPTION

The user can simplify the design of the circuitry connecting to the Microprocessor Serial Interface by tying both the SDO and SDI pins together, and reading data from and/or writing data to this "combined" signal. This simplification is possible because only one of these signals are active at any given time. The inactive signal will be tri-stated.

FIGURE 6. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

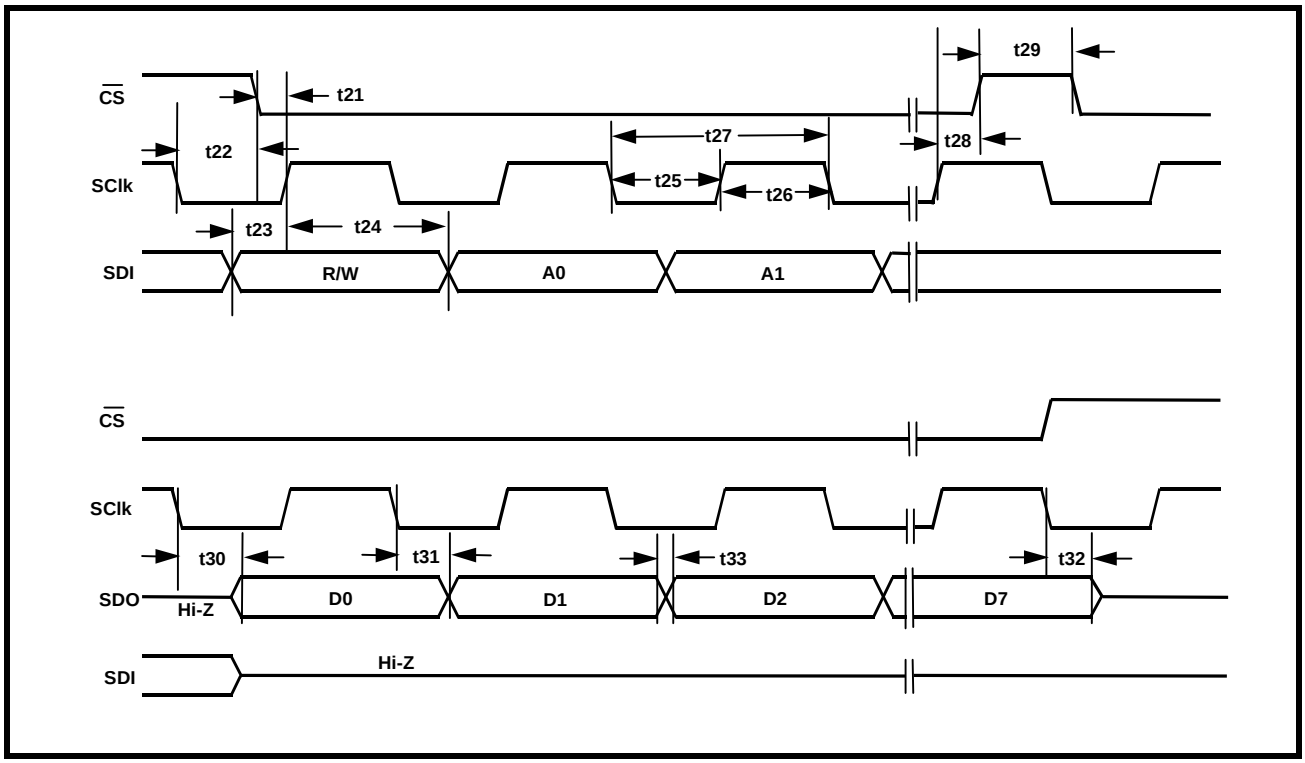


FIGURE 7. INPUT/OUTPUT TIMING

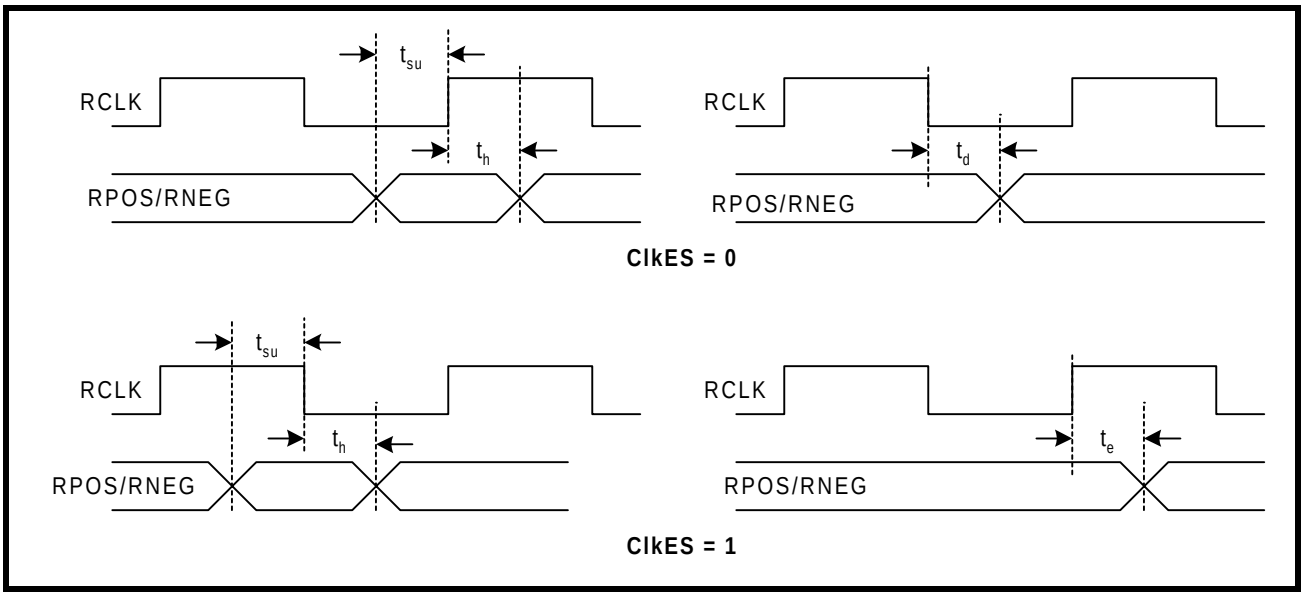


Table 3 summarizes the results of jitter transfer characteristics testing, performed on the XRT71D00.

Table 4 summarize4s the results of jitter tolerance testing, performed on the XRT71D00.

TABLE 3: XRT71D00 JITTER TRANSFER FUNCTION

APPLICATION	DS3				E3			
BWS	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH
INPUT JITTER	1UIPP		10UIPP		1UIPP		10UIPP	
FREQ. (HZ)	Jitter Gain (dB)				Jitter Gain (dB)			
5	0.02	-0.33	0.36	0.06	0.44	0.37	0.83	0.04
10	-0.10	-0.10	-0.30	-0.01	-0.15	0.20	-0.22	-0.02
20	-2.04	-0.24	-2.24	-0.13	-3.16	0.35	-3.24	-0.32
30	-3.63	-0.35	-4.33	-0.36	-5.51	0.05	-5.93	-0.73
40	-5.98	-0.53	-6.16	-0.72	-7.68	-0.68	-7.99	-1.24
50	-7.55	-1.00	-7.82	-1.12	-10.36	-1.15	-9.61	-1.85
60	-9.57	-1.46	-9.17	-1.66	-12.50	-2.53	-11.27	-2.45
80	-12.54	-2.25	-11.28	-2.64	-15.20	-3.56	-13.59	-3.76
100	-14.67	-3.07	-13.36	-3.52	-16.22	-4.69	-15.51	-5.02
125	-16.67	-3.88	-14.91	-4.76	-17.38	-5.78	-17.07	-6.50
150	-17.32	-5.74	-16.78	-5.89	-19.45	-7.43	-18.75	-7.74
200	-18.77	-7.75	-18.96	-7.90	-20.36	-10.71	-21.11	-9.94
300	-21.43	-12.04	-21.81	-10.89	-22.96	-13.58	-24.46	-13.23
500	-22.22	-16.74	-26.09	-14.98	-23.78	-17.66	-28.84	-17.16
>1000	-25.42	-21.13	-33.44	-20.66	-23.51	-20.96	-35.77	-23.35

TABLE 4: XRT71D00 MAXIMUM JITTER TOLERANCE

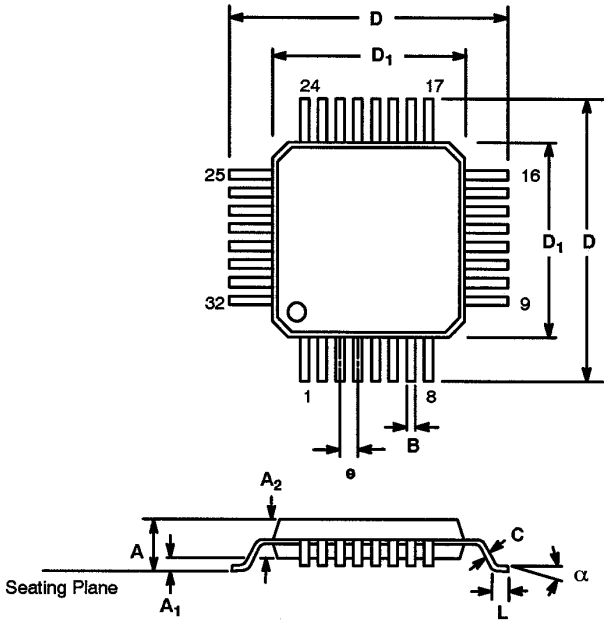
APPLICATION	DS3				E3			
BWS	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH
FIFO SIZE	16		32		16		32	
FREQ. (HZ)	UI (PEAK TO PEAK)				UI (PEAK TO PEAK)			
10	34.313	>64	>64	>64	26.689	>64	53.313	>64
20	21.439	>64	43.188	>64	18.564	52.188	37.438	>64
30	18.314	46.313	36.813	>64	16.689	36.688	33.938	>64
40	16.939	36.188	34.313	>64	16.064	29.314	32.688	58.438
50	16.314	30.314	33.188	60.313	15.689	25.064	32.063	50.438
60	16.064	26.689	32.563	53.188	15.564	22.564	31.689	45.438
80	15.689	22.314	31.814	44.813	15.314	19.689	31.314	39.688
100	15.439	20.064	31.439	40.434	15.314	18.064	31.189	36.813
125	15.439	18.439	31.314	37.313	15.189	17.064	31.064	34.813
150	15.314	17.564	31.189	35.438	15.189	16.564	31.064	33.688
200	15.314	16.464	31.064	33.563	15.189	15.939	30.939	32.438
300	15.189	15.814	30.939	32.063	15.064	15.564	30.939	31.564
500	15.189	15.439	30.939	31.314	15.064	15.314	30.939	31.189
>1000	15.0189	15.189	30.939	30.939	15.189	15.189	30.939	30.939

PACKAGE INFORMATION

32 LEAD TQFP PACKAGE DIMENSIONS

32 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.4 mm TQFP)

Rev. 2.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT71D00IQ	32 Lead TQFP	-40^0C to $+85^0$C

REVISIONS

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Datasheet February 2000

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