XRD9814/XRD9816

3-Channel 14/16-Bit Linear CCD/CIS Sensor Signal Processors

December 1999-2

FEATURES

- 14-Bit (XRD9814) or 16-Bit (XRD9816) A/D Converter
- No Missing Codes
- Triple-Channel, 2.5 MSPS Color Scan Mode
- Single-Channel, 6 MSPS Monochrome Scan Mode
- Triple Correlated Double Sampler
- Triple 10-Bit Programmable Gain Amplifier
- Triple 10-Bit Offset Compensation DAC
- Fully Differential or Single-Ended Inputs
- CDS or S/H Mode
- Inverting or Non-Inverting Mode
- Internal Voltage Reference
- Serial Control: On Data Bus or Separate Pins
- 14-Bit or 8-Bit (Nibble) Parallel Data Output (XRD9814)
- 16-Bit or 8-Bit (Nibble) Parallel Data Output (XRD9816)
- 5V Operation and 3V I/O Compatibility
- Low Power CMOS: 500mW @ 5V

APPLICATIONS

- 48-Bit Color Scanners (XRD9816)
- 42-Bit Color Scanners (XRD9814)
- CCD or CIS Color Imagers
- Gray Scale Scanners
- Film Scanners

GENERAL DESCRIPTION

The XRD9814/9816 is a fully integrated, high-performance analog signal processor/digitizer specifically designed for use in 3-channel linear Charge Coupled Device (CCD) and Contact Image Sensitive (CIS) imaging applications.

Each channel of the XRD9814/9816 includes a Correlated Double Sampler (CDS), Programmable Gain Amplifier (PGA) and channel offset adjustment. After gain and offset adjustment, the analog inputs are sequentially sampled and digitized by an accurate 14/16-bit A/D converter. The analog front-end can be configured for inverting/non-inverting input, CDS or sample-hold (S/H) mode, or AC/DC coupling, making the XRD9814/9816 suitable for use in CCD, CIS and other data acquisition applications.

The CDS mode of operation supports both line and pixel-clamp modes and can be used to achieve significant reduction in system 1/f noise and CCD reset clock feed-through. In S/H mode the internal DC-restore voltage clamp can be enabled or disabled to support AC-coupled or DC inputs. Sampling mode, 10-bit PGA gain (1024 linear steps), 8-bit fine offset adjustment (256 linear steps), 2-bit gross offset adjustment and input signal polarity are all programmable through a serial interface. PGA gain range is 1 to 10, and channel offset range is -300mV to 300mV for fine adjustment and additional -400mV to +200mV for gross offset adjustment. The A/D Full-Scale Range (FSR) is programmable to 2V or 3V.

ORDERING INFORMATION

Part No.	Package Type	Temperature Range
XRD9814ACV	48-Lead TQFP	0°C to +70°C
XRD9816ACV	48-Lead TQFP	0°C to +70°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 • (510) 668-7000 • FAX (510) 668-7017 • www.exar.com

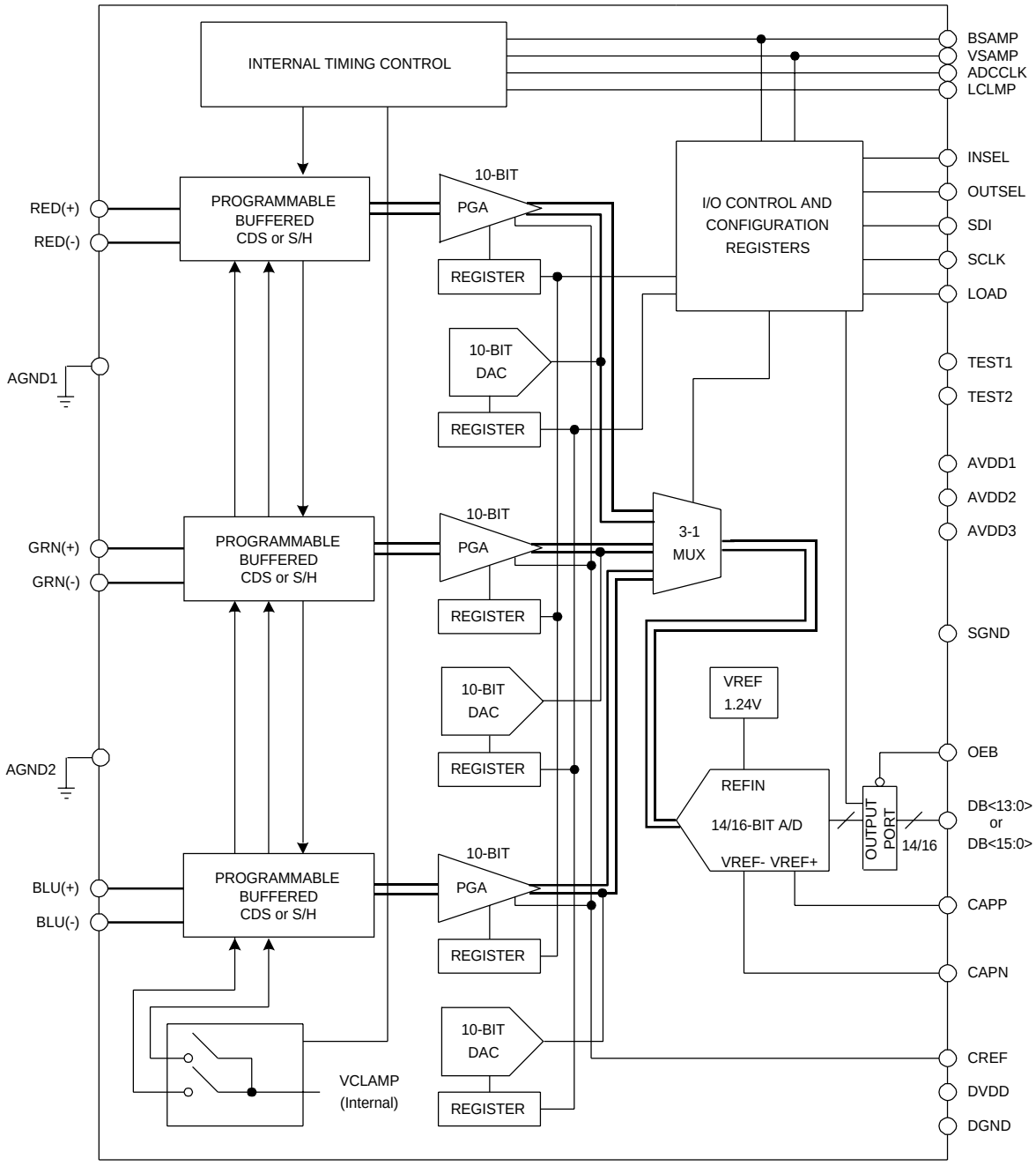
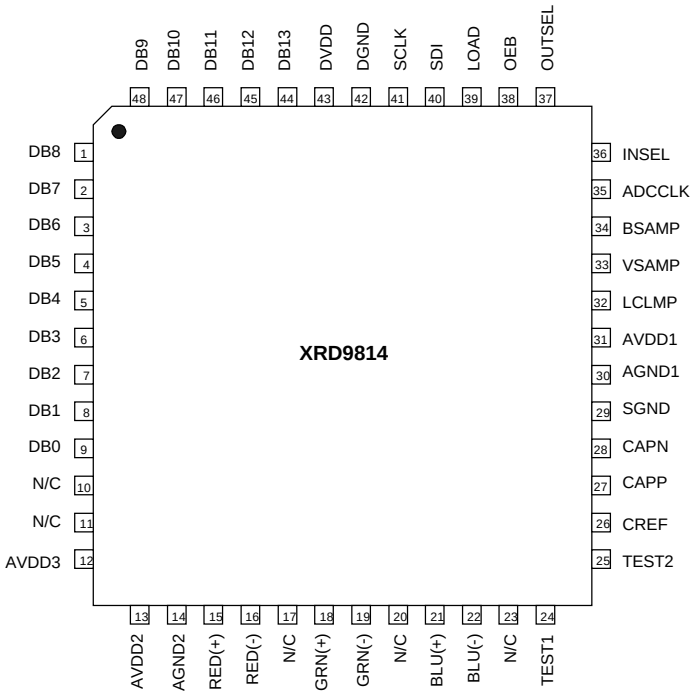


Figure 1. Block Diagram

PIN CONFIGURATION



Note:

Pins 17,20 and 23 should be connected to AGND2 to improve noise immunity

PIN DESCRIPTION - XRD9814

Pin No.	Name	Description
1	DB8	Data Output Bit 8
2	DB7	Data Output Bit 7
3	DB6	Data Output Bit 6
4	DB5	Data Output Bit 5
5	DB4	Data Output Bit 4
6	DB3	Data Output Bit 3
7	DB2	Data Output Bit 2
8	DB1	Data Output Bit 1
9	DB0	Data Output Bit 0
10	N/C	No Connect
11	N/C	No Connect
12	AV_{DD3}	Analog Power Supply
13	AV_{DD2}	Analog Power Supply
14	AGND2	Analog Ground (Substrate)
15	RED(+)	Red Positive Analog Input

PIN DESCRIPTION - XRD9814 (CONT'D)

Pin No.	Name	Description
16	RED(-)	Red Negative Analog Input
17	N/C	No Connect, (Note 5)
18	GRN(+)	Green Positive Analog Input
19	GRN(-)	Green Negative Analog Input
20	N/C	No Connect, (Note 5)
21	BLU(+)	Blue Positive Analog Input
22	BLU(-)	Blue Negative Analog Input
23	N/C	No Connect, (Note 5)
24	TEST1	Internal Use Only
25	TEST2	Internal Use Only
26	CREF	Decoupling Cap for CDS Reference
27	CAPP	Decoupling Cap for Positive Reference
28	CAPN	Decoupling Cap for Negative Reference
29	SGND	Substrate Gnd
30	AGND1	Analog Ground (Substrate)
31	AV_{DD1}	Analog Power Supply
32	LCLMP	Line Clamp Enable
33	VSAMP	Video Level Sampling Clock
34	BSAMP	Black Level Sampling Clock
35	ADCCLK	A/D Converter Clock
36	INSEL	Input Mode Select (Note 1)
37	OUTSEL	Output Mode Select (Note 2)
38	OEB	Data Output Enable
39	LOAD	Register Write Enable (Note 5)
40	SDI	Serial Data Input (Note 4)
41	SCLK	Serial Shift Clock (Note 3)
42	DGND	Ground (Output Drivers and Internal Decode Logic)
43	DV_{DD}	Digital Power Supply (Output Drivers and Internal Decode Logic)
44	DB13	Data I/O Bit 13 (Note 4)
45	DB12	Data I/O Bit 12 (Note 3)
46	DB11	Data Output Bit 11
47	DB10	Data Output Bit 10
48	DB9	Data Output Bit 9

Note 1: *INSEL=0 —> SCLK, SDI, and LOAD pins are active for serial programming; INSEL=1 —> SCLK and SDI pins are inactive, and the serial programming is done through I/O pins DB12 and DB13 as described in Notes 3~4 with LOAD tri-stating DB12 and DB13.*

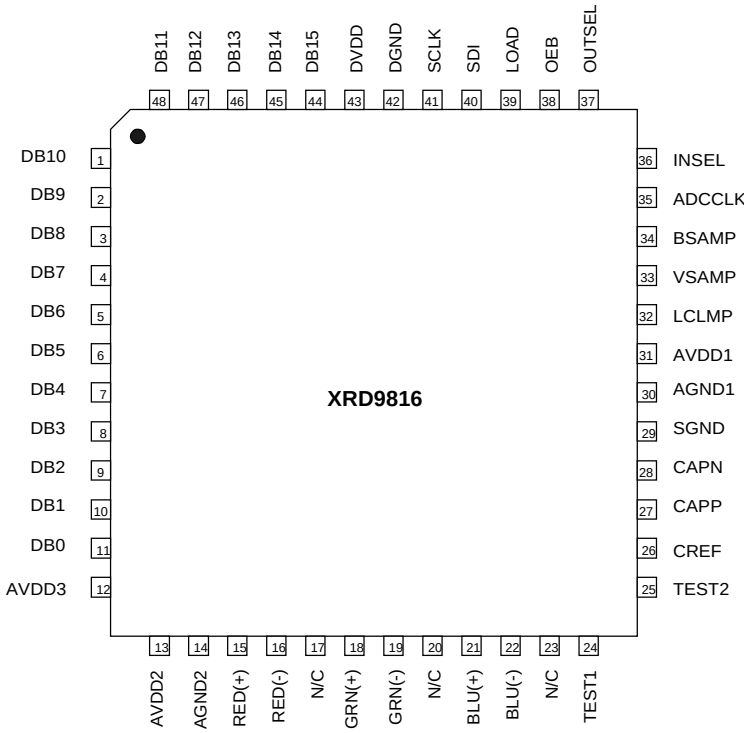
Note 2: *OUTSEL=0 —> 14-bit parallel output mode select; OUTSEL=1 —> 8-bit nibble output mode select.*

Note 3: *For INSEL=1, DB12 becomes the SCLK input during serial programming.*

Note 4: *For INSEL=1, DB13 becomes the SDI input during serial programming.*

Note 5: *Pins 17, 20 and 23 may be connected to AGND2 to improve noise immunity.*

PIN CONFIGURATION



Note:

Pins 17,20 and 23 should be connected to AGND2 to improve noise immunity

Pin No.	Name	Description
1	DB10	Data Output Bit 10
2	DB9	Data Output Bit9
3	DB8	Data Output Bit 8
4	DB7	Data Output Bit 7
5	DB6	Data Output Bit 6
6	DB5	Data Output Bit 5
7	DB4	Data Output Bit 4
8	DB3	Data Output Bit 3
9	DB2	Data Output Bit 2
10	DB1	Data Output Bit 1
11	DB0	Data Output Bit 0
12	AV_{DD3}	Analog Power Supply
13	AV_{DD2}	Analog Power Supply
14	AGND2	Analog Ground (Substrate)
15	RED(+)	Red Positive Analog Input

Pin Configuration - XRD9816

Pin No.	Name	Description
16	RED(-)	Red Negative Analog Input
17	N/C	No Connect, (Note 5)
18	GRN(+)	Green Positive Analog Input
19	GRN(-)	Green Negative Analog Input
20	N/C	No Connect, (Note 5)
21	BLU(+)	Blue Positive Analog Input
22	BLU(-)	Blue Negative Analog Input
23	N/C	No Connect, (Note 5)
24	TEST1	Internal Use Only
25	TEST2	Internal Use Only
26	CREF	Decoupling Cap for CDS Reference
27	CAPP	Decoupling Cap for Positive Reference
28	CAPN	Decoupling Cap for Negative Reference
29	SGND	Substrate Gnd
30	AGND1	Analog Ground (Substrate)
31	AV_{DD1}	Analog Power Supply
32	LCLMP	Line Clamp Enable
33	VSAMP	Video Level Sampling Clock
34	BSAMP	Black Level Sampling Clock
35	ADCCLK	A/D Converter Clock
36	INSEL	Input Mode Select (Note 1)
37	OUTSEL	Output Mode Select (Note 2)
38	OEB	Data Output Enable
39	LOAD	Register Write Enable (Note 5)
40	SDI	Serial Data Input (Note 4)
41	SCLK	Serial Shift Clock (Note 3)
42	DGND	Ground (Output Drivers and Internal Decode Logic)
43	DV_{DD}	Digital Power Supply (Output Drivers and Internal Decode Logic)
44	DB15	Data I/O Bit 15 (Note 4)
46	DB13	Data Output Bit 13
45	DB14	Data I/O Bit 14 (Note 3)
47	DB12	Data Output Bit 12
48	DB11	Data Output Bit 11

Note 1: *INSEL=0 —> SCLK, SDI, and LOAD pins are active for serial programming; INSEL=1 —> SCLK and SDI pins are inactive, and the serial programming is done through I/O pins DB14 and DB15 as described in Notes 3~4 with LOAD tri-stating DB14 and DB15.*

Note 2: *OUTSEL=0 —> 16-bit parallel output mode select; OUTSEL=1 —> 8-bit nibble output mode select.*

Note 3: *For INSEL=1, DB14 becomes the SCLK input during serial programming.*

Note 4: *For INSEL=1, DB15 becomes the SDI input during serial programming.*

Note 5: *Pins 17, 20 and 23 may be connected to AGND2 to improve noise immunity.*

ELECTRICAL CHARACTERISTICS

AV_{DD}=DV_{DD}=5.0V, ADCCLK=6MHz, Input Range = 2V, Ta=25°C unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
A/D CONVERTER						
Resolution	R	14			BITS	XRD9814
Resolution	R	16			BITS	XRD9816
Maximum Conversion Rate	Fc	6	8		MSPS	
Differential Non-Linearity	DNL		+/-0.8		LSB	XRD9814
Differential Non-Linearity	DNL		-0.95/+1.2		LSB	XRD9816
Monotonicity	M		Yes			XRD9814
Monotonicity	M		Yes			XRD9816
Input Referred Offset	ZSE		40		mV	
Offset Drift	ZSD		15		uV/°C	
Input Referred Gain Error	FSE		+/- 2		% FS	
Gain Error Drift	FSD		0.003		% FS °C	
Input Voltage Range						
2V Full-Scale Range	IVR	0		2.0	V	PB5=0, Config Reg #1
3V Full-Scale Range	IVR	0		3.0	V	PB5=1, Config Reg #1
CDS - S/H SPECIFICATIONS						
Input Voltage Range						
Input Buffer Disabled (Note 1)	INVSR	AGND		AVDD	V	Pixel Clamp, PB1=0, Config Reg #1
Input Buffer Enabled	INVSRB	0.5		AVDD-1	V	Line Clamp, PB1=1, Config Reg #1
Input Bias Current						
Input Buffer Disabled (Note 2)	IB		25		uA	Gain=1, PB1=0, Config Reg #1
Input Buffer Enabled	IBB			25	nA	T_A=70° C, PB1=1, Config Reg #1
Input Switch On -Resistance	Ron		150	250	Ω	Clamp Enabled
Input Switch Off -Resistance	Roff	100	1000		MΩ	Clamp Disabled
Internal Voltage Clamp						
CCD Input (Inverting)	Vclamp	4.0	4.2	4.4	V	PB2=0, Config Reg #1
S/H Input (Non-Inverting)	Vclamp	0.6	0.8	1.0	V	PB2=1, Config Reg #1

***Note 1**: ADC digitizing range = (A/D Full-Scale Range/PGA Gain)*
***Note 2:** Due to switch capacitor input.*

ELECTRICAL CHARACTERISTICS (CONT'D)
AVDD=DVDD=5.0V, ADCCLK=6MHz, Ta=25C unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
OFFSET SPECIFICATIONS						
Fine Offset Adjustment Min	OFR	-270	-300	-330	mV	
Fine Offset Adjustment Max	OFR	+270	+300	+330	mV	
Fine Offset Adjustment Step	OFRES		2.34		mV	8-Bit, 256 Settings
Fine Offset Adjustment Linearity	OFRL		+/-1.5%			
Gross Offset Adjustment Min	OFGR	-360	-400	-440	mV	
Gross Offset Adjustment Max	OFGR	+360	+200	+440	mV	
Gross Offset Adjustment Step	OFGRES		+200		mV	2-Bit, 4 Settings
PGA SPECIFICATIONS						
Gain Range Min (Absolute Value)	GRAN	1.0	1.10	1.20	V/V	-1 for PB2=0, +1 for PB2=1, Config Reg #1
Gain Range Max (Absolute Value)	GRAN	8.5	9.5	10.5	V/V	-10 for PB2=0, +10 for PB2=1, Config Reg#1
Gain Resolution	GRES		0.0083		V/V	10-Bit 1024 Steps
SYSTEM SPECIFICATIONS (Includes CDS, PGA and A/D)						
Differential Non-Linearity	DNL	-0.9	+/-0.8	+1.5	LSB	XRD9814, PGA Gain = 1
Differential Non-Linearity	DNL	-0.95	-0.95/+1.2	+2.0	LSB	XRD9816, PGA Gain = 1
Integral Non-Linearity	INL		+/-10.0		LSB	XRD9814, PGA Gain = 1
Input Referred Noise PGA Gain = -1.63	IRN_{min}		+3.4		LSB	XRD9814, 1-Channel CIS Mode, 6MSPS, Low Gain
PGA Gain = -5.0	IRN_{max}		+1.1		LSB	XRD9814, 1-Channel CIS Mode, 6MSPS, Low Gain
System Offset PGA Gain= -1	IRO_{min}		+70		mV	XRD9814/9816, 3-Channel Mode, 6MSPS
PGA Gain= -10	IRO_{max}		+70		mV	XRD9814/9816, 3-Channel Mode, 6MSPS

ELECTRICAL CHARACTERISTICS (CONT'D)
AVDD=DVDD=5.0V, ADCCLK=6MHz, Ta=25C unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
TIMING SPECIFICATIONS						
ADCCLK Pulse Width	taclk	66.5			ns	
BSAMP falling edge delay from rising ADCCLK	tbfcr	10			ns	
BSAMP falling edge to VSAMP falling edge.	tbvf	70			ns	
ADCCLK Period (1 Ch. Mode)	tcp1	166			ns	
ADCCLK Period (3 Ch. Mode)	tcp3	133			ns	
1-Channel Conversion Period	tcr1	166			ns	
3-Channel Conversion Period	tcr3	400			ns	
BSAMP Pulse Width	tpwb	30			ns	
VSAMP Pulse Width	tpwv	30			ns	
VSAMP falling edge to BSAMP falling edge.	tvbf	70			ns	
VSAMP falling edge delay from rising ADCCLK.	tvfcr	30			ns	All modes except 1-Channel S/H
VSAMP falling edge delay from rising ADCCLK	tvfcr	70			ns	1-Channel S/H, Config REG #1, PB2=1, PB7=1
PGA Settling Time	tstl	70			ns	
Aperture Delay	tap		5		ns	
VSAMP TIMING OPTION #1						
VSAMP rising edge delay from falling ADCCLK (Note 1)	tvrcf	15			ns	tvrcr is not required, Config REG #1, PB0=0
VSAMP TIMING OPTION #2						
VSAMP rising edge delay from rising ADCCLK (Note 1)	tvrcr	15			ns	tvrcf is not required, Config REG # 1, PB0=1
WRITE SPECIFICATIONS						
Data Setup Time	tds	15			ns	
Data Hold Time	tdh	15			ns	
Load Setup Time	tlcs	15			ns	
Load Hold Time	tlch	15			ns	
Load Pulse Width	tplw	25			ns	

***Note 1**: VSAMP Timing Option #2 allows additional timing flexibility by allowing the rising edge of VSAMP to occur approximately one-half ADCCLK period earlier than Option #1. Option #2 is only available in 3-Channel Operation (PB4=0, PB3=0, Configuration Register #1).*

ELECTRICAL CHARACTERISTICS (CONT'D)
AVDD=DVDD=5.0V, ADCCLK=6MHz, Ta=25C unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
DATA READBACK SPECIFICATIONS						
Address Access Time	taa (1)		15		ns	
Output Enable Access Time	taoe (1)		15		ns	
ADC DIGITAL OUTPUT SPECIFICATIONS						
Output Delay	tod		20		ns	
Tri-State to Data Valid	tlz		8		ns	
Output Enable High to Tri-State	thz		8		ns	
Latency RGB inputs	lat		7		ADCCLK	
DIGITAL INPUTS						
Input High Logic Level	V_{IH}	80			% DV_{DD}	DV_{DD}=3-5V
Input Low Logic Level	V_{IL}			20	% DV_{DD}	DV_{DD}=3-5V
High Level Input Current	I_{IH}		5		uA	
Low Level Input Current	I_{IL}		5		uA	
Input Capacitance	C_{IN}		10		pF	
DIGITAL OUTPUTS (DV_{DD}=5V)						
Output High Voltage	V_{OH}	4.2			V	IL=2ma
Output Low Voltage	V_{OL}			0.4	V	IL=-2ma
Output Capacitance	C_{OUT}		10		pF	
DIGITAL OUTPUTS (DV_{DD}=3.3V)						
Output High Voltage	V_{OH}	2.8			V	IL=2ma
Output Low Voltage	V_{OL}			0.3	V	IL=-2ma
Output Capacitance	C_{OUT}		10		pF	
POWER SUPPLY						
Analog Power Supply	AV_{DD}	4.5	5.0	5.5	V	
Digital Power Supply	DV_{DD}	3.0	5.0	5.5	V	
Analog Supply Current	IDDA		110		mA	3CH CDS Mode
Digital Supply Current	IDDD		2		mA	Digital Output CLoad=30pF, all pins.
Stand-By Mode Power	PDoff		65	80	mW	

***Note 1**: Start of valid data depends on which timing becomes effective last, taoe or taa.*

Function	A2	A1	A0	PB9-PB0
Configuration Reg #1	0	0	0	See Configuration Register #1
Configuration Reg #2	0	0	1	See Configuration Register #2
Red Gain	0	1	0	10-Bit Gain
Green Gain	0	1	1	10-Bit Gain
Blue Gain	1	0	0	10-Bit Gain
Red Offset	1	0	1	2-Bit Gross Offset Adjustment: 8-Bit Fine Offset Adjustment
Green Offset	1	1	0	2-Bit Gross Offset Adjustment: 8-Bit Fine Offset Adjustment
Blue Offset	1	1	1	2-Bit Gross Offset Adjustment: 8-Bit Fine Offset Adjustment

Table 1. XRD9814/9816 Register Overview

A2 A1 A0 Address	Bit Assignment	PB9-PB0 Bit Definition
0 0 0	**PB9** Single Channel Power Save Mode	0 Unused channels are powered down to 0 save power (single channel mode only) 1 Unused channels are powered up
	PB8 Digital Reset	0 No Reset 1 Resets all registers to the default configuration
	PB7 PB6 Clamp Mode	00 CDS pixel 01 CDS line clamp 10 No clamp 11 S/H line clamp
	PB5 A/D Full Scale Range	0 2Vpp Full Scale 1 3Vpp Full Scale (recommended for better performance)
	PB4 PB3 Color Select	00 RGB 3 channel color mode 01 Red single channel mode 10 Green single channel mode 11 Blue single channel mode
	PB2 Input Signal Polarity	0 Inverted for CCD or negative going signals 1 Non-inverted for CIS or positive going signals
	PB1 Input Buffer Enable	0 No buffer (DC coupled or AC coupled inputs with pixel clamp mode 1 Buffer enabled (AC Coupled inputs for line clamp or no clamp mode
	PB0 VSAMP Timing	0 Timing option #1 (see Figure 3, 4, 7 & 8 for details) 1 Timing option #2 (see Figure 3, 4, 7 & 8 for details)

Table 2. Configuration Register #1 Definition (Default Configuration is 000H)

A2 A1 A0 Address	Bit Assignment	PB9-PB0 Bit Definition	
0 0 1	**PB9** Not Used	0 1	Normal This register should be set to zero for normal operation Do Not Use
	PB8 Not Used	0 1	Normal This register should be set to zero for normal operation Do Not Use
	PB7 Not Used	**0** 1	Normal This register should be set to zero for normal operation Do Not Use
	PB6 Not Used	0 1	Normal This register should be set to zero for normal operation Do Not Use
	PB5 Not Used	0 1	Normal This register should be set to zero for normal operation Do Not Use
	PB4 PB3 CDS Clamp Voltage (Black Level)	00 01 10 11	AV_{DD}-0.8V (4.2V for AVDD = 5V) (See Figures 11 & 12 for VClamp Settings) AV_{DD}-1.3V (3.7V for AVDD = 5V) AV_{DD}-1.8V (3.2V for AVDD = 5V) AV_{DD}-2.3V (2.7V for AVDD = 5V)
	PB2 Not Used	0 1	Normal This register should be set to zero for normal operation Do Not Use
	PB1 Stand-By Mode	0 1	All circuits active Low power mode (75mW, requires 5uS back to normal operation)
	PB0 Read Back Mode	0 1	A/D digital outputs Read back mode (A2:A1:A0 select register data)

Table 3. Configuration Register #2 Definition (Default Configuration is 000H)

A2	A1	A0	Function	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0	1	0	Red Gain	MSB									LSB
0	1	1	Green Gain	MSB									LSB
1	0	0	Blue Gain	MSB									LSB
1	0	1	Red Offset PB9-PB8 gross adj PB7-PB0 fine adj	00 01 10 11	0V +200mV -200mV -400mV	MSB							LSB
1	1	0	Green Offset PB9-PB8 gross adj PB7-PB0 fine adj	00 01 10 11	0V +200mV -200mV -400mV	MSB							LSB
1	1	1	Blue Offset PB9-PB8 gross adj PB7-PB0 fine adj	00 01 10 11	0V +200mV -200mV -400mV	MSB							LSB

Table 4. Gain and Offset Registers (Default Configuration is 000H)

GENERAL DESCRIPTION

The XRD9814/9816 contains all of the circuitry required to create a complete 3-channel signal processor /digitizer for use in CCD/CIS imaging systems. Each channel includes a correlated double sampler (CDS), programmable gain amplifier (PGA) and channel offset adjustment. The input stage can also be configured for use with inverting/non-inverting, AC or DC coupled signals. In order to maximize flexibility, the specific operating mode is programmable through two configuration registers. In addition, the gain and offset of each channel can be independently programmed through separate gain and offset registers. Configuration register data is loaded serially through a 3-pin serial interface. Specific details for register writes are detailed below. After signal conditioning the three PGA outputs are digitized by a 14-bit/16-bit A/D converter.

Writing Registers Data

The XRD9814/9816 utilizes eight 10-Bit registers to store configuration, gain and offset information. Register data is written through the 3-pin serial interface consisting of SDI (serial data input), SCLK (serial shift clock) and LOAD (positive edge write enable). A write consists of pulling LOAD low, shifting in 3 bits of address (MSB first) and 10 bits of data (MSB first). Data is written on the rising edge of SCLK and the last 13 bits are latched. The timing for writing to registers is shown in Figure 17 and 18.

When INSEL=0, SCLK, SDI, and LOAD pins are active for serial programming.

When INSEL=1, SCLK and SDI pins are inactive, and the serial programming is done through I/O pins DB12/ DB14 and DB13/DB15 while LOAD pin is low.

Configuration Register #1

The bit assignment and definition for this register is detailed in the Configuration Register #1 Definition Table (Table 2). The primary purpose of this register is to configure the analog input blocks for CCD or S/H operation.

Clamp Mode

The clamp mode setting determines the conditions when the internal clamp is enabled (see Table 5). The pixel and CCD line-clamp modes are used to DC-restore AC coupled CCD input signals to the PGA common-mode input voltage while using correlated double sampling. S/H line mode should be used to DC-restore AC coupled inputs which do not utilize correlated double sampling and have only one control input (VSAMP). No-clamp mode should be used for DC coupled S/H inputs.

Pixel Mode (CCD with CDS)

The input clamp is active each pixel period with a pulse-width determined by the Black- level Sampling Input (BSAMP). The position of BSAMP can be optimized to eliminate the effects of the CCD reset pulse. Since the input capacitor is recharged to the clamp voltage on each pixel, common-mode droop errors are eliminated.

CCD Line Mode (CCD with CDS)

The input clamp is enabled only at the beginning of the line by gating BSAMP with LCLMP. Gating with LCLMP maintains the ability to position the clamp pulse (BSAMP) away from the CCD reset for varying LCLMP position and width. Since the input capacitor is clamped only at the beginning of each line a larger input capacitor is required to satisfy the common-mode input requirements of the analog front-end. (See Coupling Capacitor Requirements.) The input buffer should be enabled in this mode (PB1=1, Register #1).

S/H Line Mode (S/H with AC Coupling)

The S/H Line mode clamp is used to DC-restore AC coupled inputs which do not utilize CDS. VSAMP is used to sample and hold the input signal and LCLMP performs the clamp function. This differs from the CDS line and pixel modes which use BSAMP to clamp to the reference level and VSAMP to hold the video input. The input buffer should be enabled in this mode (PB1=1, Register #1).

No-Clamp Mode (S/H with DC input)

Used for DC coupled inputs. AC coupled inputs must be externally clamped to the proper common-mode input voltage of the XRD9814/9816.

Note: *Pixel clamp is the default clamp mode.*

Clamp Mode	PB7	PB6	Clamp Enable
Pixel	0	0	*BSAMP*
CDS Line	0	1	*BSAMP* • $\overline{LCLMP}$
No Clamp	1	0	Disabled
S/H Line	1	1	$\overline{LCLMP}$

Table 5. Clamp Enable Definition

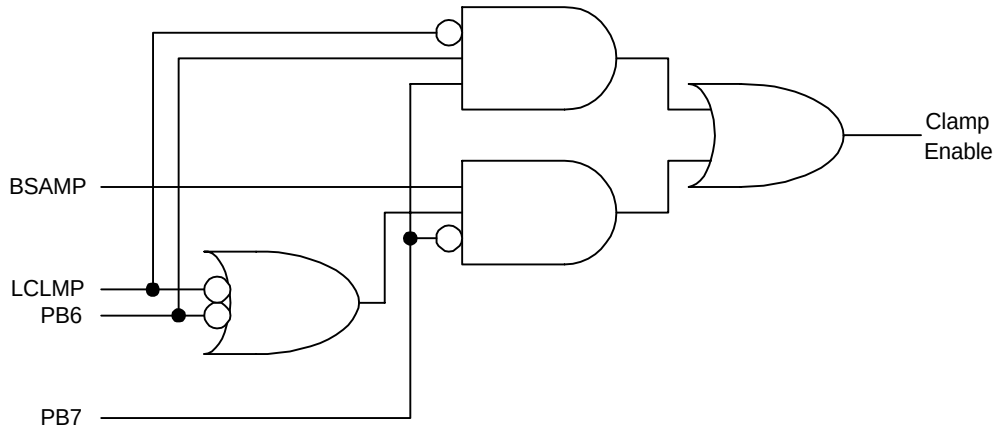


Figure 2. Clamp Enable Logic

A/D Full-Scale Range

This bit sets the Full-Scale Range (FSR) of the A/D converter to 2V or 3V. Use the 3V FSR for lowest noise performance.

Color Select

The color input corresponds to the signal input to be digitized by the A/D converter. If set to RGB (default) the A/D input is sequentially cycled through the red, green and blue channels. The green channel is synchronized on the rising edge of the first ADCCLK after the falling edge of VSAMP. If set in single-channel mode, the A/D multiplexer will not sequence and the A/D converter input will be continually connected to the channel that is selected, RED, GRN or BLU.

Signal Polarity

This bit configures the analog inputs for positive or negative transitioning inputs. This is required to provide the correct signal polarity to the A/D input and to set the correct input clamp level. The default configuration is set to inverting mode (CCD input).

Input Buffer Enable

This bit enables the input buffer to the PGA amplifier and is required only for AC coupled inputs operating in CDS line or S/H line clamp modes. Since this input buffer reduces the input voltage range its use is not recommended under DC or pixel-mode operation. The input buffer is disabled in the default configuration.

VSAMP Timing

This allows the user to select one of two VSAMP timing controls. Timing Option #2 allows the rising edge of VSAMP to occur approximately one-half ADCCLK earlier than Option #1. This does not affect internal timing and is provided only to allow additional flexibility in the external timing control. Timing Option #2 is available only in the 3-channel mode of operation (See timing diagrams Figure 3 and Figure 4).

Configuration Register #2

The bit assignment and definition for this register is detailed in the Configuration Register #2 Definition Table. A diagnostic read-back mode allows gain, offset and configuration data to be output as the 8 or 10 MSBs on the digital output bus depending on the selection of OUTSEL (see Reading Register Data session for details). Additional bits are used to enable a low-power stand-by state and manufacturing test mode.

Digital Reset

Setting this bit to one resets all registers to all zeros.

Test Mode

This is a reserved bit for testing and must be set to 0 in all writes to Configuration Register #2.

Stand-By Mode

Setting this bit to one forces the circuit into a low-power standby mode. Configuration, offset and gain registers remain unchanged in stand-by mode. Pull OEB High to set DB<15:0> to high impedance during stand-by mode.

Read Back Mode

This is a special diagnostic mode which can aid in the debugging of new system designs. Setting this bit to 1 allows all configuration, gain and offset register contents to be output on the data output bus (explained below).

Reading Register Data

In order to enter read-back mode, set configuration register #2, PB0 to 1. Follow the write timing in Figures 17 and 18.

In order to read a specific register, shift in 3-bits of register address data (MSB first), followed by 10 dummy data bits. In the case of reading back configuration register #2, PB0 has to stay 1 and cannot be a dummy.

Read-Back Registers and Address

Address Data	Register
001 XXXXXXXXXX	Cfig1
001 XXXXXXXXX1	Cfig2
010 XXXXXXXXXX	Red Gain
011 XXXXXXXXXX	Grn Gain
100 XXXXXXXXXX	Blu Gain
101 XXXXXXXXXX	Red Offset
110 XXXXXXXXXX	Grn Offset
111 XXXXXXXXXX	Blu Offset

In order to exit read-back mode perform a write to configuration register 2, PB0=0.

(OUTSEL = 0) In read-back mode the A/D output is bypassed and internal register data is output to the 10 most significant bits of the data output bus. The remaining LSB bits should be ignored. Register data will be valid after the load pin goes high.

(OUTSEL = 1) In nibble mode, the output bus is limited to 8-bits. Therefore, in read-back mode, the 8 MSBs are valid when ADCCLK is high, and the 2 LSBs are valid when ADCCLK is low. Configuring and exiting the read-back mode is done in the same manner of OUTSEL = 0.

Important: *The entire byte of register #2 is re-written when exiting the readback mode. If any bits of configuration register #2 were programmed prior to entering the read-back mode, they must be re-programmed when exiting read-back. See Figure 19 for read-back timing.*

PGA Gain Settings

The gain for each color input is individually programmable from 1 to 10 in 1024 linear steps.

$$PGA\ Gain = \left(\frac{Code}{1024}\right) \cdot 9.0 + 1$$

where Code represents the binary contents of the 10-bit gain setting register.

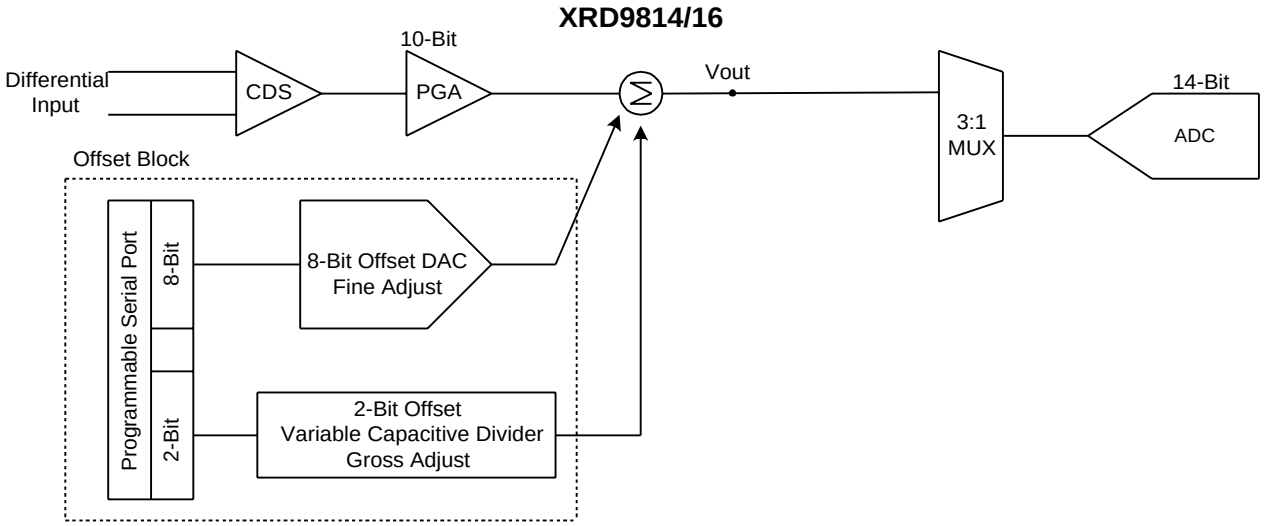
Channel Offset Adjustment

The gross offset correction for each channel is progammable from -400mV to +200mV. It is adjusted by toggling PB9 and PB8 of Offset Registers (Table 4).

The fine offset correction for each channel is programmable from -300mV to +300mV.

$$Fine\ Channel\ Offset = PB7 \cdot \left[\frac{(Code)}{128}\right] \cdot 300mV$$

PB7=1 equals -1
PB7=0 equals +1
Code = (PB6:PB0) of the 10-bit offset register.



Block Diagram of the Fine and Gross Offset Adjustment DAC

(Correlated Double Sampling)

Correlated double sampling is a technique used to level shift and acquire CCD output signals whose information is equal to the difference between consecutive reference (black) and signal (video) samples. The CDS process consists of three steps:

1) Sampling and holding the reference black level.
2) Sampling the video level.
3) Subtracting the two samples to extract the video information.

Once the video information has been extracted it can be processed further through amplification and/or offset adjustment. Since system noise is also stored and subtracted during the CDS process, signals with bandwidths less than half the sampling frequency will be substantially attenuated.

In order to reject higher frequency power supply noise which is not attenuated near the sampling frequency the XRD9814/9816 utilizes a fully differential input structure.
Since the CDS process uses AC coupled inputs the coupling capacitor must be charged to the common-mode range of the analog front-end. This can be accomplished by clamping the coupling capacitor to the internal clamp voltage when the CCD is at a reference level. This clamp may occur during each pixel (Pixel Clamp), or at the beginning of each line (CDS Line Clamp). If CDS Line Clamp mode is used the input buffer (configuration register #1, PB1) must be enabled to eliminate the effects of input bias current. If Pixel mode is selected the input buffer is not required or recommended.

3-Channel CDS Mode

This mode allows simultaneous CDS of the red, green and blue inputs . Black-level sampling occurs on each pixel and is equal to the width of the BSAMP sampling input. The black level is held on the falling edge of BSAMP and the PGA will immediately begin to track the signal input until the falling edge of VSAMP.

Two VSAMP timing modes are supported to allow additional flexibility in the VSAMP pulse width (see timing diagrams). At the end of the video sampling phase the difference between the reference and video levels is inverted, amplified and offset depending on the contents of the PGA gain and offset registers. The RGB channels are then sequentially converted by a high speed A/D converter. A/D converter data appears on the data output bus after 7 ADCCLK cycles. The green channel is synchronized on the rising edge of the first ADCCLK after the falling edge of VSAMP. The power-up default mode is for CDS sampling a CCD input (Pixel Clamp, Inverting Input, No Input Buffer).

1-Channel CDS Mode

The 1-Channel CDS mode allows high-speed acquisition and processing of a single channel. The timing, clamp and buffer configurations are similar to the 3-channel mode described previously. To select a single channel input the color bits of configuration register 1 must be set to the appropriate value. The A/D input will begin to track the selected color input on the next positive edge of ADCCLK. If the configuration is toggled from single color to 3-channel mode RGB scanning will not occur until the circuit is resynchronized on the falling edge of VSAMP.

3-Channel CIS/Sample and Hold Mode

The XRD9814/9816 also supports operation for Contact Image Sensor (CIS) and S/H applications. The green channel is synchronized on the rising edge of the first ADCCLK after the falling edge of VSAMP.

For DC coupled inputs the reference clamp and input buffer should be disabled and input polarity should be set to 1 (non-inverting). In this mode of operation the BSAMP input is connected to DGND and input sampling occurs on the falling edge of VSAMP.

When using AC coupled inputs the coupling capacitor must be clamped to the required common-mode input voltage when the signal source output is at a reference level. This can be accomplished by enabling the S/H Line clamp mode in configuration register 1 and clamping the input capacitor to the internal clamp voltage at the beginning of each line via the LCLMP input. The required width of the LCLMP signal is dependent on the value of the coupling capacitor, XRD9814/9816 clamp resistance, source output resistance and desired accuracy. This is explained further in Coupling Capacitor Requirements. If AC coupling is used the input buffer (configuration register 1) must be enabled to eliminate input-bias current errors inherent to the sampling process. The input buffer is not required or recommended in DC coupled applications.

1-Channel CIS/ Sample and Hold Mode

The 1-channel CIS S/H mode allows high-speed acquisition and processing of a single channel. The timing, clamp and buffer configurations are similar to the 3-channel mode with the exception that VSAMP timing option #2 is not supported. To select a single channel input the color bits of configuration register 1 must be set to the appropriate value. The A/D input will begin to track the selected color input on the next positive edge of ADCCLK. If the configuration is toggled from single color to 3-channel mode, RGB scanning will not occur until the circuit is resynchronized.

Power Supplies and Digital I/O

The XRD9814/9816 utilizes separate analog and digital power supplies. All digital I/O pins are 3V/5V compatible and allow easy interfacing to external digital ASICs. For single supply systems the analog and digital supply pins can be separately connected and bypassed to reduce noise coupling from digital to analog circuits.

Coupling Capacitor Requirements

The size of the external coupling capacitors depends on a number of items including the clamp mode, pixel rate, channel gain, black-level variation and system accuracy requirements. The major limitation for each clamp mode is shown below:

	CDS Mode	S/H Mode
Pixel Clamp (Buffer Disabled)	Black level pixel-pixel variation Initial charging	Not Applicable
Line Clamp (Buffer Enabled)	Initial charging Capacitor droop (common-mode range)	Initial charging Capacitor droop range) (accuracy error)

Table 5. Coupling Capacitor Limitation

Maximum Capacitance (CDS Pixel Mode)

Limitation #1

Since the black level is clamped during each pixel period the input bias current contributes an insignificant amount of droop during one pixel period. However, pixel-pixel variations in the black level may appear as errors . For a worst case gain of -10, 2V A/D FSR and 14-bit accuracy, one lsb of error corresponds to 12.5uV input-referred. Assuming 1mV of pixel-pixel variation in the black level, the maximumcoupling capacitor can be determined as a function of the clamping period and internal clamp resistance.

$$C\,max = \frac{tpwb}{(Rc + Rs)\cdot ln\left(\frac{1\,mV}{12.5\,\mu V}\right)}$$

where tpwb=clamp pulse width (BSAMP)
Rc=Clamp resistance
Rs=Signal source-resistance

For typical values of tpwb=65ns, Rc=100Ω, Rs=50Ω, C_{MAX}≤100pF.

Limitation #2

The maximum input capacitance may also be limited by the time allowed to charge the input capacitor to the difference between the black level and clamp levels. The capacitor value can be related to the number of clamp pulses allowed before the capacitor voltage settles to within the desired accuracy.

$$C\ max = \frac{tpwb \cdot N}{(Rc + Rs)\cdot ln\left(\frac{Vr - Vc}{V\varepsilon}\right)}$$

where tpwb = clamp pulse width (BSAMP)
N = number of pixels allowed to settle
Rc = clamp resistance
Rs = signal source-resistance
Vr = black level
Vc = XRD9814/9816 clamp voltage
Vε = error voltage

Assuming that Vr=5V, Vc=4V, Vε=12.5uV, Rc=100Ω, Rs=50Ω, tpwb=65ns and N=10 the maximum allowable input capacitor is equal to 384pF. In this case the input capacitance is limited by pixel-pixel changes in the black level (first calculation).

Minimum Capacitance (CDS Pixel Mode)

The minimum coupling capacitance is limited by parasitic effects including pin and board capacitance. A minimum value of 68pF is recommended.

Maximum Capacitance (CDS Line Mode)

Since the coupling capacitor is charged only at the beginning of each line and not clamped at each pixel, the pixel-pixel variation in the black level has no effect on the capacitor size. The maximum size will be limited by the number of clamp pulses, clamp pulse-width and number of lines allowed to charge to a given accuracy.

$$C\,max = \frac{N \cdot L \cdot tpwb}{(Rc + Rs)\cdot ln\left(\frac{Vr - Vc}{V\varepsilon}\right)}$$

where tpwb = clamp pulse width (BSAMP)
N = number of pixels allowed to settle
Rc = clamp resistance
Rs = signal source-resistance
Vr = black level
Vc = XRD9814/9816 clamp voltage
Vε = error voltage

Assuming that Vr=5V, Vc=4V, Ve=12.5uV, Rc=100Ω, Rs=500Ω, tpwb=65ns and N=10, the maximum allowable input capacitor is equal to 767pF.
If it is desired to settle within one line (L=1) for a given capacitor value, the number of clamp pulses or the clamp pulse-width must be increased using the above equation.

Minimum Capacitance (CDS Line Mode)

In general, the minimum value coupling capacitance is limited by the amount of droop which can occur before the input voltage range of the input amplifier is exceeded. The input capacitor droop is related to the input bias current by:

$$Vdroop = \frac{Ibias \cdot n \cdot T}{C}$$

where I_{bias} = input bias current
n = number of pixels per line
T = pixel period

If the minimum input voltage is allowed to equal the 0V input voltage of the XRD9814/9816, the maximum allowable droop will be equal to the clamp level minus the difference between the black and video levels. For example, if Vc=4V, and the CCD video output is -2V relative to the black level the maximum allowable droop is equal to 2V.

Using the previous equation and assuming T=500ns, n=3000

$$C\ min = \frac{10nA \cdot 3000 \cdot 500ns}{2V} = 7.5pF$$

Note: *These are the absolute minimum capacitor requirements. As stated for pixel-mode, a minimum value of 68pF is recommended.*

Minimum Capacitance (S/H Line Mode)

Unlike Line or Pixel CDS modes voltage droop across a line appears as an absolute error and is the dominant factor in determining the minimum coupling capacitor size.

$$C\ min = \frac{Ibias \cdot n \cdot T}{V\varepsilon}$$

where I_{bias}=input bias current
n=number of pixels per line

Assuming n=3000, T=500nS, I=10nA and Ve=12.5uV, the minimum required capacitor is 1.2uF.

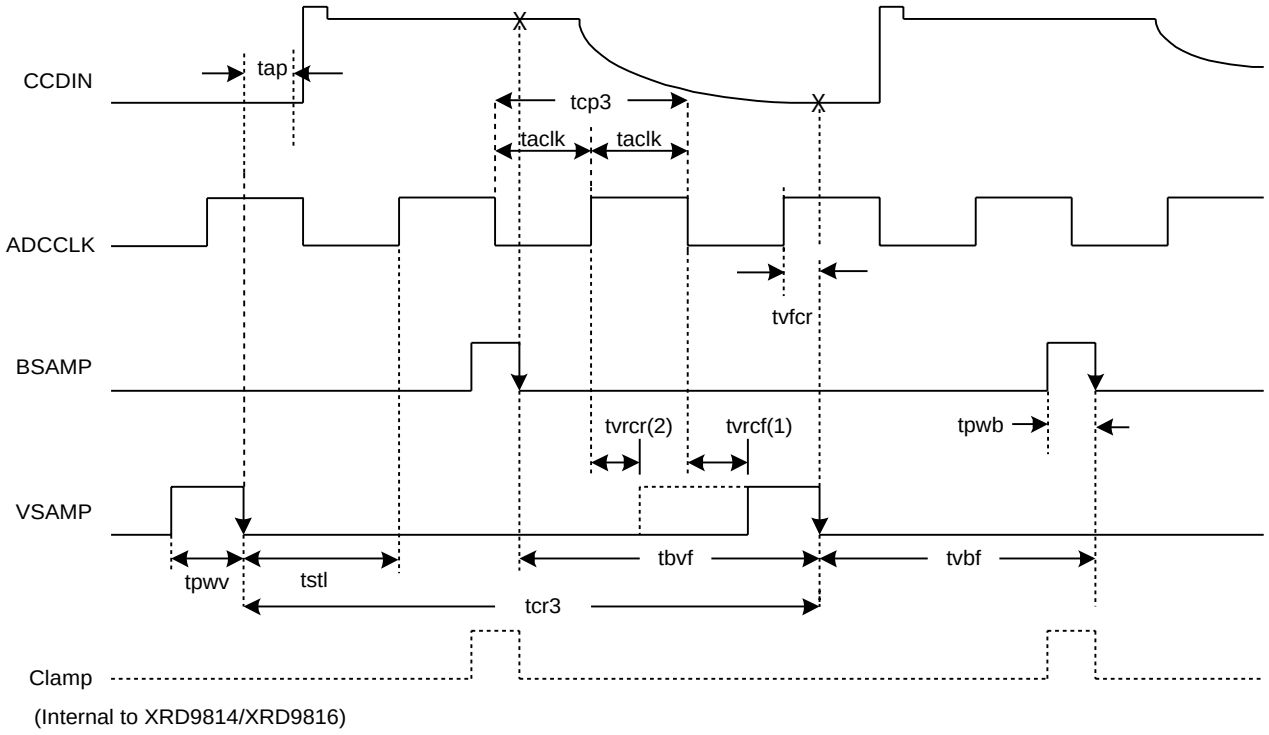
Maximum Capacitance (S/H Line Mode)

The maximum capacitance is determined by the amount of time allowed to charge the coupling capacitor. In order to minimize the charging time, the maximum capacitor can be set to the minimum value as previously calculated. In this case the time required to charge the capacitor is:

$$t = (Rs + Rc) \cdot C\ min \cdot ln\left(\frac{Vr - Vc}{V\varepsilon}\right)$$

where t = clamp pulse - width ($\overline{SYNCH}$)
Rc = clamp resistance
Rs = signal source - resistance
Vr = input reference level
Vc = XRD9814/9816 clamp voltage
Vε = error voltage
Cmin = coupling capacitor

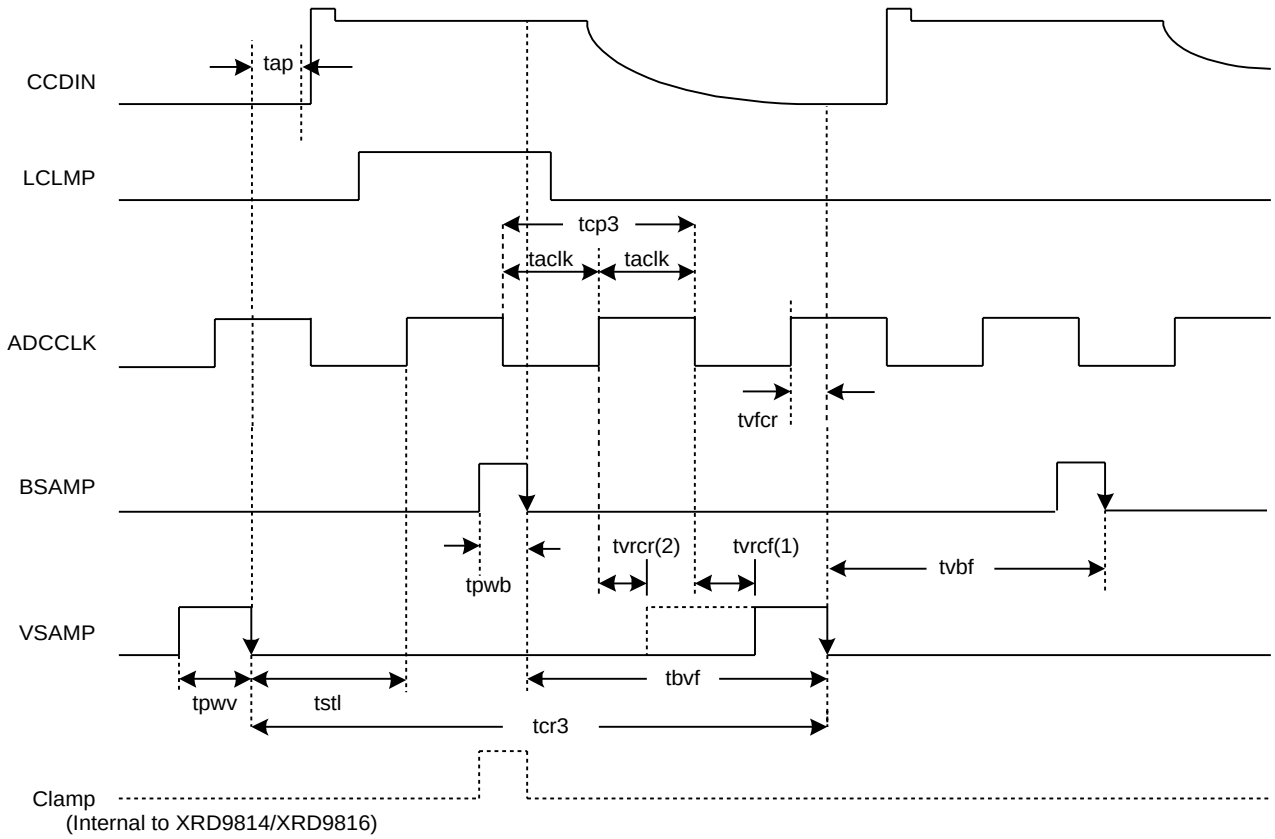
Assuming that Vr=.5 Vc=0V, Vε=12.5uV, Rc=100Ω, Rs=500Ω and C=1.2uF, the minimum clamp period is equal to 1.9mS.



Notes: *(1) VSAMP Timing Option #1 uses tvrcf (tvrcr is not required)*
(2) VSAMP Timing Option #2 uses tvrcr (tvrcf is not required)
VSAMP Timing Option #2 only available in 3-Channel Operation

Figure 3. 3-Channel CDS Mode - Pixel Clamp

Configuration Register #1: Pixel Clamp (PB7=0, PB6=0)
RGB (PB4=0, PB3=0)
Inverted Polarity (PB2=0)
Input Buffer Disabled (PB1=0)



Notes: *(1) VSAMP Timing Option #1 uses tvrcf (tvrcr is not required)*
(2) VSAMP Timing Option #2 uses tvrcr (tvrcf is not required)
VSAMP Timing Option #2 only available in 3-Channel Operation

Figure 4. 3-Channel CDS Mode - Line Clamp

Configuration Register #1: CDS Line (PB7=0, PB6=1)
RGB (PB4=0, PB3=0)
Inverted Polarity (PB2=0)
Input Buffer Enabled (PB1=1)

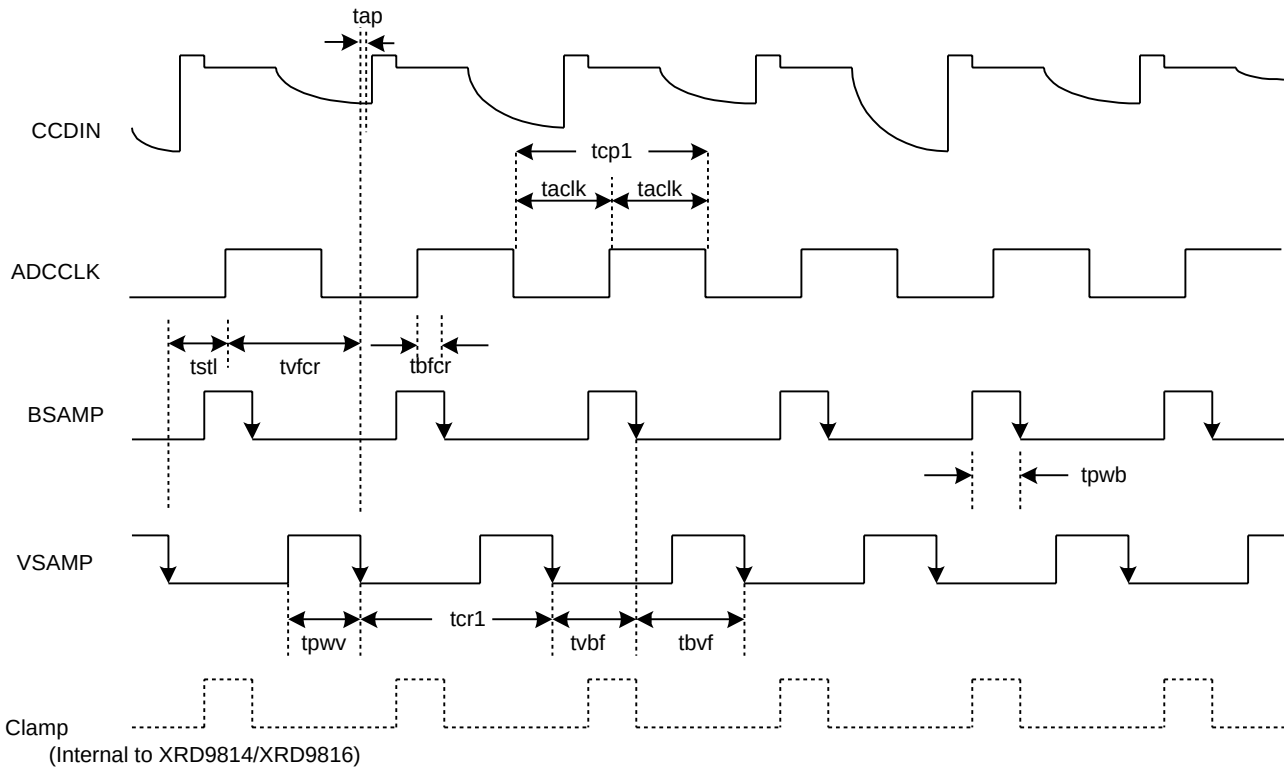
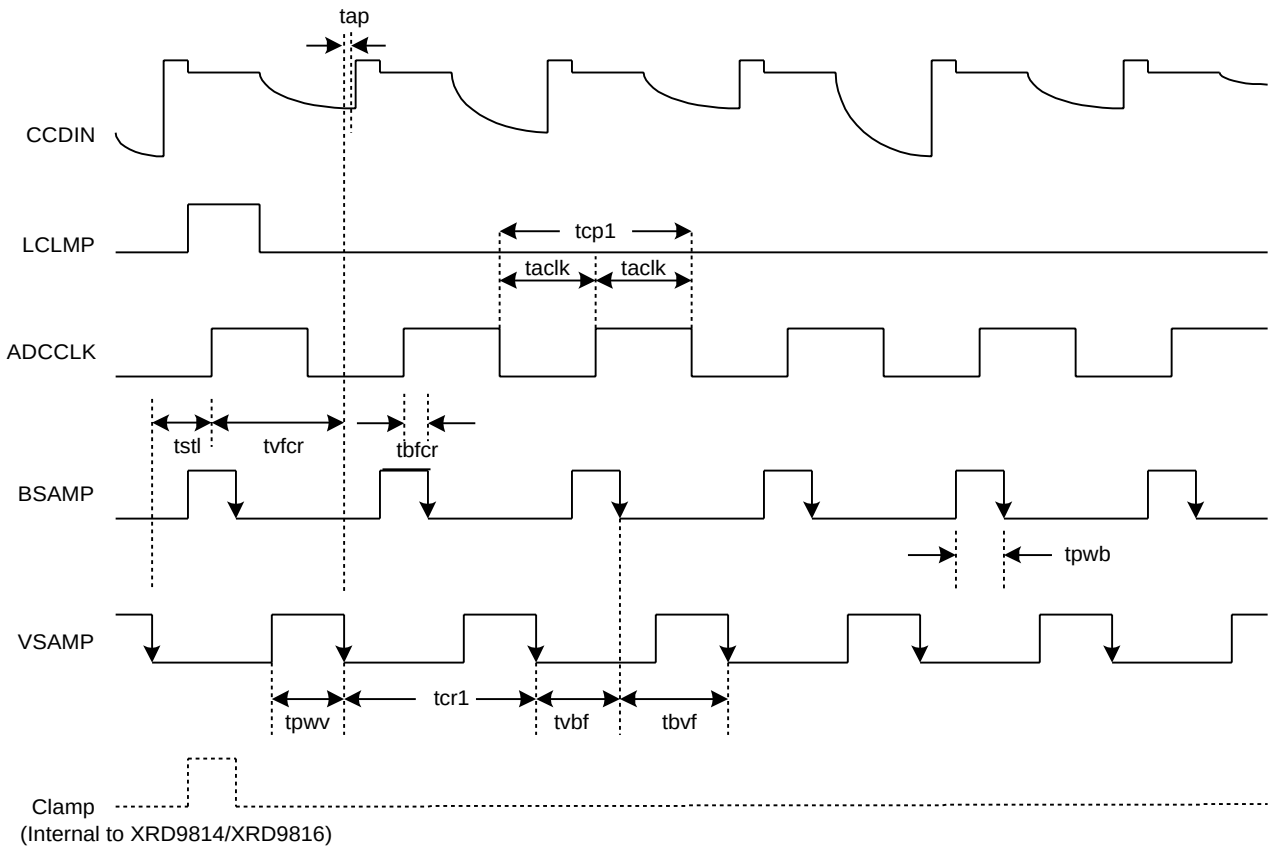


Figure 5. 1-Channel CDS Mode - Pixel Clamp

Configuration Register #1: Pixel Clamp (PB7=0, PB6=0)
Single Channel (PB4, PB3-RED 01, GRN 10, BLU 11)
Inverted Polarity (PB2=0)
Input Buffer Disabled (PB1=0)



Notes: *(1) Only VSAMP timing option #1 is supported in 1-channel mode*

Figure 6. 1-Channel CDS Mode - Line Clamp

Configuration Register #1: CDS Line Clamp (PB7=0, PB6=1)
Single Channel (PB4, PB3-RED 01, GRN 10, BLU 11)
Inverted Polarity (PB2=0)
Input Buffer Enabled (PB1=1)

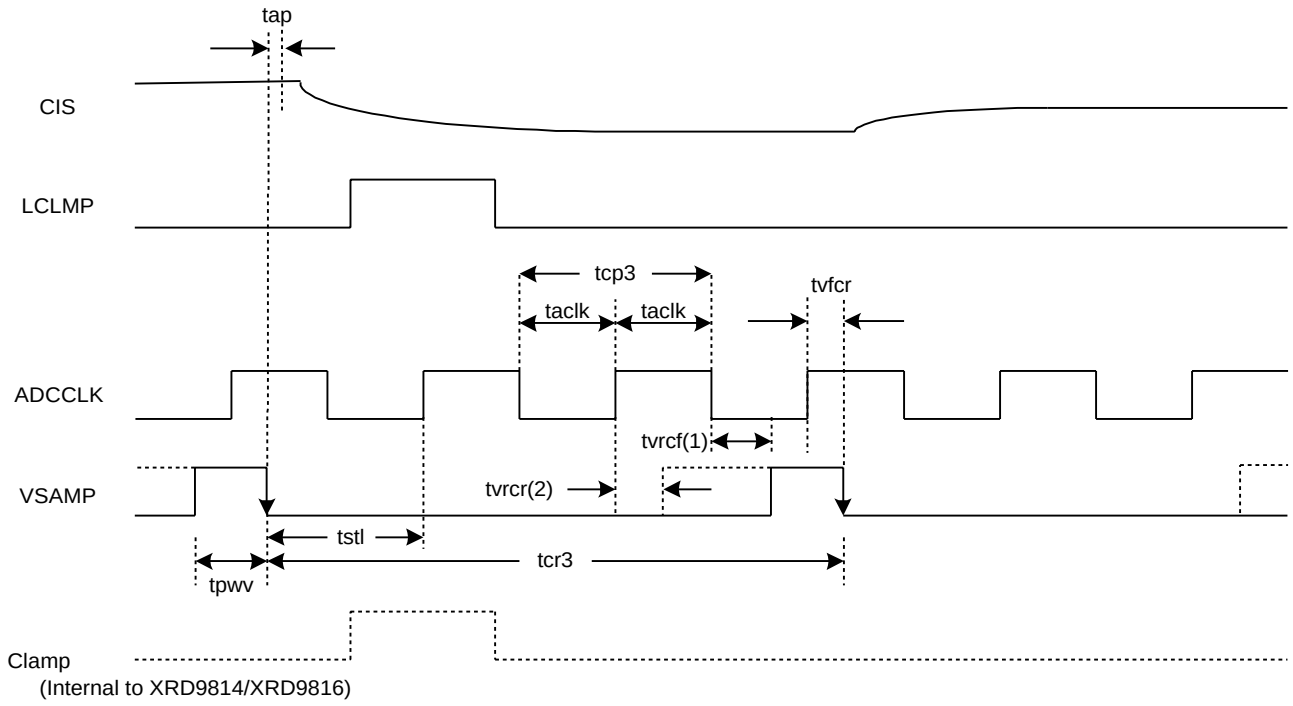
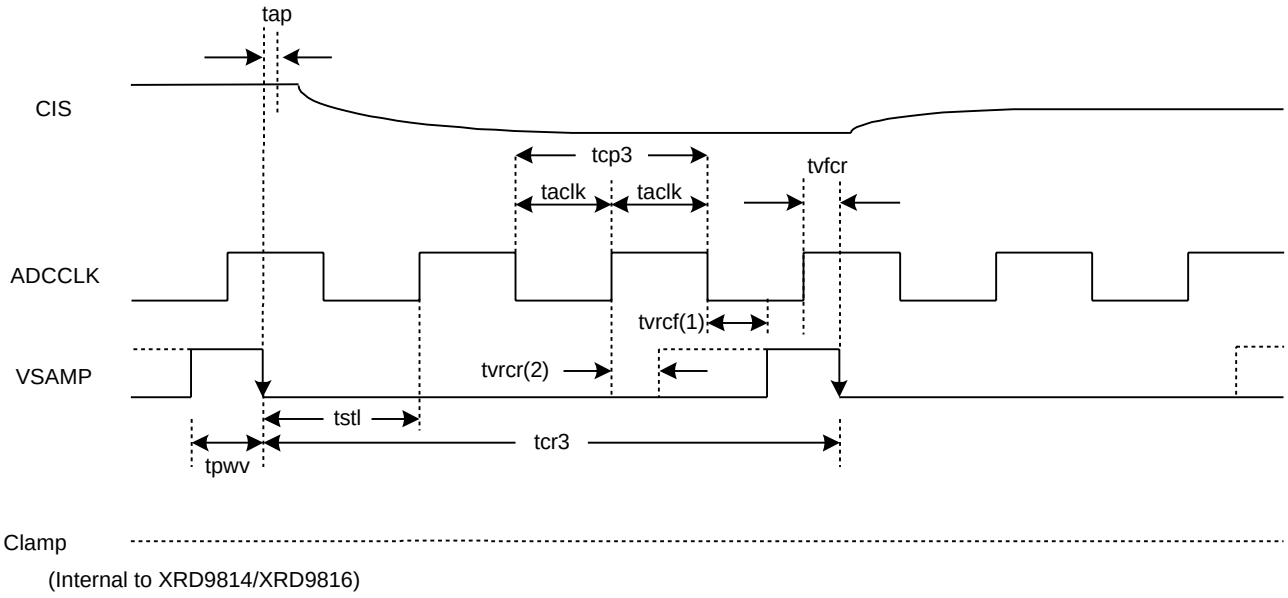


Figure 7. 3-Channel S/H Mode - Line Clamp (AC Coupled)

Configuration Register #1: S/H Line Clamp (PB7=1, PB6=1)
RGB (PB4=0, PB3=0)
Non-Inverted Polarity (PB2=1)
Input Buffer Enabled (PB1=1)



Notes: *(1) VSAMP Timing option #1 uses tvrcf (tvrcr is not required)*
(2) VSAMP Timing option #2 uses tvrcr (tvrcf is not required)

Figure 8. 3-Channel S/H Mode - No Clamp (DC Coupled)

Configuration Register #1: S/H No Clamp (PB7=1, PB6=0)
RGB (PB4=0, PB3=0)
Non-Inverted Polarity (PB2=1)
Input Buffer Disabled (PB1=0)

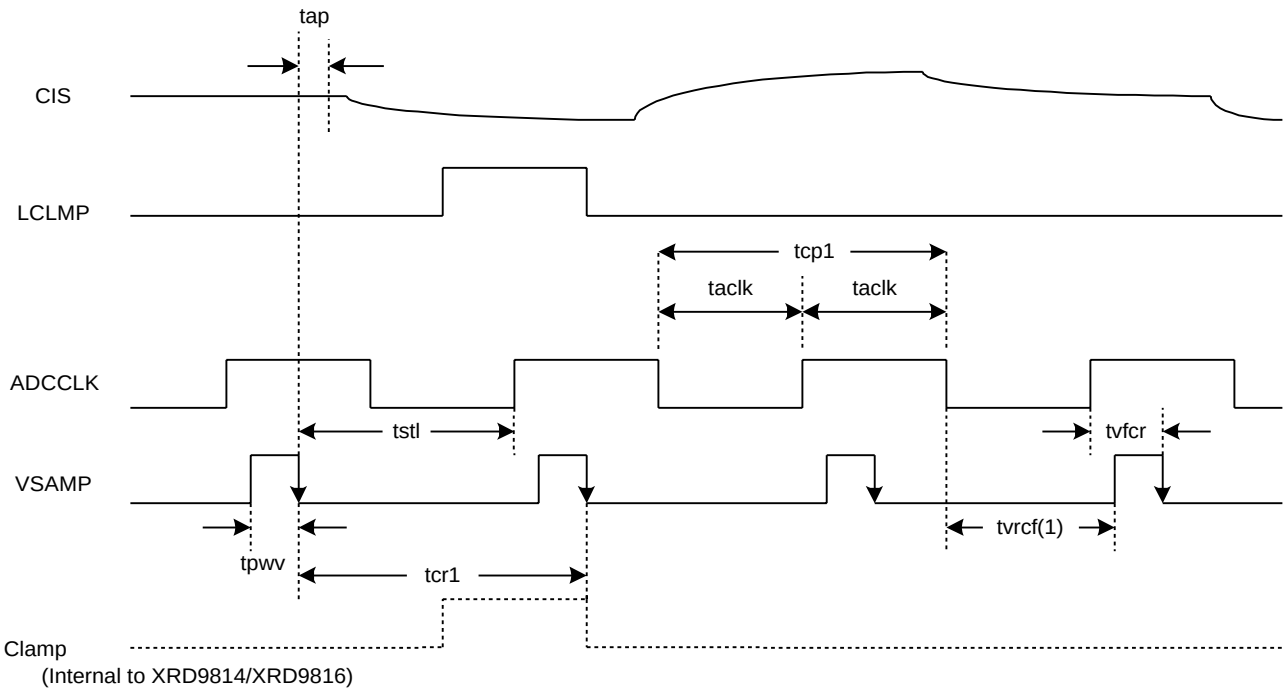
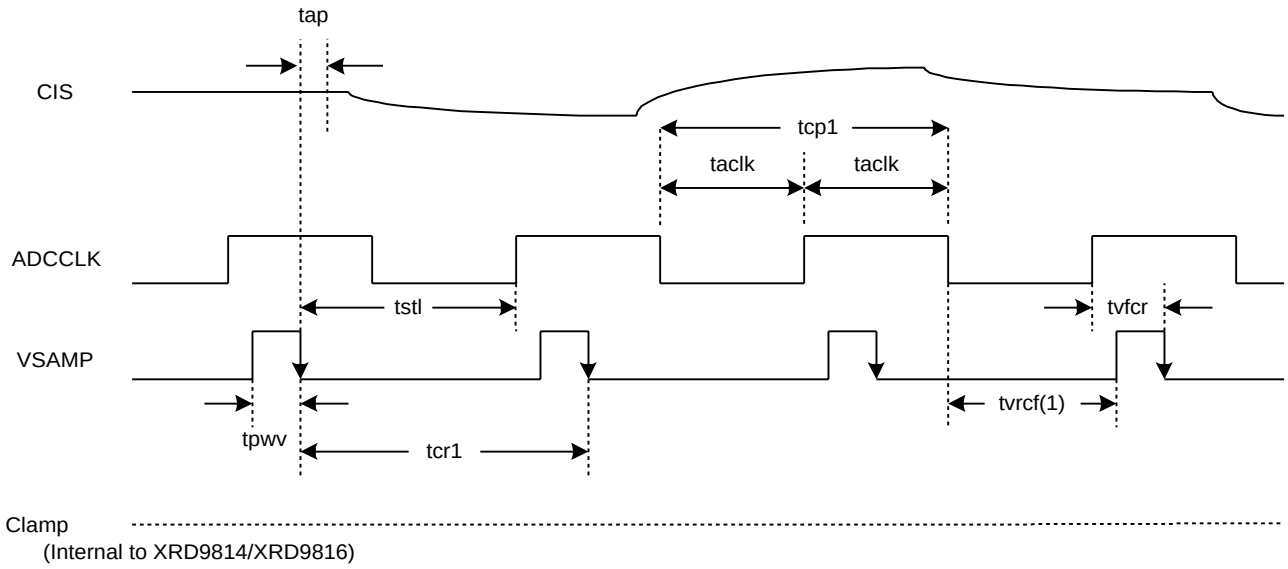


Figure 9. 1-Channel S/H Mode - Line Clamp (AC Coupled)

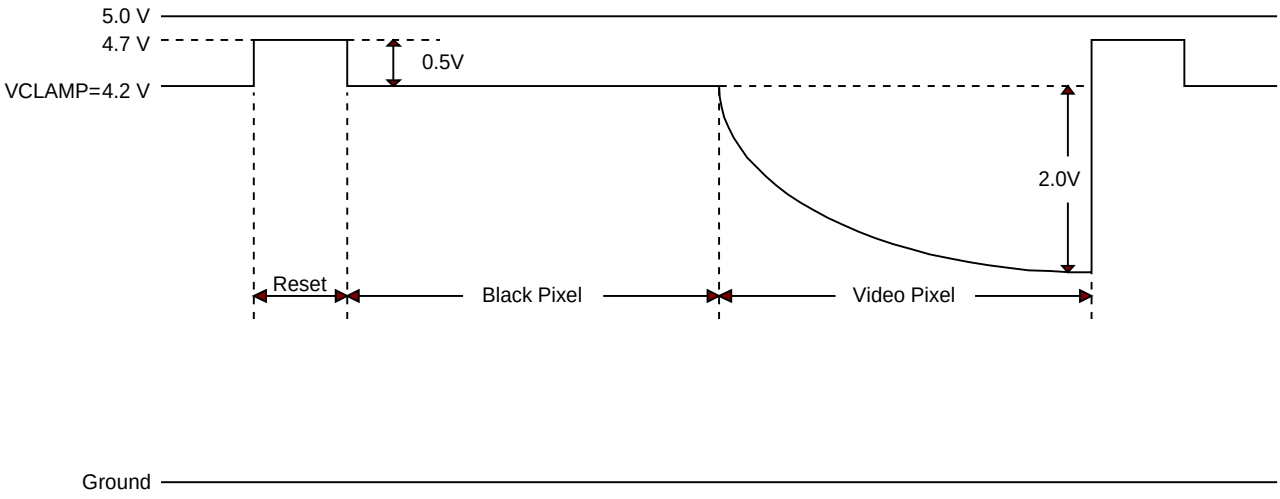
Configuration Register #1: S/H Line Clamp (PB7=1, PB6=1)
Single Channel (PB4, PB3-RED 01, GRN 10, BLU 11)
Non-Inverted Polarity (PB2=1)
Input Buffer Enabled (PB1=1)



Notes: *(1) Only VSAMP timing option #1 is supported in 1-channel mode*

Figure 10. 1-Channel S/H Mode - No Clamp (DC Coupled)

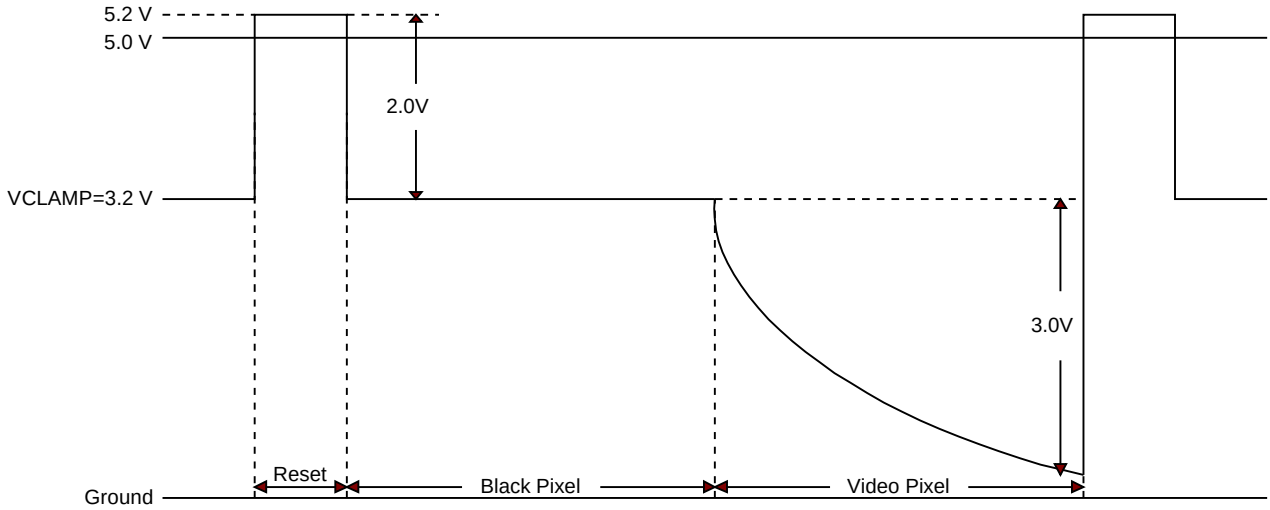
Configuration Register #1: S/H No Clamp (PB7=1, PB6=0)
Single Channel (PB4, PB3-RED 01, GRN 10, BLU 11)
Non-Inverted Polarity (PB2=1)
Input Buffer Disabled (PB1=0)



Typical Operation, VCLAMP = 4.2V, (PB4 = 0, PB3 = 0)

VRESET = 0.5V, VVIDEO = 2.0V = FSR of XRD9814/9816

Figure 11. VCLAMP Setting Example 1



Marginal Operation, VCLAMP = 3.2V, (PB4 = 1, PB3 = 0)

VRESET = 2.0V, VVIDEO = 3.0V = FSR of XRD9814/9816

Notes (3) Input signal does not exceed VDD + 0.3V (Reset)

Notes (4) Input signal does not go below 0V (Video pixel)

Figure 12. VCLAMP Setting Example 2

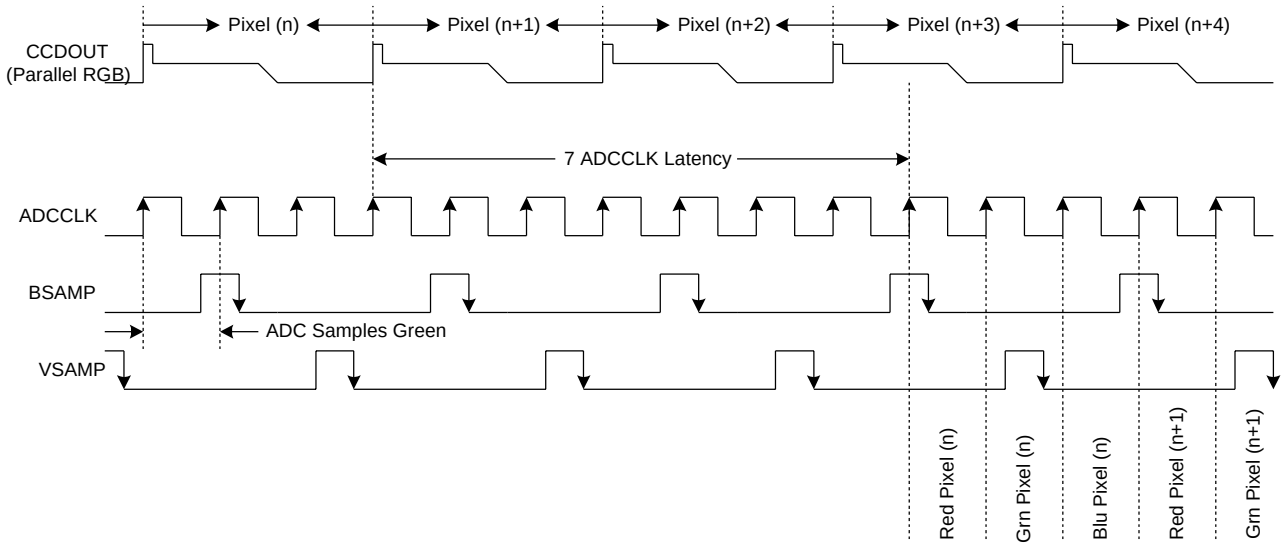


Figure 13. 3-Channel CDS Pixel Clamp Synchronization and ADC Latency Timing

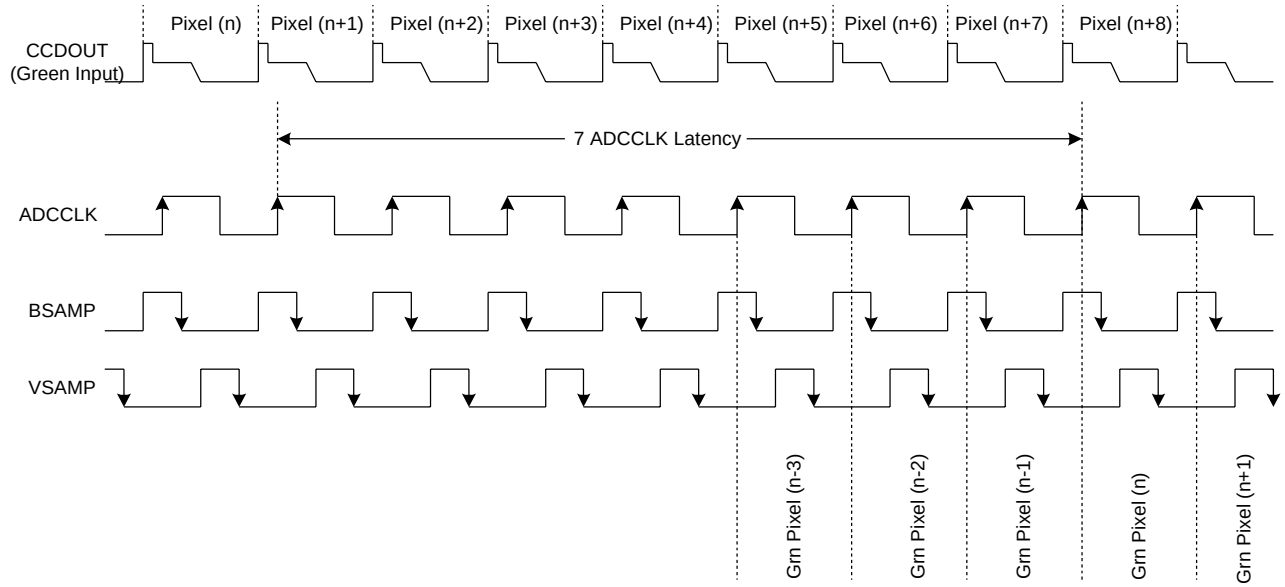


Figure 14. 1-Channel CDS Pixel Clamp Synchronization and ADC Latency Timing

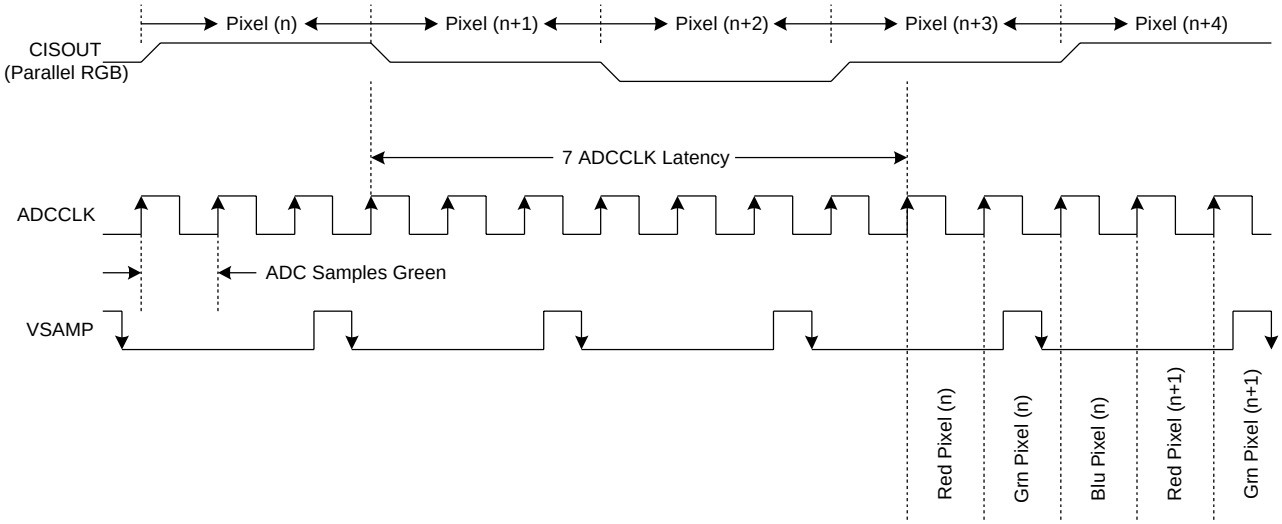


Figure 15. 3-Channel S/H Synchronization and ADC Latency Timing

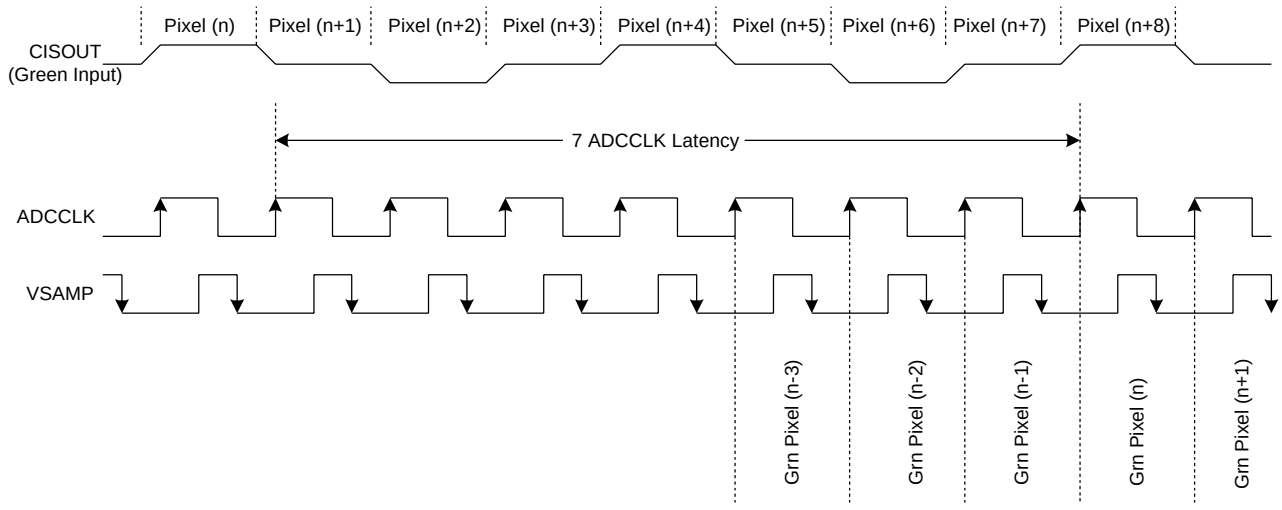


Figure 16. 1-Channel S/H Synchronization and ADC Latency Timing

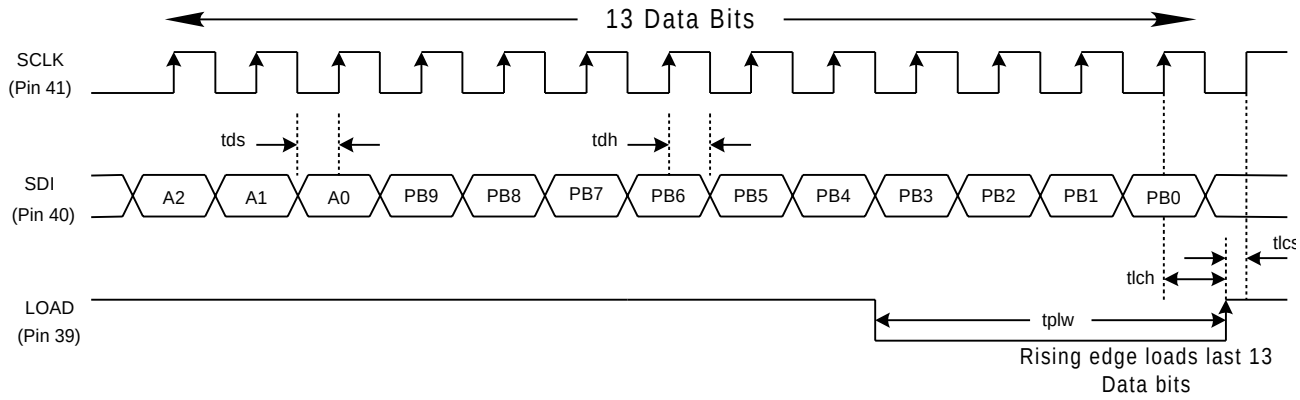


Figure 17. Write Timing (INSEL = 0)

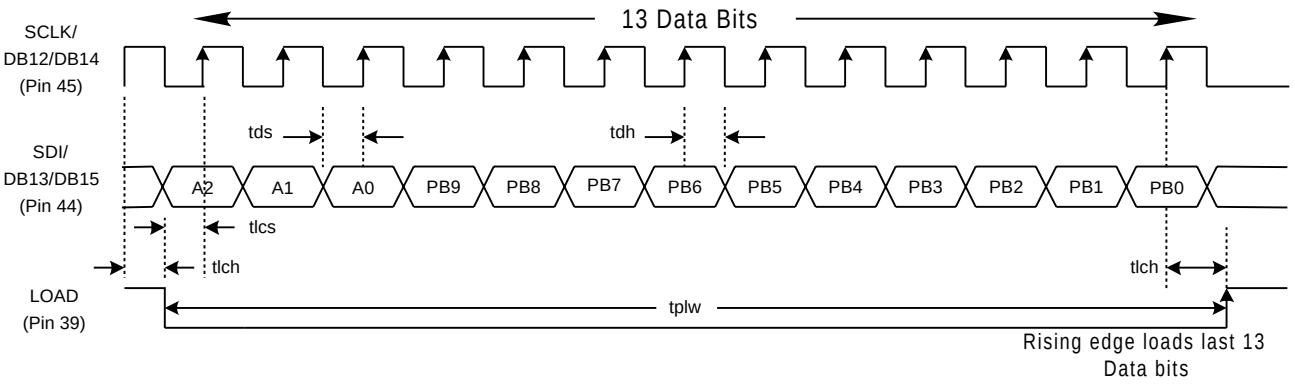


Figure 18. Write Timing (INSEL = 1)

XRD9814/9816 Read Back Timing

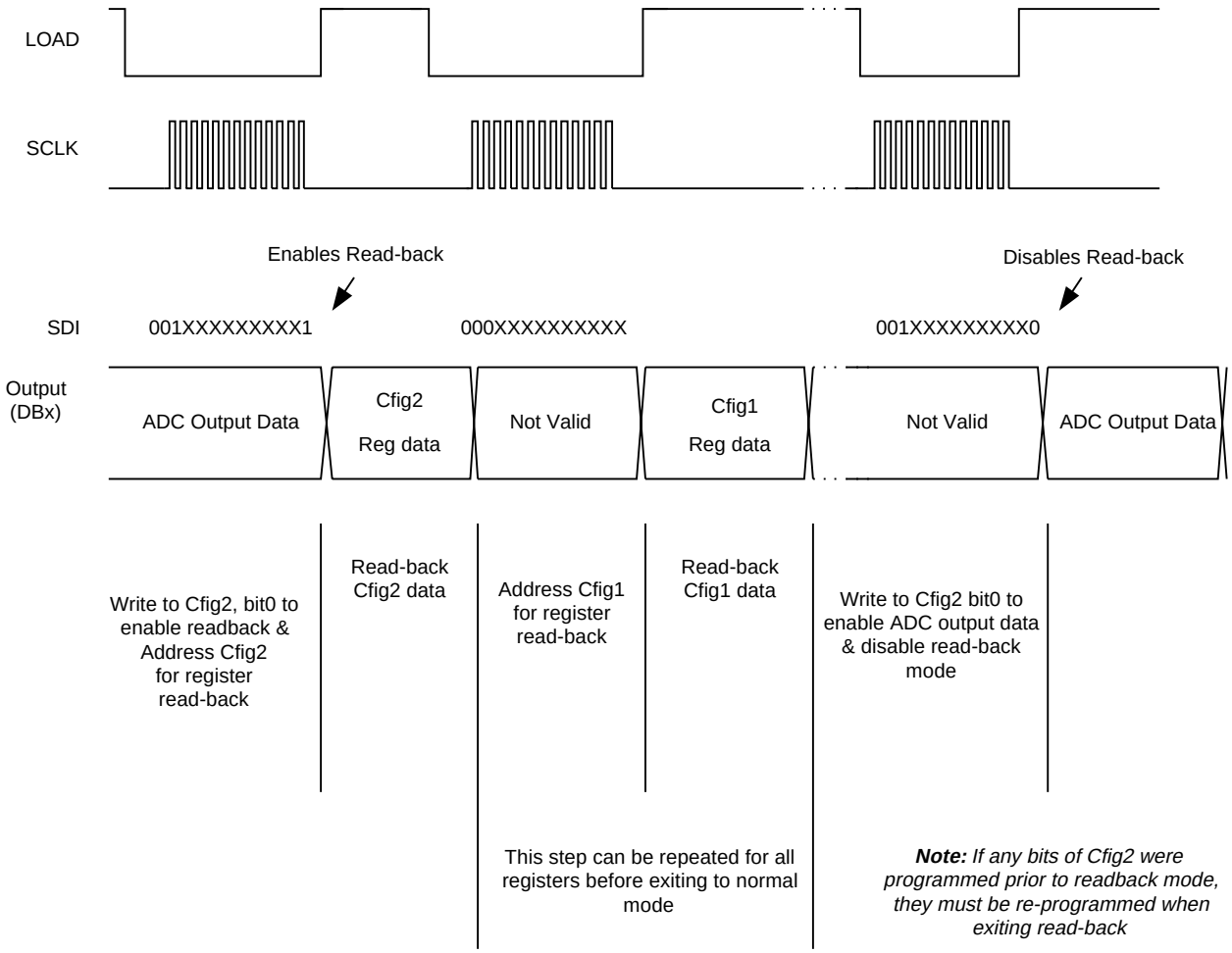


Figure 19. XRD9814/9816 Read-Back Timing

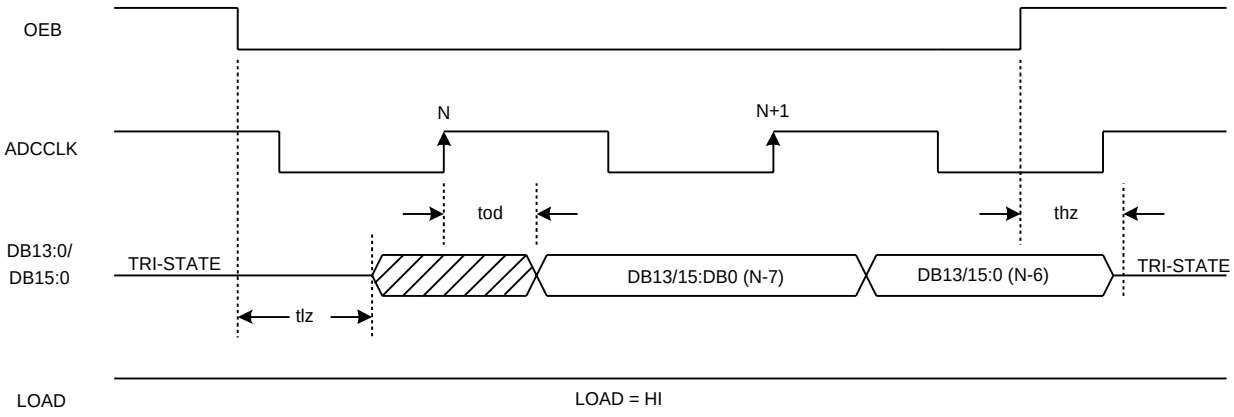


Figure 20. ADC Digital Output Timing (OUTSEL = 0)

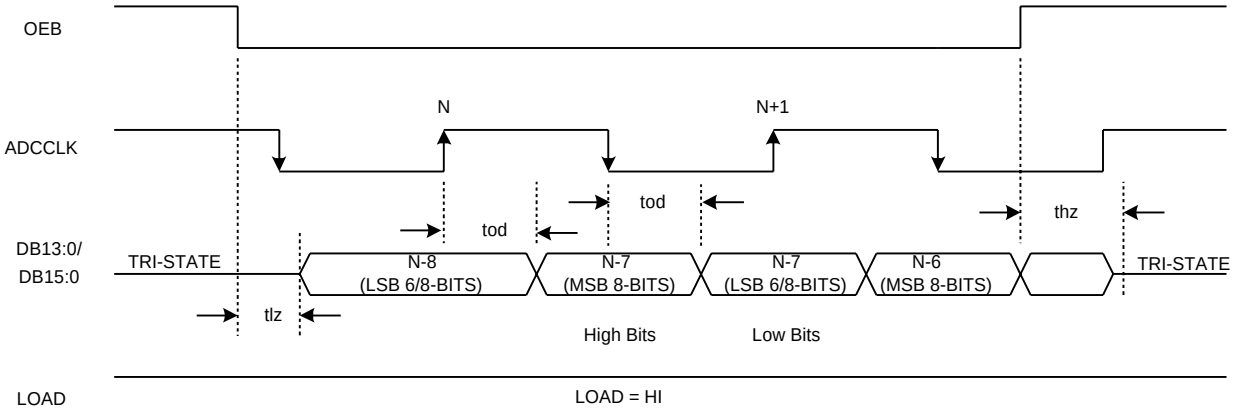


Figure 21. ADC Digital Output Timing (OUTSEL = 1)

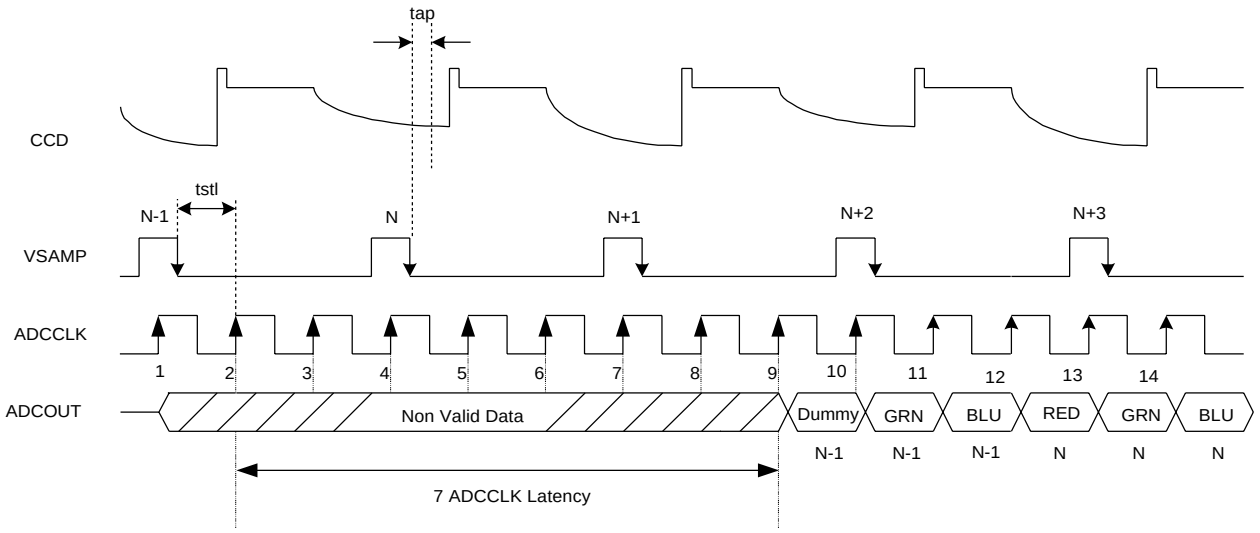


Figure 22. XRD9814/XRD9816 Pipeline Latency

ADCCLK/SYNCHRONIZATION EVENTS

① Necessary / No Sampling Events Occur

② Beginning of Synchronization / Samples Green (N-1) / Converts Unkown Dummy Value

③ Samples Blue (N-1) / Converts Green (N-1)

④ Samples Red (N) / Converts Blue (N-1)

⑤ Synchronization / Samples Green (N) / Converts Red (N)

⑥ Samples Blue (N) / Converts Green (N)

⑦ Samples Red (N+1) / Converts Blue (N)

⑧ Synchronization / Samples Green (N+1) / Converts Red (N+1)

⑨ Dummy Pixel (N-1) Valid Generated From ADCCLK #2

⑩ GRN Pixel (N-1) Valid Generated From ADCCLK #3

⑪ BLU Pixel (N-1) Valid Generated From ADCCLK #4

⑫ RED Pixel (N) Valid Generated From ADCCLK #5

⑬ GRN Pixel (N) Valid Generated From ADCCLK #6

⑭ BLU Pixel (N) Valid Generated From ADCCLK #7

Note: *Green Channel is Synchronized on the First Rising Edge of ADCCLK After the Falling Edge of VSAMP*

Application Notes

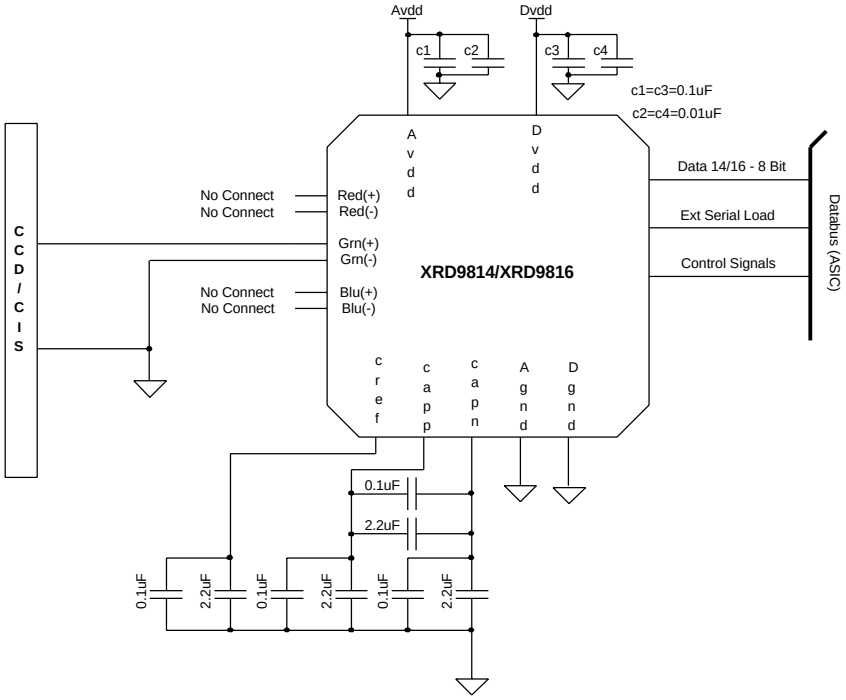


Figure 23. Single Channel DC-Coupled Mode

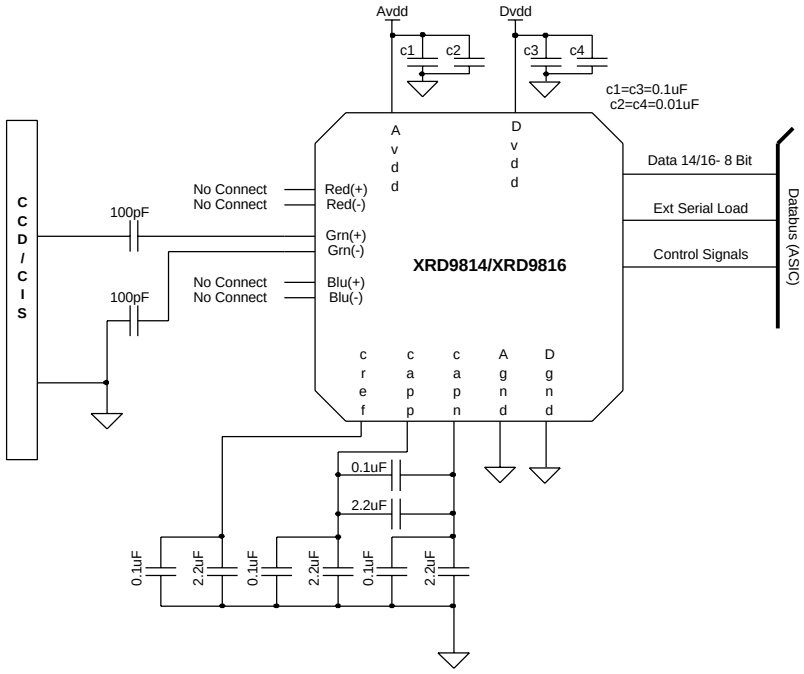


Figure 24. Single Channel AC-Coupled Mode

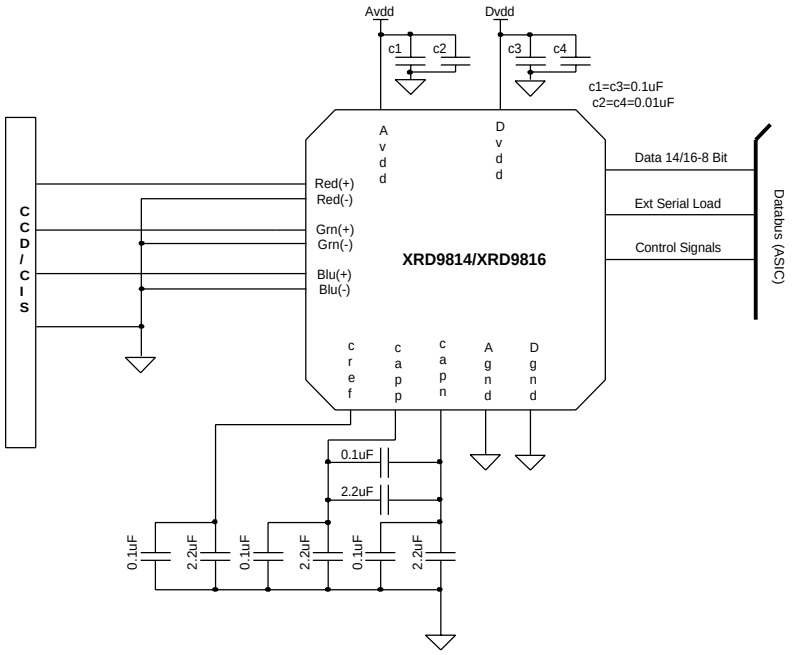


Figure 25. Triple Channel DC-Coupled Mode

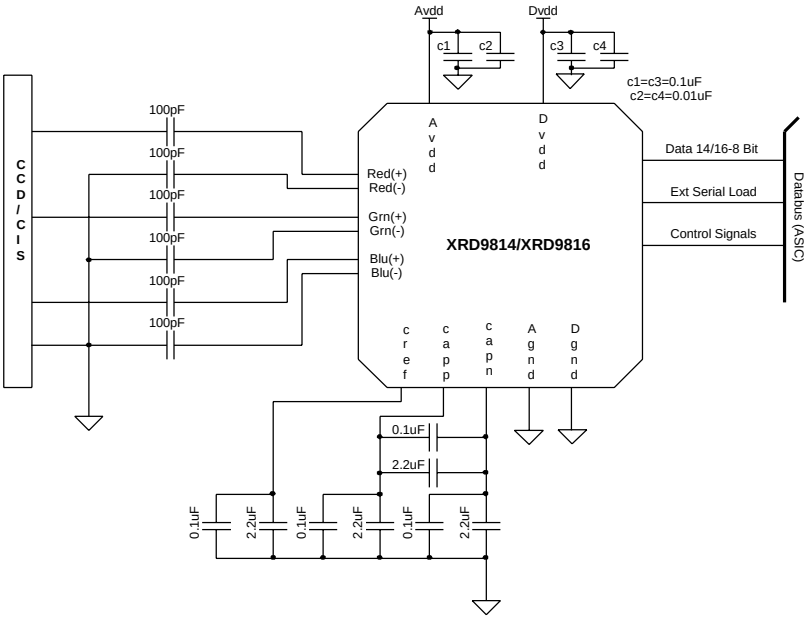


Figure 26. Triple Channel AC-Coupled Mode

INSEL/OUTSEL Data Output Format

There are two control signals for setting the output data format and the serial load control. INSEL is used to select the mode for programming the serial port. To use the external pins sdi, sclk and load, INSEL must be low (Figure 17). When INSEL is set to high, DB13/ sdi and DB12/sclk become inputs through the bi-directional output bus to load the internal control registers (Figure 18). The load pin is still used to latch the data. This helps to reduce the pin count requirements for the ASIC that drives the XRD9814/9816. OUTSEL is used to select the output data format of the XRD9814/9816. The XRD9814/9816 supports 14/16-bit parallel and 8-bit nibble output modes. When OUTSEL is low, the output bus is standard 14/16-bit parallel (Figure 20). To use the 8-bit nibble output mode, OUTSEL must be set high (Figure 21). In either 14/16-bit or 8-bit nibble applications, the output bus is tri-stated when the bi-directional serial load signal is pulled low.

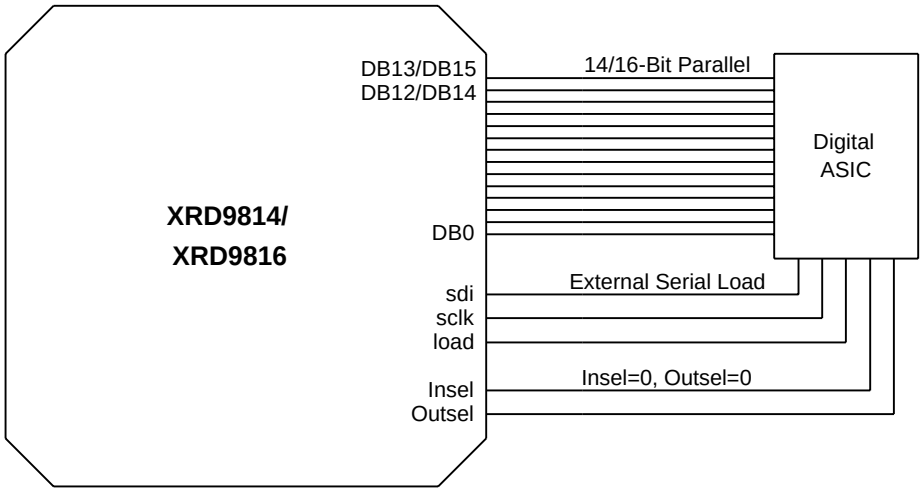


Figure 27. 14/16-Bit Output (OUTSEL=0), External Serial Load (INSEL=0)

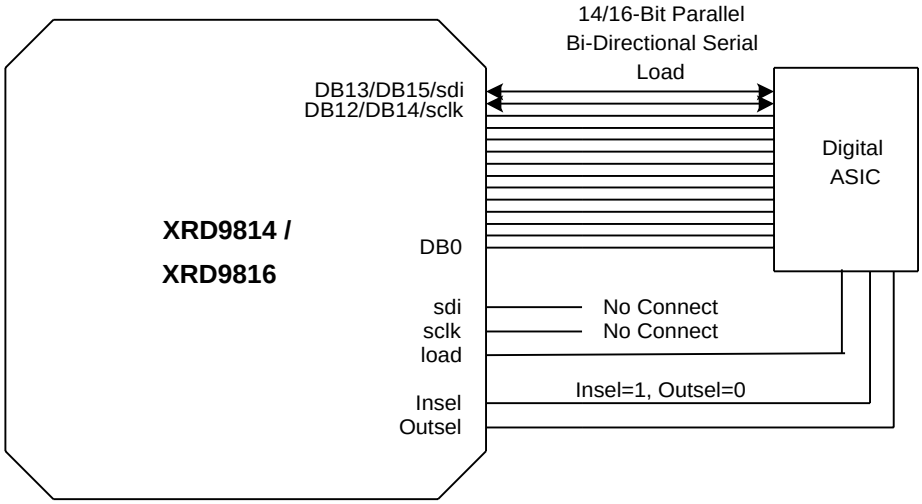


Figure 28. 14/16-Bit Output (OUTSEL=0), Bi-Directional Serial Load (INSEL=1)

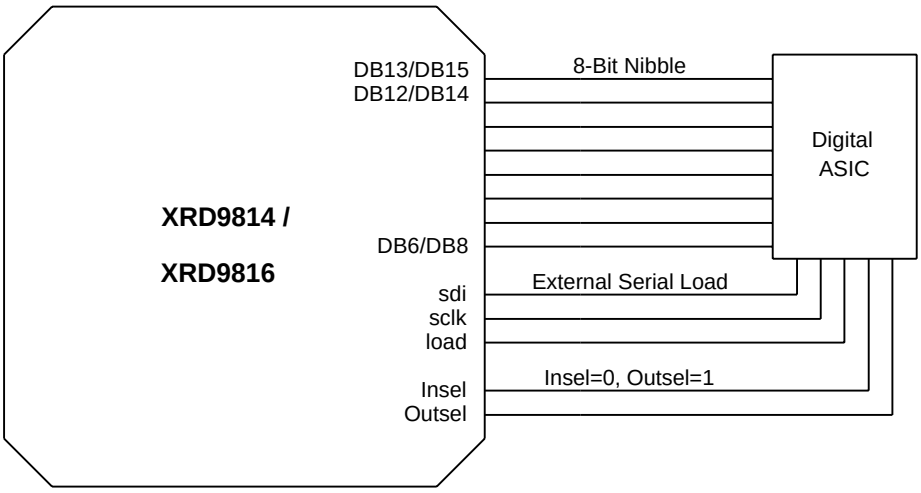


Figure 29. 8-Bit Nibble Output (OUTSEL=1), External Serial Load (INSEL=0)

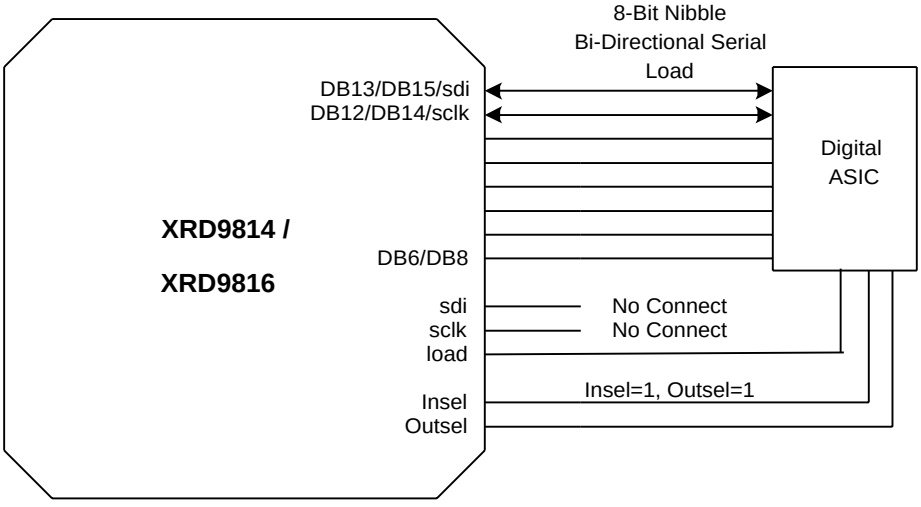
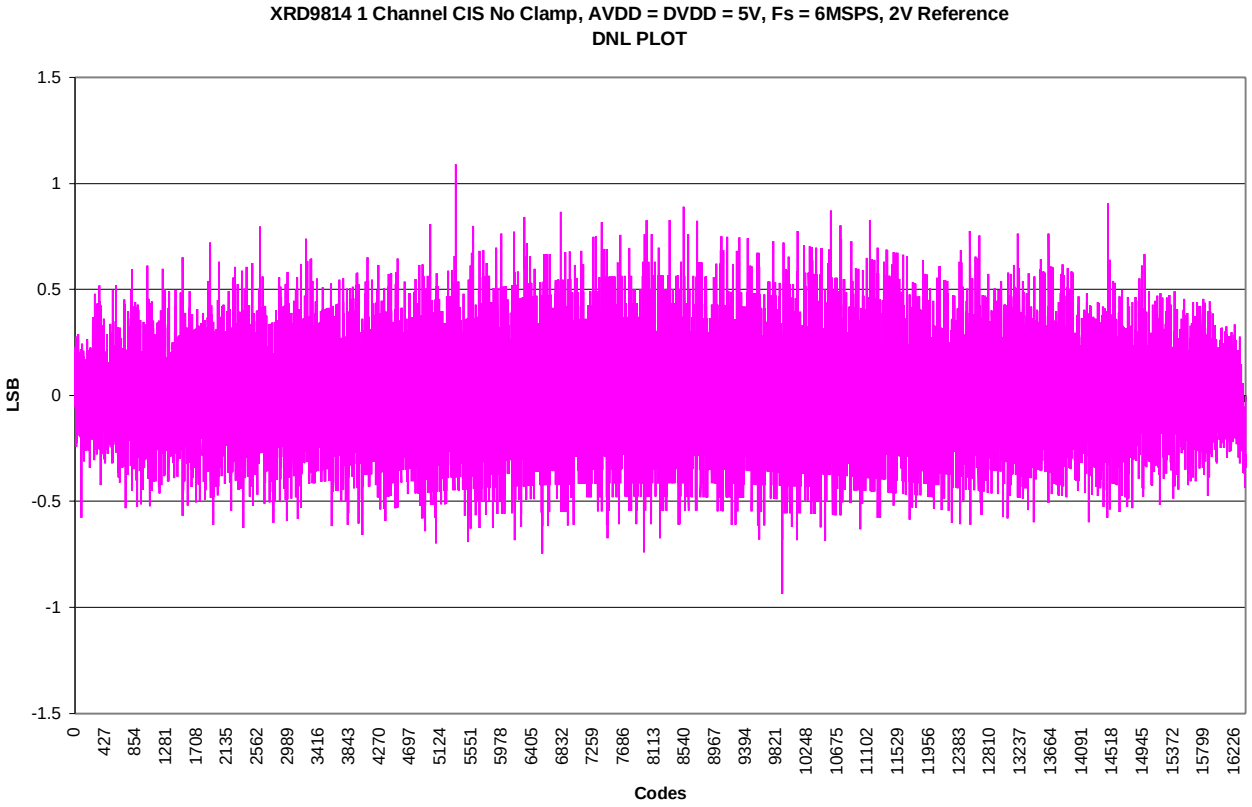
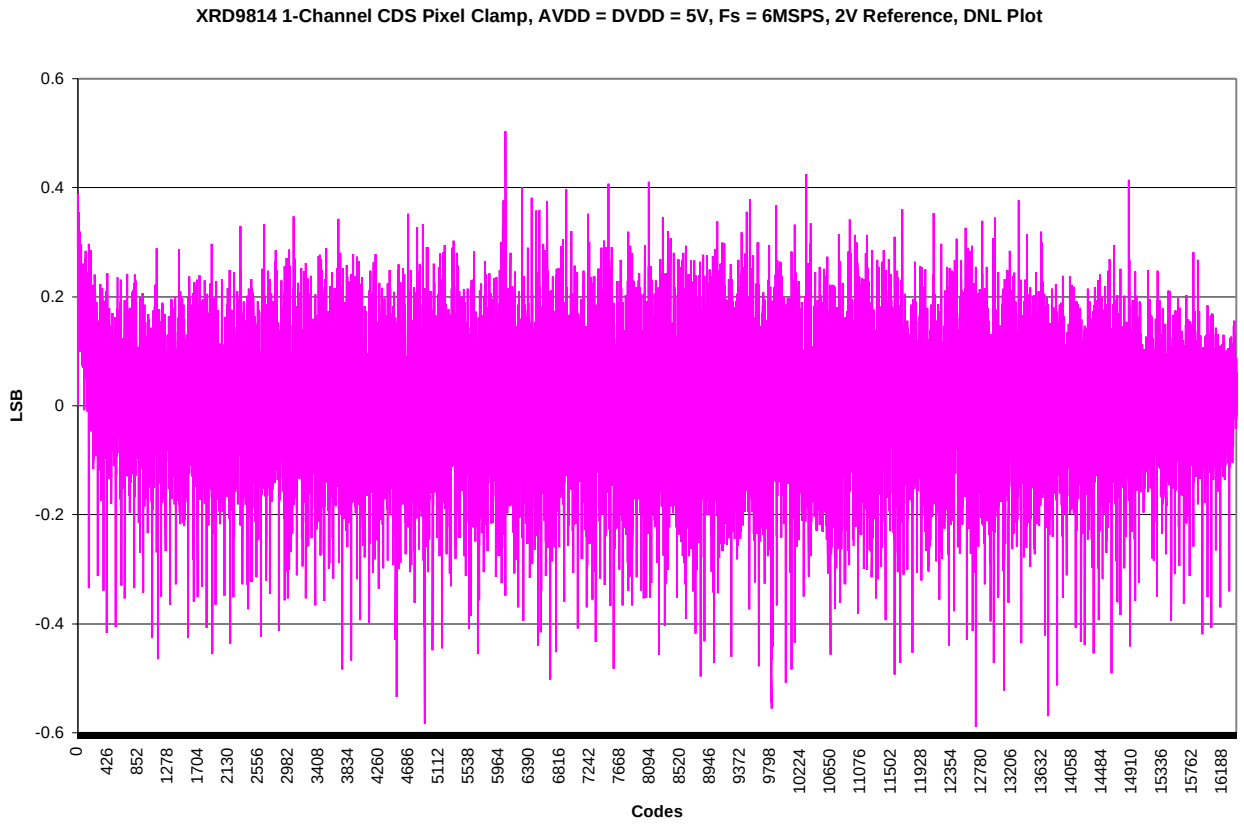


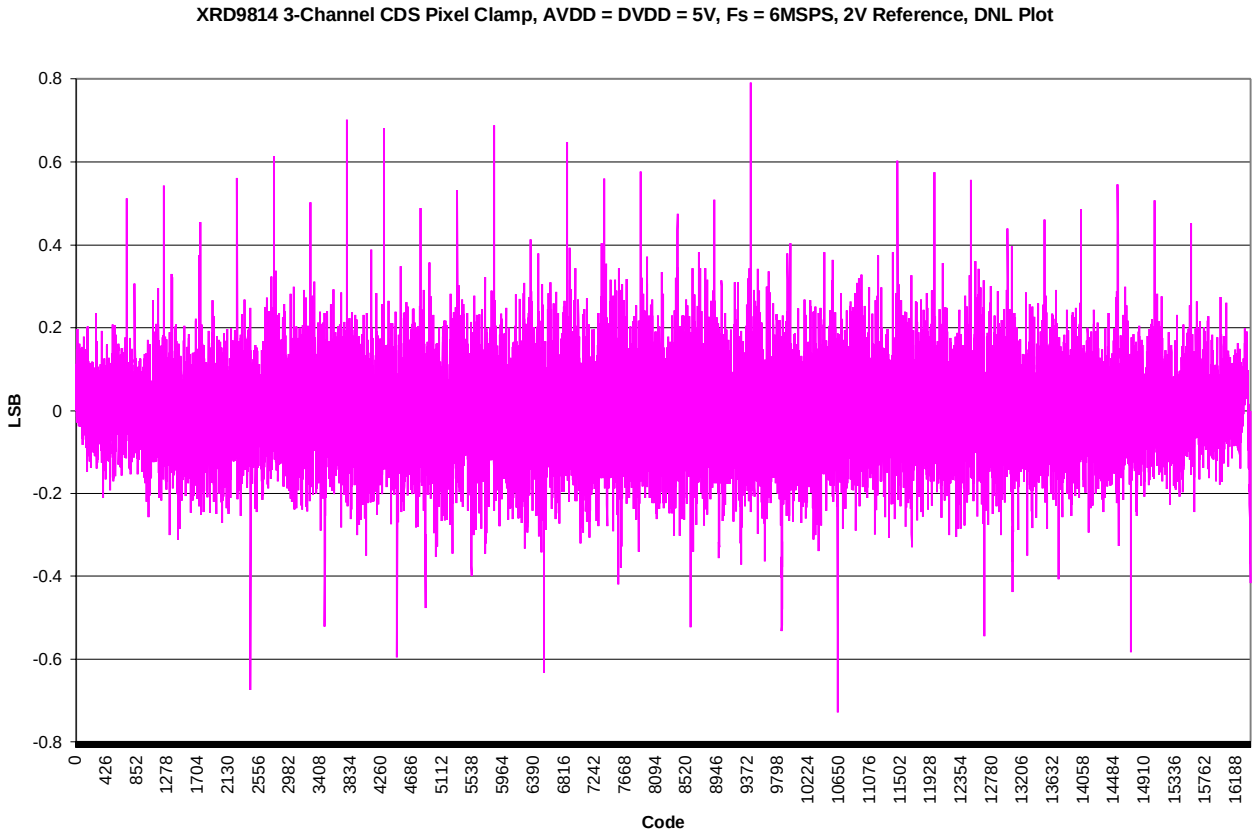
Figure 30. 8-Bit Nibble Output (OUTSEL=1), Bi-Directional Serial Load (INSEL=1)



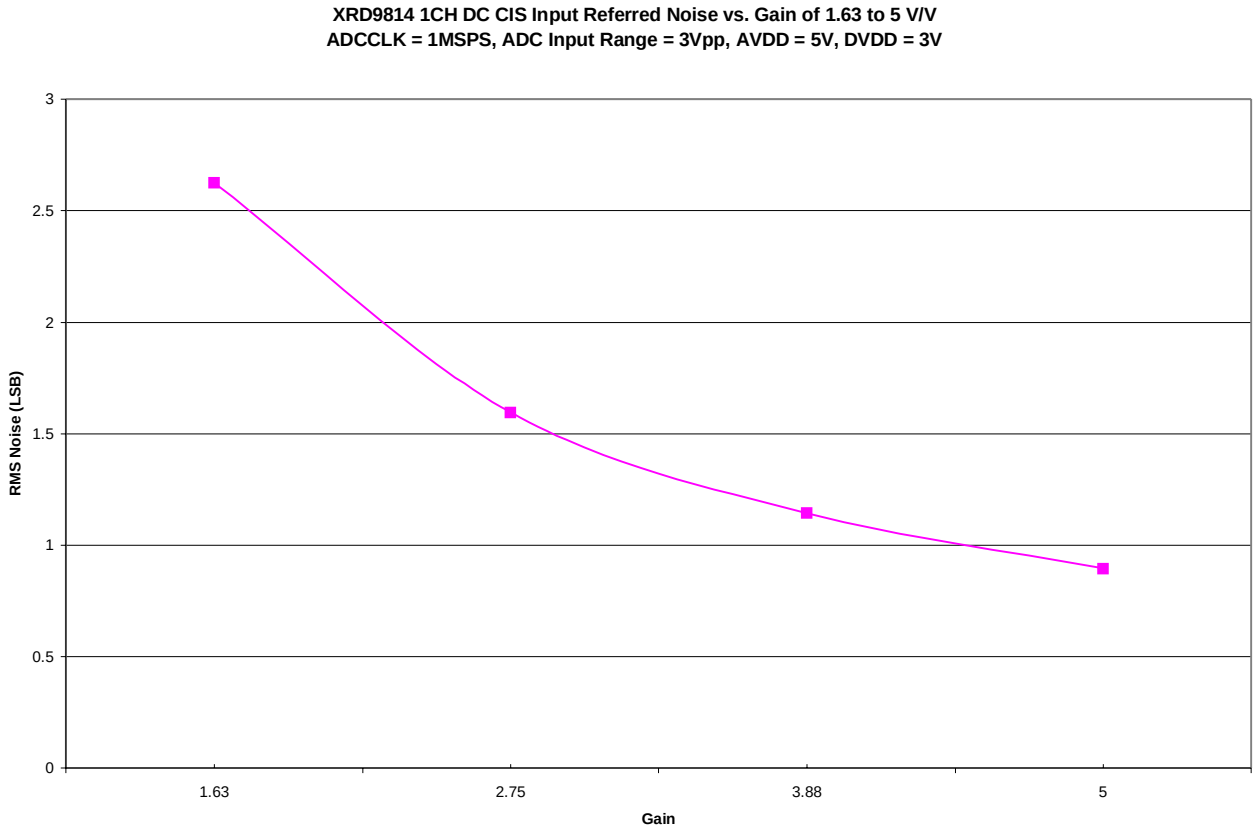
Graph 1. XRD9814 1-Channel CIS S/H No Clamp DNL Plot



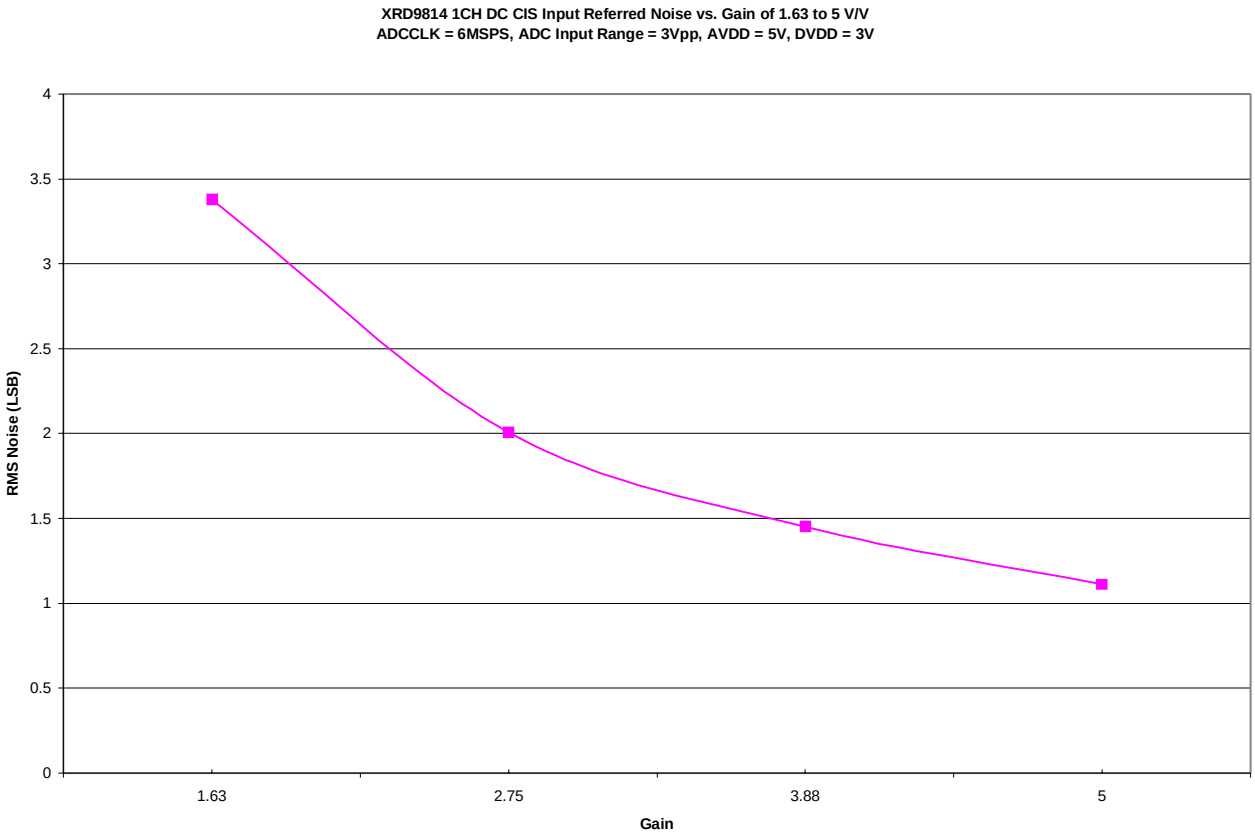
Graph 2. XRD9814 1-Channel CDS Pixel Clamp DNL Plot



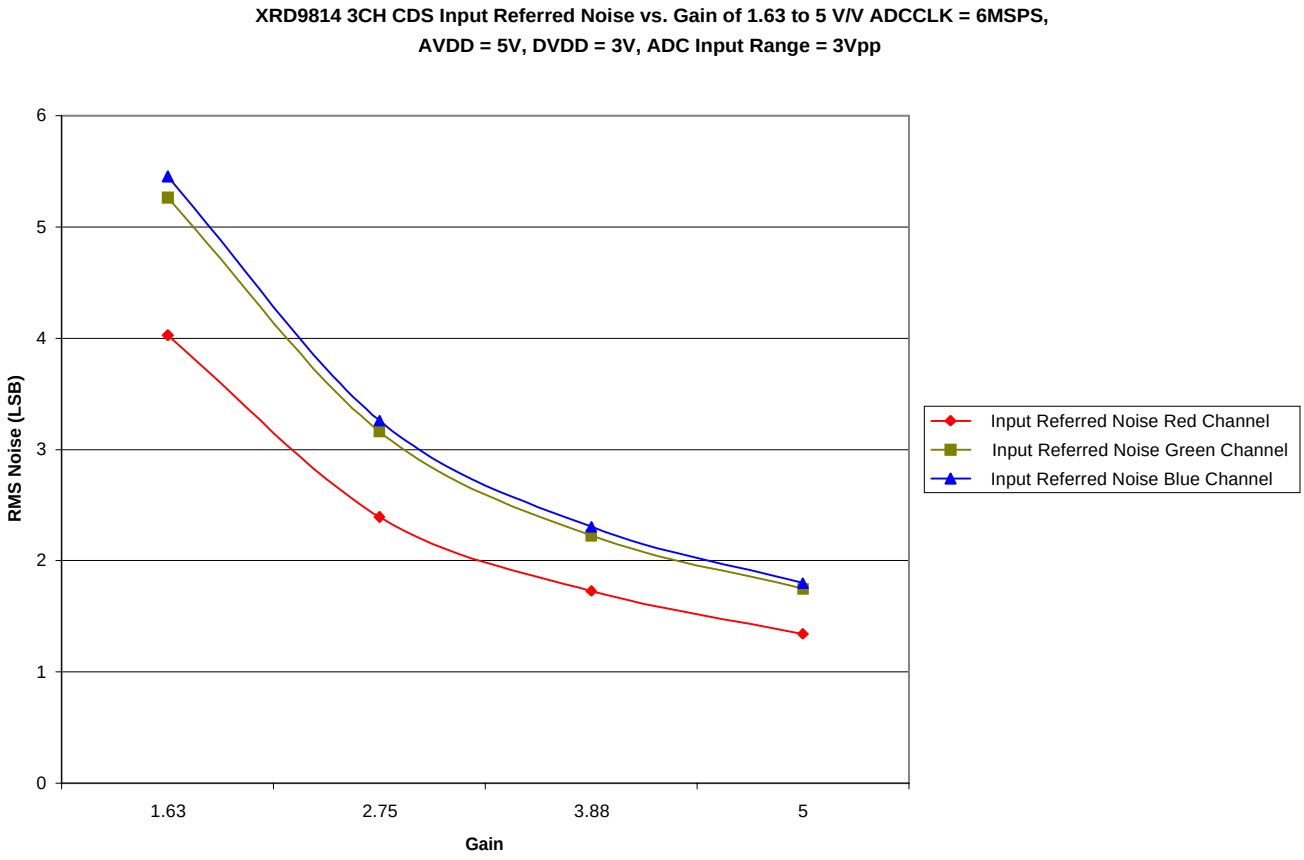
Graph 3. XRD9814 3-Channel CDS Pixel Clamp DNL Plot



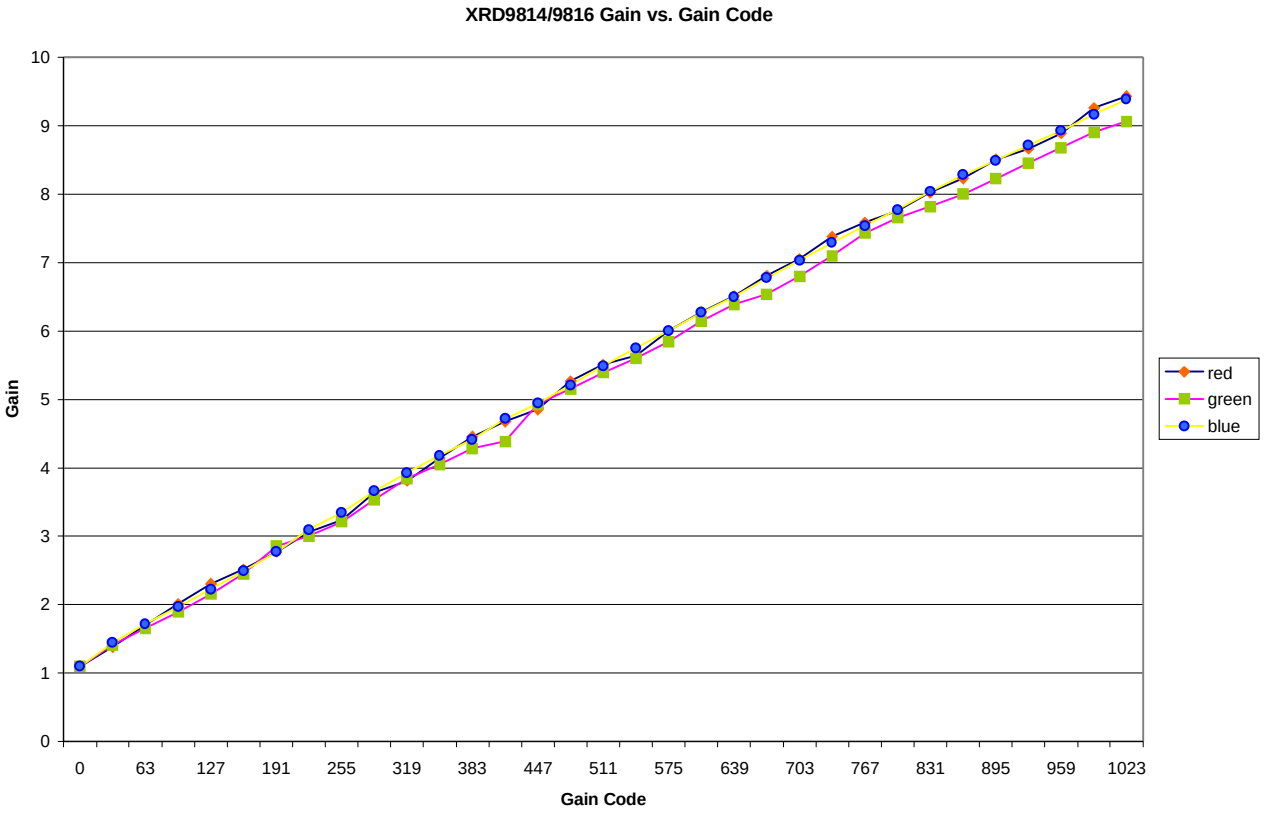
Graph 4. XRD9814 1-Channel CIS S/H No Clamp Input Referred Noise vs. Gain (1 MSPS)



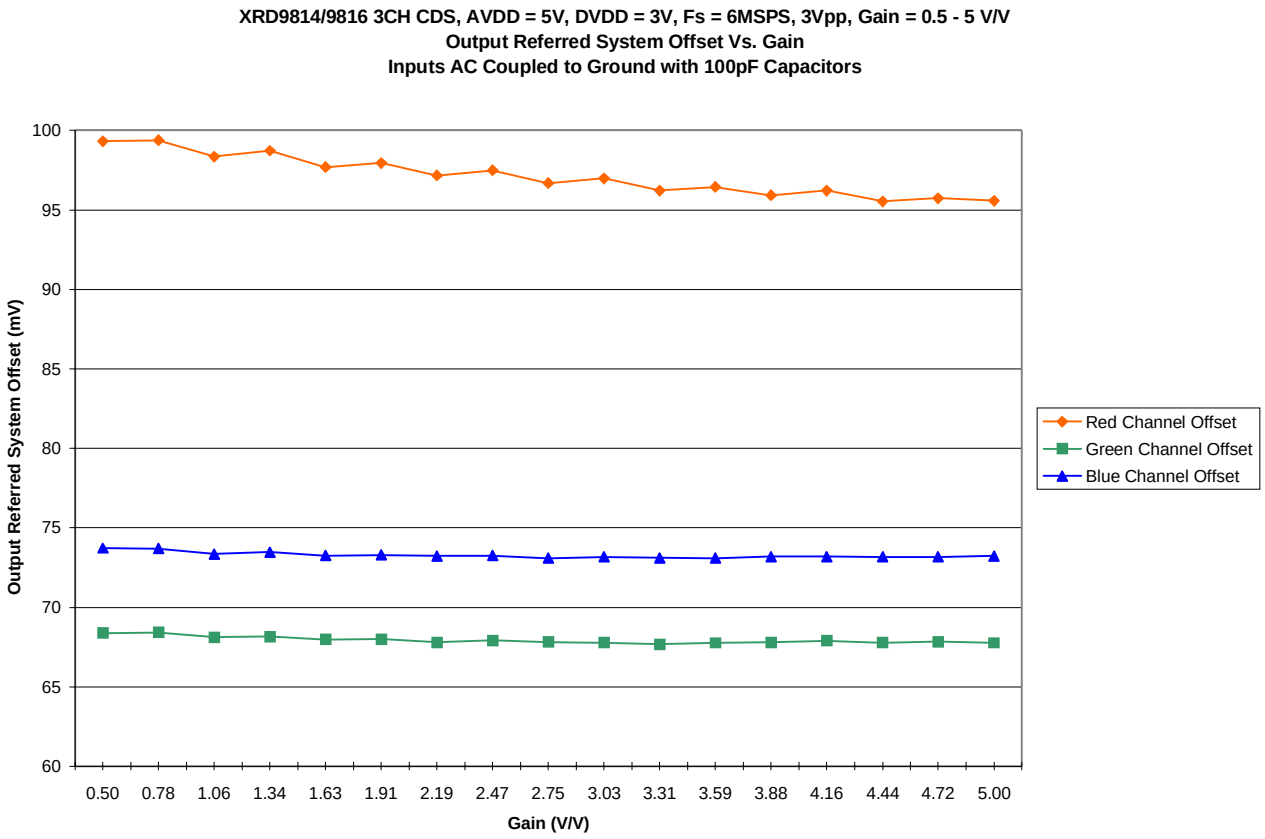
Graph 5. XRD9814 1-Channel CIS S/H No Clamp Input Referred Noise vs. Gain (6 MSPS)



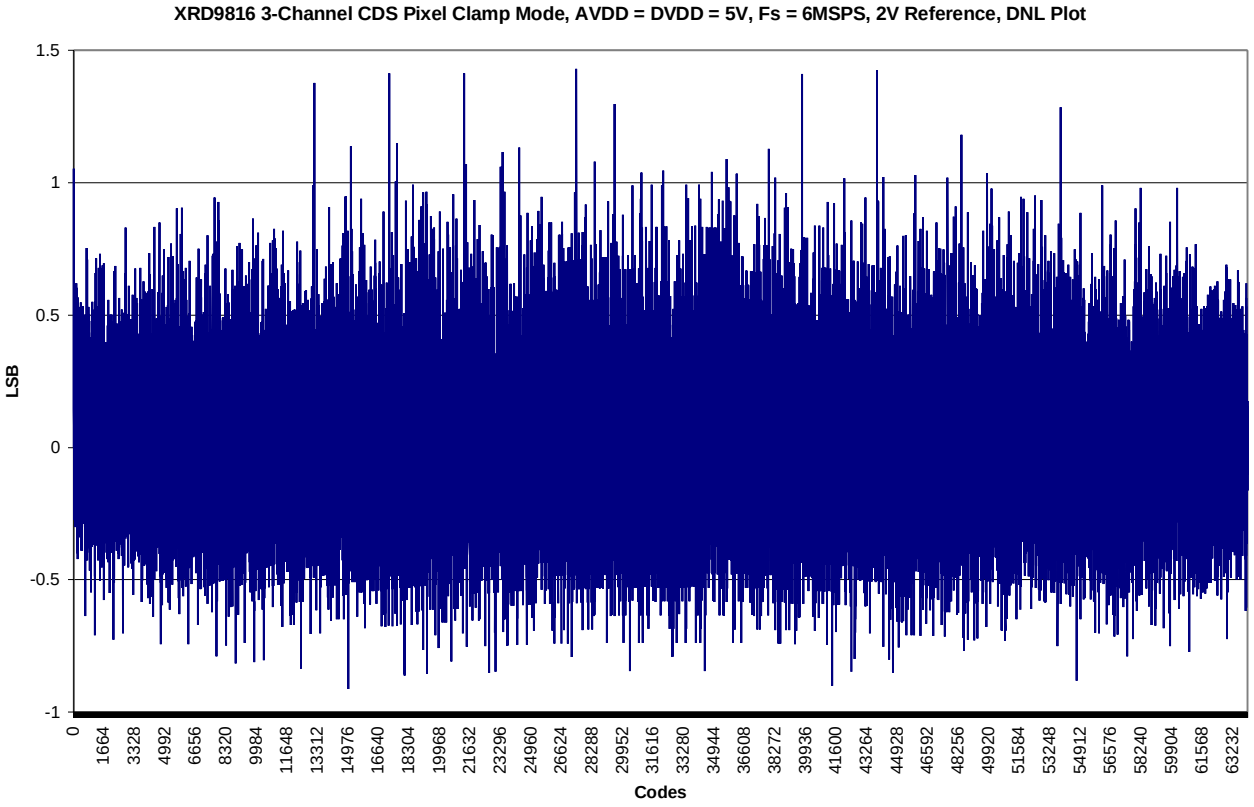
Graph 6. XRD9814 3-Channel CDS Pixel Clamp Input Referred Noise vs. Gain



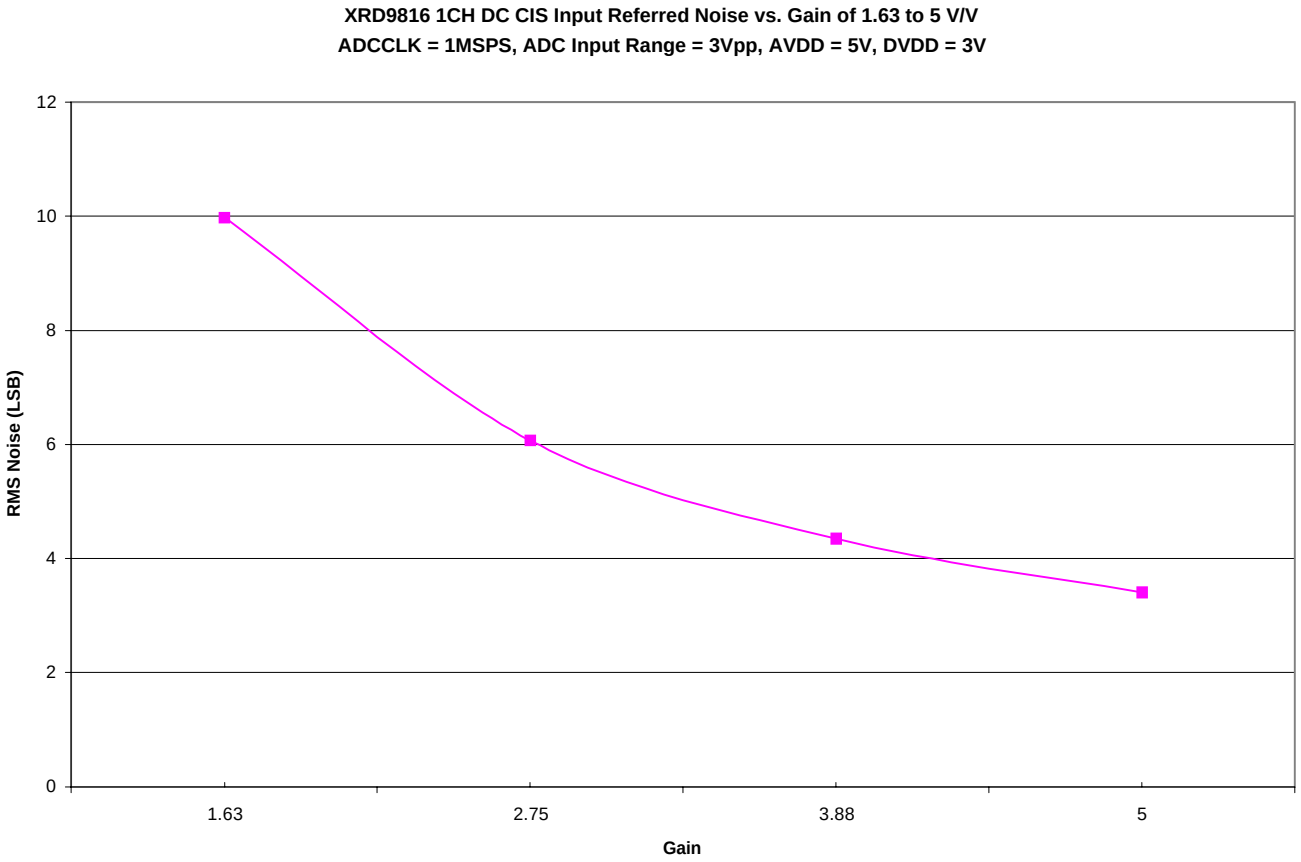
Graph 7. XRD9814/9816 Gain vs. Gain Code



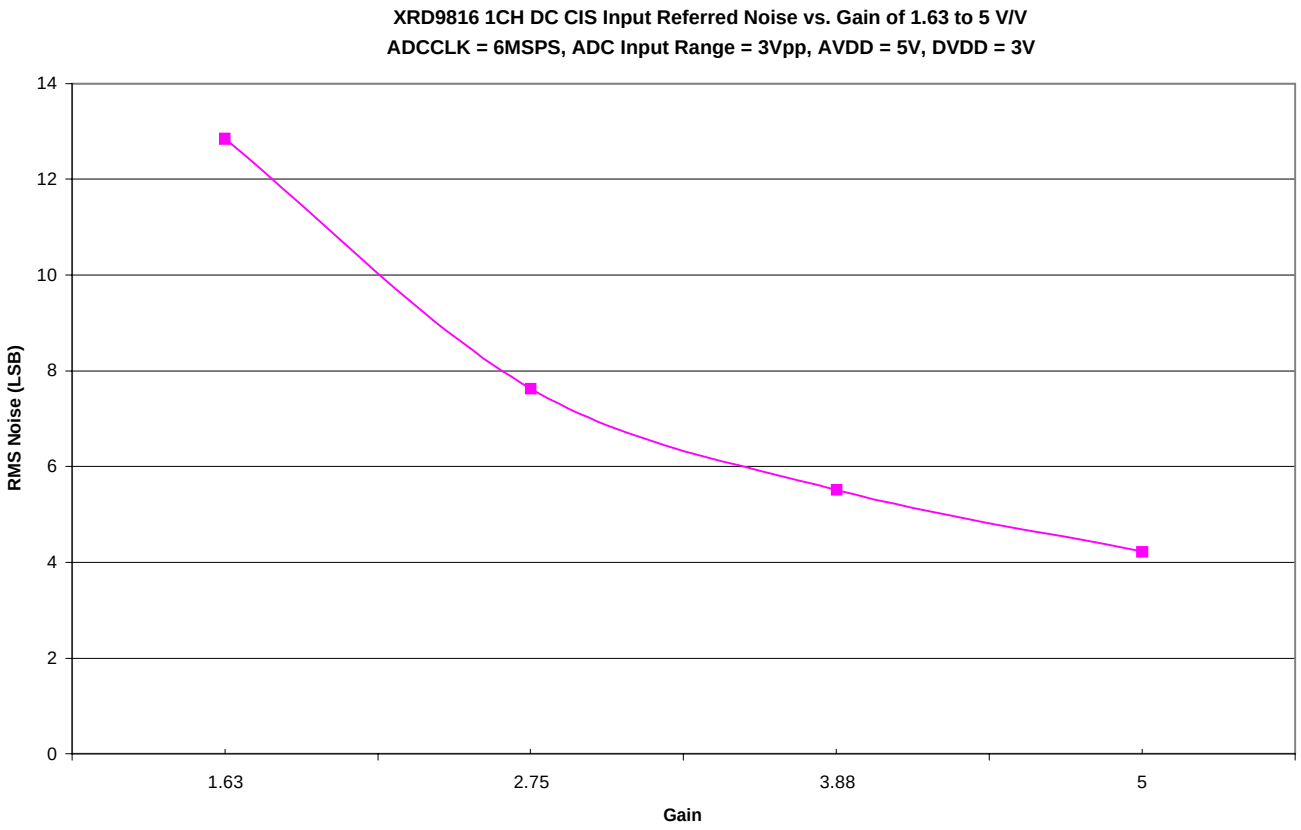
Graph 8. XRD9814 /9816 3-Channel CDS Pixel Clamp System Offset vs. Gain



Graph 9. XRD9816 3-Channel CDS Pixel Clamp DNL Plot



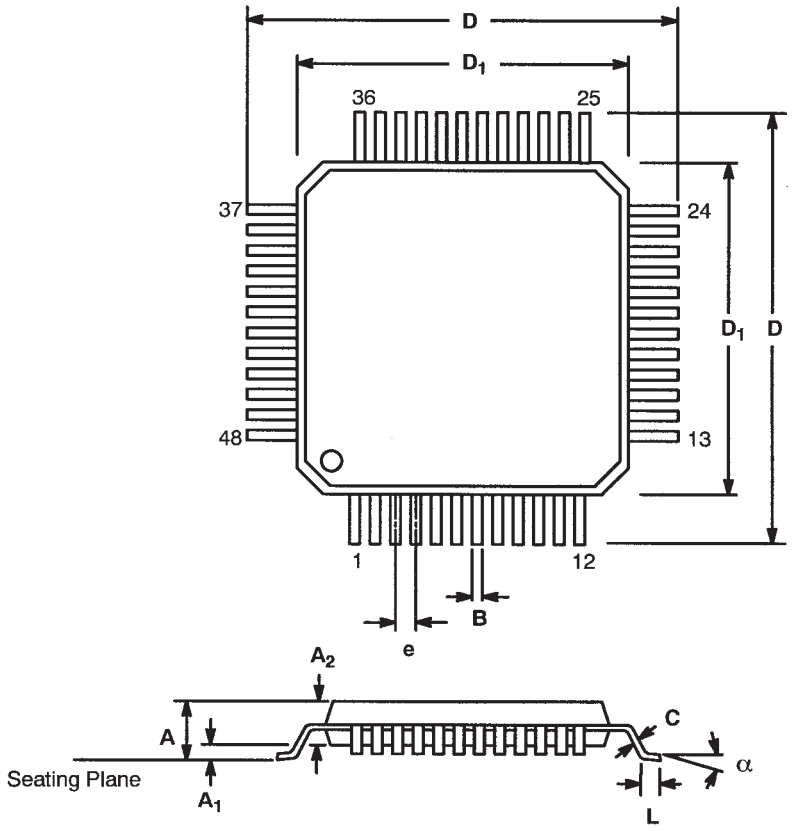
Graph 10. XRD9816 1-Channel CIS SS/H No Clamp Input Referred Noise vs. Gain (1 MSPS)



Graph 11. XRD9816 1-Channel CIS SS/H No Clamp Input Referred Noise vs. Gain (6 MSPS)

48 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.4 mm, TQFP)

Rev. 2.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

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