XDS560 Emulator Technical Reference

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TEXAS INSTRUMENTS



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Preface

Read This First

About This Manual

This technical reference describes the fundamentals of XDS560 PCI Emulator and Pod and how to interface it to a target system.

How to Use This Manual

This document contains the following chapters:

- Chapter one contains a brief overview of the features available with the XDS560 PCI Emulator and Pod.
- Chapter two contains mechanical specification and installation instructions for the XDS560 PCI Emulator and Pod
- Chapter three discusses target design considerations for using the XDS560 PCI Emulator and Pod

Notational Conventions

This document uses the following conventions.

- Program listings, program examples, and interactive displays are shown in a `special typeface` similar to a typewriter's. Examples use a **`bold version`** of the special typeface for emphasis; interactive displays use a **`bold version`** of the special typeface to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

  Here is a sample program listing:

```
0011  0005  0001         .field    1, 2
0012  0005  0003         .field    3, 4
0013  0005  0006         .field    6, 3
0014  0006               .even
```

  Here is an example of a system prompt and a command that you might enter:

```
C:  csr -a /user/ti/simuboard/utilities
```

- In syntax descriptions, the instruction, command, or directive is in a **bold typeface** font and parameters are in an *italic typeface*. Portions of a syntax that are in **bold** should be entered as shown; portions of a syntax that are in *italics* describe the type of information that should be entered. Here is an example of a directive syntax:

  .asect **"***section name***",** *address*

  .asect is the directive. This directive has two parameters, indicated by *section name* and *address*. When you use .asect, the first parameter must be an actual section name, enclosed in double quotes; the second parameter must be an address.

- Square brackets (**[** and **]**) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets; you don't enter the brackets themselves. Here's an example of an instruction that has an optional parameter:

  LALK *16−bit constant [, shift]*

  The LALK instruction has two parameters. The first parameter, *16-bit constant*, is required. The second parameter, *shift*, is optional. As this syntax shows, if you use the optional second parameter, you must precede it with a comma.

  Square brackets are also used as part of the pathname specification for VMS pathnames; in this case, the brackets are actually part of the pathname (they are not optional).

- Braces ({ and }) indicate a list. The symbol **|** (read as *or*) separates items within the list. Here's an example of a list:

  { * | *+ | *− }

  This provides three choices: *, *+, or *−.

  Unless the list is enclosed in square brackets, you must choose one item from the list.

- Some directives can have a varying number of parameters. For example, the .byte directive can have up to 100 parameters. The syntax for this directive is:

  .byte $value_1$ *[, ... ,* $value_n$*]*

  This syntax shows that .byte must have at least one value parameter, but you have the option of supplying additional value parameters, separated by commas.

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following books are and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477−8924. When ordering, please identify the book by its title and literature number.

Microprocessor Development Systems Customer Support Guide (literature number SPDU082) describes the registration, customer support services, service and warranty, and software license agreements. Precautions and safety considerations are also covered in this document.

JTAG/MPSD Emulation Technical Reference (literature number SPDU079) provides the design requirements of the XDS510™ emulator controller, discusses JTAG designs (based on the IEEE 1149.1 standard), and modular port scan device (MPSD) designs.

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Chapter 1

XDS560 Overview

This chapter is a brief overview of the features available in the XDS560 PCI Emulator and Pod.

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1.1 XDS560 Features 1-2

1.1 XDS560 Features

This technical reference describes the fundamentals of XDS560 PCI Emulator and Pod and how to interface it to a target system.

The XDS560 emulator target interface and connector are designed to be backwards compatible with the XDS510 emulator using either the 3/5V or 1.8/5V pod.

Features of the XDS560:

- ❑ PCI-bus based emulator board
- ❑ Support for HS-RTDX enabled devices
- ❑ Wide dynamic operating voltage: 0.5 to 5.0 volts
- ❑ Programmable TCK: 500KHz to 35MHz
- ❑ Overall cable/pod length of 6ft (1.5m) with the pod dimensions of 1.5” x 3” x 0.4” (38mm x 75mm x 10mm)
- ❑ All output target signals are Hi-Z™ when connected or powered-on
- ❑ All pod signals are ESD protected
- ❑ Hardware detection of power losses and cable disconnects

Texas Instrument’s emulation logic and emulation tools are specifically designed to work together complimenting TI’s Digital Signal Processors.

A fundamental understanding of emulation will accelerate your set up, development and software debug. This knowledge will also aid in troubleshooting potential problems in your debugging setup

Chapter 2

Hardware

This chapter contains mechanical specifications and installation instructions for the XDS560 Emulator Pod.

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2.1 Mechanical Specifications

The Texas Instruments XDS560 emulator consists of a PCI-based emulator board and a complementary interconnecting target cable assembly.

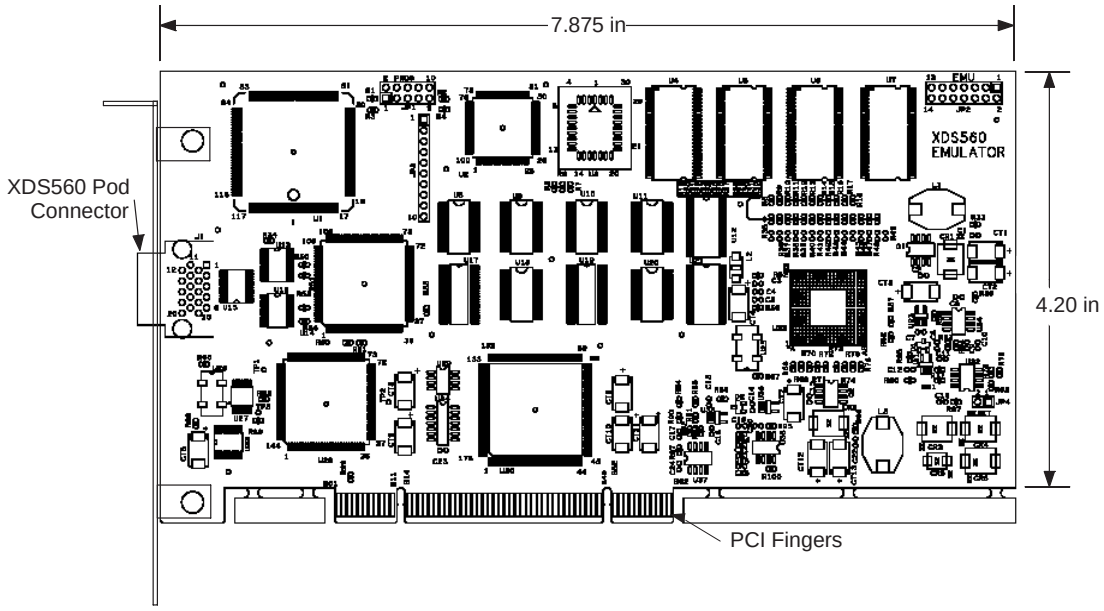
The PCI-based emulator board is designed to operate as an universal card in either a 5.0-V, 3.3-V or universal 32-bit PCI expansion slot.

The PCI interface is complaint with revision 2.2 of the PCI bus specification. The emulator board uses only the +5 V and requires a maximum current of 2.0 amperes, derived from applicable pins within the PCI slot.

2.1.1 Mechanical Dimensions

Figure 2−1 shows the mechanical dimensions of the PCI-based emulator board. The emulator board requires a full-height, ¾-length PCI slot to accommodate the installation of the board.

Figure 2−1. XDS560 PCI Emulator Dimensions



The target cable/pod consists of a 1.5m section of jacketed cable, an active cable pod, and a short section of jacketed cable that connects to the target system. The overall cable length is approximately 1.7 meters.

Figure 2−2 and Figure 2−3 illustrate the mechanical dimensions for the target cable pod assembly.

Note that the pin-to-pin spacing on the connector is 0.100 inches in both the X and Y planes, (identical to existing TI 14pin JTAG products).

The cable pod and the end connector cases are made of nonconductive medium-impact resistant plastic.

Figure 2−2. XDS560 Cable and Pod Dimensions

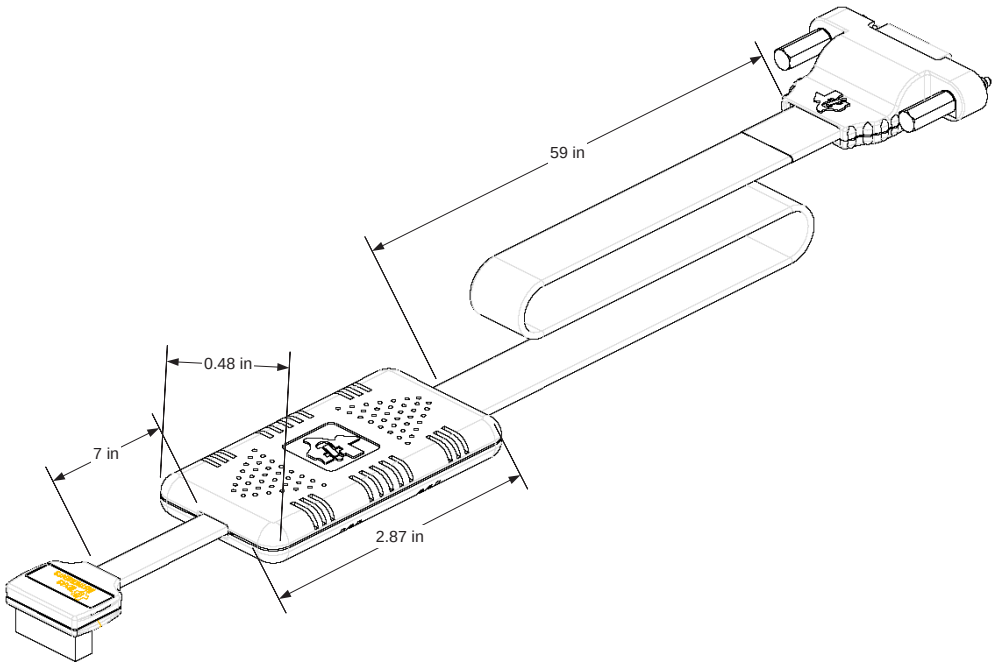
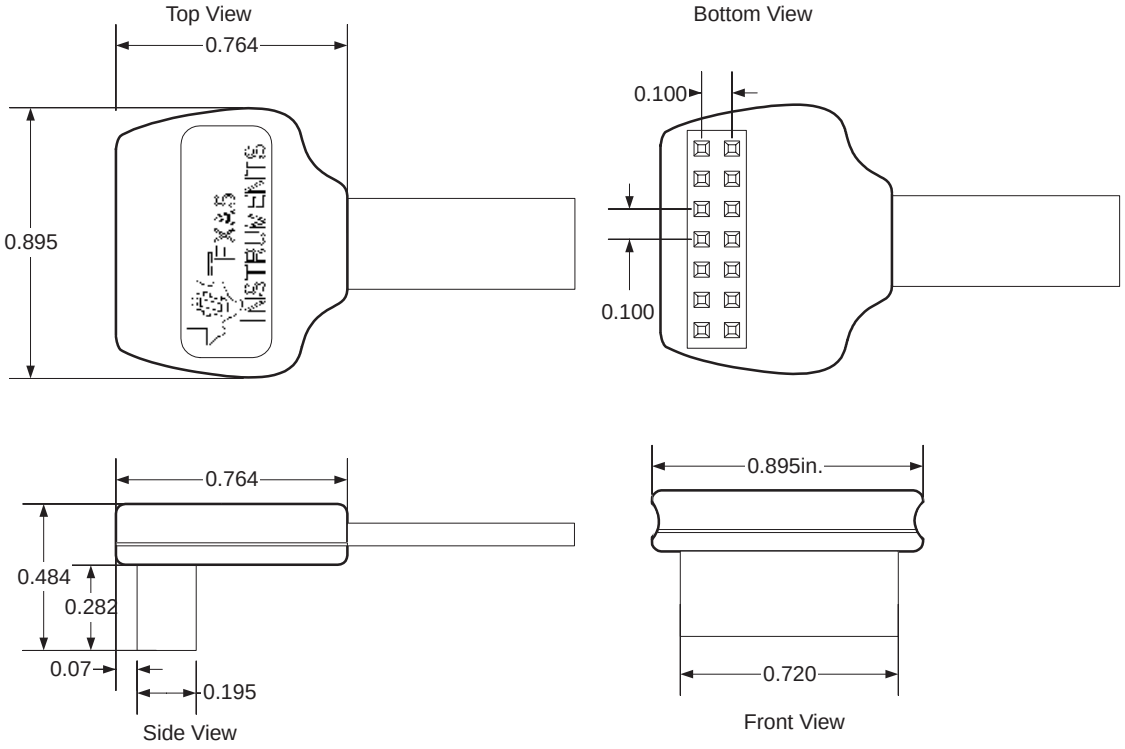


Figure 2−3. XDS560 Target Header Dimensions



2.1.2 Environmental Specifications

The emulator card has been design to operate within normal PC environmental conditions, i.e., 0°C−55°C. Elevated temperatures, beyond the range specified may provide unknown performance results.

The emulator card is designed to operate within a relative humidity of 20%−70%, Non-condensing. Operation of any electronic products outside of this range could permanently damage your equipment. Care should be taken regarding moisture condensation and static discharge (ESD).

The emulator pod assembly has been designed to operate within normal debug ambient environmental conditions, i.e., 0°C−55°C.

Lower temperatures may have an impact on it's structural and mechanical integrity. Elevated ambient temperatures, beyond 70°C may produce unknown performance results.

Elevated temperature applications that come in direct contact with the pod cable assembly should used additional means to maintain an interface temperature less than 60°C on the cable assembly.

The emulator pod cable assembly is designed to operate within a relative humidity of 20%−70%, Non Condensing. Operation of any electronic products outside of this range could permanently damage your equipment.

Care should be taken regarding moisture condensation and static discharge (ESD).

2.1.3 Physical Specifications

The emulator pod cable assembly has been designed to withstand normal flex, Angle, Twist, Force, Strain, and Jerk operations. The chart below indicates the minimum criteria deemed acceptable for laboratory grade debug equipment such as the XDS560 emulator pod cable assembly

Table 2−1. Emulator Cable Specification

Test Description	Cycles	Set Up Criteria
Flex	100,000	90° flex bend during test
Angle	50,000	30° angle bend during test
Twist	5,000	180° twist across short axis during test
Force (Gurney)	1,000	50lb, 6” diameter, 1.25” wide wheel
Strain	1	10lb weight applied, vertically for 2 hours
Jerk	1	1lb weight dropped from a height of 3’

The cable assembly has been tested to withstand these criteria; any failure indicates excessive or incorrect usage or conditions outside of these parameters.

2.1.4 PCI

For more information concerning the PCI 2.2 standard, refer to the latest standards. Standards can be obtained directly from PCISIG (PCI Special Interest Group (PCI-SIG)

Web Address: http://www.pcisig.com

Address: 5440 SW Westgate Dr., #217
Portland, OR 97221

Phone: (503) 291−2569

FAX: (503)297−1090

2.2 XDS560 Installation

Minimizing Personal Injury

Minimizing Personal Injury: To minimize the risk of personal injury, always turn off the power to your PC and unplug the power cord before installing the XDS560.

Minimizing Electrical Shock

Minimizing Electrical Shock and Fire Hazard: To minimize the risk of electric shock and fire hazard, be sure that all major components that you interface with Texas Instruments devices are limited in energy and certified by one or more of the following agencies: UL, CSA, VDE, or TUV.

Minimizing Static Shock

Minimizing Static Shock: Special handling methods and materials should be used to prevent equipment damage. You should be familiar with identification and handling of ESD sensitive devices before attempting to perform the procedures described in this manual.

1) Shutdown PC and unplug the power cord from the supply outlet (mains).
2) Remove the cover / case of your PC.
3) Remove the mounting bracket and screw from an unused PCI slot.
4) Carefully but firmly push the XDS560 PCI board into the PCI slot.
5) Reinstall the mounting bracket screw to the PC and tighten.
6) Connect the XDS560 Pod to the connector on the back of the XDS560 PCI bracket. Secure the cable with the attached thumbscrews.
7) Replace the PC cover / case and plug back in the power cord to the original power source (mains).
8) Turn on power to the PC and start boot process.
9) Next, follow the software installation instructions completely. This properly installs all necessary software and drivers.

Chapter 3

Target Design Considerations for Using the XDS560 Emulation Pod

The following sections will discuss the design issues of designing a target system to support using the XDS560 emulator.

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3.1 Emulation Signals

There are five standard signals and a ground used for JTAG connections to control the JTAG† Test Access Port (TAP) Controller, as defined by the IEEE 1149.1 standard.

These signals are shown in Table 3−1.

As a method of confirming a proper connection of the emulation hardware, TI also uses two other signals provided on the JTAG header (Table 3−2):

- The Target Voltage Detect signal
- The Target Disconnect signal

The Target Voltage Detect signal is used to set the I/O voltage of the XDS560 Target pod. The Target Disconnect signal should be tied to ground on the target board.

† The term JTAG, as used in this book, refers to TI scan-based emulation, which is based on the IEEE 1149.1 standard.

Table 3−1. Standard TAP Controller JTAG Signals

Signal Name	Description	Emulator Signal Type†	Target Signal Type‡
TRST‡	Test Reset‡	O	I
TMS	Test Mode Select	O	I
TDI	Test Data Input	O	I
TDO	Test Data Output	I	O
TCK	Test Clock (XDS560 POD sourced)	O	I
TCK_RET	Test Clock Return (Buffered or un-buffered connection of TCK coming back from the target)	I	O
GND	Ground		GND

† I = Input, O = Output
‡ Do not use pullup resistors on TRST: it has an internal pull-down device. In a low-noise environment, TRST can be left floating. In a high-noise environment, an additional pull-down resistor may be needed. (The size of this resistor should be based on electrical current considerations.)

Table 3−2. XDS560 Connection Signals

Signal Name	Description	Emulator Signal Type†	Target Signal Type
TVD($V_{I/O}$)	Target Voltage Detect: TVD should be tied to the I/O Voltage of the target processor.	I	O
TDIS	Target Disconnect	I	GND

† I = Input, O = Output

Additionally, Texas Instruments adds two more signals, used for advanced emulation capability, to the JTAG header.

These signals, shown in Table 3−3, provide the capability to perform High-Speed Real-Time Data eXchange (RTDX), benchmarking, software profiling and multi-processor emulation with inter-processor breakpoint capabilities.

Table 3−3. TI Advance Emulation Signals

Signal Name	Description	Emulator Signal Type†	Target Signal Type
EMU0	Emulation Pin 0	I/O	I/O
EMU1	Emulation Pin 1	I/O	I/O

† I = Input, O = Output

The TI advanced emulation JTAG signals are used by the XDS560 to perform clocking capabilities when performing software benchmarking and software profiling.

Other capabilities include:

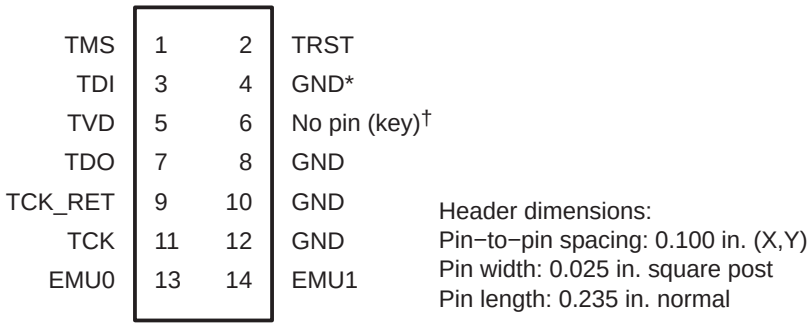
- Assistance with multi-processor debugging.
- As an output and driven low by a device as a result of breakpoint conditions being met.
- As inputs monitored in the debugging logic, which allows one core to set the EMU signal, and another device to break as a result.
- On an HS−RTDX enabled target device, Each EMU signal can support an RTDX transmit and receive data channel.

3.2 Target System’s Emulator Connector

JTAG target devices support emulation through a dedicated emulation port. This port is a superset of the IEEE 1149.1 standard and is accessed by the emulator.

To communicate with the emulator, **your target system must have a 14-pin header** (two rows of seven pins) and configured as shown in Figure 3−1. If this pinout for this header is changed, it may have an affect on operation and signal integrity.

Figure 3−1. 14-Pin Target Header Pin Dimensions



† On the XDS560 emulator pod connection this is the TDIS signal. This male pin must be connected to the target board’s ground for proper operation.
‡ While the corresponding female position on the cable connector is plugged to prevent improper connection, the cable lead for pin 6 is present in the cable and is grounded, as shown in the schematics and wiring diagrams in this document.

Although you can use other headers, some recommended parts are shown in Table 3−4:

Table 3−4. Recommended Header Parts

Manufacturer	Part Number	Description
3M	939836-01-36	Thru-Hole Needs to be cut to length and pin 6 removed
AMP	4-102977-0	Thru-Hole, Needs to be cut to length and pin 6 removed
SAMTEC	TSW-107-07-L-D-006	Thru-hole, Pin 6 removed.
SAMTEC	TSM-107-01-L-DV-006	SMT, Pin 6 removed.
Sullins	PTC36DAAN	Thru-Hole, Needs to be cut to length and pin 6 removed

3.3 For More Information About the IEEE 1149.1 Standard

IEEE Customer Service can be reached at:

Address:	IEEE Customer Service 445 Hoes Lane Piscataway, NJ 08855-1331
Phone:	(800) 678–IEEE in the US and Canada (732) 981–0060 outside the US and Canada
FAX:	(731) 981–9667

3.4 Bus Protocol

The IEEE 1149.1 standard covers the requirements for the test access port (TAP) bus slave devices and provides certain rules, summarized as follows:

- The TMS/TDI inputs are sampled on the rising edge of the TCK signal of the slave device.
- The TDO output is clocked from the falling edge of the TCK signal of the slave device.

When these devices are linked together in series, the TDO of one device has approximately one-half TCK cycle setup time before the next device's TDI signal.

This type of timing scheme minimizes race conditions that would occur if both TDO and TDI were timed from the same TCK edge. The penalty for this timing scheme is a reduced TCK frequency.

The IEEE 1149.1 standard does not provide rules for bus master (emulator) devices. Instead, it states that it expects a bus master to provide bus slave compatible timings. The XDS560 emulator provides timings that meet the bus slave rules.

3.5 XDS560 Emulator Cable Pod Logic

Figure 3−2 shows a portion of the XDS560 emulator cable pod. The following items are characteristics of the XDS560 pod:

- Signals TMS, TDI and TRST are series terminated to reduce signal reflections.
- The TCK signal output has a medium-current drive capability of 24 mA I_{OL}/I_{OH}. The TCK signal is AC termination on the return side of the TCK (TCK_RET). The termination voltage is set to ½ of the TVD voltage to minimize loading effects.
- The TDO signal from the slave device is terminated at the pod of the cable with a 10K Ω resistor pulled up to the same voltage as set by TVD voltage.
- The trigger level for high-to-low and low-to-high transition for TDO, TCK_RET, and EMU0/EMU1 is set to ½ of the TVD signal. For TVD voltages greater than 3.3 V, the trigger level is set to approximately 1.65 V.
- Signals TMS and TDI, by default, are generated on the rising-edge of the TCK_RET signal, but can be generated from the falling edge of TCK_RET to be in accordance with the IEEE 1149.1 bus slave device timing rules.
- The pod provides a programmable (TCK) test clock source. The range of this TCK is 500 KHz to 50 MHz, but the operation is limited by timing of various signals and the target devices. Note: All timing for the pod and emulator are from the TCK_RET signal, therefore a user may provide their own test clock (TCK).
- All output signals from the pod are Hi-Z, whenever the pod power is turned on or TVD signal is reduced by more than one third of its reset voltage.
- Signals TCK, TMS, TDI, and TRST have a 100K pull-down resistor. This is to ensure that the target inputs are at a set level given that the outputs from the XDS560 pod are Hi-Z after a power failure or disconnect.
- Pin 4 of the emulation header is the Target Disconnect (TDIS) signal. This signal is used to detect if the target pod is connected to a target board. Pin 4 on the user target board must be connected to ground.
- The impedance of the emulation pod cable is 50 Ω.
- Design Note: Pin 6 of the target emulation header is normally connected to a ground signal on the target board. The target board designer may use this pin 6 as an optional Host Disconnect (HDIS) signal. This signal could be used within the target board to detect if the JTAG emulator cable/pod header is connected.

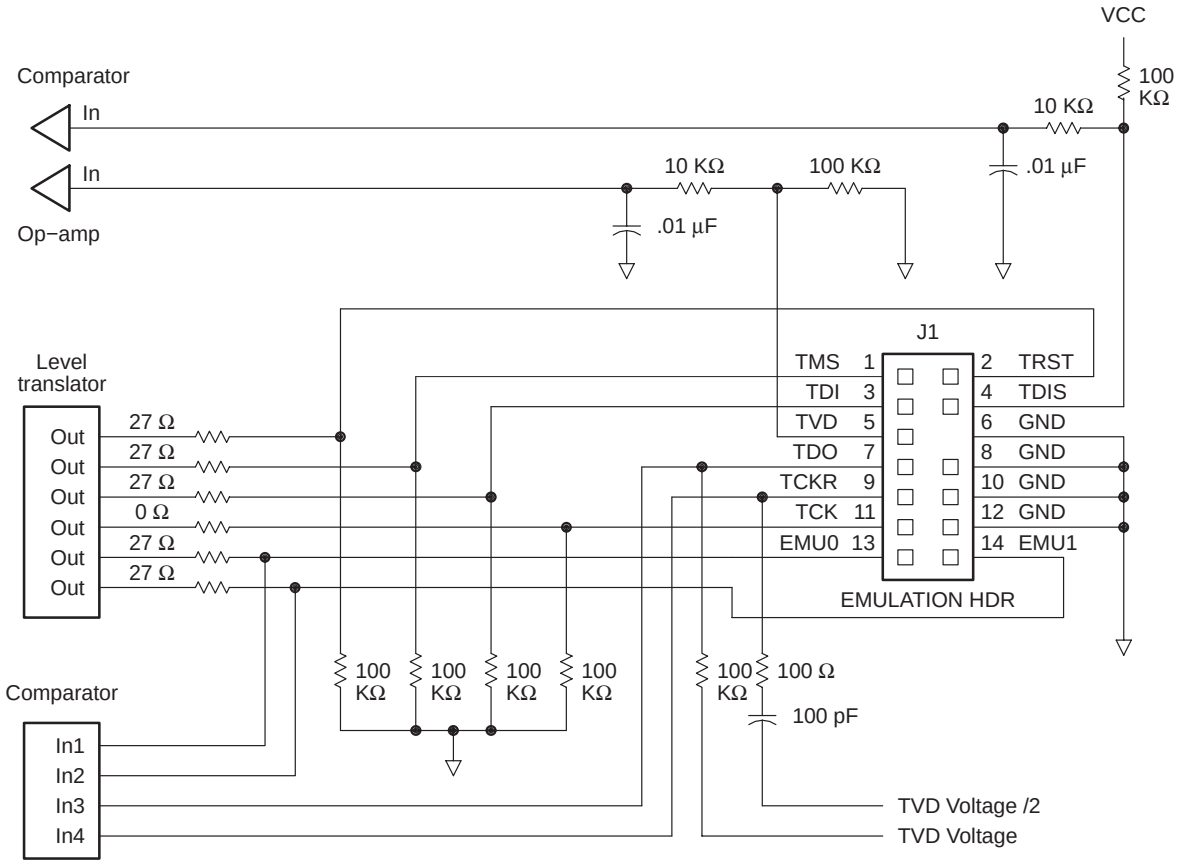
To support selection of the proper I/O voltage, the target header has a Target Voltage Detect (TVD) signal. This signal (pin 5) should be tied to the I/O voltage of the target processor.

If the target system needs to supports multiple I/O voltages on the scan string, the lowest voltage devices should be placed first.

A translation buffer should be used to connect the rest of the scan string. TCK, TMS, and TRST must have similar considerations.

Two copies of each signal may be required with each driving a different voltage level.

Figure 3−2. JTAG Emulator Cable/Pod Interface



3.6 XDS560 Emulator Cable Pod Signal Timing

Figure 3−3 shows the default timing waveforms for the XDS560 emulator cable pod. Table 3−5 defines the timing parameters. These timing parameters are calculated from values specified in the standard data sheets for the emulator and cable pod and are for reference only.

The presented timing parameters are calculated for the end of the 14-pin target cable header. Texas Instruments does not test or guarantee these timings.

The XDS560 emulator cable pod uses TCK_RET as its clock source for internal synchronization. TCK is provided as an optional target system test-clock source.

Figure 3−3. XDS560 Emulator Cable Pod Timing Waveforms

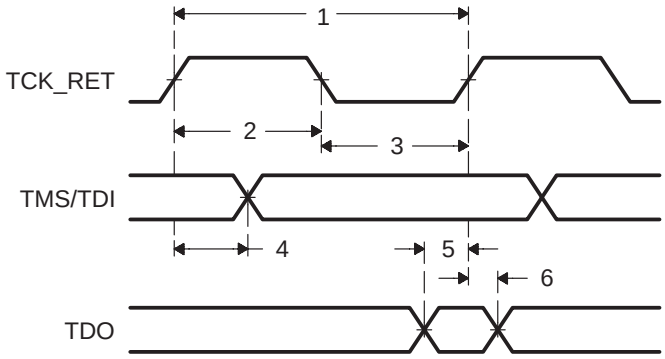


Table 3−5. Emulator Cable Pod Timing Parameters

No.	Reference	Description	Min	Max	Units
1	$t_{c(TCK)}$	Cycle time, TCK_RET	20		ns
2	$t_{w(TCKH)}$	Pulse duration, TCK_RET high	10		ns
3	$t_{w(TCKL)}$	Pulse duration, TCK_RET low	10		ns
4	$t_{pd(TMS-TDI)}$	Delay time, TMS/TDI valid from TCK_RET high	18	31	ns
5	$T_{su(TDO)}$	Setup time, TDO valid before TCK_RET high	2.5		ns
6	$T_{hd(TDO)}$	Hold time, TDO valid after TCK_RET high	0		ns

Note: The delay time for TMS/TDI valid in calculated for the default rising edge TCK_RET. The delay time for TMS/TDI valid for a falling edge TCK_RET configuration is very similar.

3.6.1 Emulation Timing Calculations

The following examples help you calculate emulation timings in your system. For actual target timing parameters, see the appropriate device data sheet.

Assumptions:

$t_{su(TTMS)}$	Setup time, target TMS/TDI before TCK high	10 ns
$t_{pd(TTDO)}$	Delay time, TCK low to valid target TDO	15 ns
$t_{pd(bufmax)}$	Delay time, target buffer – maximum	10 ns
$t_{pd(bufmin)}$	Delay time, target buffer – minimum	1 ns
$T_{bufskew)}$	Skew time, target buffer between two devices in the same package: $[t_{d(bufmax)} - t_{d(bufmin)}] \cdot 0.15$	1.35 ns
$T_{(TCKfactor)}$	40/60 clock duty cycle	0.4(40%)

Given in Table 3−5:

$t_{d(TMSmax)}$	Delay time, emulator TMS/TDI valid from TCK_RET high	31 ns
$t_{su(TDOmin)}$	Setup time, TDO before emulator TCK_RET high, minimum	2.5 ns

There are two key timing paths to consider in the emulation design:

- The TCK_RET-to-TMS/TDI path, called $t_{pd(TCK_RET–TMS/TDI)}$, and
- The TCK_RET-to-TDO path, called $t_{pd(TCK_RET–TDO)}$.

Of the following two cases (Equation 3−1 and Equation 3−2), the *worst-case path delay* is calculated to determine the maximum system test clock frequency.

Equation 3−1. Key Timing Path Case 1

Case 1: Single processor, direct connection, TMS/TDI timed from TCK_RET high.

$$t_{pd\,(TCK_RET-TMS/TDI)} = t_{pd\,(TMSmax)} + t_{su\,(TTMS)}$$

$$= 31\,ns + 10\,ns$$

$$= 41\,ns\ (24.4\,MHz)$$

$$t_{pd\,(TCK_RET-TDO)} = \frac{\left[t_{d(TTDO)} + t_{su(TDOmin)}\right]}{t_{(TCKfactor)}}$$

$$= \frac{[15\,ns + 2.5\,ns]}{0.4}$$

$$= 43.75\,ns\,(22.9\,MHz)$$

In this case, the TCK_RET-to-TDO path is the limiting factor.

Equation 3−2. Key Timing Path Case 2

Case 2: Single/multiprocessor, TMS/TDI/TCK buffered input, TDO buffered output,

TMS/TDI timed from TCK_RET high.

$$t_{pd\,(TCK_RET-TMS/TDI)} = t_{d(TMSmax)} + t_{su(TTMS)} + t_{(bufskew)}$$

$$= [31\,ns + 10\,ns + 1.35\,ns]$$

$$= 42.35\,ns\,(23.6\,MHz)$$

$$t_{pd\,(TCK_RET-TDO)} = \frac{\left[t_{d(TTDO)} + t_{su(TDOmin)} + t_{d(bufmax)}\right]}{t_{(TCKfactor)}}$$

$$= \frac{[15\,ns + 2.5\,ns + 10\,ns]}{0.4}$$

$$= 68.75\,ns\,(14.5\,MHz)$$

In this case, the TCK_RET-to-TDO path is the limiting factor.

3.7 Connections Between the Emulator and the Target System

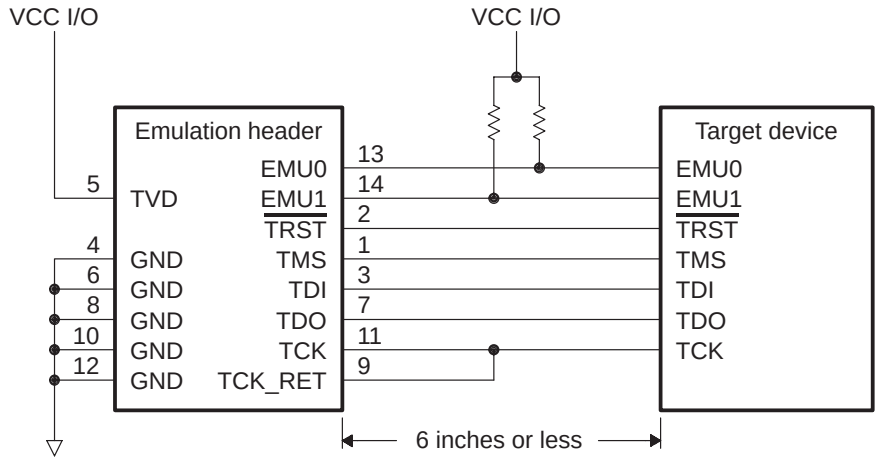
It is extremely important to provide high-quality signals between the emulator and the JTAG target system. Depending upon the situation, you must supply the correct signal buffering, test clock inputs, and multiple processor interconnections to ensure proper emulator and target system operation.

Signals applied to the EMU0 and EMU1 pins on the JTAG target device can be either an input or an output (I/O). In general, these two pins are used as both input and output in multiprocessor systems to handle global run/stop operations.

3.7.1 Buffering Signals

If the distance between the emulation header and the JTAG target device is greater than six inches, the emulation signals must be buffered. If the distance is less than six inches, no buffering is necessary. The following illustrations depict these two situations.

Figure 3−4. Unbuffered Signal Connections



❑ No signal buffering. In this situation, the distance between the header and the JTAG target device should be no more than six inches.

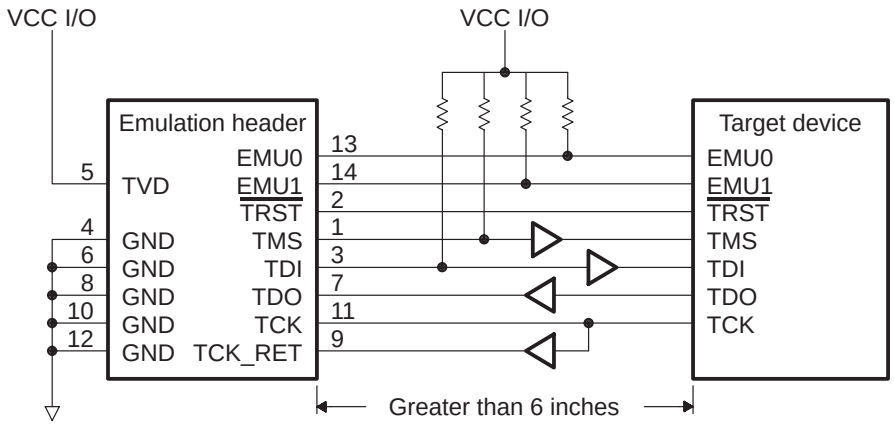
The EMU0 and EMU1 signals must have pull-up resistors connected to V_{CC} to provide a signal rise time of less than 10 µs. A 4.7-kΩ resistor is suggested for most applications.

Buffered transmission signals. In this situation, the distance between the emulation header and the processor is greater than six inches. Emulation signals TMS, TDI, TDO, and TCK_RET are buffered through the same package.

Importance of Good Design Practices

The target board designer should use good design practices to minimize signal crosstalk and signal skew. The designer must also take into account any propagation delays of these signals and the effect that they will have on the timing of the emulation.

Figure 3−5. Buffered Signal Connections

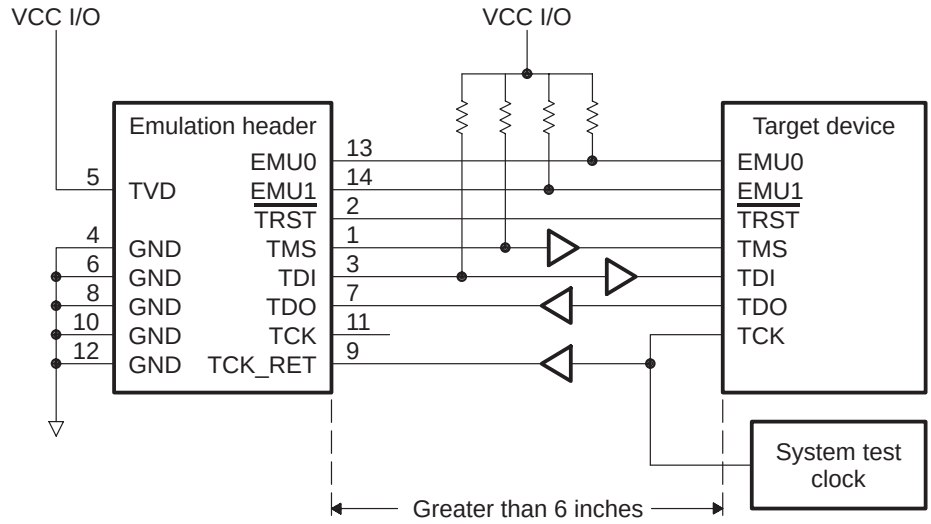


- The EMU0 and EMU1 signals must have pullup resistors connected to V_{CC} to provide a signal rise time of less than 10 µs. A 4.7-kΩ resistor is suggested for most applications.
- The input buffers for TMS and TDI should have pull-up resistors connected to V_{CC} to hold these signals at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested.
- To have high-quality signals (especially the processor TCK and the emulator TCK_RET signals), you may have to employ special care when routing the PWB trace. You also may have to use termination scheme, which is appropriate for your design to match the trace impedance. The emulator pod provides optional internal parallel terminators on the TCK_RET and TDO. TMS and TDI provide fixed series termination.
- Since TRST is an asynchronous signal, it should be buffered as needed to insure sufficient current to all target devices.
- Additional considerations should be taken into account when designing a target board. Such considerations include signal loading of vias and the like.

3.7.2 Using a Target-System Clock

Figure 3−6 shows an application with the system test clock generated in the target system. In this application, the TCK signal is left unconnected.

Figure 3−6. Target System Generated Test Clock



Note: When the TMS/TDI lines are buffered, pullup resistors should be used to hold the buffer inputs at a known level when the emulator cable is not connected.

A benefit to having the target system generate the test clock, there may be other devices in your system that require a test clock when the emulator is not connected. The system test clock also serves this purpose.

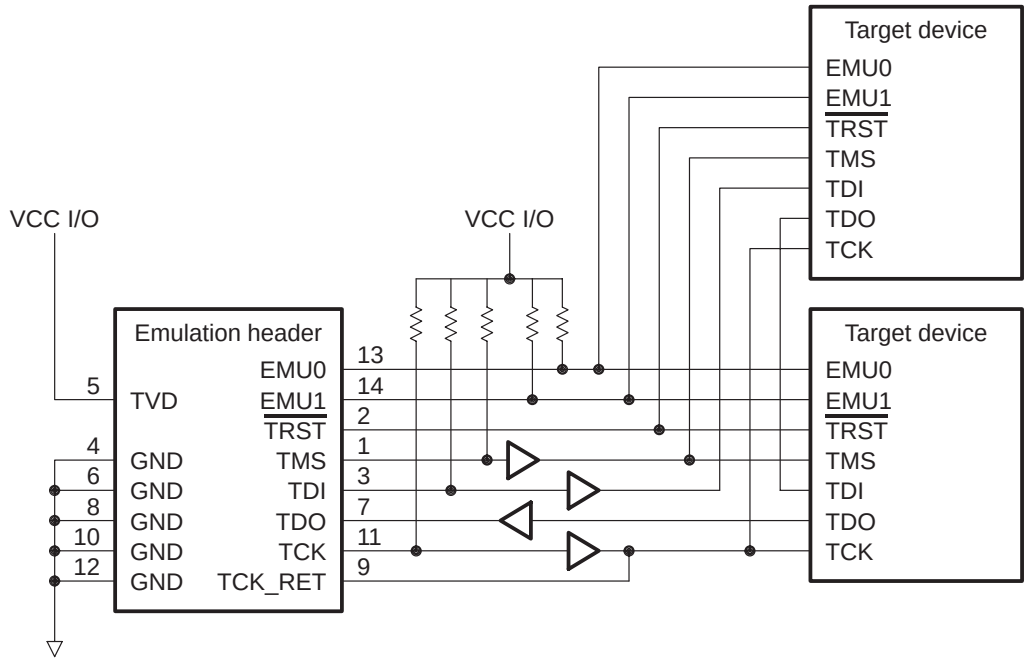
3.7.3 Configuring Multiple Processors

Figure 3−7 shows a typical series linked multiprocessor configuration, which meets the minimum requirements of the IEEE 1149.1 standard. The emulation signals in this example are buffer to isolate the processor from the emulation and provide adequate signal drive for the target system. One of the benefits of this type of interface is that you can generally slow down the test clock to eliminate timing problems. Use the following guidelines for multiprocessor support:

- ❏ The processor TMS, TDI, TDO, and TCK signals should be buffered through the same physical package for better control of timing skew.
- ❏ The input buffers of TMS, TDI, and TCK should have pull-up resistors connected to V_{CC} I/O to hold these signals at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested.

- Buffering EMU0 and EMU1 is optional but highly recommended to provide isolation. These are not critical signals and do not have to be buffered through the same physical package a TMS, TCK, TDI, and TDO. Unbuffered and buffered signals are shown in this section

Figure 3−7. Multiprocessor Connections



3.8 EMU0−EMU1 Signal Considerations

The EMU0−EMU1 signals are bi-directional multifunctional signals. These signals are used for software benchmarking and software profiling.

On multi-processor systems, they can be used to assist in debugging by causing an interrupt or breakpoint to occur from one device to another. These signals are used for HS-RTDX (High-Speed Real Time Data eXchange).

HS-RTDX is a form of bi-directional data transfer.

Each EMU signal supports a single channel of data transfer.

This form of communication uses TCK and the EMU0 and/or EMU1 to achieve up to 2 Megabytes/second transfer rate. Also, the EMU0−EMU1 signals may be used to select different modes of the device.

These modes are set when the device RESET signal is release, for normal emulation the EMU0−EMU1 signal should be pulled high to the device Input/ Output voltage.

For designs with target devices that don't support HS-RTDX the only requirement is that it is necessary to ensure that the EMU0–EMU1 lines can go from a logic low level to a logic high level in less than 10 μs. This can be calculated using the formula in Equation 3−3:

Equation 3−3. Calculating EMU0-EMU1 Lines That Don't Support HS-RTDX

$$\begin{aligned} t_r &= 5(R_{pullup} \times N_{devices} \times C_{load_per_device}) \\ &= 5(4.7K\Omega \times 16 \times 15pF) \\ &= 5.64\mu s \end{aligned}$$

For designs with target devices that support HS-RTDX, the requirements are the same for a low number of devices. But as the number devices increases the response of the EMU0−EMU1 signal will increase which will require the user to reduced the TCK frequency.

To maximize the TCK rate, the user will be required to manually adjust the TCK frequency and run the HS-RTDX confidence tests until a frequency is found where the HS-RTDX confidence tests pass reliability.

It is suggested that after a frequency is found, that the user reduce the frequency by additional 10% to guarantee that temperature and environmental changes don't affect the operation of the emulator.

For some multi-processor designs crossbar technology (CBT) devices could be used to break the number of devices into a bank of devices.

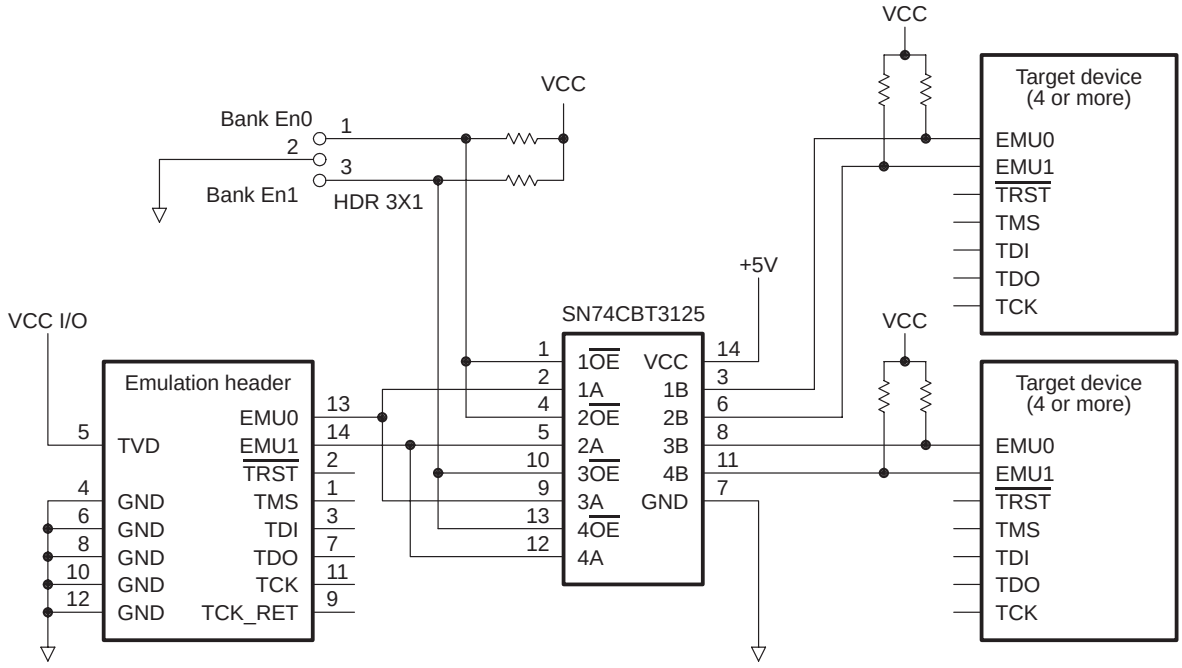
The CBT device could be used to limit the number of devices that the driving EMU0−EMU1 signal is loaded with; thereby limiting the amount of capacitance loading that is seen by the driving EMU0−EMU1 signal.

Using this solution would require the user to have a manual jumper selection to enable which bank of devices that emulator would able to establish HS-RTDX communication with.

Figure 3−8 shows a possible solution to minimize the loading effects of having to many target devices connected on the EMU0/EMU1 signals.

Please refer to Section 3.7 for recommended connections of the JTAG signals.

Figure 3−8. Bank Selection of EMU Signals



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