XB1007-BD

Buffer Amplifier
4.0-11.0 GHz

Rev. V1

Mimix Broadband

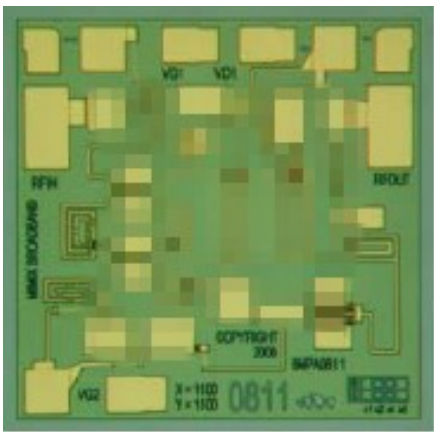
Features

- Excellent Transmit LO/Output Buffer Stage
- Compact Size
- 23.0 dB Small Signal Gain
- +20.0 dBm P1dB Compression Point
- 4.5 dB Noise Figure
- Variable Gain with Adjustable Bias
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Commercial-Level Visual Inspection Using Mil-Std-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

Description

M/A-COM Tech's two stage 4.0-11.0 GHz GaAs MMIC buffer amplifier has a small signal gain of 23.0 dB with a +20.0 dBm P1dB output compression point. The device also provides variable gain regulation with adjustable bias. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Microwave and Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Chip Device Layout



Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage (Vd)	+4.3 VDC
Supply Current (Id1)	180 mA
Gate Bias Voltage (Vg)	0 V
Input Power (Pin)	+20.0 dBm
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Ta)	-55 °C to +85 °C
Channel Temperature (Tch)	175 °C

Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

Ordering Information

Part Number	Package
XB1007-BD-000V	"V" - vacuum release gel paks
XB1007-BD-EV1	evaluation module

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Electrical Specifications: 4-11 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11)	dB	-	20.0	-
Output Return Loss (S22)	dB	-	12.0	-
Small Signal Gain (S21)	dB	-	23.0	-
Gain Flatness (ΔS21)	dB	-	+/-1.5	
Reverse Isolation (S12)	dB	-	65.0	-
Noise Figure	dB	-	4.5	
Output Power for 1dB Compression Point (P1dB)[2]	dBm	-	+20.0	-
Saturated Output Power (Psat)	dBm	-	+21.0	-
Drain Bias Voltage (Vd2)	VDC	-	+4.0	+4.0
Gate Bias Voltage (Vg2)	VDC	-1.0	-0.35	-0.1
Supply Current (Id) (Vd=4.0 V, Vg2=-0.5 V Typical)	mA	-	100	130

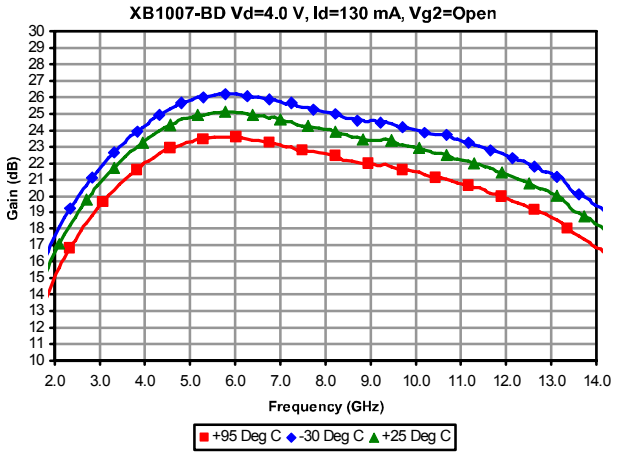
2. Measured using constant current

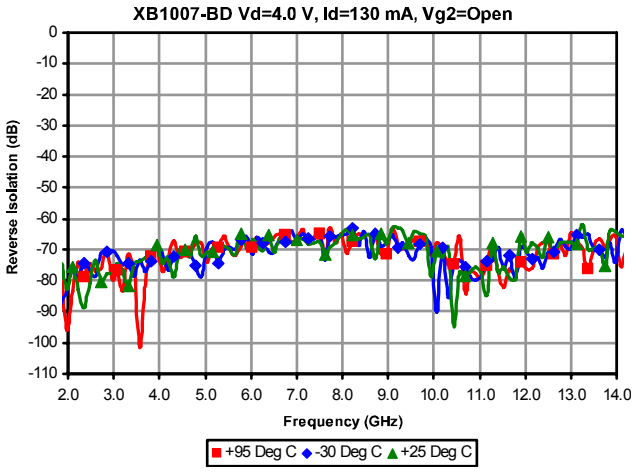
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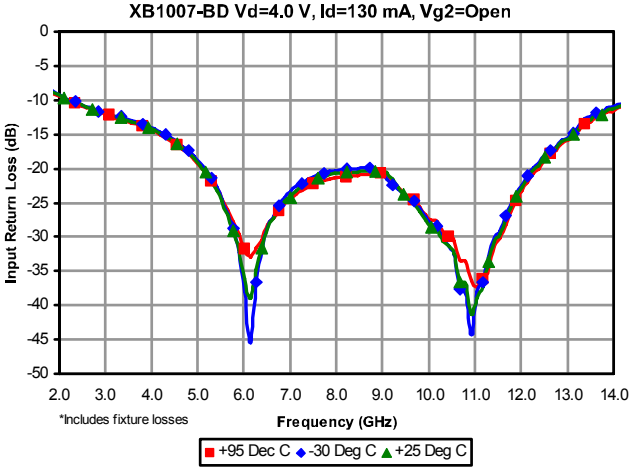
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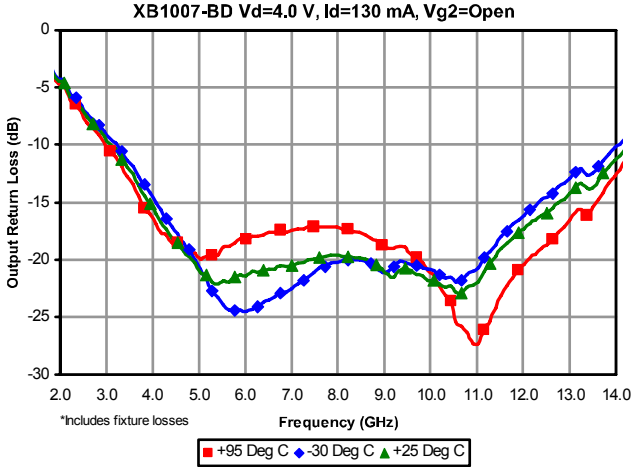
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Typical Performance Curves









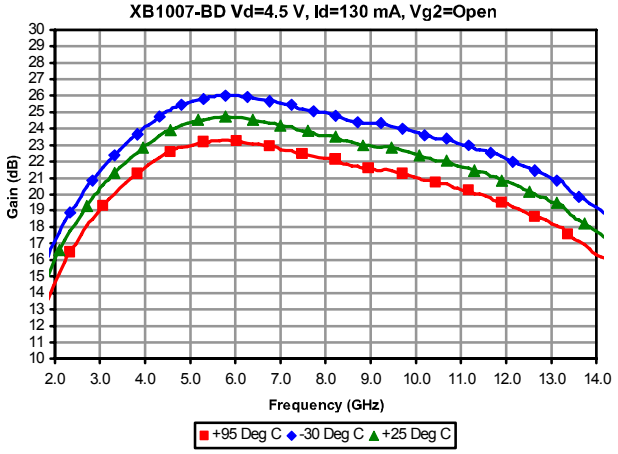
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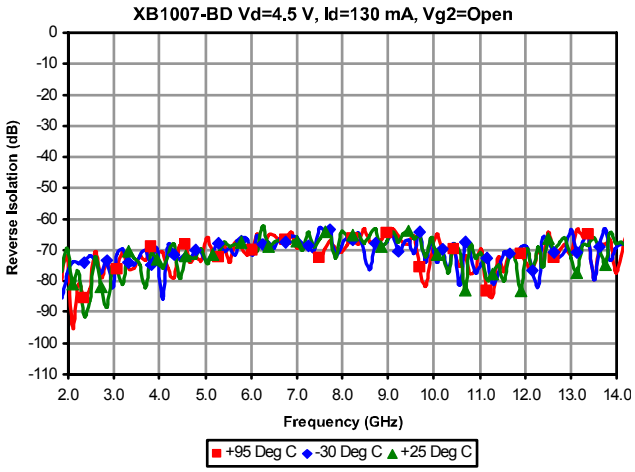
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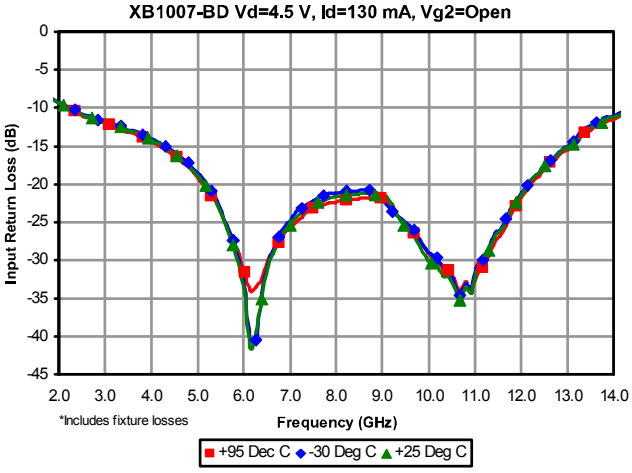
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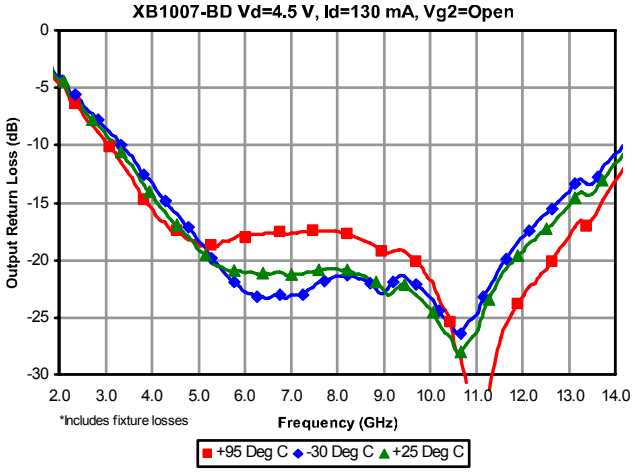
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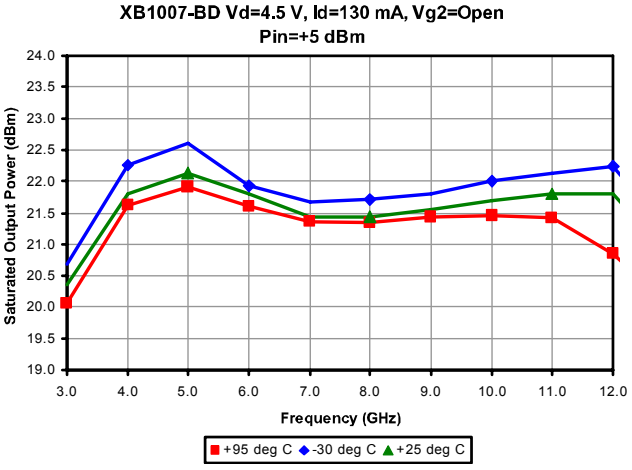
Typical Performance Curves (cont.)











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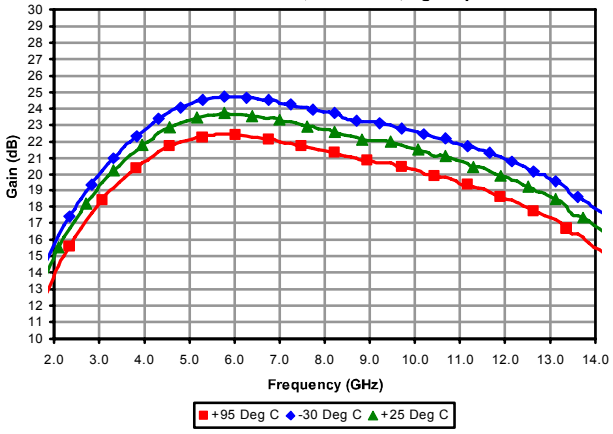
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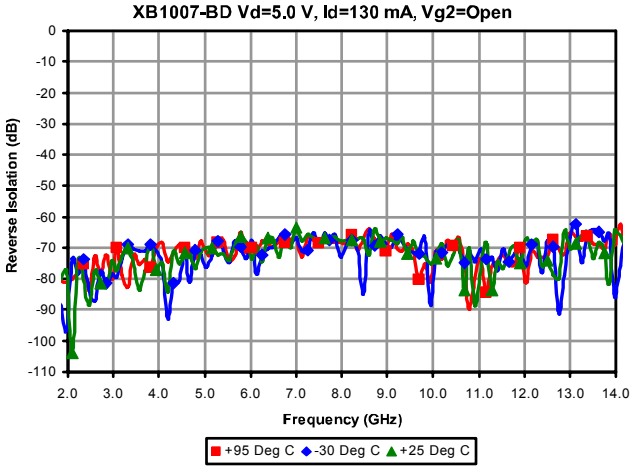
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Typical Performance Curves (cont.)

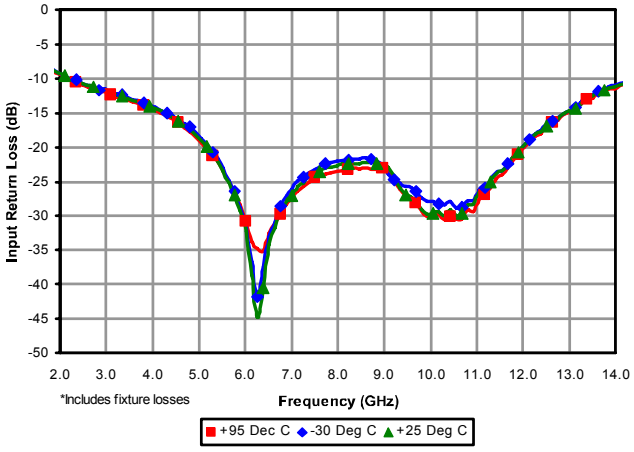
XB1007-BD Vd=5.0 V, Id=130 mA, Vg2=Open



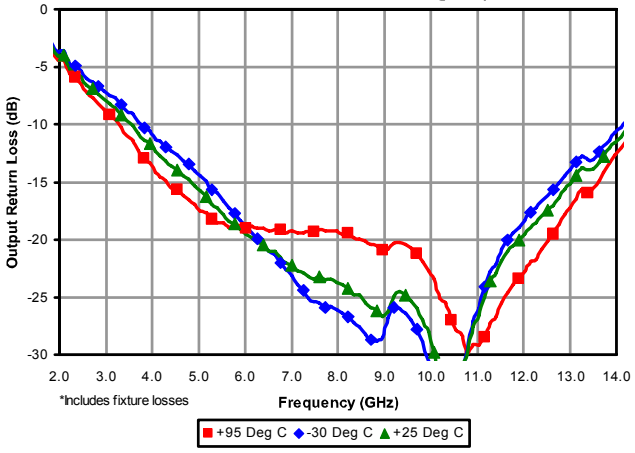
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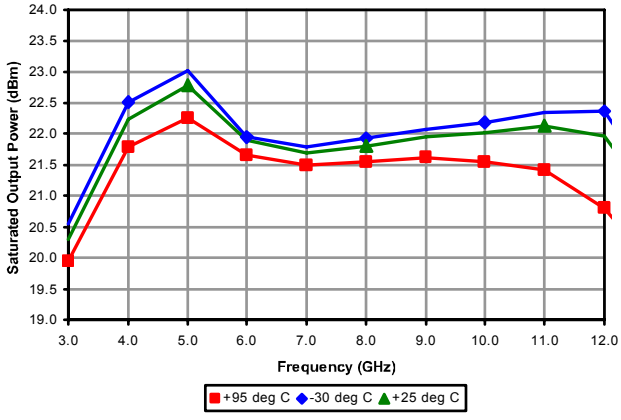
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XB1007-BD Vd=5.0 V, Id=130 mA, Vg2=Open



XB1007-BD Vd=5.0 V, Id=130 mA, Vg2=Open
Pin=+5 dBm

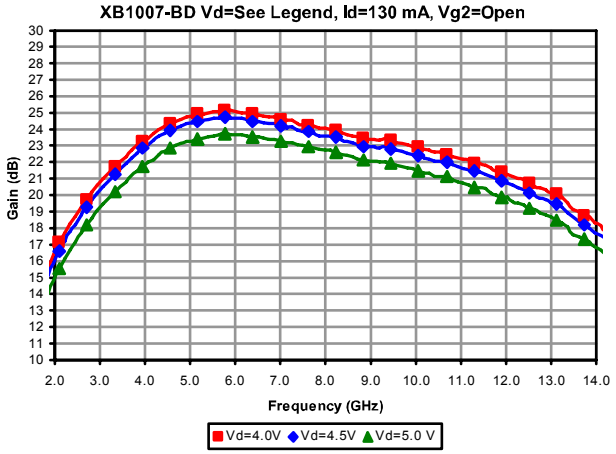


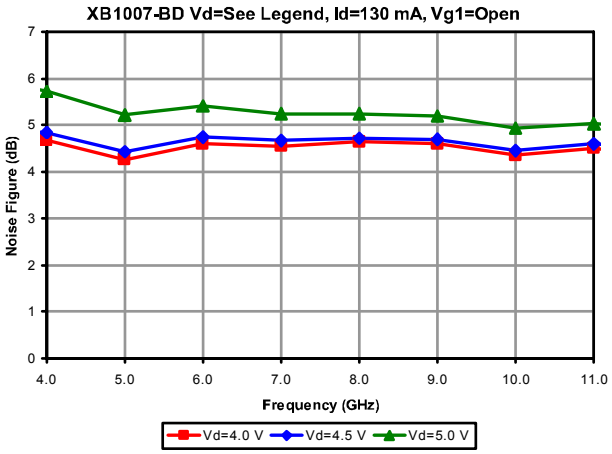
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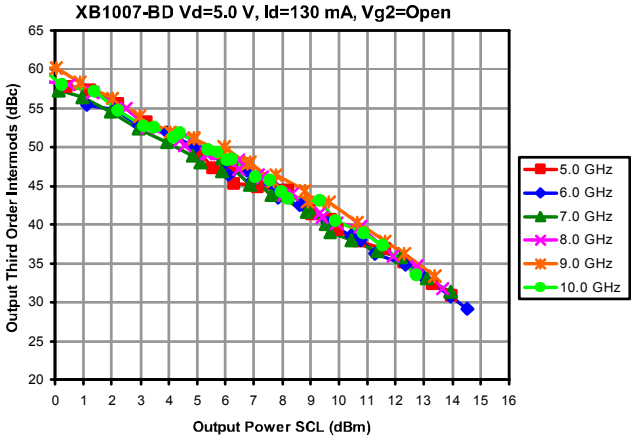
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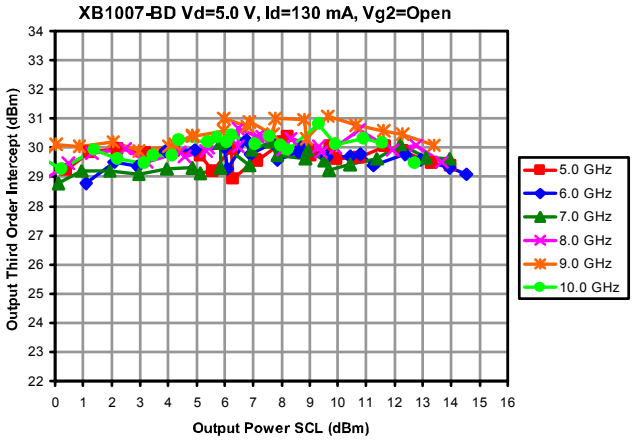
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S-Parameters

Typcial S-Parameter Data for XB1007-BD
Vd=4.5 V, Id=130 mA

Frequency (GHz)	S11 (Mag)	S11 (Ang)	S21 (Mag)	S21 (Ang)	S12 (Mag)	S12 (Ang)	S22 (Mag)	S22 (Ang)
0.045	0.978	-4.96	0.025	-167.48	0.0012	2.71	1.000	-3.23
1.0	0.558	-47.76	2.108	96.03	0.0001	-117.16	0.881	-75.42
2.0	0.292	-50.93	5.334	55.58	0.0009	141.34	0.646	-133.66
3.0	0.211	-59.68	8.848	17.23	0.0016	81.43	0.502	176.53
4.0	0.189	-81.69	12.975	-20.85	0.0013	32.52	0.392	126.19
5.0	0.148	-92.58	16.002	-61.20	0.0010	14.48	0.299	71.12
6.0	0.049	-131.19	17.813	-103.17	0.0006	-143.50	0.235	2.95
7.0	0.031	103.39	16.657	-140.92	0.0010	90.00	0.183	-58.81
8.0	0.052	40.99	16.006	-173.62	0.0018	76.58	0.177	-98.54
9.0	0.089	14.70	14.867	154.53	0.0027	60.07	0.160	-133.12
10.0	0.044	20.61	14.065	123.27	0.0021	-3.97	0.127	-159.96
11.0	0.014	91.02	12.785	91.14	0.0014	-34.03	0.049	-166.81
12.0	0.058	124.81	11.218	59.48	0.0018	-103.20	0.074	-66.32
13.0	0.141	114.80	9.492	28.22	0.0021	-159.33	0.216	-78.40
14.0	0.223	104.74	7.781	-2.27	0.0037	160.77	0.370	-101.39
15.0	0.279	92.29	6.067	-31.02	0.0041	132.87	0.501	-122.23
16.0	0.329	77.30	4.663	-57.12	0.0038	133.16	0.610	-142.71
17.0	0.361	67.40	3.548	-80.79	0.0030	141.13	0.693	-159.49
18.0	0.376	60.85	2.701	-103.10	0.0058	134.50	0.760	-175.38
19.0	0.373	52.87	2.084	-123.45	0.0082	102.56	0.794	170.52
20.0	0.361	48.90	1.623	-142.31	0.0105	61.49	0.804	159.64

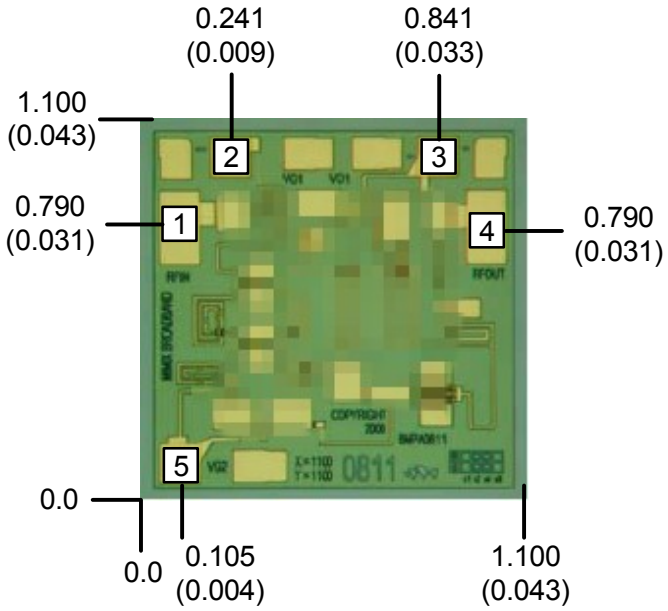
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Mechanical Drawing

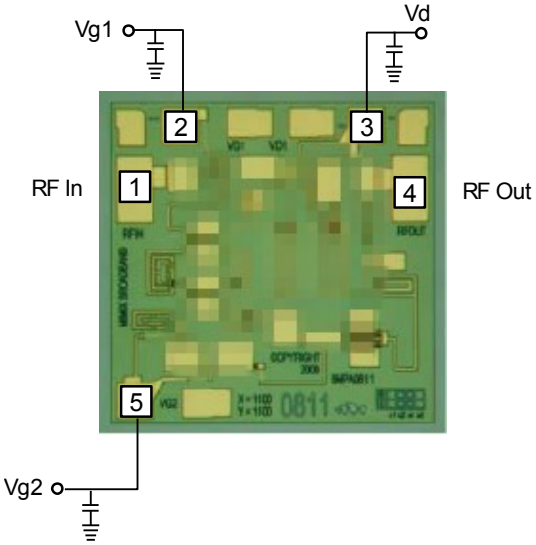


(Note: Engineering designator is 8MPA0811)

Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
All DC Bond Pads (except Vd3) are 0.100 x 0.100 (0.004 x 0.004). All RF Bond Pads (and Vd3) are 0.100 x 0.200 (0.004 x 0.008)
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 0.75 mg.

Bond Pad #1 (RF In)
Bond Pad #2 (Vg1)
Bond Pad #3 (Vd)
Bond Pad #4 (RF Out)
Bond Pad #5 (Vg2)

Bias Arrangement



Bypass Capacitors - See App Note [2]

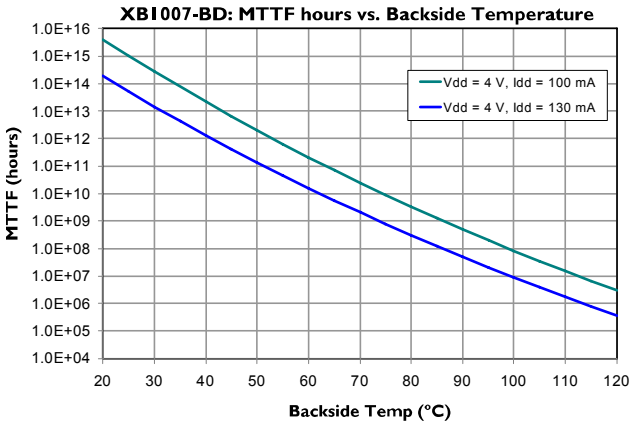
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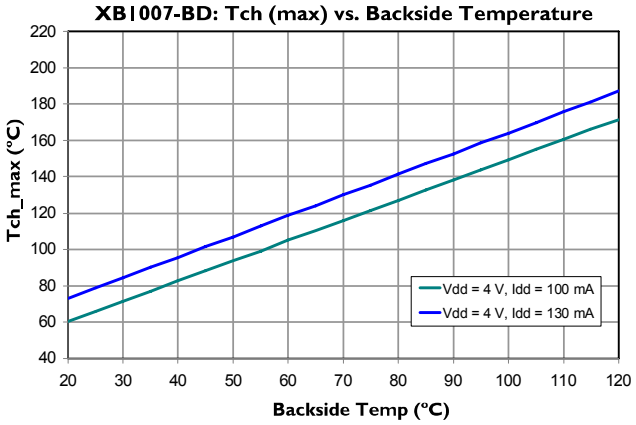
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MTTF

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.





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App Note [1] Biasing - The device provides variable gain with adjustable bias regulation. For optimum linearity performance, it is recommended to bias this device at Vd=4 V with Id=90 mA (Vg2 at approximately -0.5 V and Vg1 left open). It is also recommended to use active biasing to control the drain currents because this gives the most reproducible results over temperature or RF level variations. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.5 V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement - For Individual Stage Bias (Recommended for saturated applications) -- Each DC pad (Vd and Vg1,2) needs to have DC bypass capacitance (~100-200 pF) as close to the device as possible. Additional DC bypass capacitance (~0.01 uF) is also recommended.

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Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.

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