X28HC256

256k, 32k x 8-Bit, 5V, Byte Alterable EEPROM

FN8108
Rev 5.00
August 27, 2015

The X28HC256 is a second generation high performance CMOS 32k x 8 EEPROM. It is fabricated with Intersil's proprietary, textured poly floating gate technology, providing a highly reliable 5V only nonvolatile memory.

The X28HC256 supports a 128-byte page write operation, effectively providing a 24µs/byte write cycle, and enabling the entire memory to be typically rewritten in less than 0.8s. The X28HC256 also features $\overline{\text{DATA}}$ polling and Toggle bit polling, two methods of providing early end of write detection. The X28HC256 also supports the JEDEC standard software data protection feature for protecting against inadvertent writes during power-up and power-down.

Endurance for the X28HC256 is specified as a minimum 100,000 write cycles per byte and an inherent data retention of 100 years.

Features

- Access time: 90ns
- Simple byte and page write
  - Single 5V supply
  - No external high voltages or V_{P-P} control circuits
  - Self timed
  - No erase before write
  - No complex programming algorithms
  - No overerase problem
- Low power CMOS
  - Active: 60mA
  - Standby: 500µA
- Software data protection
  - Protects data against system level inadvertent writes
- High speed page write capability
- Highly reliable Direct Write™ cell
  - Endurance: 100,000 cycles
  - Data retention: 100 years
- Early end of write detection
  - $\overline{\text{DATA}}$ polling
  - Toggle bit polling
- RoHS compliant

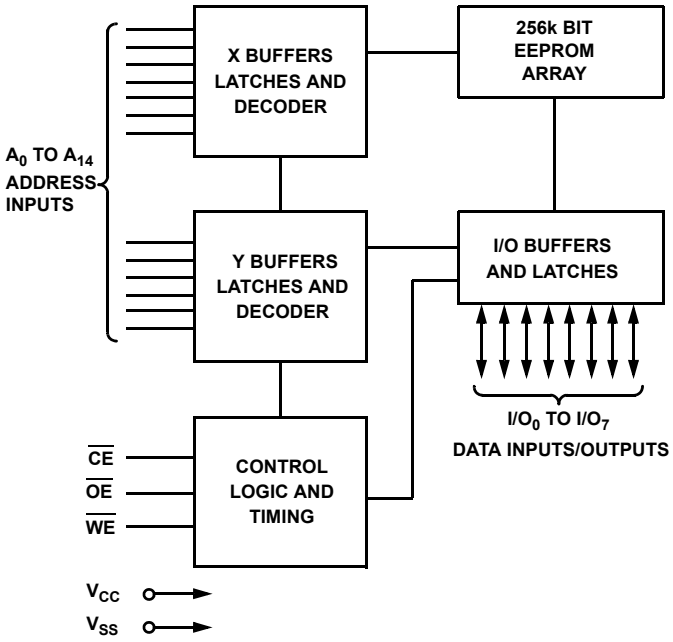


FIGURE 1. BLOCK DIAGRAM

Ordering Information

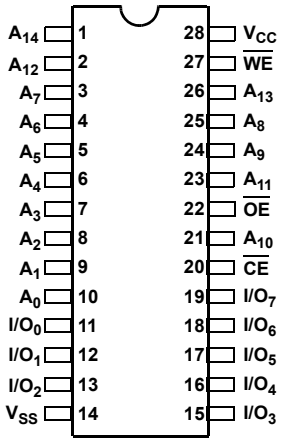
PART NUMBER (Note 4)	PART MARKING	ACCESS TIME (ns)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
X28HC256JZ-15 (Notes 1, 3)	X28HC256J-15 ZHY	150	0 to +70	32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC256JI-15 (Note 1)	X28HC256JI-15 HY	150	-40 to +85	32 Ld PLCC	N32.45x55
X28HC256JIZ-15 (Notes 1, 3)	X28HC256JI-15 ZHY	150	-40 to +85	32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC256PZ-15 (Notes 2, 3)	X28HC256P-15 HYZ	150	0 to +70	28 Ld PDIP (RoHS Compliant)	E28.6
X28HC256PIZ-15 (Notes 2, 3)	X28HC256PI-15 HYZ	150	-40 to +85	28 Ld PDIP (RoHS Compliant)	E28.6
X28HC256JZ-12 (Notes 1, 3)	X28HC256J-12 ZHY	120	0 to +70	32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC256JI-12 (Note 1)	X28HC256JI-12 HY	120	-40 to +85	32 Ld PLCC	N32.45x55
X28HC256JIZ-12 (Notes 1, 3)	X28HC256JI-12 ZHY	120	-40 to +85	32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC256PZ-12 (Notes 2, 3)	X28HC256P-12 HYZ	120	0 to +70	28 Ld PDIP (RoHS Compliant)	E28.6
X28HC256PIZ-12 (Notes 2, 3)	X28HC256PI-12 HYZ	120	-40 to +85	28 Ld PDIP (RoHS Compliant)	E28.6
X28HC256SZ-12 (Note 3)	X28HC256S-12 HYZ	120	0 to +70	28 Ld SOIC (300mils RoHS Compliant)	MDP0027
X28HC256SI-12	X28HC256SI-12 HY	120	-40 to +85	28 Ld SOIC (300mils)	M28.3
X28HC256SIZ-12 (Note 3)	X28HC256SI-12 HYZ	120	-40 to +85	28 Ld SOIC (300mils RoHS Compliant)	MDP0027
X28HC256JZ-90 (Notes 1, 3)	X28HC256J-90 ZHY	90	0 to +70	32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC256JI-90 (Note 1)	X28HC256JI-90 HY	90	-40 to +85	32 Ld PLCC	N32.45x55
X28HC256JIZ-90 (Notes 1, 3)	X28HC256JI-90 ZHY	90	-40 to +85	32 Ld PLCC (RoHS Compliant)	N32.45x55
X28HC256PZ-90 (Notes 2, 3)	X28HC256P-90 HYZ	90	0 to +70	28 Ld PDIP (RoHS Compliant)	E28.6
X28HC256PIZ-90 (Notes 2, 3)	X28HC256PI-90 HYZ	90	-40 to +85	28 Ld PDIP (RoHS Compliant)	E28.6
X28HC256SI-90	X28HC256SI-90 HY	90	-40 to +85	28 Ld SOIC (300mils)	M28.3
X28HC256SIZ-90 (Note 3)	X28HC256SI-90 HYZ	90	-40 to +85	28 Ld SOIC (300mils RoHS Compliant)	MDP0027

NOTES:

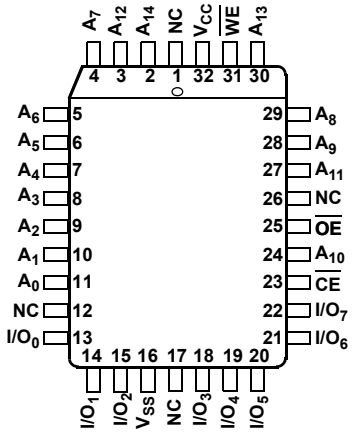
1. Add "T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see product information page for X28HC256. For more information on MSL, please see tech brief TB363.

Pin Configurations

X28HC256
(28 LD FLATPACK, PDIP, SOIC)
TOP VIEW



X28HC256
(32 LD PLCC, LCC)
TOP VIEW



Pin Descriptions

PIN NAME	PIN # PDIP, SOIC	PIN # PLCC, LCC	DESCRIPTION
A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8, A_9, A_{10}, A_{11}, A_{12}, A_{13}, A_{14}	10, 9, 8, 7, 6, 5, 4, 3, 25, 24, 21, 23, 2, 26, 1	11, 10, 9, 8, 7, 6, 5, 4, 29, 28, 24, 27, 3, 30, 2	**Addresses (A_0 to A_{14}) -** Address inputs. The address inputs select an 8-bit memory location during a read or write operation.
I/O_0, I/O_1, I/O_2, I/O_3, I/O_4, I/O_5, I/O_6, I/O_7	11, 12, 13, 15 16, 17, 18, 19	13, 14, 15, 18 19, 20, 21, 22	**Data In/Data Out (I/O_0 to I/O_7)** - Data input/output- Data is written to or read from the X28HC256 through the I/O pins.
$\overline{WE}$	27	31	**Write Enable ($\overline{WE}$)** - The Write enable input controls the writing of data to the X28HC256.
$\overline{CE}$	20	23	**Chip Enable ($\overline{CE}$)** - The Chip enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.
$\overline{OE}$	22	25	**Output Enable ($\overline{OE}$)** - The output enable input controls the data output buffers, and is used to initiate read operations.
V_{CC}	28	32	+5V
V_{SS}	14	16	Ground
NC	-	1, 12, 17, 26	No Connect

Absolute Maximum Ratings

Voltage on any Pin with Respect to V_{SS} . . . . . 1V to +7V
DC Output Current 10mA

Recommended Operating Conditions

Temperature Range
Commercial . . . . . 0°C to +70°C
Industrial . . . . . -40°C to +85°C
Supply Voltage . . . . . 5V ± 10%

Thermal Information

Temperature Under Bias
X28HC256 . . . . . -10°C to +85°C
X28HC256I . . . . . -65°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

DC Electrical Specifications

Across recommended operating conditions, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN (Note 7)	TYP (Note 5)	MAX (Note 7)	
V_{CC} Active Current (TTL Inputs)	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = open, address inputs = 0.4V/2.4V levels at f = 10MHz		30	60	mA
V_{CC} Standby Current (TTL Inputs)	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, All I/O's = open, other inputs = V_{IH}		1	2	mA
V_{CC} Standby Current (CMOS Inputs)	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.3V, $\overline{OE}$ = GND, All I/Os = open, other inputs = V_{CC} - 0.3V		200	500	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}			10	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}			10	µA
Input Low Voltage	V_{IL} (Note 6)		-1		0.8	V
Input High Voltage	V_{IH} (Note 6)		2		V_{CC} + 1	V
Output Low Voltage	V_{OL}	I_{OL} = 6mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4			V

NOTES:
5. Typical values are for T_A = +25°C and nominal supply voltage.
6. V_{IL} minimum and V_{IH} maximum are for reference only and are not tested.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Power-up Timing

PARAMETER	SYMBOL	MAX	UNIT
Power-up to Read	t_{PUR}, (Note 8)	100	µs
Power-up to Write	t_{PUW}, (Note 8)	5	ms

NOTE:
8. This parameter is periodically sampled and not 100% tested.

Capacitance

T_A = +25°C, f = 1MHz, V_{CC} = 5V.

SYMBOL	TEST	CONDITIONS	MAX	UNIT
$C_{I/O}$ (Note 8)	Input/output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN} (Note 8)	Input capacitance	V_{IN} = 0V	6	pF

Endurance and Data Retention

PARAMETER	MIN	MAX	UNIT
Endurance	100,000		Cycles
Data retention	100		Years

AC Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	5ns
Input and output timing levels	1.5V

Mode Selection

CE	OE	WE	MODE	I/O	POWER
L	L	H	Read	D_{OUT}	active
L	H	L	Write	D_{IN}	active
H	X	X	Standby and write inhibit	High Z	standby
X	L	X	Write inhibit	—	—
X	X	H	Write inhibit	—	—

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Equivalent AC Load Circuit

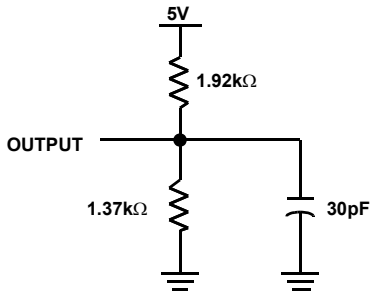


FIGURE 2. EQUIVALENT AC LOAD CIRCUIT

AC Electrical Specifications

Across recommended operating conditions, unless otherwise specified.

PARAMETER	SYMBOL	X28HC256-70		X28HC256-90		X28HC256-12		X28HC256-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	70		90		120		150		ns
Chip Enable Access Time	t_{CE}		70		90		120		150	ns
Address Access Time	t_{AA}		70		90		120		150	ns
Output Enable Access Time	t_{OE}		35		40		50		50	ns
$\overline{CE}$ LOW to Active Output	t_{LZ} (Note 9)	0		0		0		0		ns
$\overline{OE}$ LOW to Active Output	t_{OLZ} (Note 9)	0		0		0		0		ns
$\overline{CE}$ HIGH to High Z Output	t_{HZ} (Note 9)		35		40		50		50	ns
$\overline{OE}$ HIGH to High Z Output	t_{OHZ} (Note 9)		35		40		50		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns

NOTE:

9. t_{LZ} minimum, t_{HZ}, t_{OLZ} minimum and t_{OHZ} are periodically sampled and not 100% tested, t_{HZ} and t_{OHZ} are measured with C_L = 5pF, from the point when $\overline{CE}$, $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven..

Read Cycle

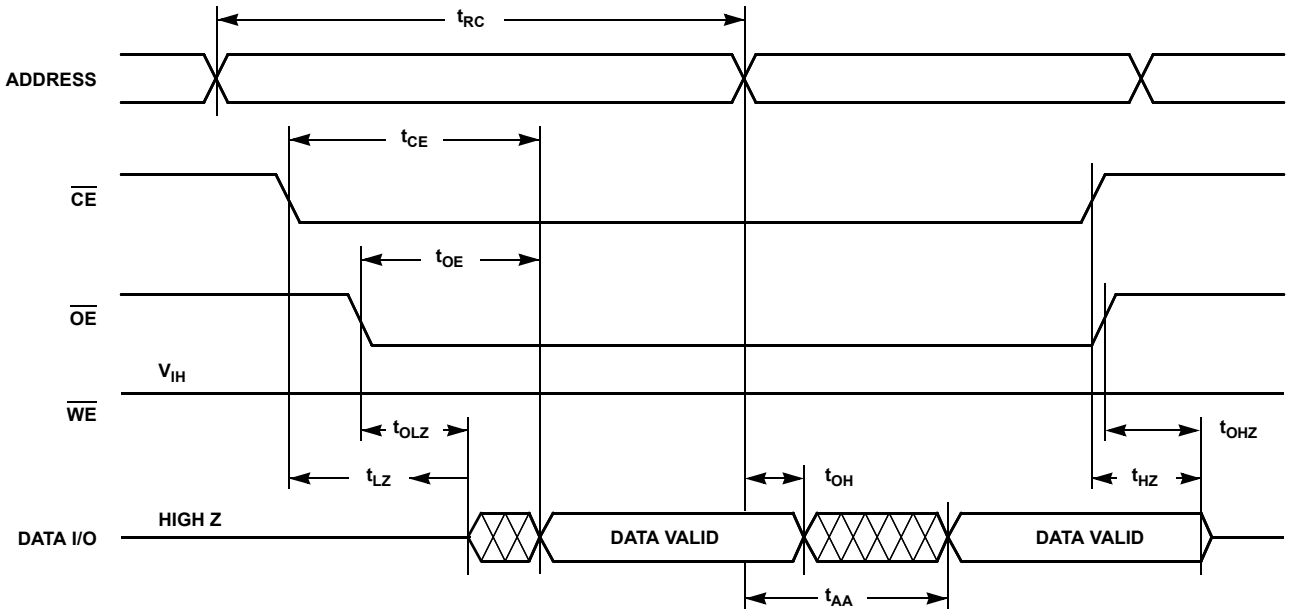


FIGURE 3. READ CYCLE

Write Cycle Limits

PARAMETER	SYMBOL	MIN	TYP (Note 10)	MAX	UNIT
Write Cycle Time	t_{WC} (Note 11)		3	5	ms
Address Setup Time	t_{AS}	0			ns
Address Hold Time	t_{AH}	50			ns
Write Setup Time	t_{CS}	0			ns
Write Hold Time	t_{CH}	0			ns
$\overline{CE}$ Pulse Width	t_{CW}	50			ns
$\overline{OE}$ HIGH Setup Time	t_{OES}	0			ns
$\overline{OE}$ HIGH Hold Time	t_{OEH}	0			ns
$\overline{WE}$ Pulse Width	t_{WP}	50			ns
$\overline{WE}$ HIGH Recovery (page write only)	t_{WPH} (Note 12)	50			ns
Data Valid	t_{DV}			1	µs
Data Setup	t_{DS}	50			ns
Data Hold	t_{DH}	0			ns
Delay to Next Write After Polling is True	t_{DW} (Note 12)	10			µs
Byte Load Cycle	t_{BLC}	0.15		100	µs

NOTES:

10. Typical values are for T_A = +25°C and nominal supply voltage.
11. t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
12. t_{WPH} and t_{DW} are periodically sampled and not 100% tested.

$\overline{WE}$ Controlled Write Cycle

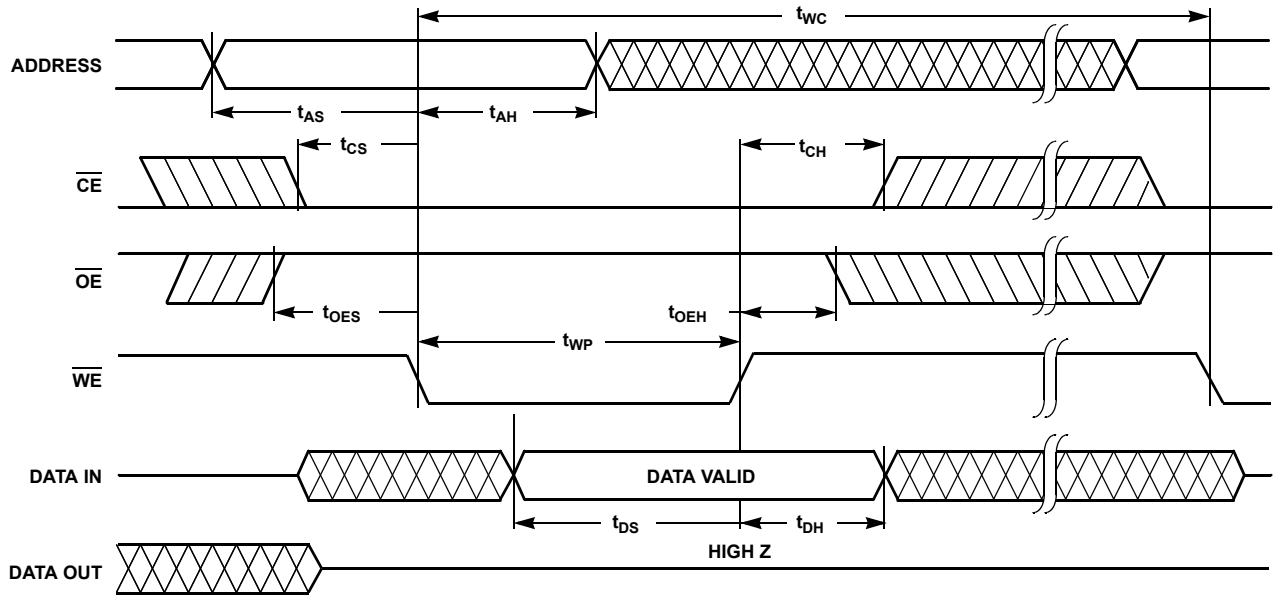


FIGURE 4. $\overline{WE}$ CONTROLLED WRITE CYCLE

$\overline{CE}$ Controlled Write Cycle

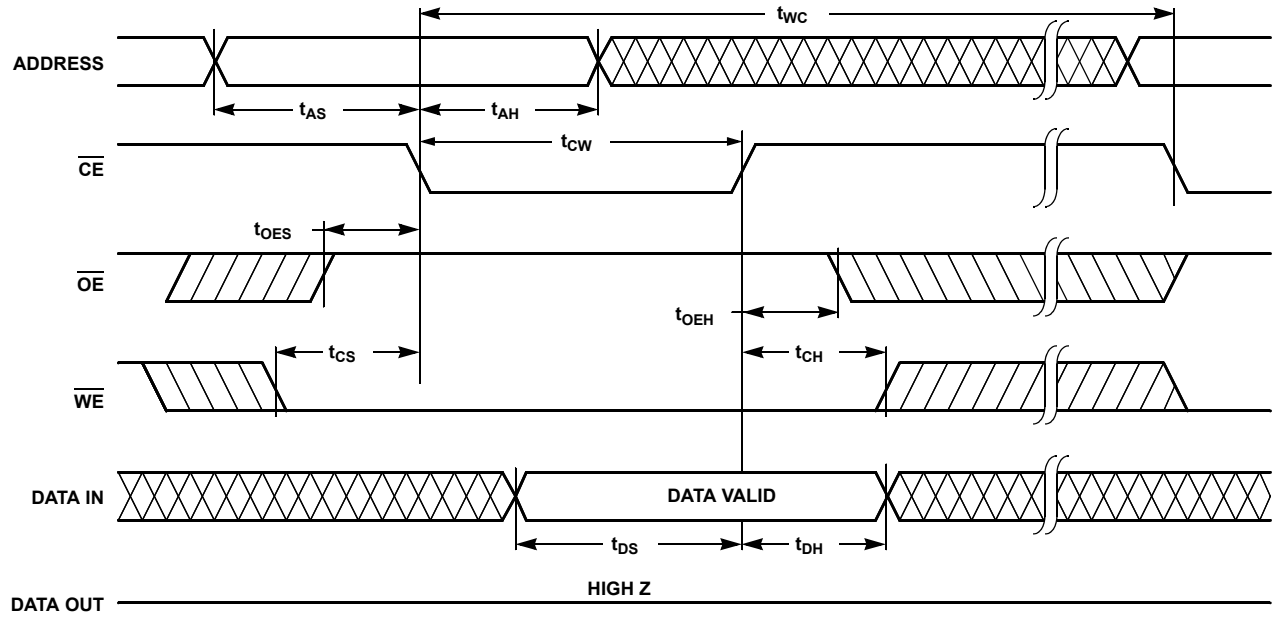


FIGURE 5. $\overline{CE}$ CONTROLLED WRITE CYCLE

Page Write Cycle

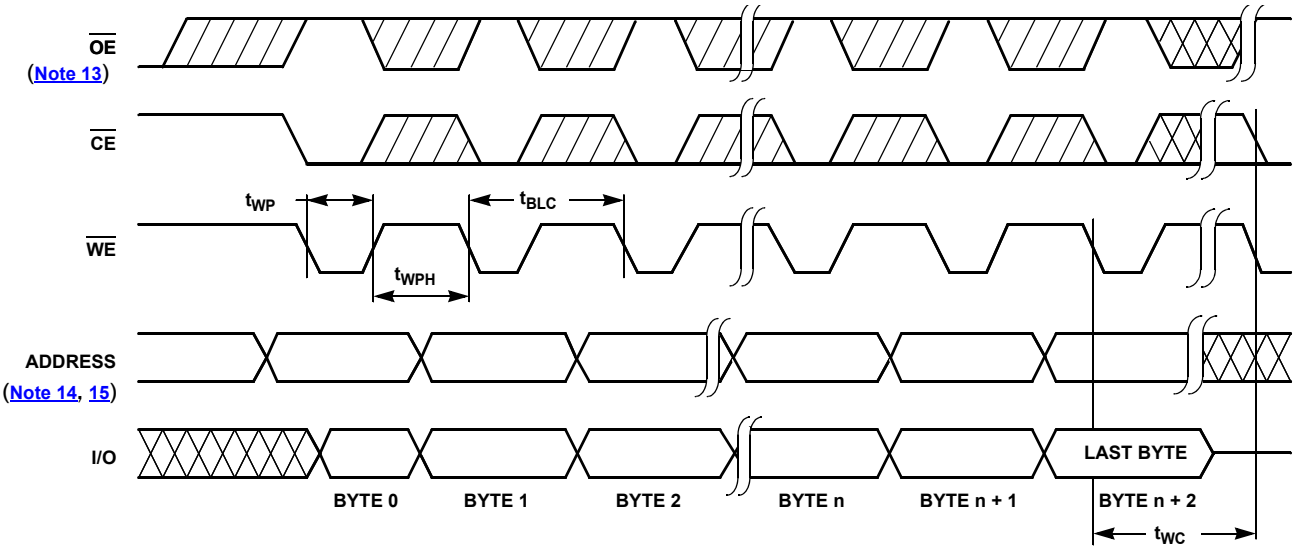


FIGURE 6. PAGE WRITE CYCLE

NOTES:

13. Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.
14. The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.
15. For each successive write within the page write operation, A7 to A15 should be the same or writes to an unknown address could occur.

$\overline{\text{DATA}}$ Polling Timing Diagram (Note 16)

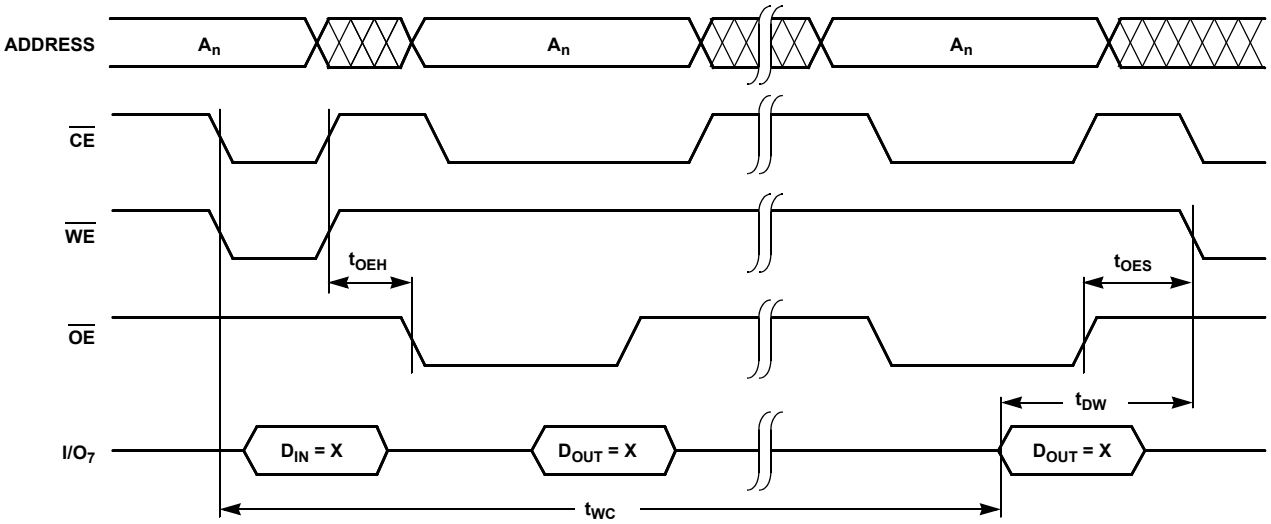


FIGURE 6. $\overline{\text{DATA}}$ POLLING TIMING DIAGRAM

Toggle Bit Timing Diagram (Note 16)

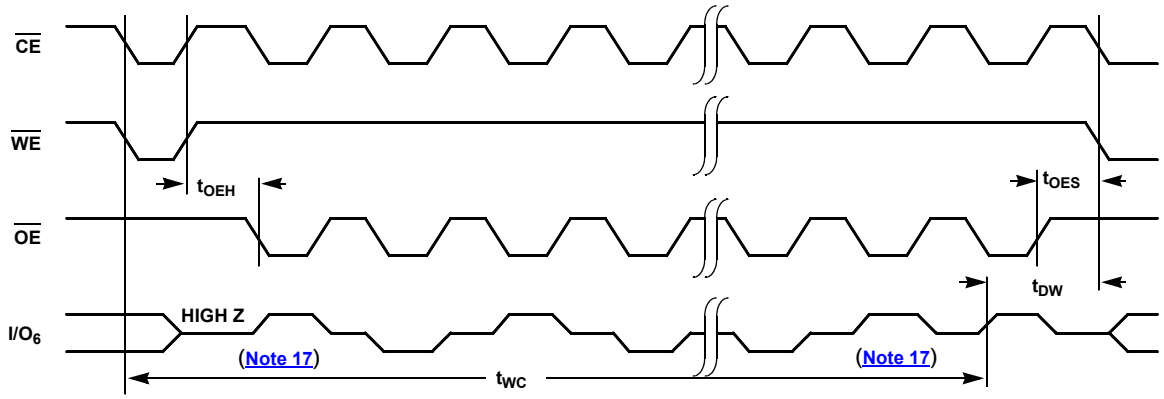


FIGURE 7. TOGGLE BIT TIMING DIAGRAM

NOTES:

16. Polling operations are by definition read cycles and are therefore subject to read cycle timings.
17. I/O_6 beginning and ending state will vary, depending upon actual t_{WC}.

Device Operation

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28HC256 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3ms.

Page Write Operation

The page write feature of the X28HC256 allows the entire memory to be written in typically 0.8 seconds. The page write allows up to 128 bytes of data to be consecutively written to the X28HC256, prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_7 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to 127 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ high-to-low transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ high-to-low transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28HC256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 7.

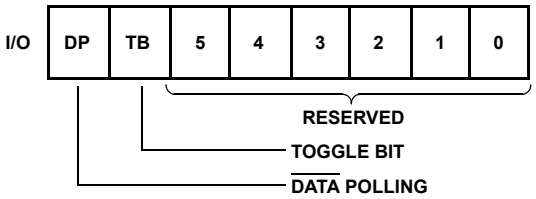


FIGURE 7. STATUS BIT ASSIGNMENT

$\overline{DATA}$ Polling (I/O_7)

The X28HC256 features $\overline{DATA}$ polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ polling allows a simple bit test operation to determine the status of the X28HC256. This eliminates additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

Toggle Bit (I/O_6)

The X28HC256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from high-to-low and high-to-low on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read and write operations.

$\overline{DATA}$ Polling I/O

$\overline{DATA}$ polling can effectively halve the time for writing to the X28HC256. The timing diagram in Figure 8 on page 11 illustrates the sequence of events on the bus. The software flow diagram in Figure 9 on page 11 illustrates one method of implementing the routine.

The Toggle Bit I/O

The toggle bit can eliminate the chore of saving and fetching the last address and data in order to implement $\overline{DATA}$ polling. This can be especially helpful in an array comprised of multiple X28HC256 memories that is frequently updated. The timing diagram in Figure 10 on page 12 illustrates the sequence of events on the bus. The software flow diagram in Figure 11 on page 12 illustrates a method for polling the toggle bit.

Hardware Data Protection

The X28HC256 provides two hardware features that protects nonvolatile data from inadvertent writes.

- Default V_{CC} Sense — All write functions are inhibited when V_{CC} is 3.5V typically.
- Write Inhibit — Holding either $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

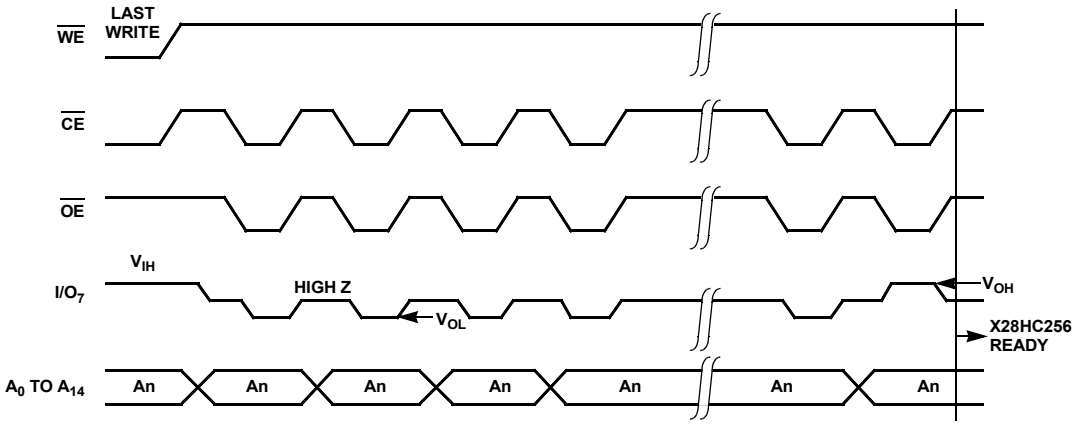


FIGURE 8. $\overline{\text{DATA}}$ POLLING BUS SEQUENCE

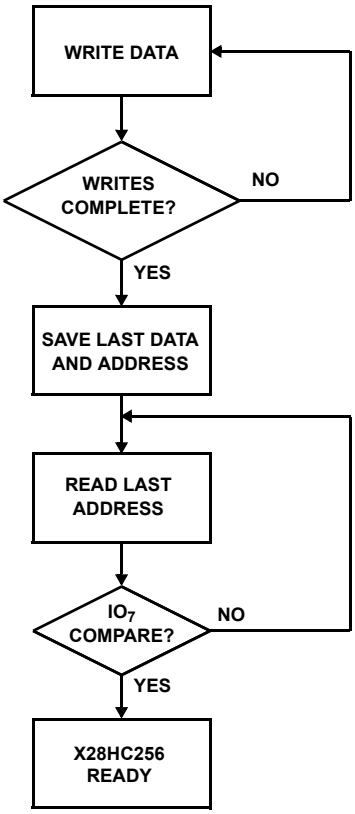
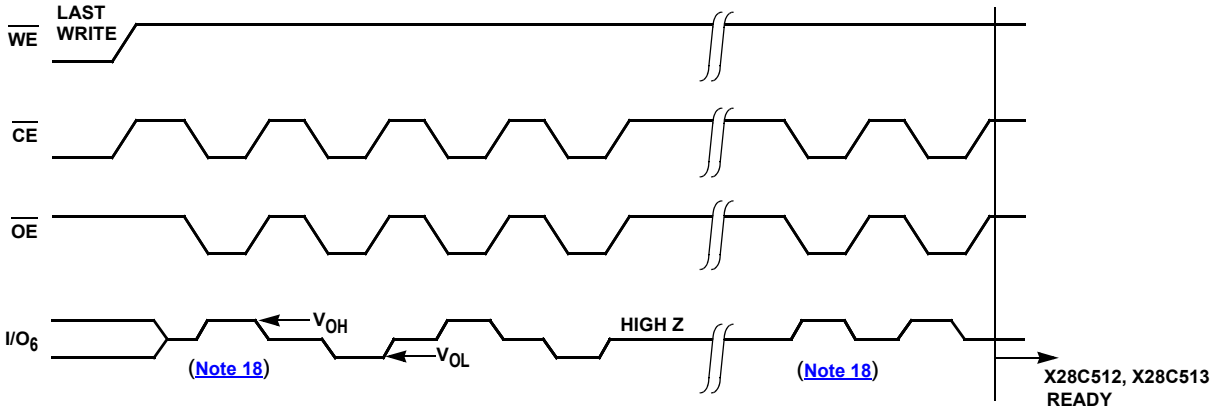


FIGURE 9. $\overline{\text{DATA}}$ POLLING SOFTWARE FLOW



NOTE:
18. I/O6 Beginning and ending state of I/O6 will vary.

FIGURE 10. TOGGLE BIT BUS SEQUENCE

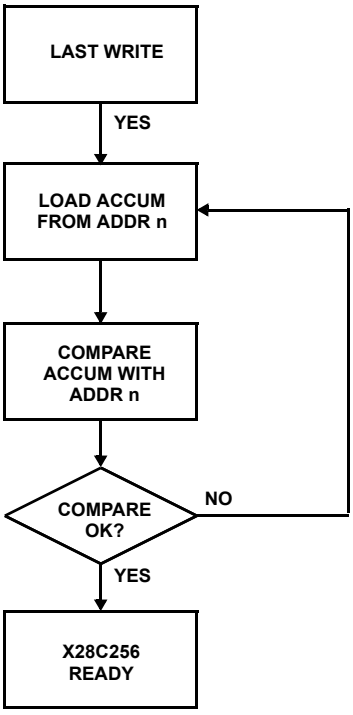


FIGURE 11. TOGGLE BIT SOFTWARE FLOW

Software Data Protection

The X28HC256 offers a software controlled data protection feature. The X28HC256 is shipped from Intersil with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28HC256 can be automatically protected during power-up and power-down (without the need for external circuits) by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation, utilizing the software algorithm. This circuit is nonvolatile, and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28HC256 is also protected from inadvertent and accidental writes in the powered up state. That is, the software algorithm must be issued prior to writing additional data to the device.

Software Algorithm

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figures 12 and 13 on page 13 for the sequence. The 3 byte sequence opens the page write window, enabling the host to write from one to 128 bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Software Data Protection

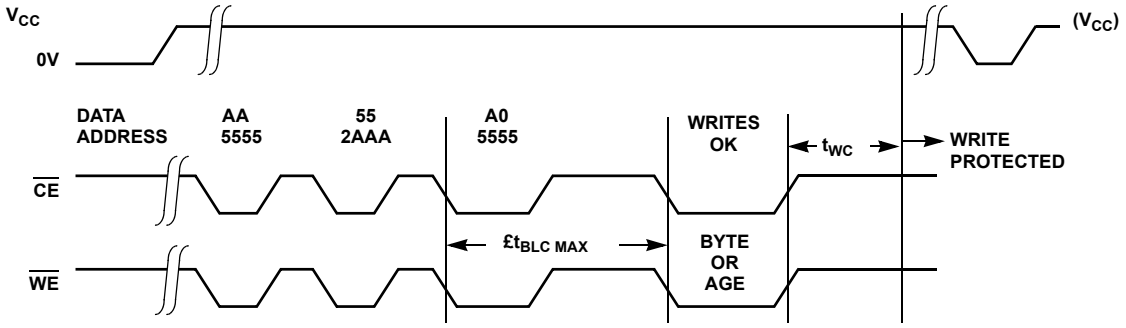


FIGURE 12. TIMING SEQUENCE BYTE OR PAGE WRITE

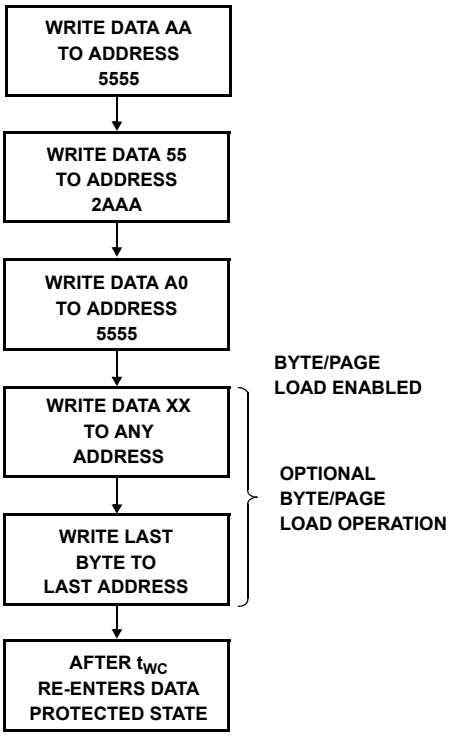


FIGURE 13. WRITE SEQUENCE FOR SOFTWARE DATA PROTECTION

Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28HC256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28HC256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

Resetting Software Data Protection

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an EEPROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28HC256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

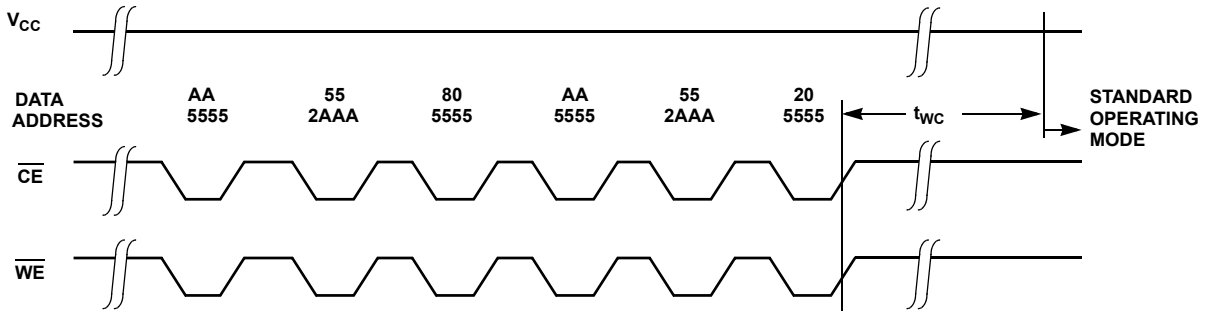


FIGURE 14. RESET SOFTWARE DATA PROTECTION TIMING SEQUENCE

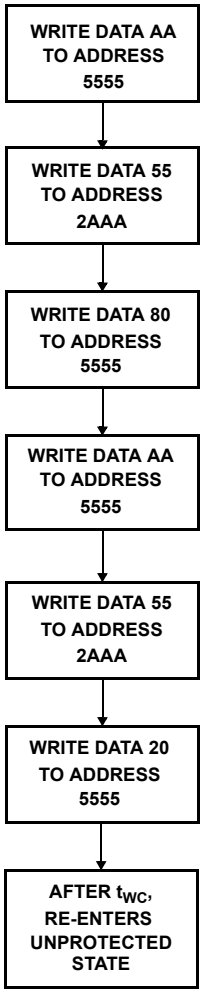


FIGURE 15. WRITE SEQUENCE FOR RESETTING SOFTWARE DATA PROTECTION

System Considerations

Because the X28HC256 is frequently used in large memory arrays, it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation, this assures that all deselected devices are in their standby mode and that only the selected device(s) is/are outputting data on the bus.

Because the X28HC256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 27, 2015	FN8108.5	Removed the reference to Military part under “Recommended Operating Conditions” and “Thermal Information” Removed X28HC256J-15, X28HC256SI-15, X28HC256SIZ-15, X28HC256J-12, X28HC256S-12, and X28HC256S-90 from the Ordering Information table on page 2. Updated Pin Description table on page 3.
March 31, 2015	FN8108.4	-Updated entire datasheet to Intersil new standard. -Added revision history and about Intersil verbiage. -Third paragraph on page 1 updated From: Endurance for the X28HC256 is specified as a minimum 1,000,000 write cycles per byte and an inherent data retention of 100 years. To: Endurance for the X28HC256 is specified as a minimum 100,000 write cycles per byte and an inherent data retention of 100 years. -Features section on page 1 updated From: Highly reliable Direct Write™ cell - Endurance: 1,000,000 cycles To: Highly reliable Direct Write™ cell - Endurance: 100,000 cycles “Endurance and Data Retention” on page 4 updated Endurance from 1,000,000 to 100,000. -Ordering information table on page 2: Removed obsolete part numbers X28HC256P-15, X28HC256PI-15, X28HC256P-12, X28HC256PI-12, X28HC256P-90. -Ordering information table on page 2 updated the “Access time’ section. Thermal Information table on page 4 updated “Temperature Under Bias” section for X28HC256 value from 10°C to +85°C to -10°C to +85°C. “DC Electrical Specifications” on page 4, added a note to Min and Max values. Removed note in Electrical Spec Table that referenced an obsolete part.

About Intersil

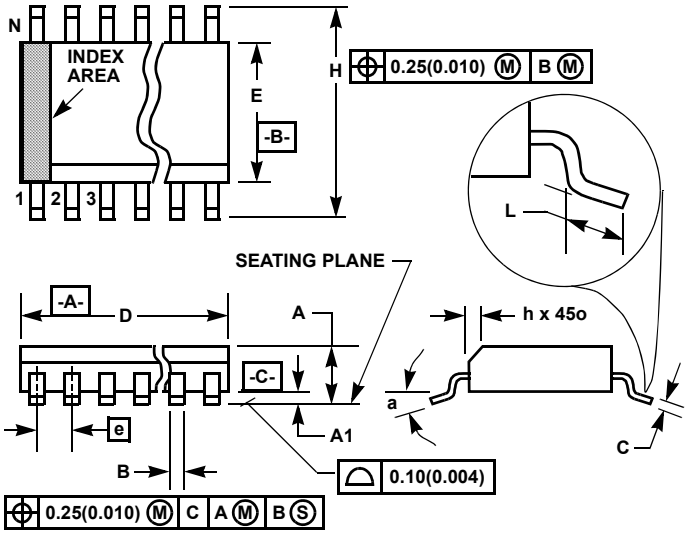
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Small Outline Plastic Packages (SOIC)

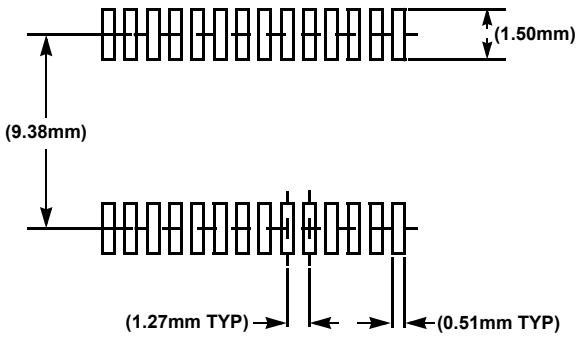


M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

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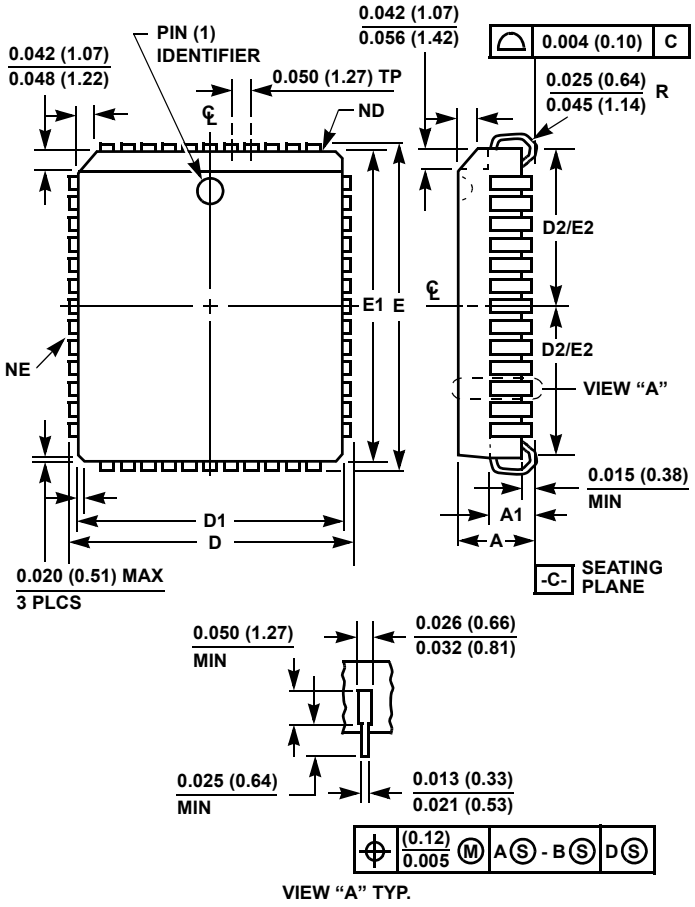
TYPICAL RECOMMENDED LAND PATTERN



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Plastic Leaded Chip Carrier Packages (PLCC)



N32.45x55 (JEDEC MS-016AE ISSUE A)

32 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

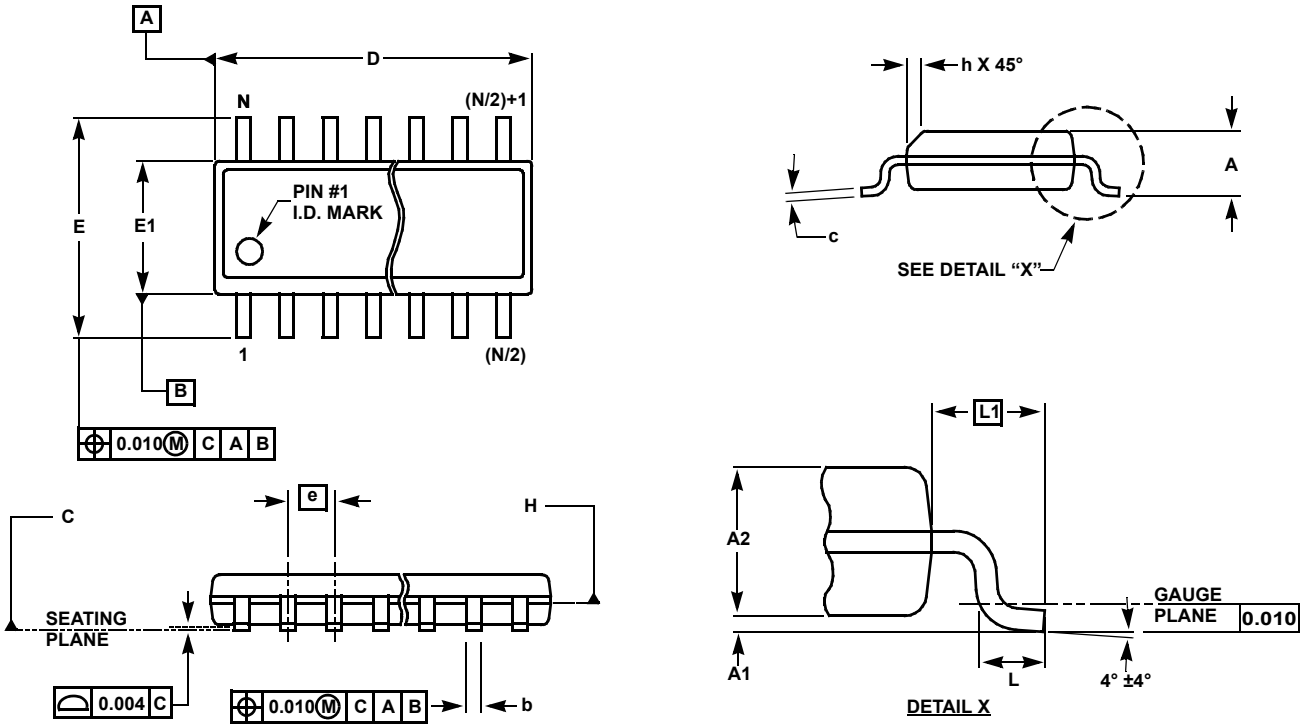
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.125	0.140	3.18	3.55	-
A1	0.060	0.095	1.53	2.41	-
D	0.485	0.495	12.32	12.57	-
D1	0.447	0.453	11.36	11.50	3
D2	0.188	0.223	4.78	5.66	4, 5
E	0.585	0.595	14.86	15.11	-
E1	0.547	0.553	13.90	14.04	3
E2	0.238	0.273	6.05	6.93	4, 5
N	28		28		6
ND	7		7		7
NE	9		9		7

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.
7. ND denotes the number of leads on the two shorts sides of the package, one of which contains pin #1. NE denotes the number of leads on the two long sides of the package.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

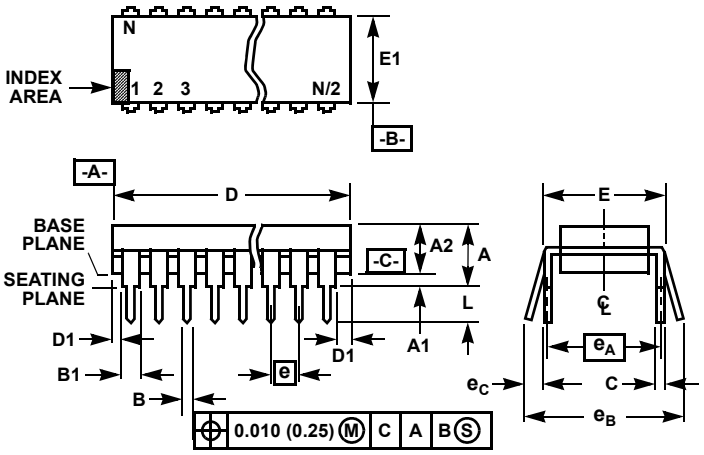
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

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NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)

28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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