5 Volt, Byte Alterable EEPROM

The Intersil X28C010 is a 128K x 8 EEPROM, fabricated with Intersil's proprietary, high performance, floating gate CMOS technology. Like all Intersil programmable non-volatile memories, the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pin out for byte-wide memories, compatible with industry standard EEPROMs.

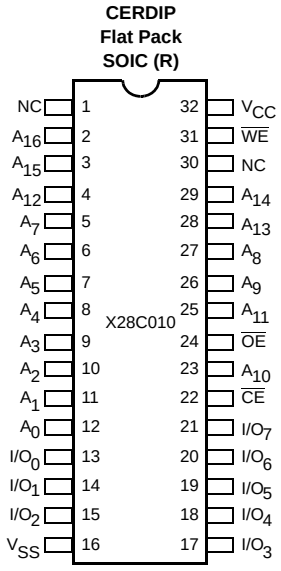
The X28C010 supports a 256-byte page write operation, effectively providing a 19µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C010 also features DATA Polling and Toggle Bit Polling, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C010 supports Software Data Protection option.

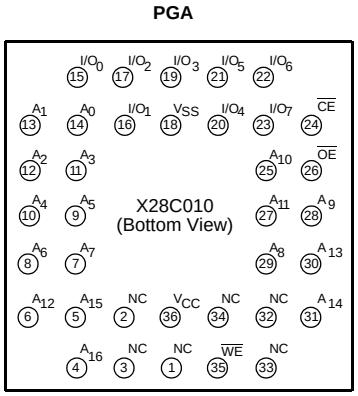
Intersil EEPROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

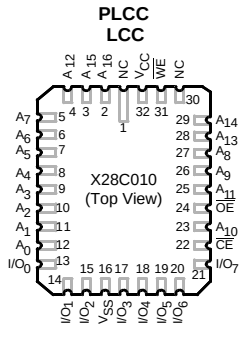
Features

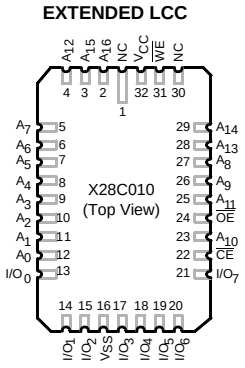
- Access time: 120ns
- Simple byte and page write
  - Single 5V supply
  - No external high voltages or V_{PP} control circuits
  - Self-timed
    - No erase before write
    - No complex programming algorithms
    - No overerase problem
- Low power CMOS
  - Active: 50mA
  - Standby: 500µA
- Software data protection
  - Protects data against system level inadvertent writes
- High speed page write capability
- Highly reliable Direct Write™ cell
  - Endurance: 100,000 write cycles
  - Data retention: 100 years
- Early end of write detection
  - $\overline{DATA}$ polling
  - Toggle bit polling

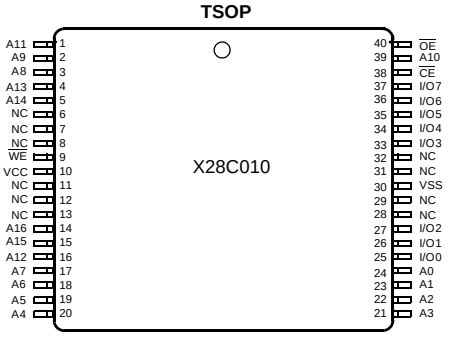
Pinouts











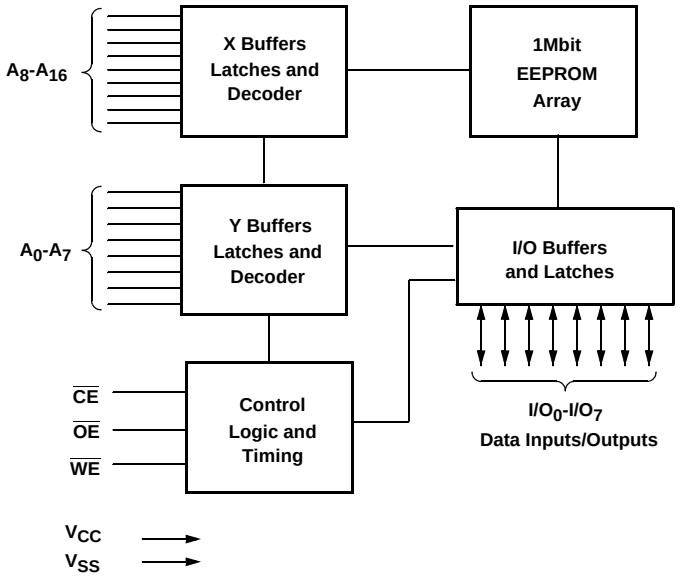
Ordering Information

PART NUMBER	ACCESS TIME	PACKAGE	TEMP RANGE (°C)
X28C010D	-	32-Ld Cerdip	0 to 70
X28C010D-12	120ns	32-Ld Cerdip	0 to 70
X28C010D-15	150ns	32-Ld Cerdip	0 to 70
X28C010DI	-	32-Ld Cerdip	-40 to +85
X28C010DI-12	120ns	32-Ld Cerdip	-40 to +85
X28C010DI-15	150ns	32-Ld Cerdip	-40 to +85
X28C010DI-15C7681	150ns	32-Ld Cerdip	-40 to +85
X28C010DM	-	32-Ld Cerdip	-55 to +125
X28C010DM-12	120ns	32-Ld Cerdip	-55 to +125
X28C010DMB-12	120ns	32-Ld Cerdip	MIL-STD-883
X28C010DMB-12C7309	120ns	32-Ld Cerdip	MIL-STD-883
X28C010DMB-12C7729	120ns	32-Ld Cerdip	MIL-STD-883
X28C010DMB-15	150ns	32-Ld Cerdip	MIL-STD-883
X28C010DMB-15C7762	150ns	32-Ld Cerdip	MIL-STD-883
X28C010DMB-20	200ns	32-Ld Cerdip	MIL-STD-883
X28C010DMC7237	-	32-Ld Cerdip	
X28C010FI-12	120ns	32-Ld Flat Pack	-40 to +85
X28C010FI-15	150ns	32-Ld Flat Pack	-40 to +85
X28C010FI-15C1009	150ns	32-Ld Flat Pack	-40 to +85
X28C010FI-20	200ns	32-Ld Flat Pack	-40 to +85
X28C010FI-25	250ns	32-Ld Flat Pack	-40 to +85
X28C010FM	-	32-Ld Flat Pack	-55 to +125
X28C010FM-12	120ns	32-Ld Flat Pack	-55 to +125
X28C010FMB-15	150ns	32-Ld Flat Pack	MIL-STD-883
X28C010FMB-15C7619	150ns	32-Ld Flat Pack	MIL-STD-883
X28C010FMB-15C7808	150ns	32-Ld Flat Pack	MIL-STD-883
X28C010K-25	250ns	36-Ld Pin Grid Array	0 to 70
X28C010KM-12	120ns	36-Ld Pin Grid Array	-55 to +125
X28C010KM-25	250ns	36-Ld Pin Grid Array	-55 to +125
X28C010KM-25C7237	250ns	36-Ld Pin Grid Array	-55 to +125
X28C010KMB-15	150ns	36-Ld Pin Grid Array	MIL-STD-883

Ordering Information (Continued)

PART NUMBER	ACCESS TIME	PACKAGE	TEMP RANGE (°C)
X28C010NM-12	120ns	32-Ld Extended LCC	-55 to +125
X28C010NM-15	150ns	32-Ld Extended LCC	-55 to +125
X28C010NMB-12	120ns	32-Ld Extended LCC	MIL-STD-883
X28C010NMB-15	150ns	32-Ld Extended LCC	MIL-STD-883
X28C010NMB-15C7309	150ns	32-Ld Extended LCC	MIL-STD-883
X28C010RI-12	120ns	32-Ld Ceramic SOIC (Gull Wing)	-40 to +85
X28C010RI-20	200ns	32-Ld Ceramic SOIC (Gull Wing)	-40 to +85
X28C010RI-20C7168	200ns	32-Ld Ceramic SOIC (Gull Wing)	-40 to +85
X28C010RI-20C7975	200ns	32-Ld Ceramic SOIC (Gull Wing)	-40 to +85
X28C010RI-20T1	200ns	32-Ld Ceramic SOIC (Gull Wing)	-40 to +85
X28C010RI-20T1C7168	200ns	32-Ld Ceramic SOIC (Gull Wing)	-40 to +85
X28C010RM-15	150ns	32-Ld Ceramic SOIC (Gull Wing)	-55 to +125
X28C010RMB-25	250ns	32-Ld Ceramic SOIC (Gull Wing)	MIL-STD-883

Block Diagram



Pin Descriptions

Addresses (A_0-A_{16})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers, and is used to initiate read operations.

Data In/Data Out (I/O_0-I/O_7)

Data is written to or read from the X28C010 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28C010.

Pin Names

SYMBOL	DESCRIPTION
A_0-A_{16}	Address Inputs
I/O_0-I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

Device Operation

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

The page write feature of the X28C010 allows the entire memory to be written in 5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_8 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty six bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

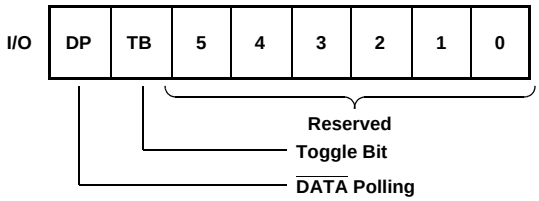


FIGURE 1. STATUS BIT ASSIGNMENT

$\overline{DATA}$ Polling (I/O_7)

The X28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C010 is in the protected state, and an illegal write operation is attempted, $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

DATA Polling I/O_7

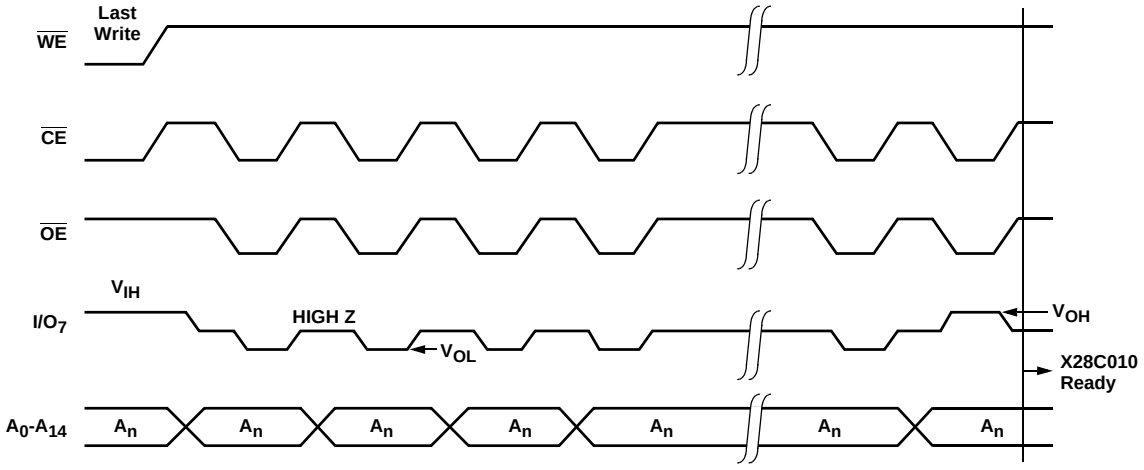


FIGURE 2. DATA POLLING BUS SEQUENCE

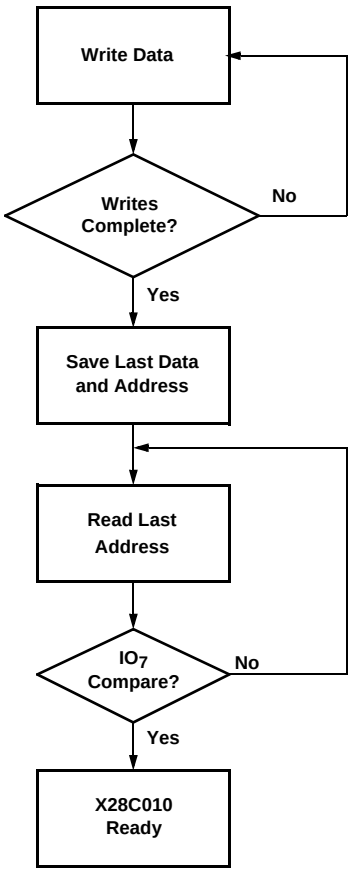
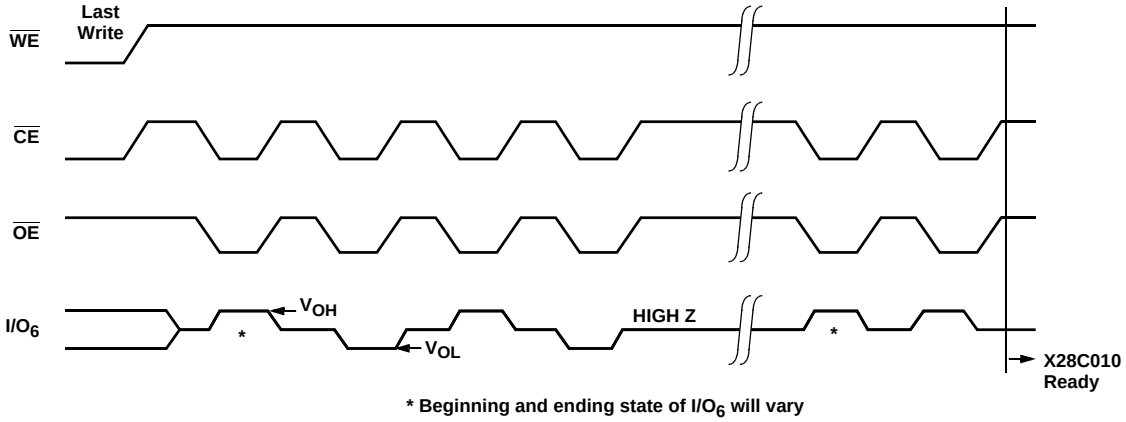


FIGURE 3. $\overline{\text{DATA}}$ POLLING SOFTWARE FLOW

$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28C010. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

The Toggle Bit I/O$_6$



* Beginning and ending state of I/O$_6$ will vary

FIGURE 4. TOGGLE BIT BUS SEQUENCE

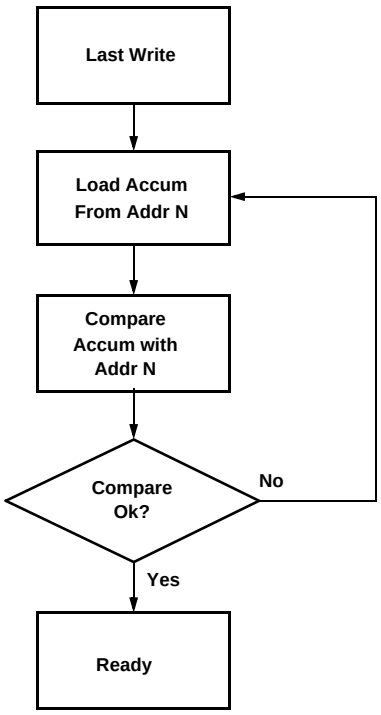


FIGURE 5. TOGGLE BIT SOFTWARE FLOW

The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C010 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

Hardware Data Protection

The X28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$ 3.5V.
- Write inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

Software Data Protection

The X28C010 offers a software controlled data protection feature. The X28C010 is shipped from Intersil with the software data protection NOT ENABLED: that is the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C010 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

Software Algorithm

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figures 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to two hundred fifty-six bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Software Data Protection

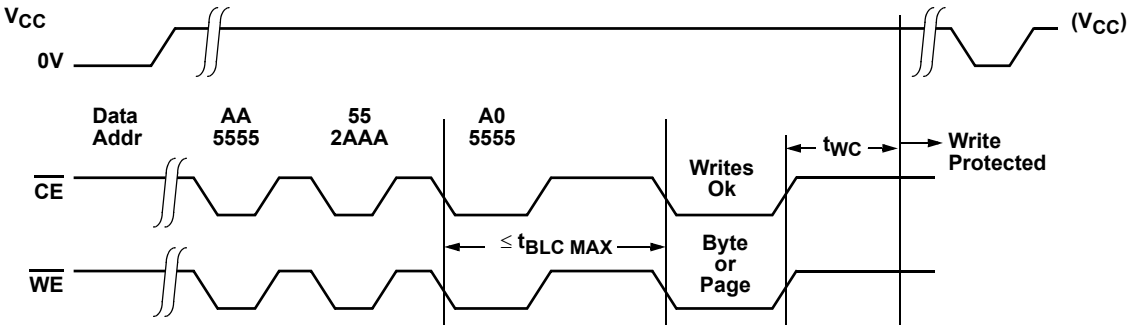


FIGURE 6. TIMING SEQUENCE—BYTE OR PAGE WRITE

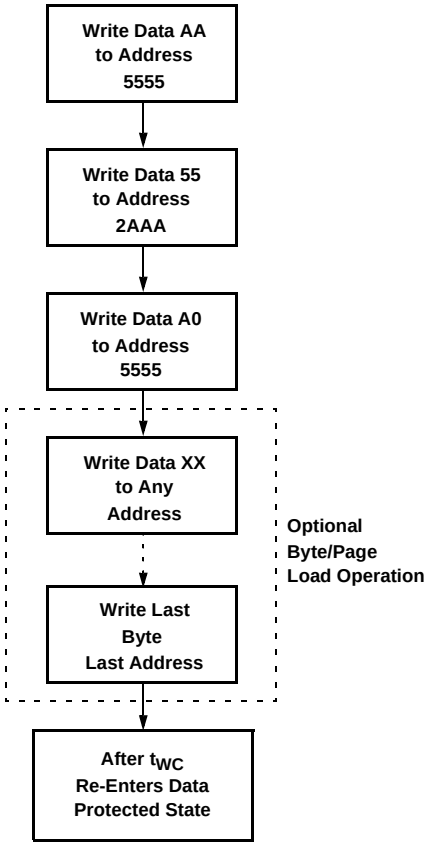


FIGURE 7. WRITE SEQUENCE FOR SOFTWARE DATA PROTECTION

Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C010 will be write protected during power-down and after any subsequent power-up. The state of A_{15} and A_{16} while executing the algorithm is don't care.

Note: Once initiated, the sequence of write operations should not be interrupted.

Resetting Software Data Protection

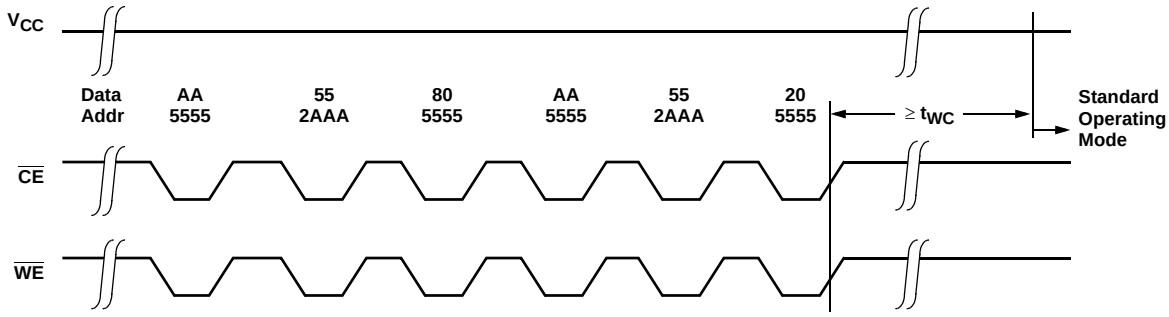


FIGURE 8. RESET SOFTWARE DATA PROTECTION TIMING SEQUENCE

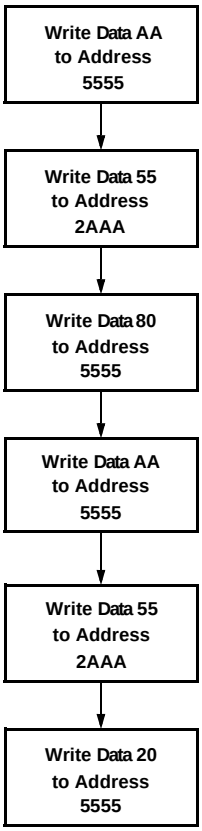


FIGURE 9. SOFTWARE SEQUENCE TO DEACTIVATE SOFTWARE DATA PROTECTION

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an EEPROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C010 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

System Considerations

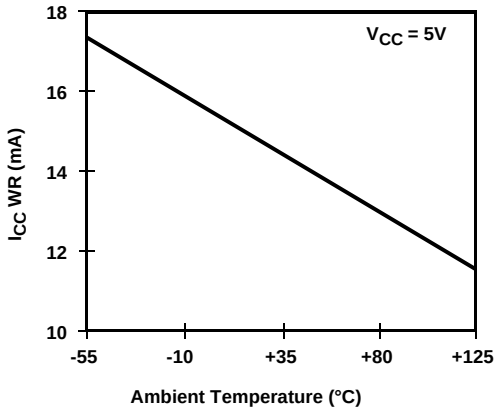
Because the X28C010 is frequently used in large memory arrays, it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

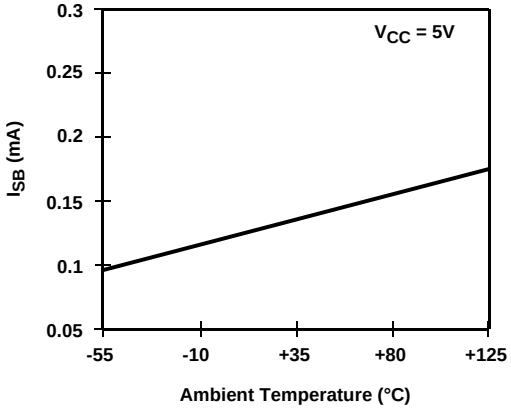
Because the X28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

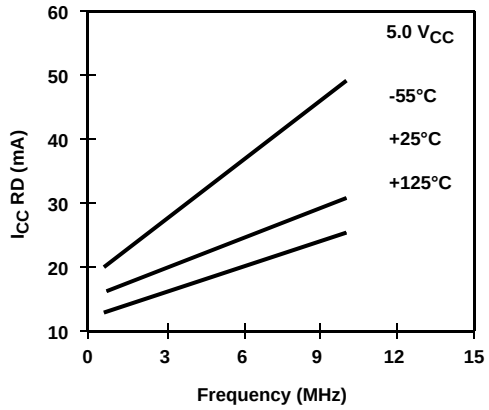
Active Supply Current vs. Ambient Temperature



Standby Supply Current vs. Ambient Temperature



I_{CC} (RD) by Temperature Over Frequency



Absolute Maximum Ratings

Temperature under bias
- X28C010 . . . . . -10°C to +85°C
- X28C010I . . . . . -65°C to +135°C
- X28C010M . . . . . -65°C to +135°C

Storage temperature . . . . . -65°C to +150°C
Voltage on any pin with respect to V_{SS} . . . . . -1V to +7V
D.C. output current. 5mA
Lead temperature
(soldering, 10 seconds) . . . . . 300°C

Recommended Operating Conditions

Commercial . . . . . 0°C to +70°C
Industrial . . . . . -40°C tp +85°C
Military . . . . . -55°C to +125°C
Supply Voltage. . . . . 5V ±10%

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions (above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Specifications

Over the recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	V_{CC} Current (Active) (TTL Inputs)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = 0.4V/2.4V Levels @ f = 5MHz		50	mA
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, All I/O's = Open, Other Inputs = V_{IH}		3	mA
I_{SB2}	V_{CC} Current (Standby) (CMOS Inputs)	$\overline{CE}$ = V_{CC} - 0.3V, $\overline{OE}$ = V_{IL}, All I/O's = Open, Other Inputs = V_{CC}		500	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}		10	µA
V_{IL} (Note 1)	Input LOW Voltage		-1	0.8	V
V_{IH} (Note 1)	Input HIGH Voltage		2	V_{CC} + 1	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -400µA	2.4		V

NOTE:

1. V_{IL} min. and V_{IH} max. are for reference only and are not tested.

Power-Up Timing

SYMBOL	PARAMETER	MAX	UNIT
t_{PUR} (Note 2)	Power-up to Read operation	100	µs
t_{PUW} (Note 2)	Power-up to Write operation	5	ms

Capacitance

T_A = +25°C, f = 1MHz, V_{CC} = 5V

SYMBOL	PARAMETER	TEST CONDITIONS	MAX	UNIT
$C_{I/O}$ (Note 2)	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN} (Note 2)	Input capacitance	V_{IN} = 0V	10	pF

NOTE:

2. This parameter is periodically sampled and not 100% tested.

Endurance and Data Retention

PARAMETER	MIN	MAX	UNIT
Endurance	10,000		Cycles per byte
Endurance	100,000		Cycles per page
Data Retention	100		Years

A.C. Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input and output timing levels	1.5V

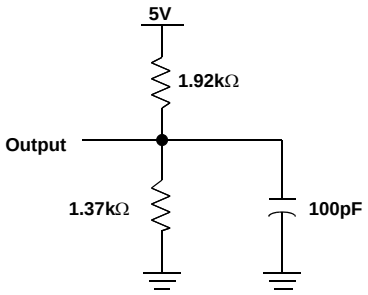
Mode Selection

CE	OE	WE	MODE	I/O	POWER
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Equivalent A.C. Load Circuit

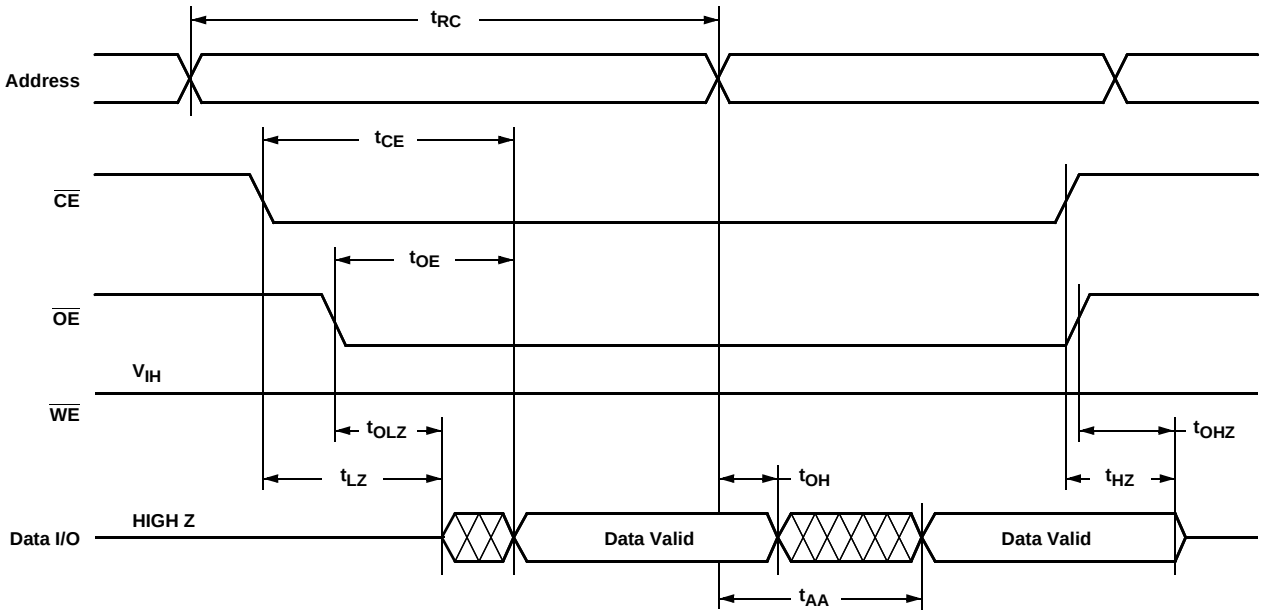


AC Electrical Specifications

Over the recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	X28C010-12		X28C010-15		X28C010-20		X28C010-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE LIMITS										
t_{RC}	Read cycle time	120		150		200		250		ns
t_{CE}	Chip enable access time		120		150		200		250	ns
t_{AA}	Address access time		120		150		200		250	ns
t_{OE}	Output enable access time		50		50		50		50	ns
t_{LZ} (Note 3)	$\overline{CE}$ LOW to active output	0		0		0		0		ns
t_{OLZ} (Note 3)	$\overline{OE}$ LOW to active output	0		0		0		0		ns
t_{HZ} (Note 3)	$\overline{CE}$ HIGH to high Z output		50		50		50		50	ns
t_{OHZ} (Note 3)	$\overline{OE}$ HIGH to high Z output		50		50		50		50	ns
t_{OH}	Output hold from address change	0		0		0		0		ns

Read Cycle



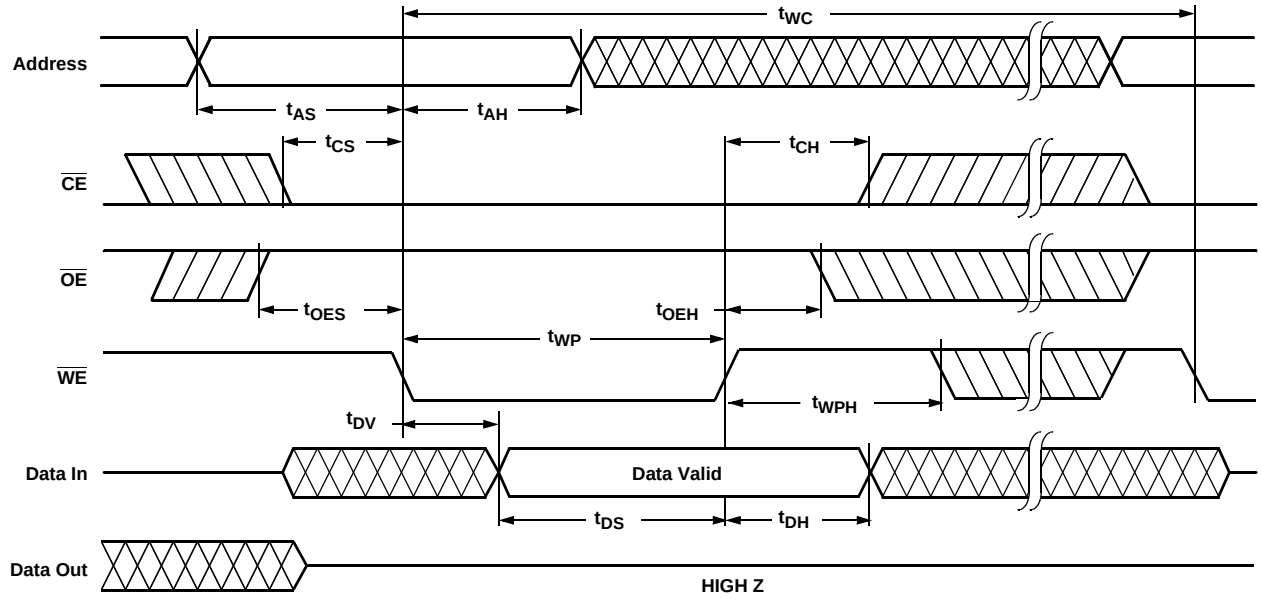
NOTE:

3. t_{LZ} min.,t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{WC} (Note 4)	Write cycle time		10	ms
t_{AS}	Address setup time	0		ns
t_{AH}	Address hold time	50		ns
t_{CS}	Write setup time	0		ns
t_{CH}	Write hold time	0		ns
t_{CW}	$\overline{CE}$ pulse width	100		ns
t_{OES}	$\overline{OE}$ HIGH setup time	10		ns
t_{OEH}	$\overline{OE}$ HIGH hold time	10		ns
t_{WP}	$\overline{WE}$ pulse width	100		ns
t_{WPH}	$\overline{WE}$ HIGH recovery	100		ns
t_{DV}	Data valid		1	µs
t_{DS}	Data setup	50		ns
t_{DH}	Data hold	0		ns
t_{DW}	Delay to next write	10		µs
t_{BLC}	Byte load cycle	0.2	100	µs

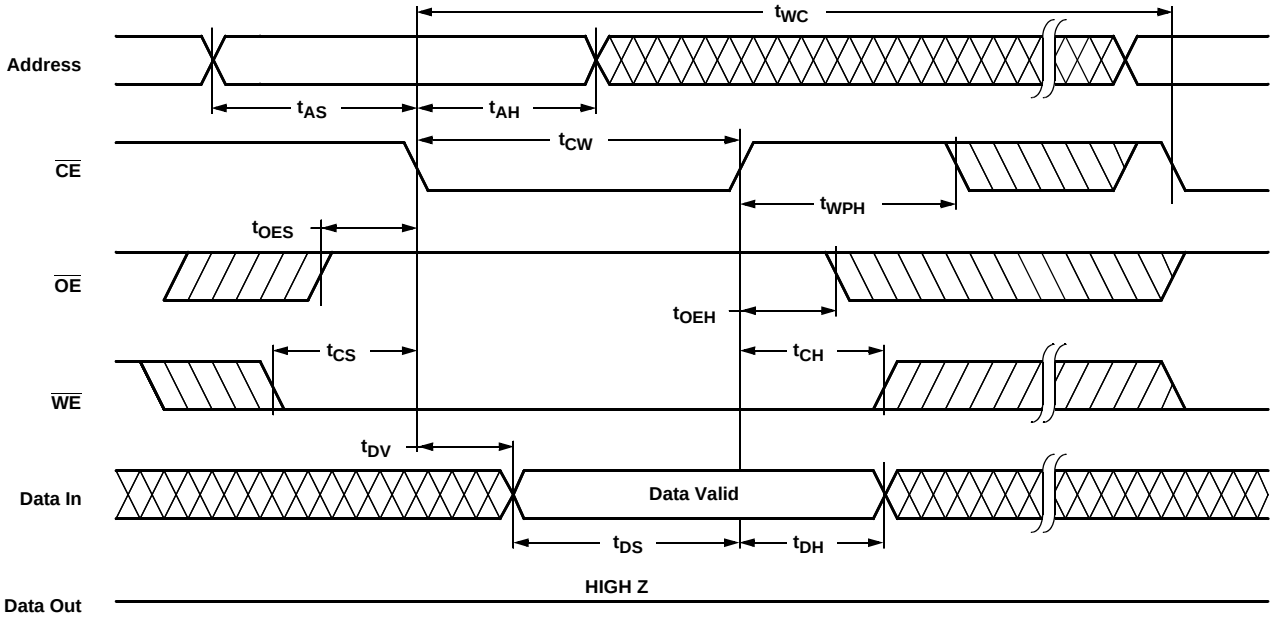
$\overline{WE}$ Controlled Write Cycle



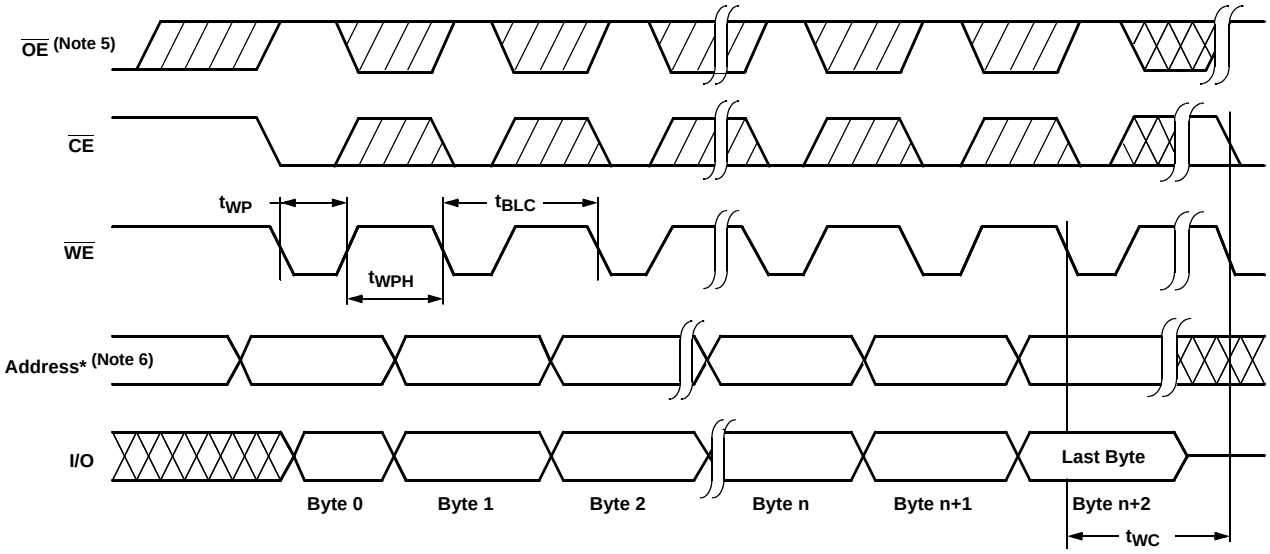
NOTE:

4. t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

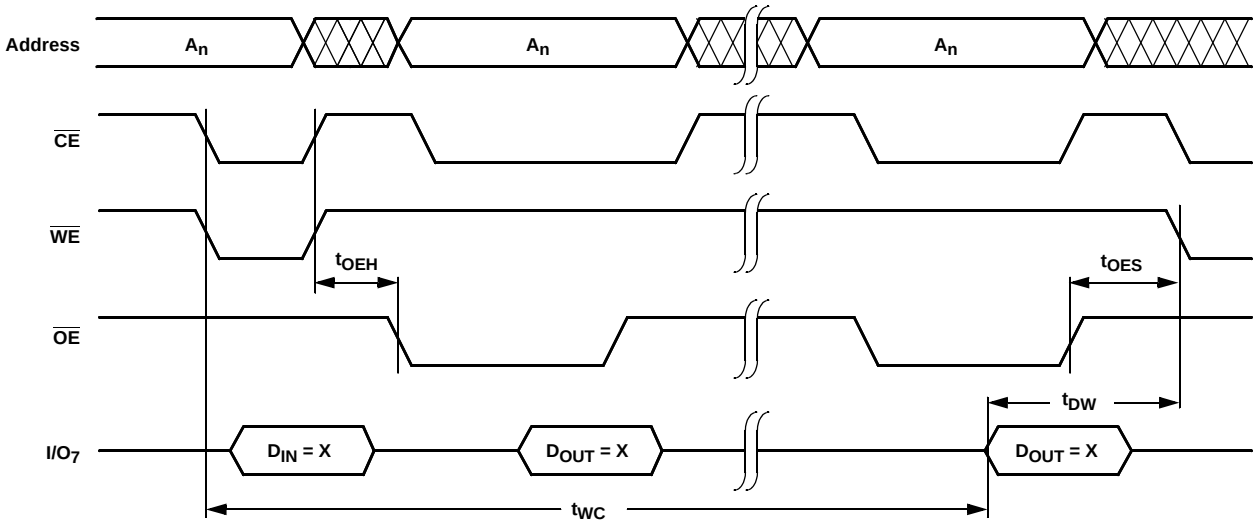


***For each successive write within the page write operation, A_8-A_{16} should be the same or writes to an unknown address could occur.**

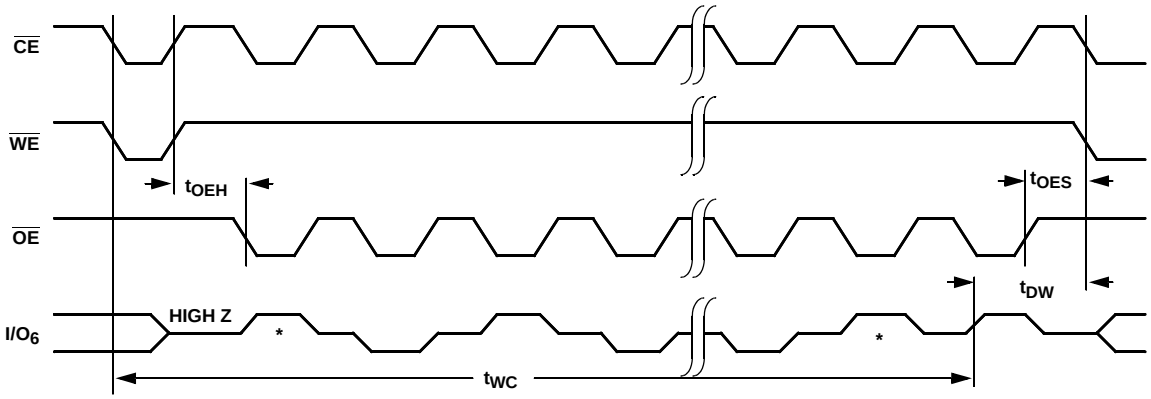
NOTES:

5. Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.
6. The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{DATA}$ Polling Timing Diagram (Note 7)



Toggle Bit Timing Diagram



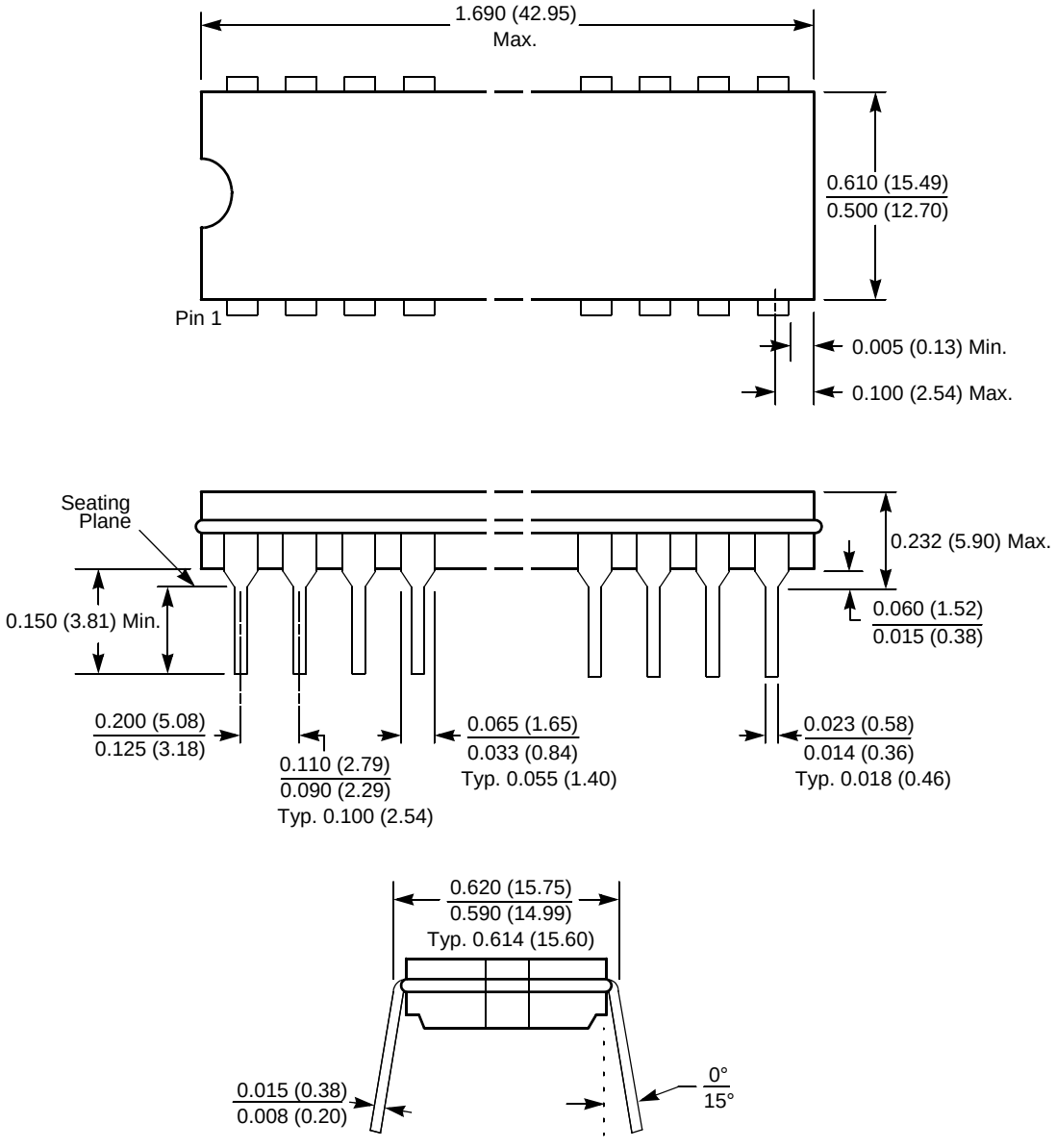
*** I/O_6 beginning and ending state will vary.**

NOTE:

7. Polling operations are by definition read cycles and are therefore subject to read cycle timings.

Packaging Information

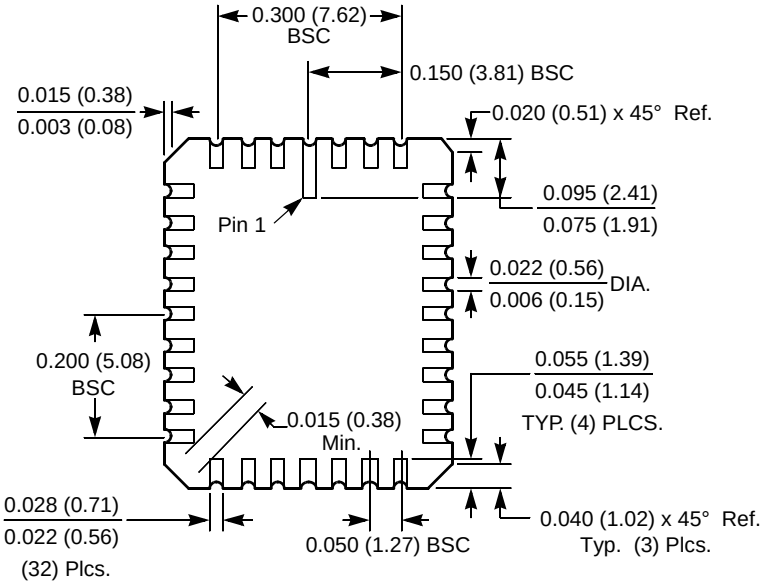
32-Lead Hermetic, CerDIP, Package Code D32

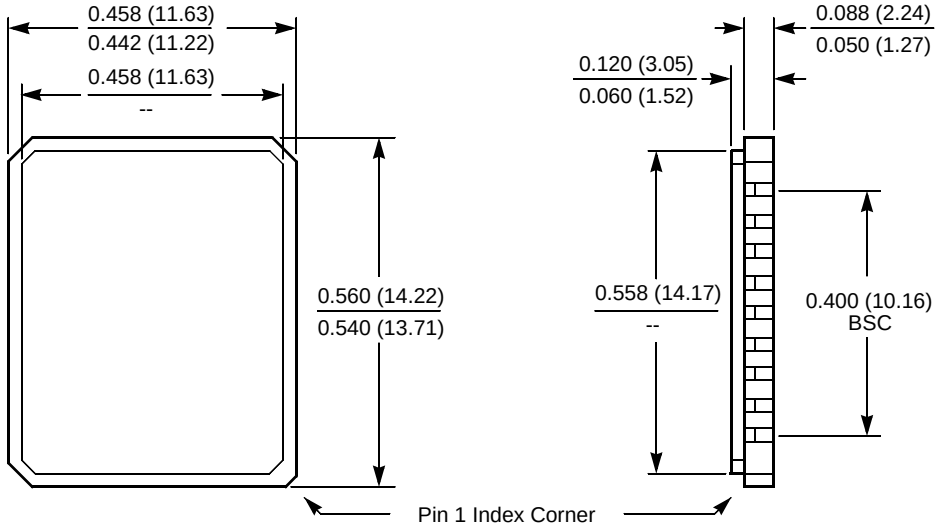


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information

32-Pad Ceramic Leadless Chip Carrier Package Type E

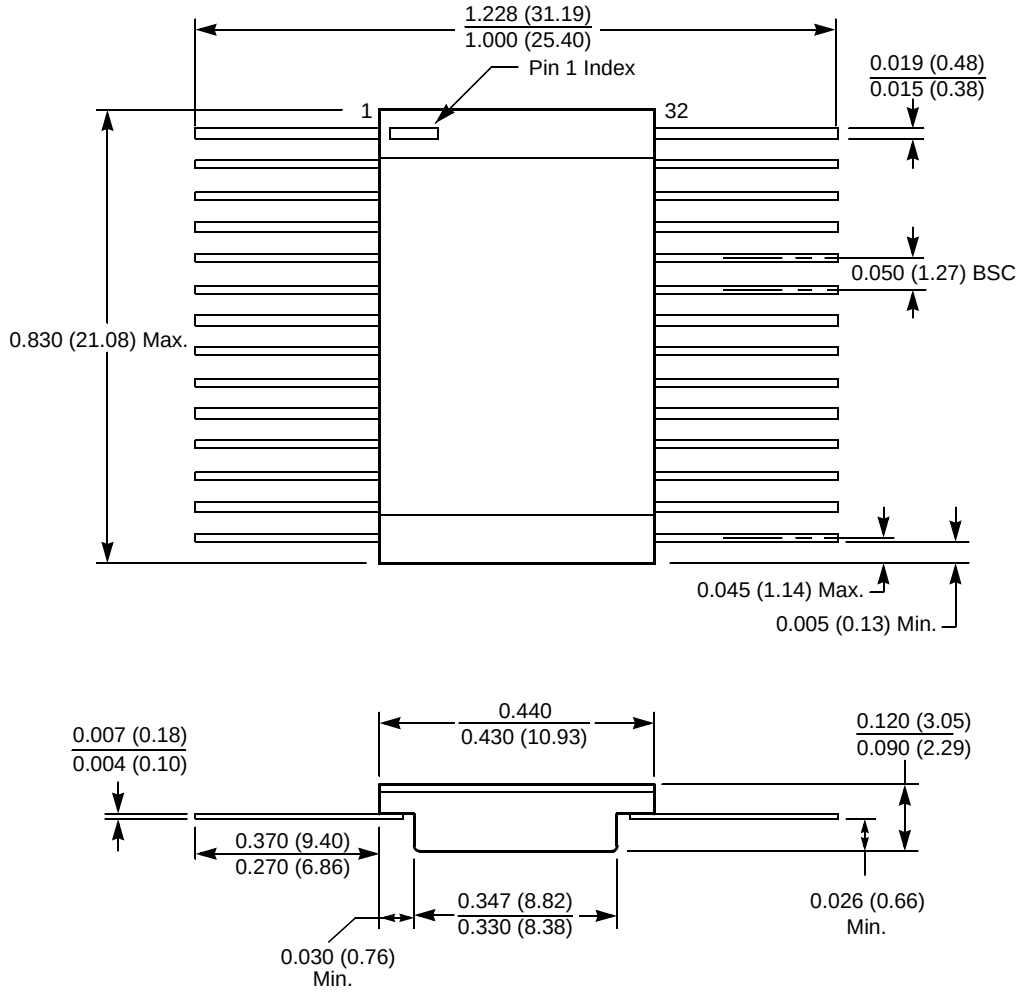




NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **TOLERANCE: ±1% NLT ±0.005 (0.127)**

Packaging Information

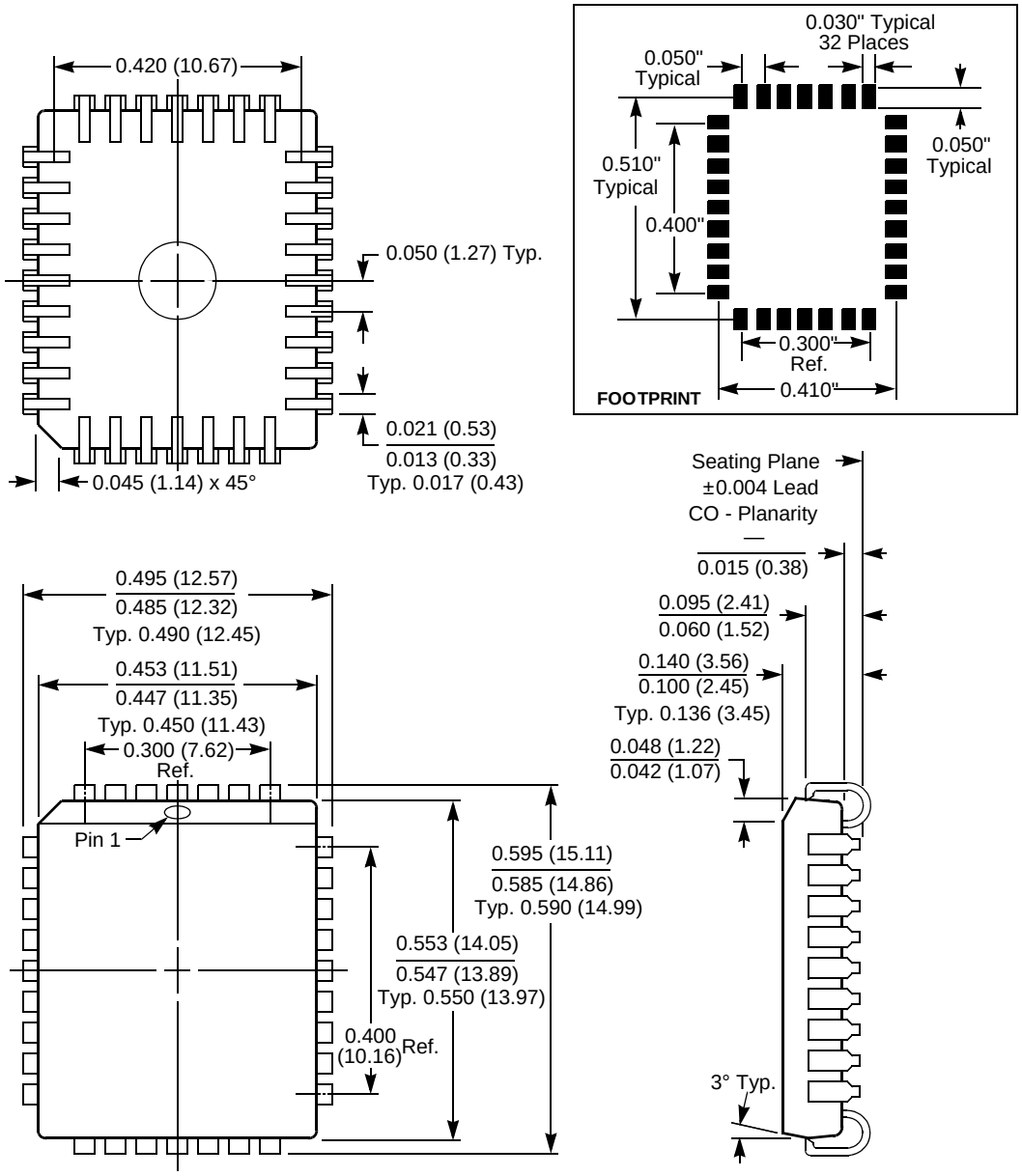
32-Lead Ceramic Flat Pack Type F



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information

32-Lead Plastic Leaded Chip Carrier Package Type J

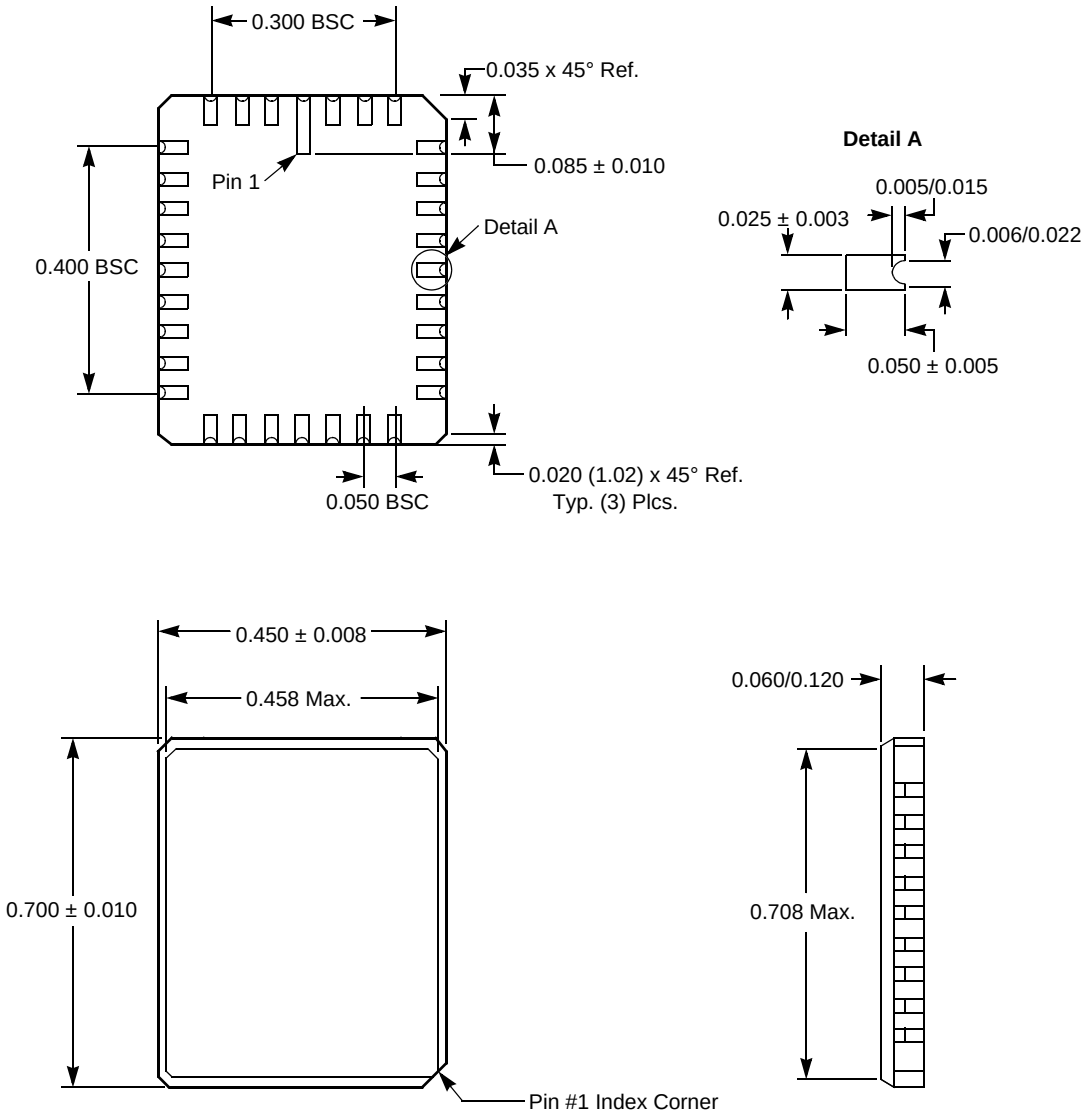


NOTES:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY**

Packaging Information

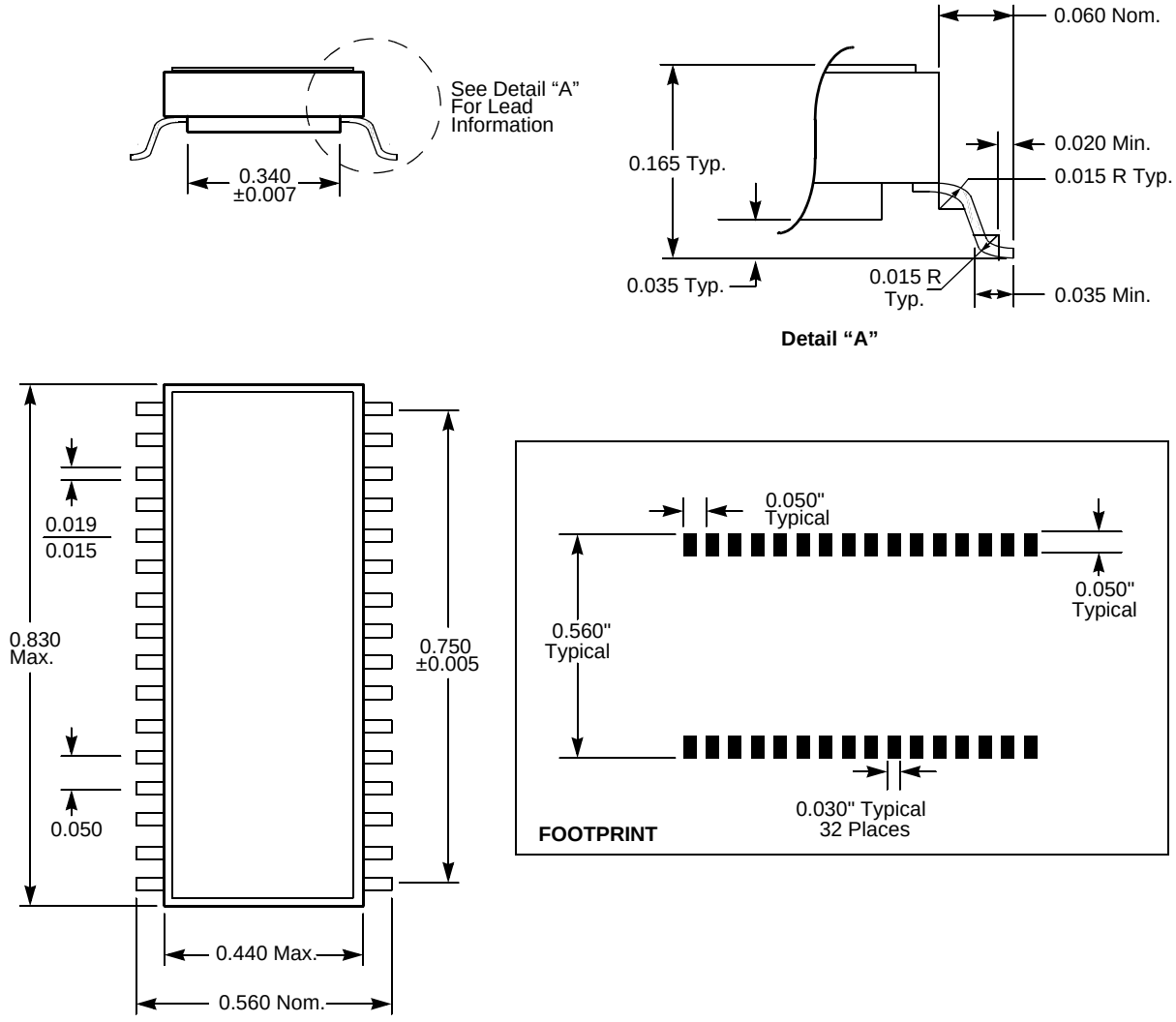
32-Pad Stretched Ceramic Leadless Chip Carrier Package Type N



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT±0.005 (0.127)

Packaging Information

32-Lead Ceramic Small Outline Gull Wing Package Type R



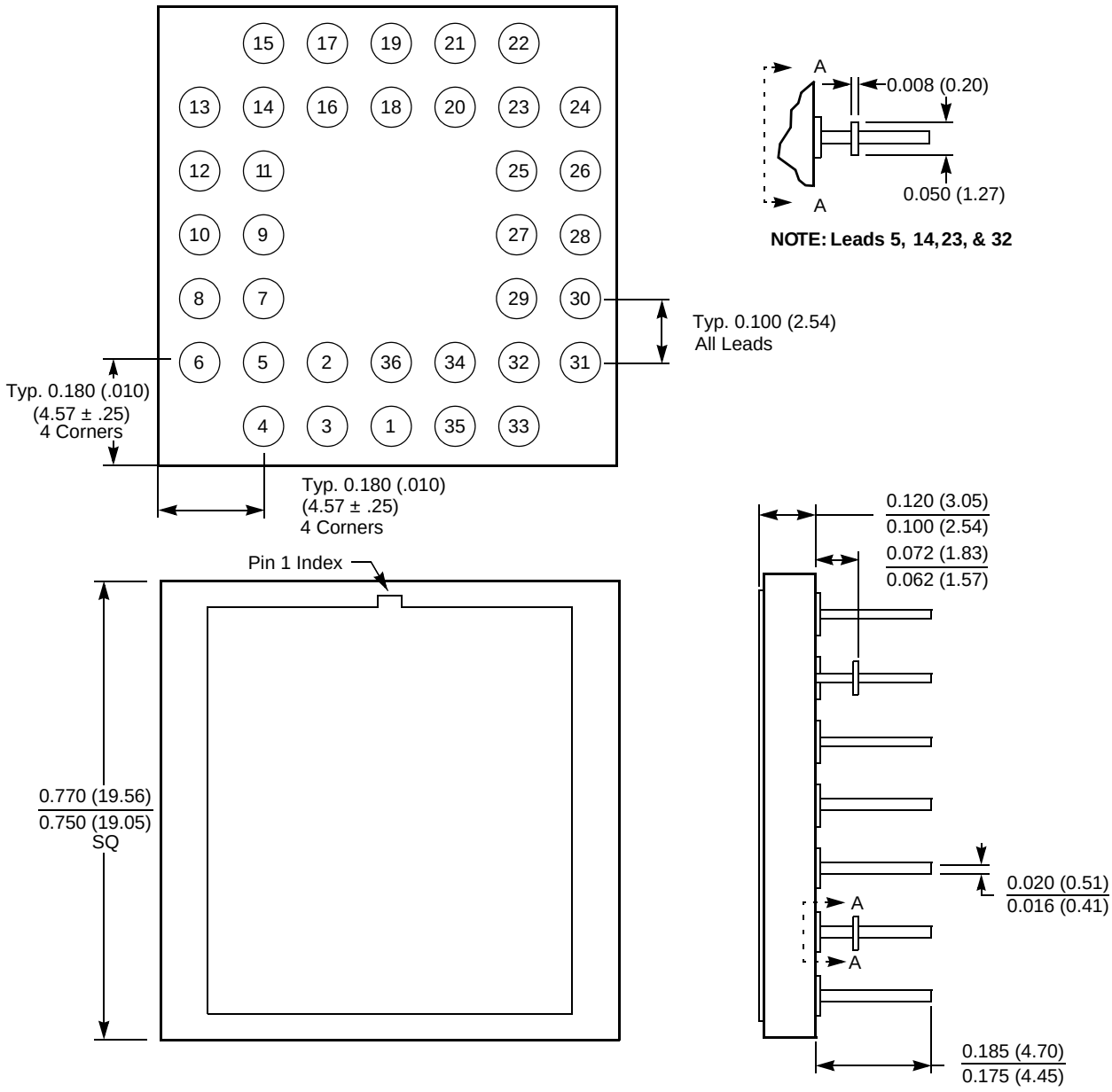
NOTES:

1. ALL DIMENSIONS IN INCHES

2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

Packaging Information

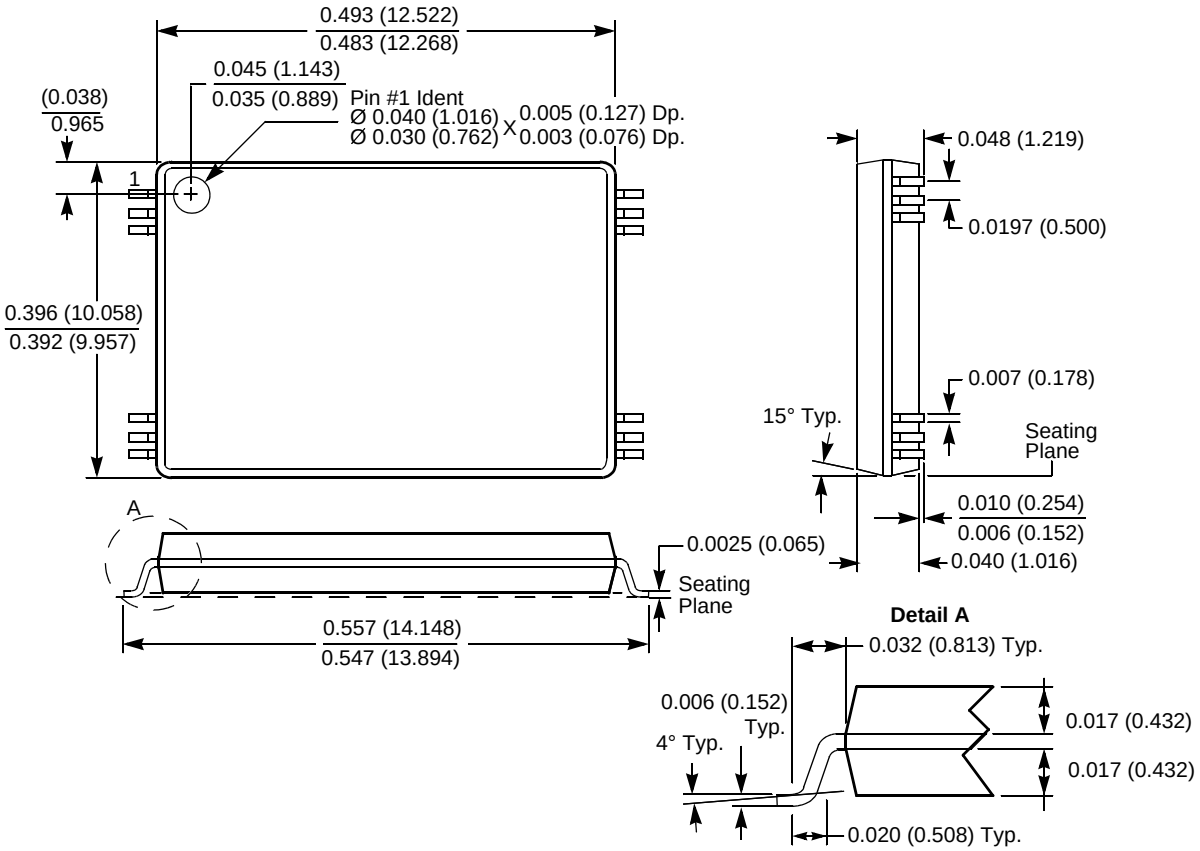
36-Lead Ceramic Pin Grid Array Package Type K

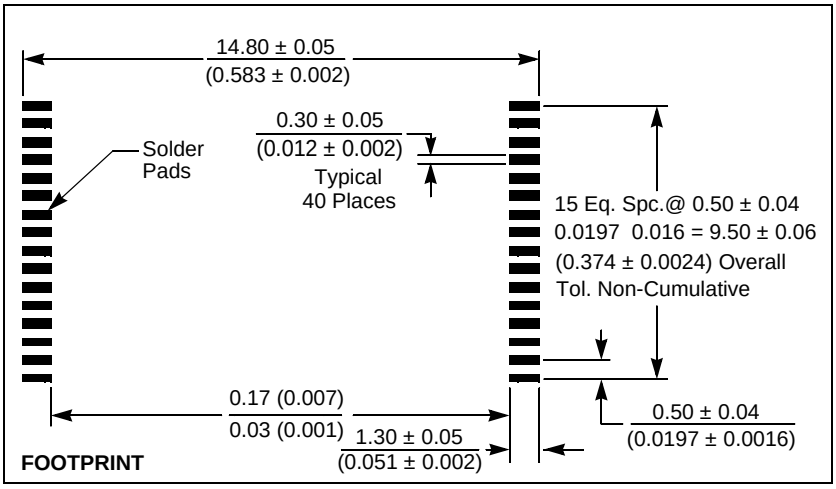


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information

40-Lead Thin Small Outline Package (TSOP) Type T





NOTE: ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES IN PARENTHESES).

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality