APPLICATION NOTE
A V A I L A B L E
AN61 • AN75 • AN77 • AN79 • AN82

X25F064/032/016/008

SerialFlash™ Memory With Block Lock™ Protection

FEATURES

- **1MHz Clock Rate**
- **SPI Serial Interface**
- **64K/32K/16K/8K Bits**
  - **—32 Byte Small Sector Program Mode**
- **Low Power CMOS**
  - **—<1μA Standby Current**
  - **—<5mA Active Current**
- **1.8V – 3.6V or 5V "Univolt" Read and Program Power Supply Versions**
- **Block Lock Protection**
  - **—Protect 1/4, 1/2, or all of E²PROM Array**
- **Built-in Inadvertent Program Protection**
  - **—Power-Up/Power-Down protection circuitry**
  - **—Program Enable Latch**
  - **—Program Protect Pin**
- **Self-Timed Program Cycle**
  - **—5ms Program Cycle Time (Typical)**
- **High Reliability**
  - **—Endurance: 100,000 cycles per byte**
  - **—Data Retention: 100 Years**
  - **—ESD protection: 2000V on all pins**
- **8-Lead PDIP Package**
- **8-Lead 150 mil SOIC Packages**
- **32K, 16K, 8K available in 14-Lead TSSOP, 64K available in 20-Lead TSSOP**

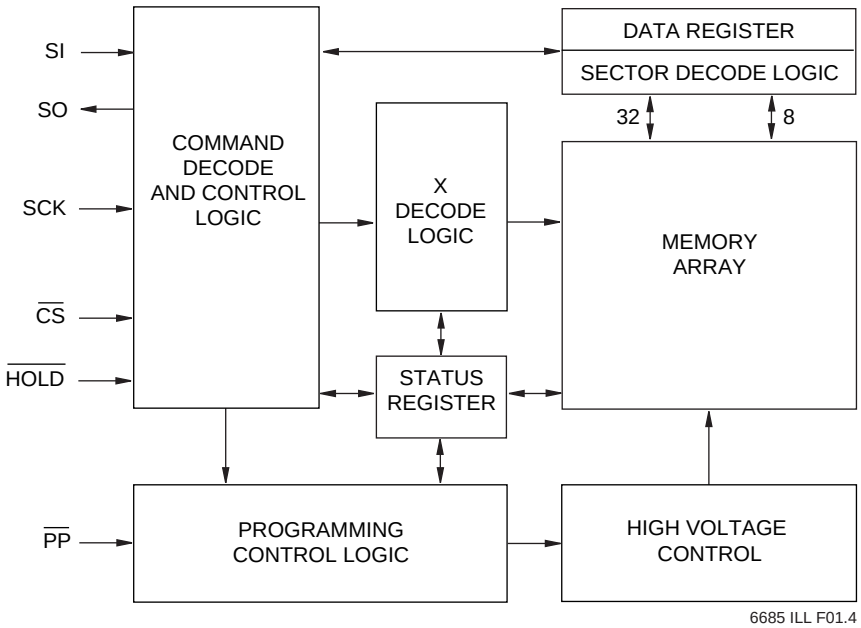
DESCRIPTION

The X25F064/032/016/008 family are 8/16/32/64K-bit CMOS SerialFlash memory, internally organized X 8. They feature a "Univolt" Program and Read voltage, Serial Peripheral Interface (SPI), and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK), plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25F064/032/016/008 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25F064/032/016/008 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{PP}$ input can be used as a hardwire input to the X25F064/032/016/008 disabling all program attempts to the status register, thus providing a mechanism for limiting end user capability of altering 0, 1/4, 1/2, or all of the memory.

The X25F064/032/016/008 utilizes Xicor's proprietary flash cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



6685 ILL F01.4

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6685-3.1 8/29/96 T3/C0/D0 SH

Characteristics subject to change without notice

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push-pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25F064/032/016/008 is deselected and the SO output pin is at high impedance and unless an internal program operation is underway the X25F064/032/016/008 will be in the standby power mode. $\overline{CS}$ LOW enables the X25F064/032/016/008, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Program Protect ($\overline{PP}$)

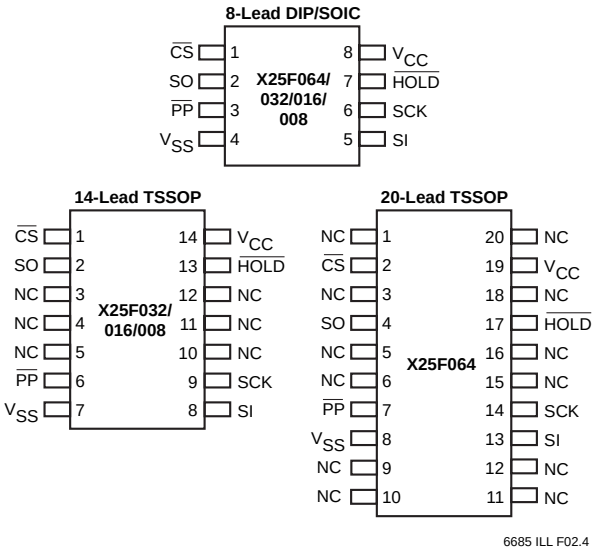
When $\overline{PP}$ is LOW and the nonvolatile bit PPEN is “1”, nonvolatile programming of the X25F064/032/016/008 status register is disabled, but the part otherwise functions normally. When $\overline{PP}$ is held HIGH, all functions, including nonvolatile programming operate normally. $\overline{PP}$ going LOW while $\overline{CS}$ is still LOW will interrupt programming of the X25F064/032/016/008 status register. If the internal program cycle has already been initiated, $\overline{PP}$ going LOW will have no effect on programming.

The $\overline{PP}$ pin function is blocked when the PPEN bit in the status register is “0”. This allows the user to install the X25F064/032/016/008 into a system with $\overline{PP}$ pin grounded and still be able to program the status register. The $\overline{PP}$ pin functions will be enabled when the PPEN bit is set “0”.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PIN CONFIGURATION



PIN NAMES

SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{PP}$	Program Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

6685 PGM T01.1

PRINCIPLES OF OPERATION

The X25F064/032/016/008 family are SerialFlash Memory designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25F064/032/016/008 family contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{PP}$ inputs must be HIGH during the entire operation. The $\overline{PP}$ input is “Don’t Care” if PPEN is set “0”.

Table 1 contains a list of the instructions and their operation codes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25F064/032/016/008 into a “PAUSE” condition. After releasing $\overline{HOLD}$, the X25F064/032/016/008 device will resume operation from the point when $\overline{HOLD}$ was first asserted.

Program Enable Latch

The X25F064/032/016/008 device contains a program enable latch. This latch must be SET before a program operation will be completed internally. The PREN instruction will set the latch and the PRDI instruction will reset the latch. This latch is automatically reset on power-up and after the completion of a sector program or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a program cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
PPEN	X	X	X	BL1	BL0	PEL	PIP

6685 PGM T02.2

PPEN, BL0, and BL1 are set by the PRSR instruction. PEL and PIP are “read-only” and automatically set by other operations.

The Programming-In-Process (PIP) bit indicates whether the X25F064/032/016/008 device is busy with a program operation. When set to a “1” programming is in progress, when set to a “0” no programming is in progress. During programming, all other bits are set to “1”.

The Program Enable Latch (PEL) bit indicates the status of the program enable latch. When set to a “1” the latch is set; when set to a “0” the latch is reset.

The Block Lock (BL0 and BL1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25F064/032/016/008 device array is divided into four equal segments. One, two, or all four of the segments may be locked. That is, the user may read the segments, but will be unable to alter (program) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Locked
BL1	BL0	
0	0	None
0	1	upper fourth
1	0	upper half
1	1	All

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Program-Protect Enable

The Program-Protect-Enable bit (PPEN) in the X25F064/032/016/008 status register acts as an enable bit for the $\overline{PP}$ pin.

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
PREN	0000 0110	Set the Program Enable Latch (Enable Program Operations)
PRDI	0000 0100	Reset the Program Enable Latch (Disable Program Operations)
RDSR	0000 0101	Read Status Register
PRSR	0000 0001	Program Status Register
READ	0000 0011	Read from Memory Array beginning at Selected Address
PROGRAM	0000 0010	Program Memory Array beginning at Selected Address (32 Bytes)

6685 PGM T04.2

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

PPEN	$\overline{PP}$	PEL	Locked Blocks	Unlocked Blocks	Status Register
0	X	0	Locked	Locked	Locked
0	X	1	Locked	Programmable	Programmable
1	LOW	0	Locked	Locked	Locked
1	LOW	1	Locked	Programmable	Locked
X	HIGH	0	Locked	Locked	Locked
X	HIGH	1	Locked	Programmable	Programmable

6685 PGM T05.2

The Program Protect ($\overline{PP}$) pin and the nonvolatile Program Protect Enable (PPEN) bit in the Status Register control the programmable hardware write protect feature. Hardware program protection is enabled when $\overline{PP}$ pin is LOW, and the PPEN bit is "1". Hardware program protection is disabled when either the $\overline{PP}$ pin is HIGH or the PPEN bit is "0". When the chip is hardware program protected, nonvolatile programming of the Status Register in disabled, including the Block Lock bits and the PPEN bit itself, as well as the Block Lock sections in the memory array. Only the sections of the memory array that are not Block Locked can be programmed.

Note: Since the PPEN bit is program protected, it cannot be changed back to a "0", as long as the $\overline{PP}$ pin is held LOW.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the SerialFlash memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25F064/032/016/008 device, followed by the 16-bit address. After the read opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached the address counter rolls over to address $0000, allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the Read SerialFlash Memory Array Operation Sequence illustrated in Figure 1.

To read the status register, the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit instruction. After the read status register opcode is sent, the contents of the status register are shifted out on the SO line. The Read Status Register Sequence is illustrated in Figure 2.

Programming Sequence

Prior to any attempt to program the X25F064/032/016/008 device, the program enable latch must first be set by issuing the PREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the PREN instruction is clocked into the X25F064/032/016/008 device. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the programming operation without taking $\overline{CS}$ HIGH after issuing the PREN instruction, the programming operation will be ignored.

To program the SerialFlash memory array, the user issues the PROGRAM instruction, followed by the address of the first location in the sector and then the data to be programmed. The data is programmed in a 256-clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The 32 bytes must reside in the same sector and cannot cross sector boundaries. If the address counter reaches the end of the sector and the clock continues, or if fewer than 32 bytes are clocked in, the contents of the sector cannot be guaranteed.

For the program operation to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte 32 is clocked in. If it is brought HIGH at any other time the program operation will not be completed. Refer to Figure 4 below for a detailed illustration of the programming sequence and time frames in which $\overline{CS}$ going HIGH is valid.

To program the status register, the PRSR instruction is followed by the data to be programmed. Data bits 0, 1, 4, 5 and 6 must be "0". This sequence is shown in Figure 5.

While the program cycle is in progress, following a status register or memory write sequence, the status register may be read to check the PIP bit. During this time the PIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is that the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The device powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The program enable latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent programming:

- The program enable latch is reset upon power-up.
- A program enable instruction must be issued to set the program enable latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a program cycle.

Figure 1. Read SerialFlash Memory Array Operation Sequence

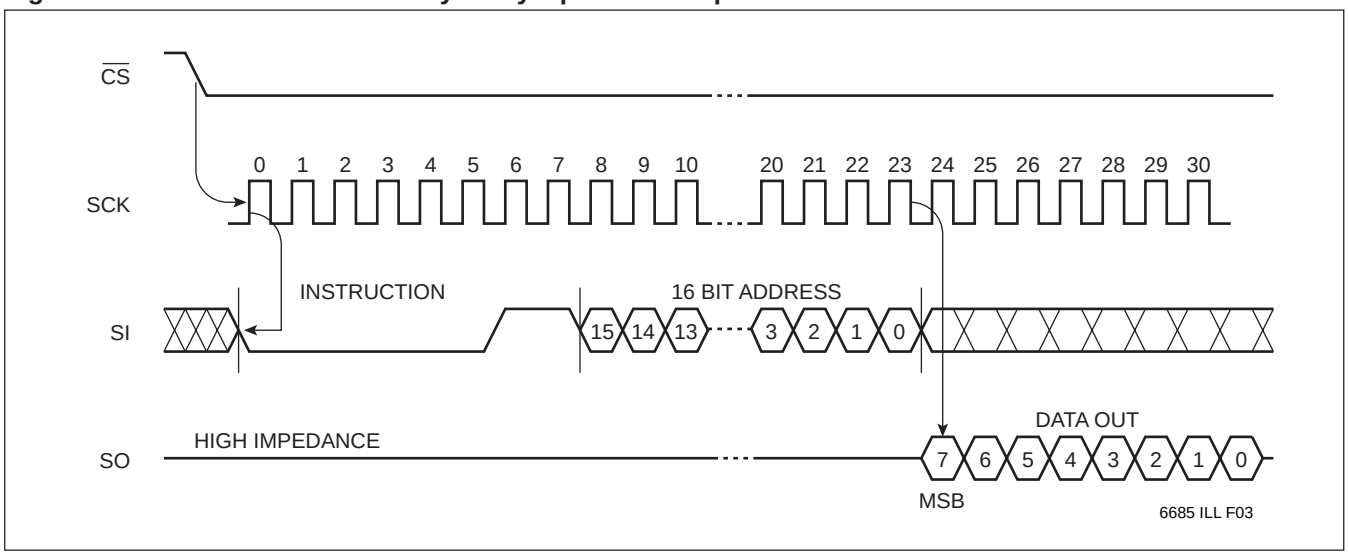


Figure 2. Read Status Register Operation Sequence

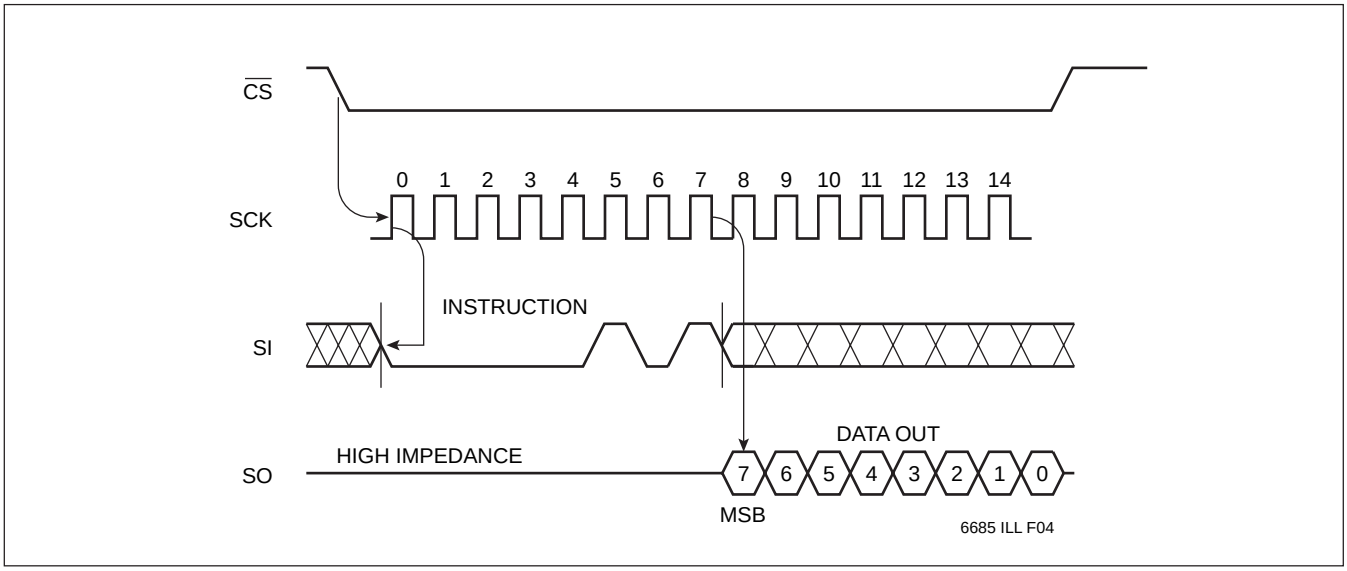


Figure 3. Program Enable Latch Sequence

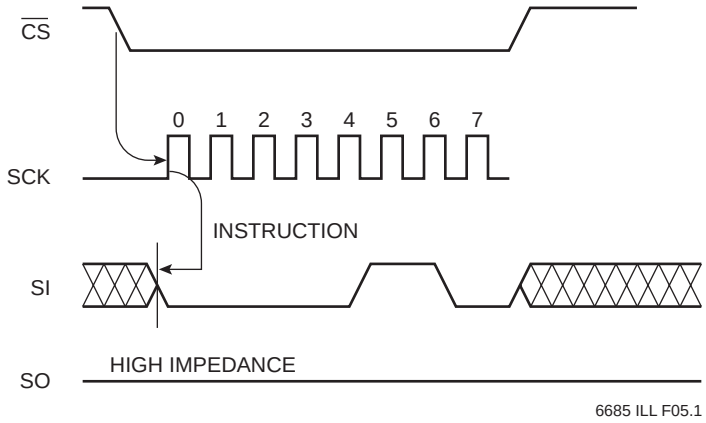


Figure 4. Programming Sequence

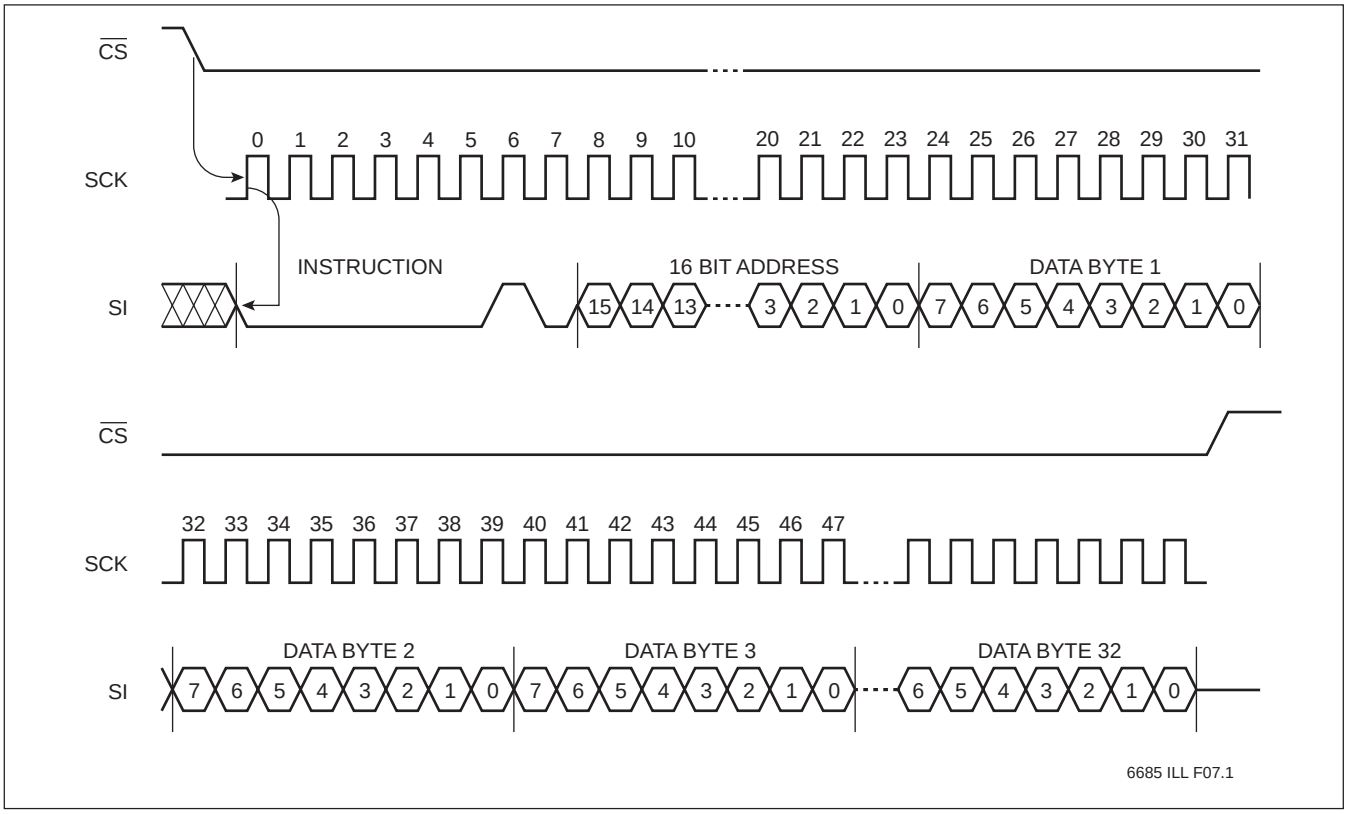
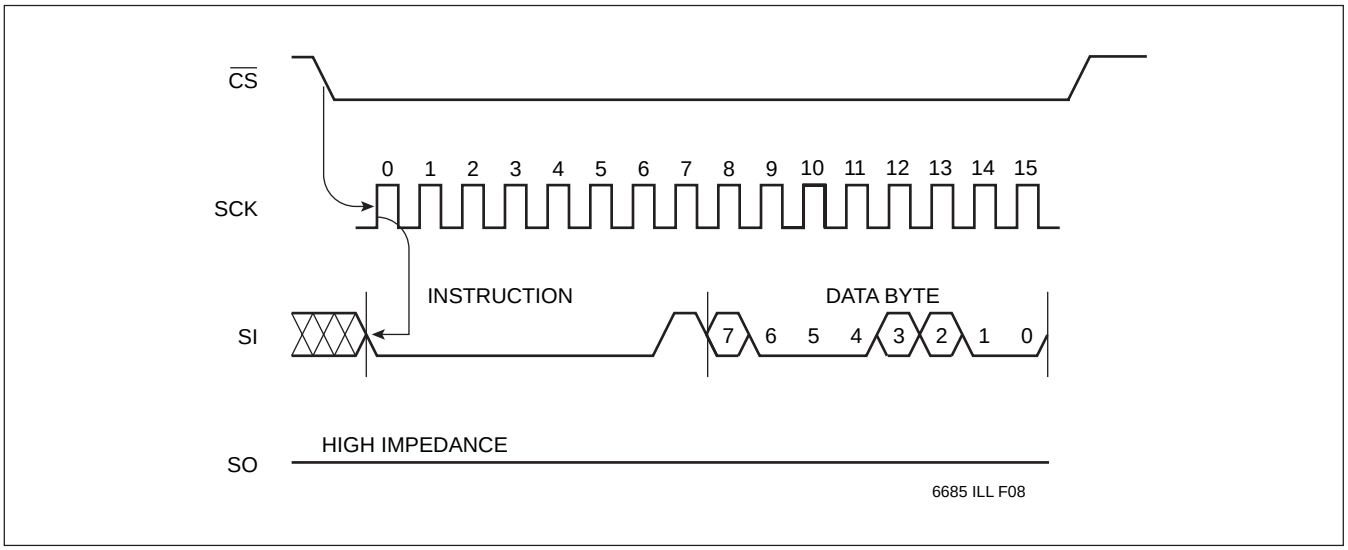


Figure 5. Program Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Extended	–20°C	+85°C
Industrial	–40°C	+85°C

6685 PGM T06.2

Supply Voltage	Limits
X25F064/032/016/008	1.8V to 3.6V
X25F064/032/016/008–5	4.5V to 5.5V

6685 PGM T07.3

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{SB1}(2)	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3.6V
I_{SB2}	V_{CC} Supply Current (Standby)		10	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current	–1	10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	V_{CC} x 0.7	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage		V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	I_{OL} = 1.5mA, V_{CC} = 2.7V
V_{OH1}	Output HIGH Voltage	V_{CC} – 0.3		V	I_{OH} = –0.4mA, V_{CC} = 2.7V
V_{OL2}	Output LOW Voltage		0.4	V	I_{OL} = 3mA, V_{CC} = 5V
V_{OH2}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = –1.6mA, V_{CC} = 5V

6685 PGM T08.4

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(3)	Power-up to Read Operation		1	ms
t_{PUW}(3)	Power-up to Write Operation		5	ms

6685 PGM T09

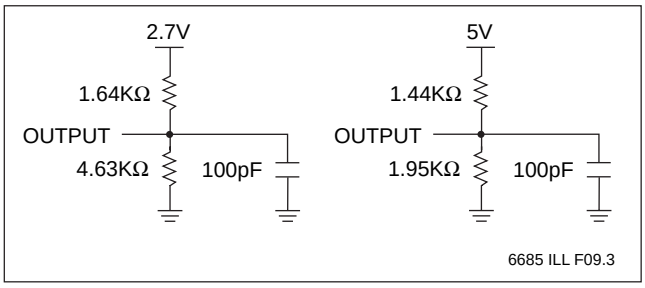
CAPACITANCE T_A = 25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

6685 PGM T10.1

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

6685 PGM T11

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock HIGH Time	400		ns
t_{WL}	Clock LOW Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}(4)	Data In Rise Time		2	µs
t_{FI}(4)	Data In Fall Time		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	200		ns
t_{CD}	$\overline{HOLD}$ Hold Time	200		ns
t_{CS}	$\overline{CS}$ Deselect Time	2		µs
t_{PC}(5)	Program Cycle Time		10	ms

6685 PGM T12.3

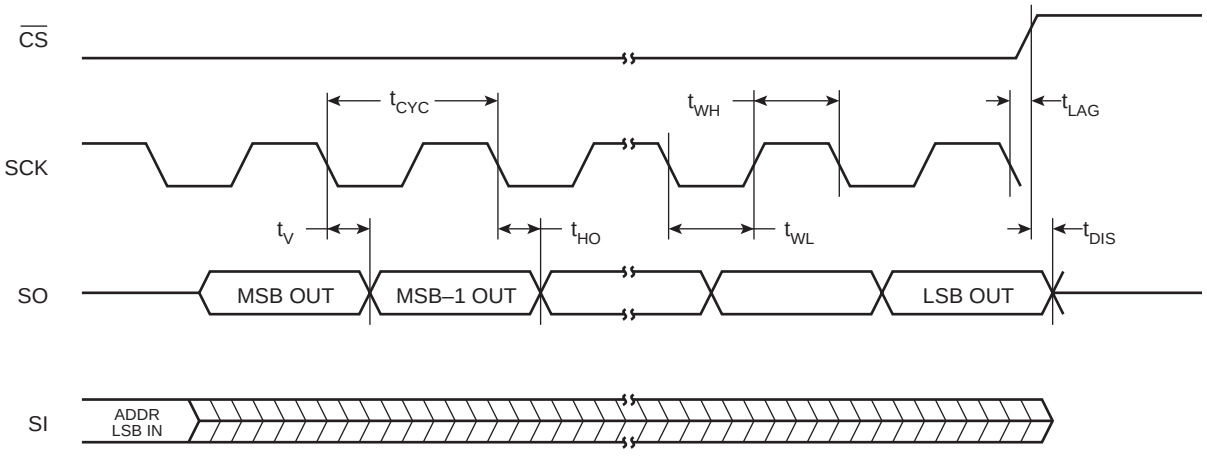
Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from Clock LOW		400	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(4)	Output Rise Time		300	ns
t_{FO}(4)	Output Fall Time		300	ns
t_{LZ}(4)	$\overline{HOLD}$ HIGH to Output in Low Z	100		ns
t_{HZ}(4)	$\overline{HOLD}$ LOW to Output in High Z	100		ns

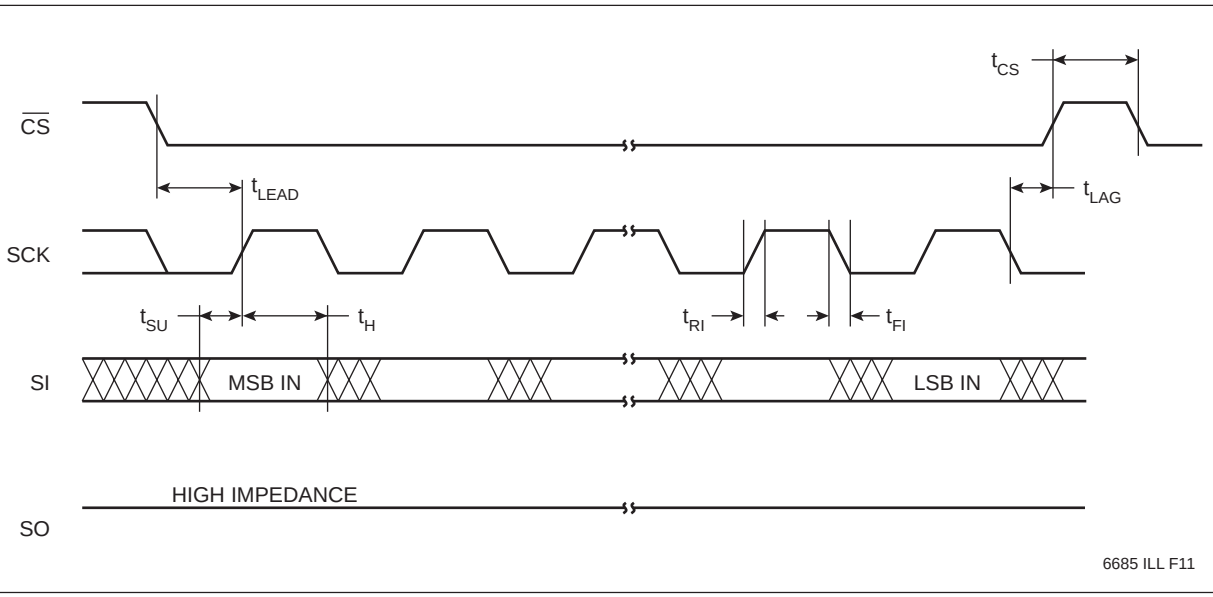
6685 PGM T13.2

Notes: (4) This parameter is periodically sampled and not 100% tested.
(5) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile program cycle.

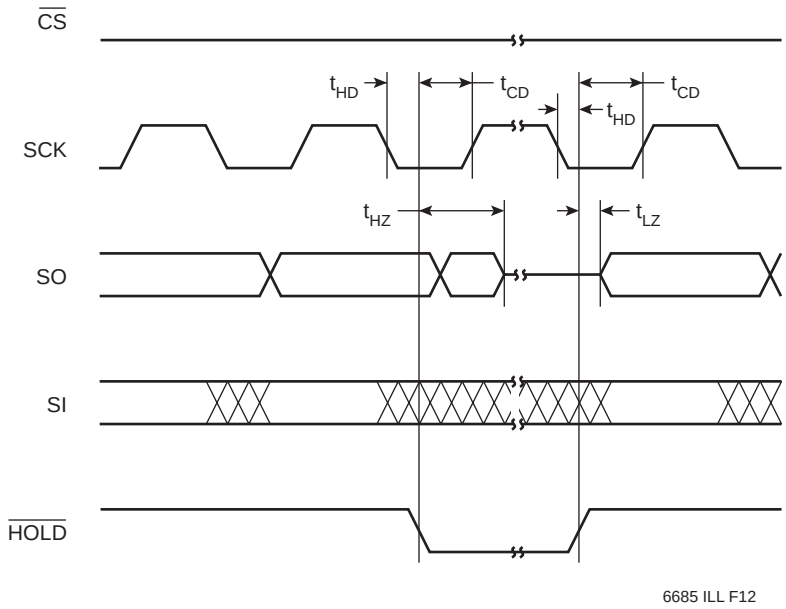
Serial Output Timing



Serial Input Timing

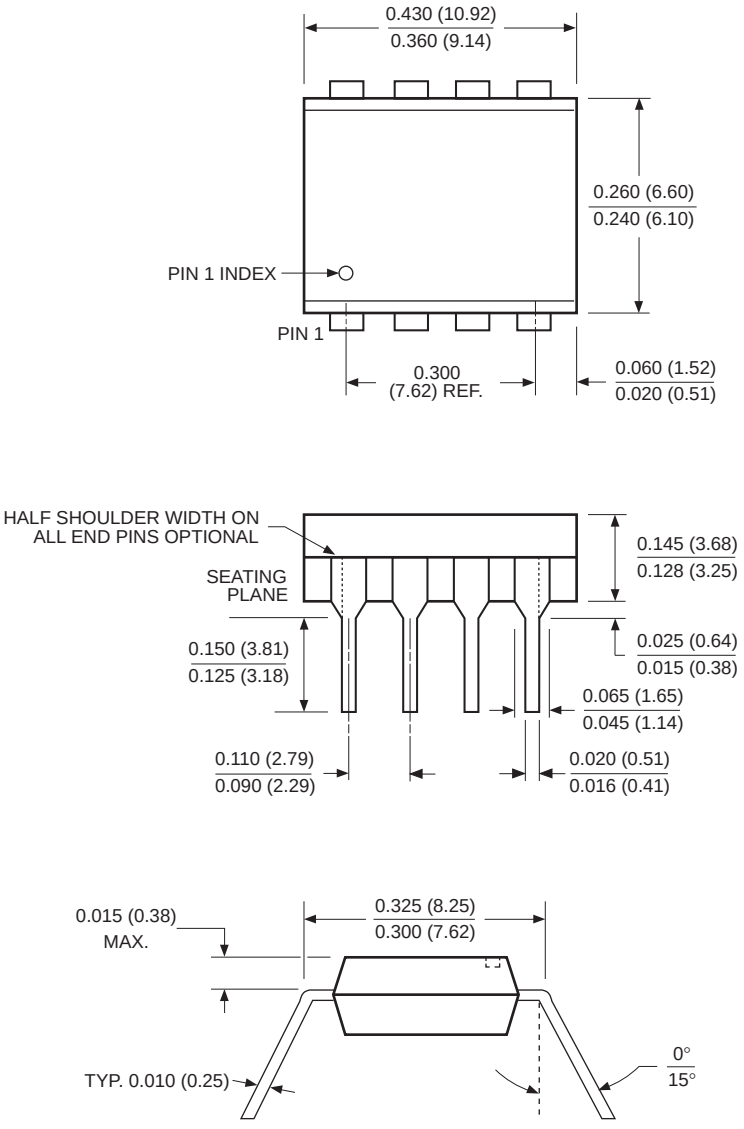


Hold Timing



PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



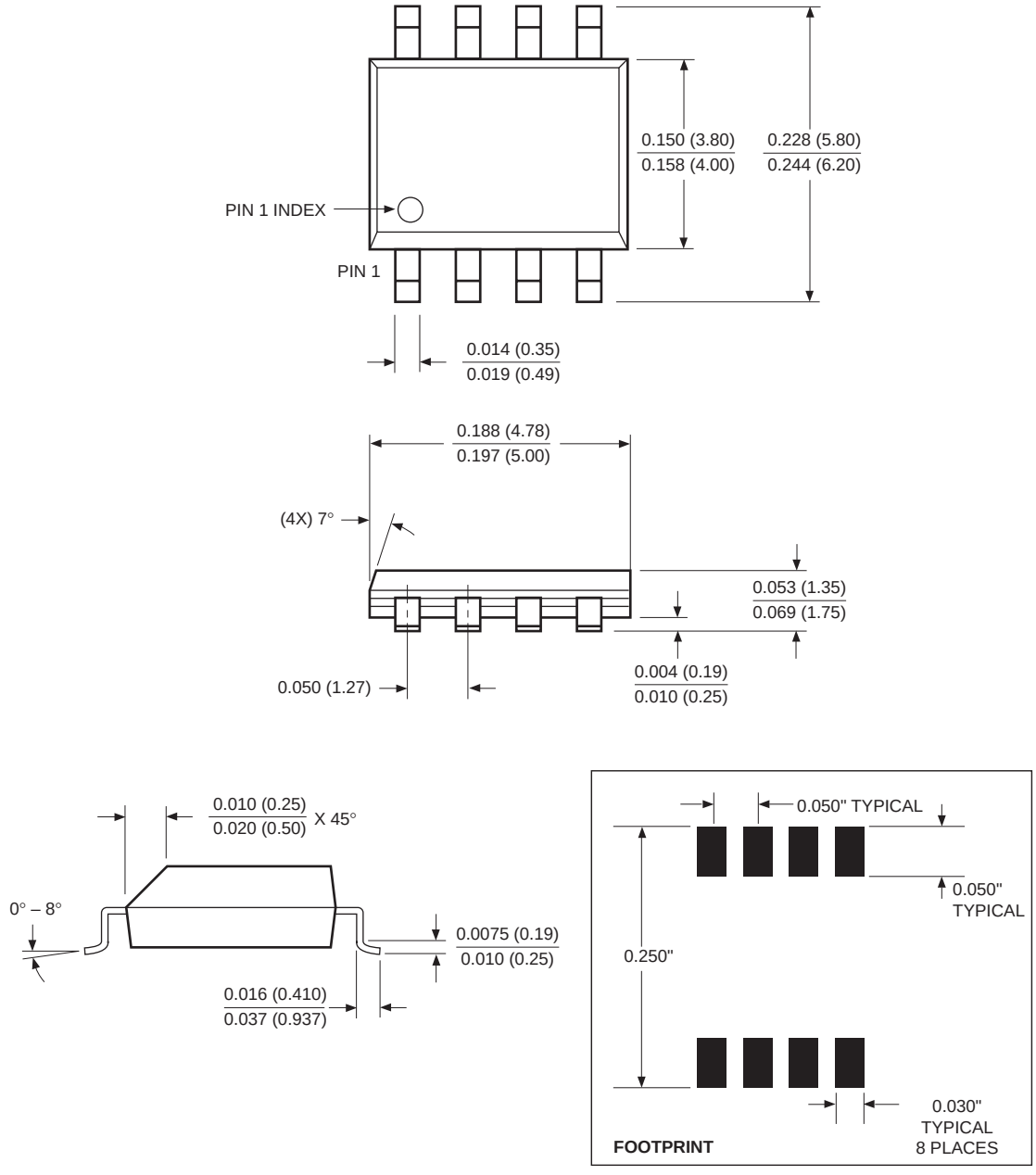
NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F01

PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

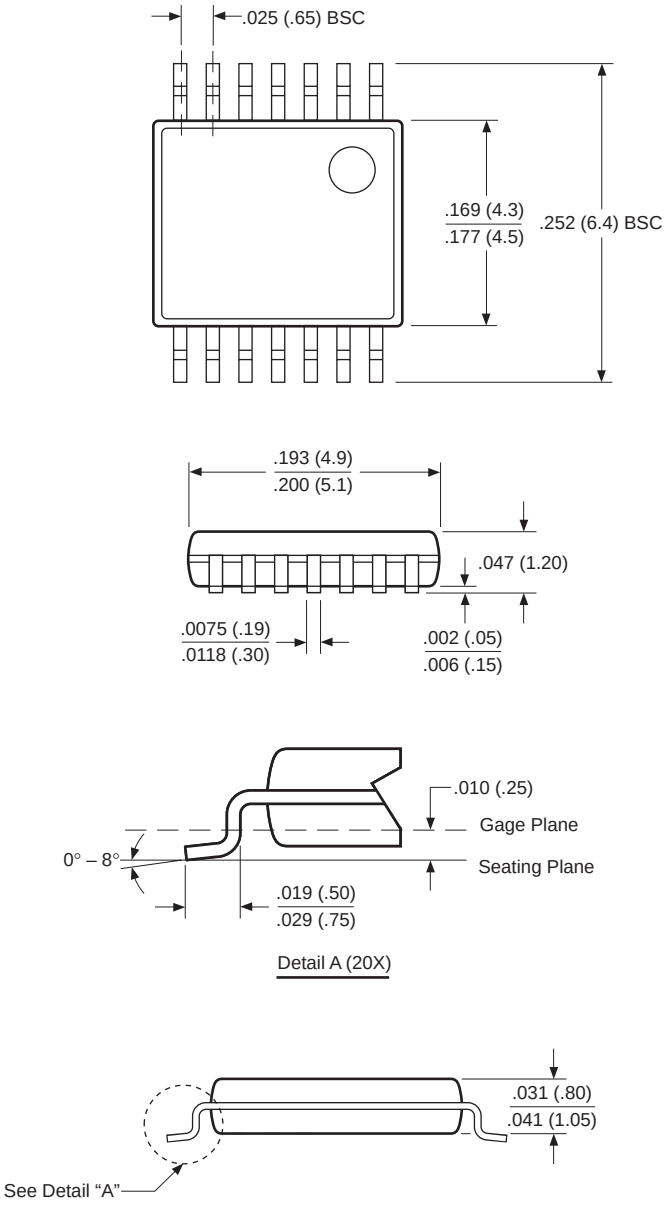


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F22.1

PACKAGING INFORMATION

14-LEAD PLASTIC, TSSOP PACKAGE TYPE V

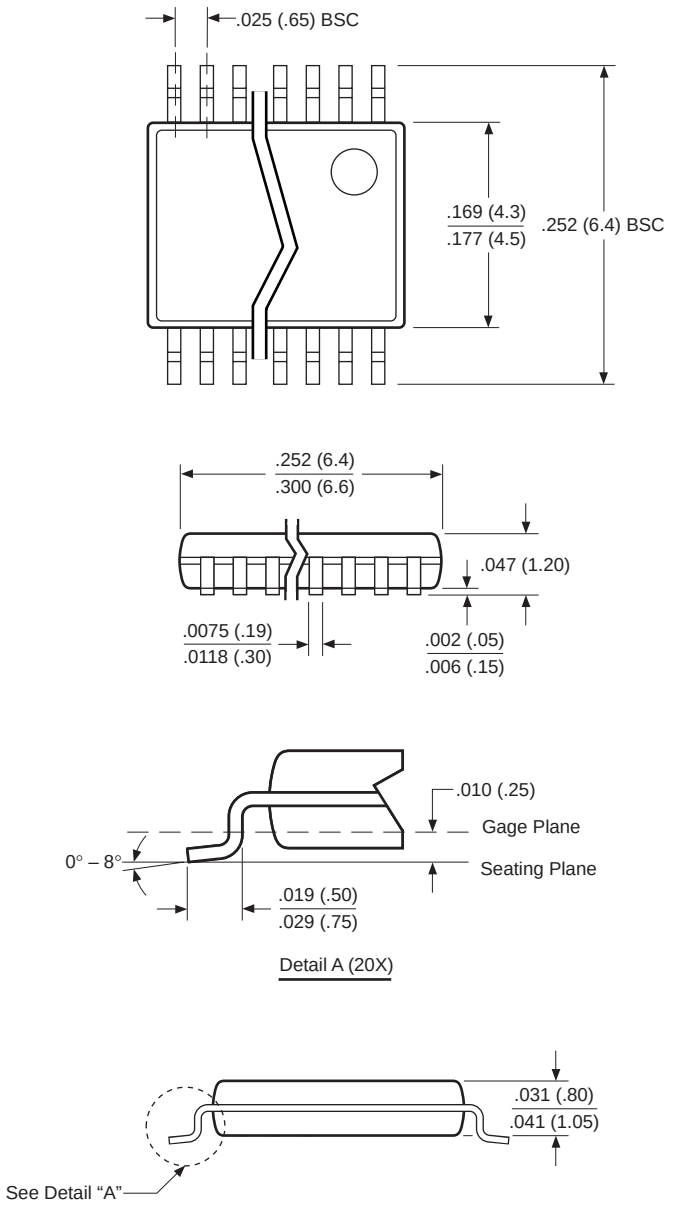


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F32

PACKAGING INFORMATION

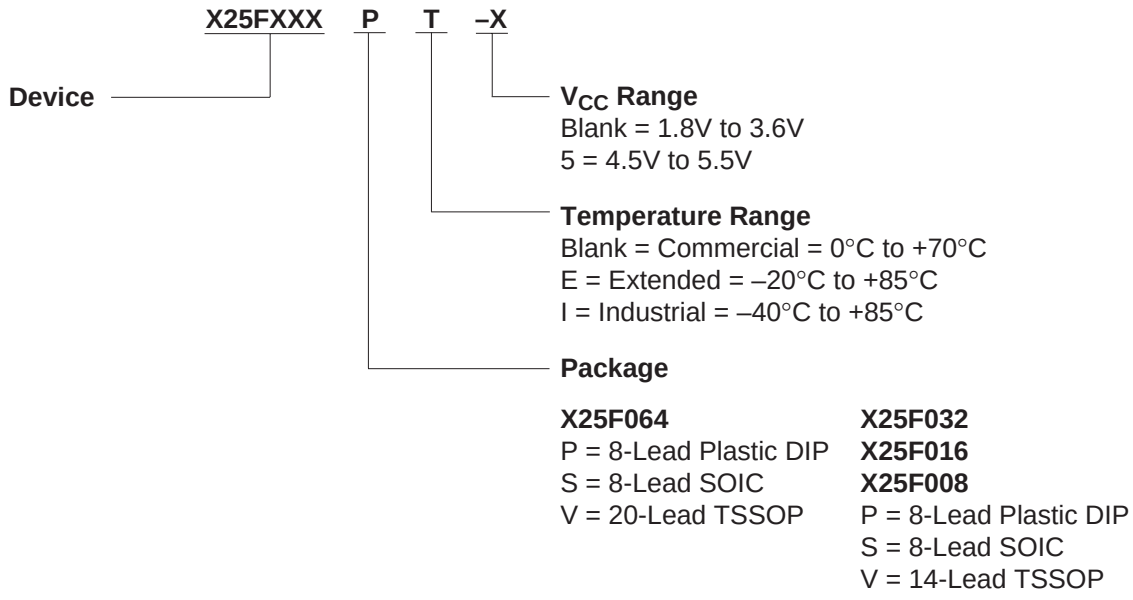
20-LEAD PLASTIC, TSSOP PACKAGE TYPE V



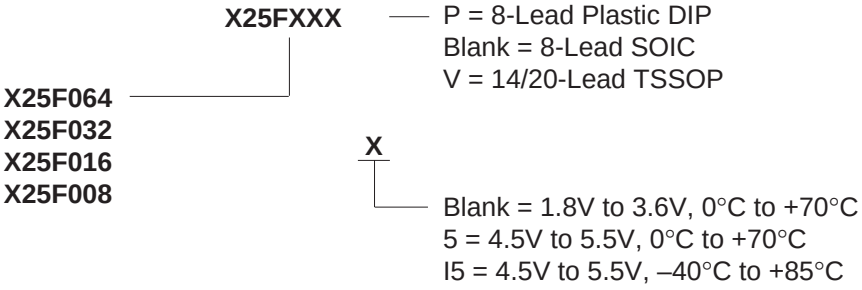
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F45

ORDERING INFORMATION



Part Mark Convention



LIMITED WARRANTY

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U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829, 482; 4,874, 967; 4,883, 976. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and backup features to prevent such an occurrence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.