ISO 7816 Compatible

2K X24026 256 x 8 Bit

Serial E2PROM

FEATURES

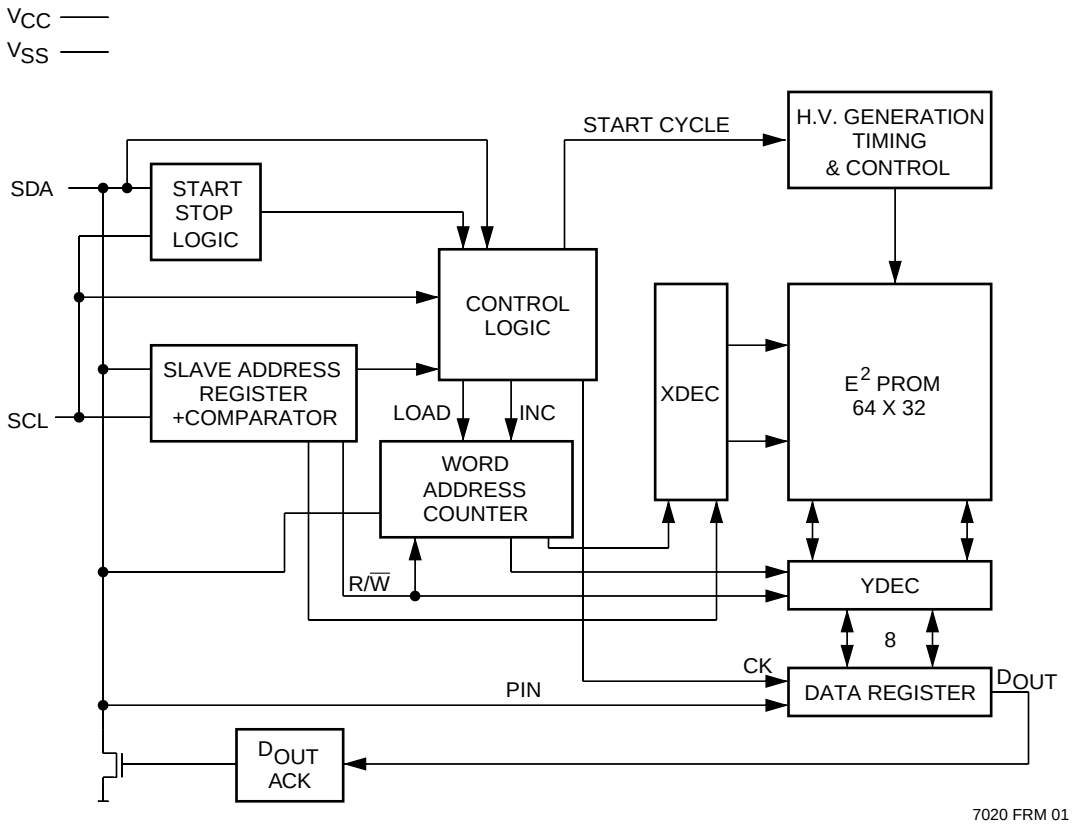
- **2.7V to 5.5V Power Supply**
- **Low Power CMOS**
  - **—Active Current Less Than 1mA**
  - **—Standby Current Less Than 50μA**
- **Internally Organized 256 x 8**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **2 Wire Serial Interface**
  - **—Bidirectional Data Transfer Protocol**
- **Four Byte Page Write Operation**
  - **—Minimizes Total Write Time Per Byte**
- **High Reliability**
  - **—Endurance: 100,000 Cycles**
  - **—Data Retention: 100 Years**
  - **—ESD Protection > 2KV**

DESCRIPTION

The X24026 is a CMOS 2048 bit serial E²PROM, internally organized 256 x 8. The X24026 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Available in DICE form with ISO 7816 compatible pinout.

FUNCTIONAL DIAGRAM



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PIN DESCRIPTIONS

Serial Clock (SCL)

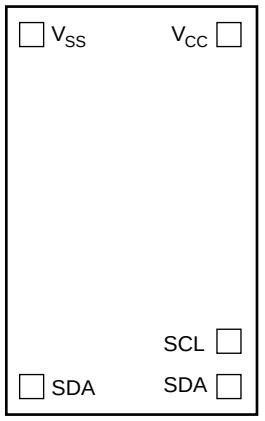
The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

DIE CONFIGURATION



X24026 Die Revision A
.055 x .079

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PIN DESCRIPTIONS

Symbol	Description
SDA	Serial Data
SCL	Serial Clock
V_{SS}	Ground
V_{CC}	+5V

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DEVICE OPERATION

The X24026 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24026 will be considered a slave in all applications.

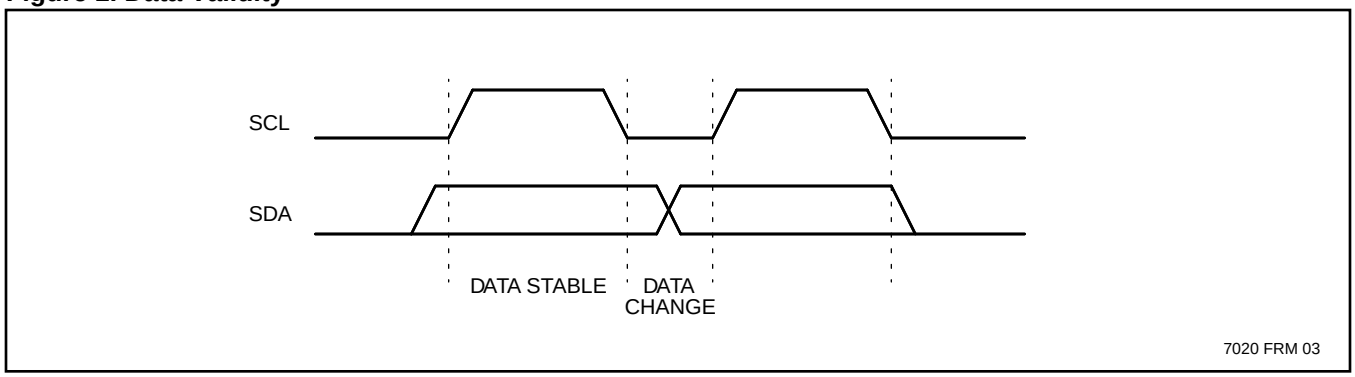
Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24026 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 1. Data Validity



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24026 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24026 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24026 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24026 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24026 will continue to transmit data. If an acknowledge is not detected, the X24026 will terminate further data transmissions. The master must then issue a stop condition to return the X24026 to the standby power mode and place the device into a known state.

Figure 2. Definition of Start and Stop

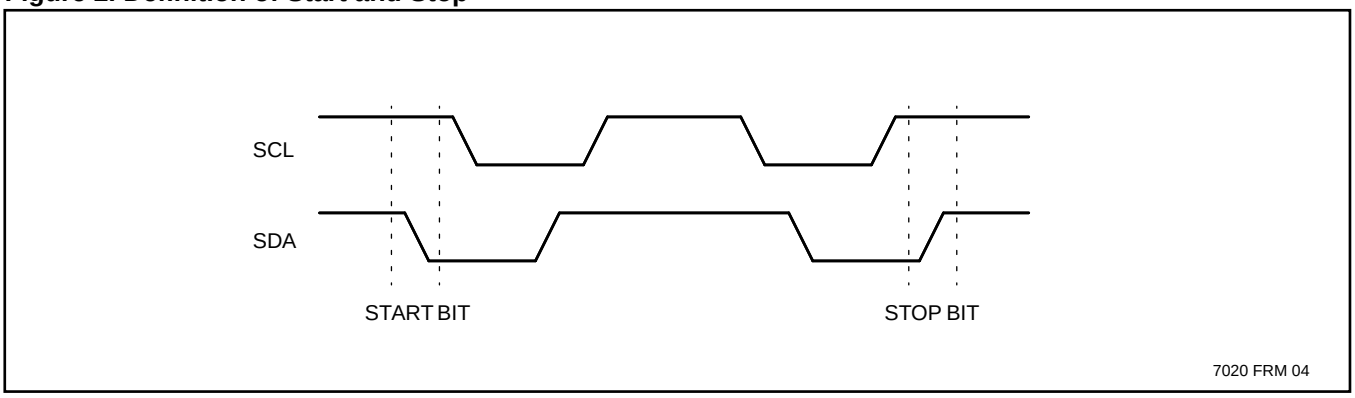
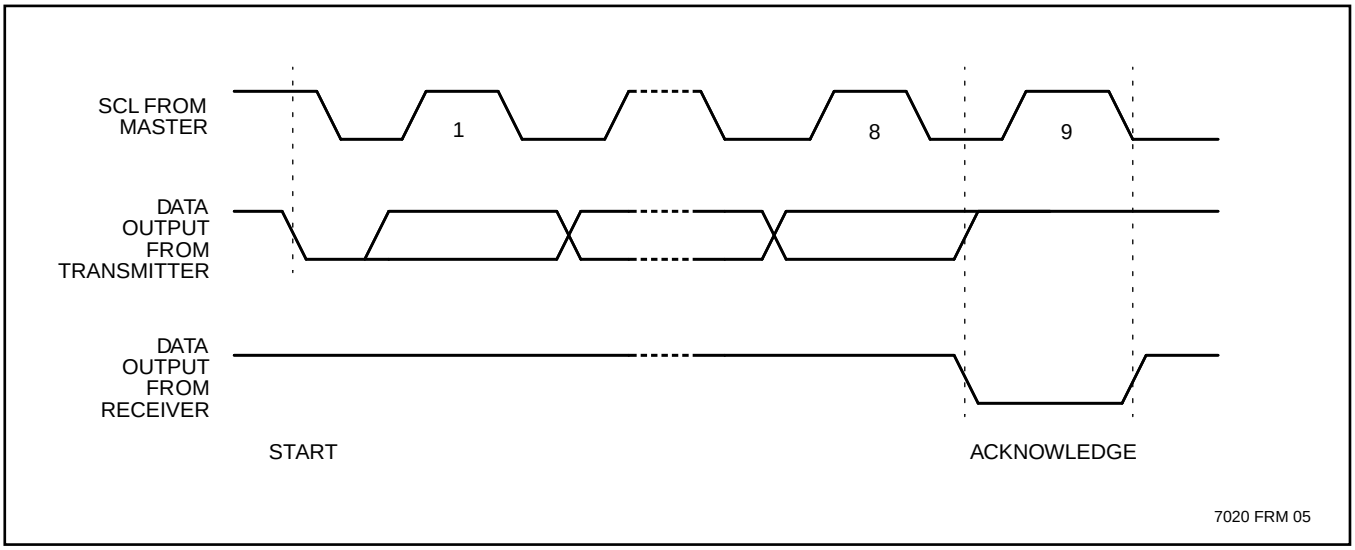


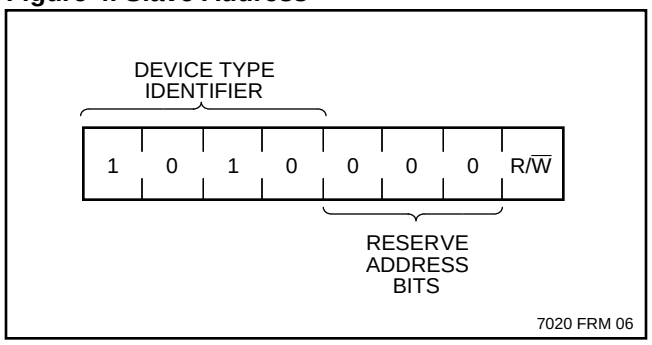
Figure 3. Acknowledge Response from Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave are the device type identifier (see Figure 4). For the X24026 this is fixed as 1010[B].

Figure 4. Slave Address



The next three significant bits are reserved address bits.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operations is selected.

Following the start condition, the X24026 monitors the SDA bus comparing the slave address being transmitted with its slave address. Upon a correct compare the X24026 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24026 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24026 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X24026 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24026 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24026 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write

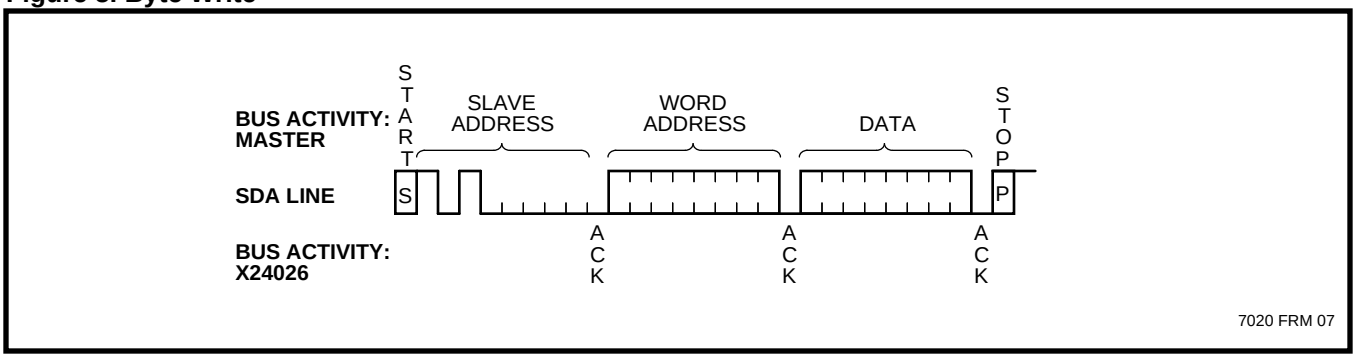
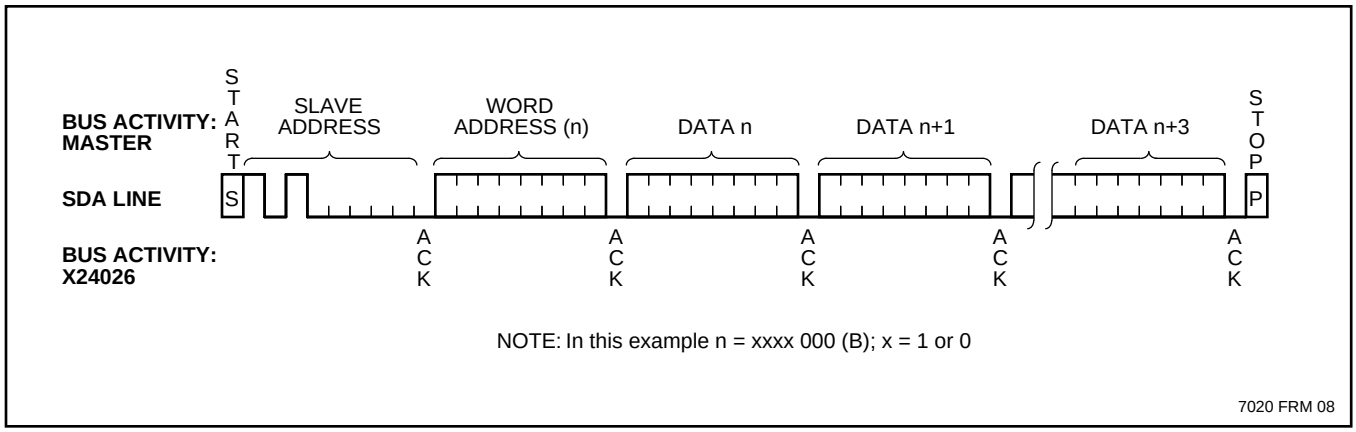


Figure 6. Page Write



Page Write

The X24026 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to three more words. After the receipt of each word, the X24026 will respond with an acknowledge.

After the receipt of each word, the two low order address bits are internally incremented by one. The high order six bits of the address remain constant. If the master should transmit more than four words prior to generating the stop condition, the address counter will “roll over” and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

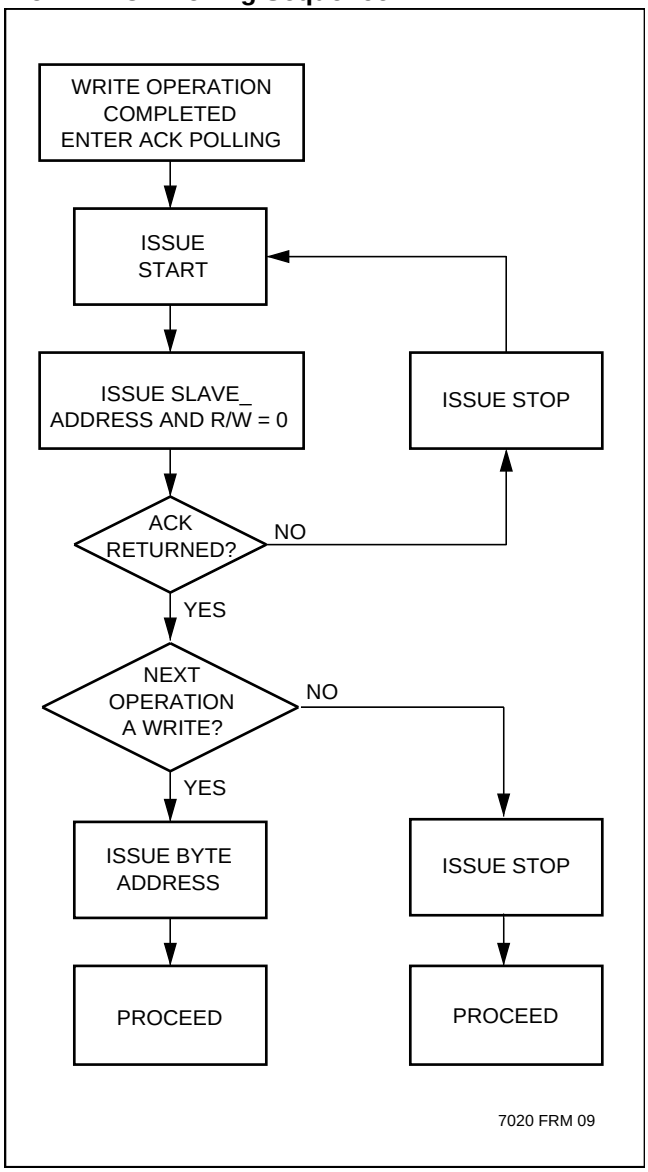
The disabling of the inputs, during the internal write operation, can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host’s write operation the X24026 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24026 is still busy with the write operation no ACK will be returned. If the X24026 has completed the write operation an ACK will be returned and the master can then proceed with the next read or write operation.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Flow 1. ACK Polling Sequence



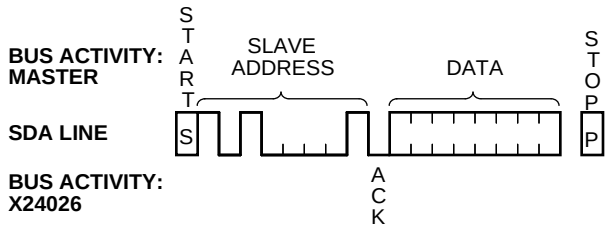
Current Address Read

Internally the X24026 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the X24026 issues an acknowledge and transmits the eight bit word during the next eight clock cycles. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

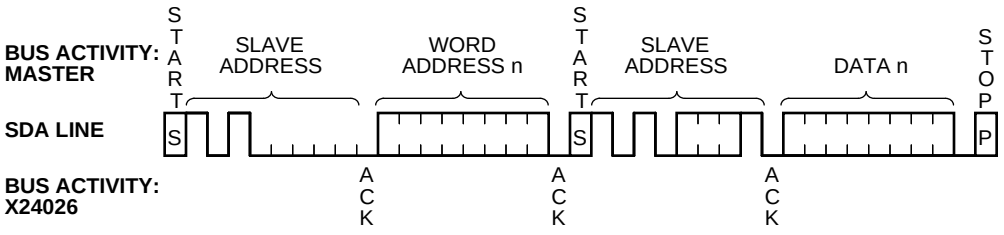
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X24026 and then by the eight bit word. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7. Current Address Read



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Figure 8. Random Read



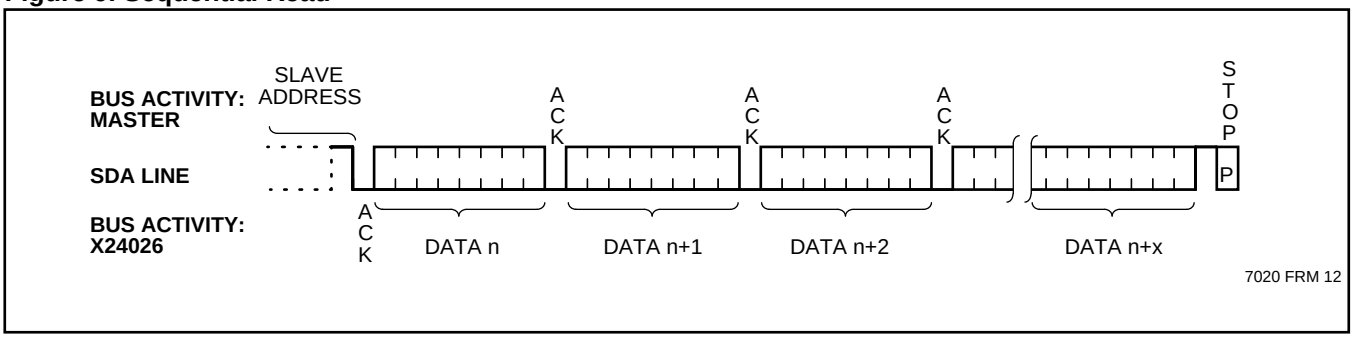
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Sequential Read

Sequential Read can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24026 continues to output data for each acknowledge received. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter “rolls over” to address 0 and the X24026 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias.....–65°C to +135°C
Storage Temperature.....–65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} .....–1.0V to +7.0V
D.C. Output Current.....5 mA
Lead Temperature (Soldering, 10 Seconds).....300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C

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Supply Voltage	Limits
X24026	4.5V to 5.5V
X24026-2.7	2.7V to 5.5V

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D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified).

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	Power Supply Current (read)		1	mA	SCL = V_{CC} x 0.1/V_{CC} x 0.9 Levels @ 100 KHz, SDA = Open
I_{CC2}	Power Supply Current (write)		2		
I_{SB}(1)	Standby Current		50	µA	SCL = SDA = V_{CC} – 0.3V, V_{CC} = 5V ±10%
I_{SB}(2)	Standby Current		30	µA	SCL = SDA = V_{CC} – 0.3V, V_{CC} = 3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	–1.0	V_{CC} x 0.3	V	
V_{IH}(2)	Input High Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 3 mA

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CAPACITANCE T_A = 25°C, f = 1 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

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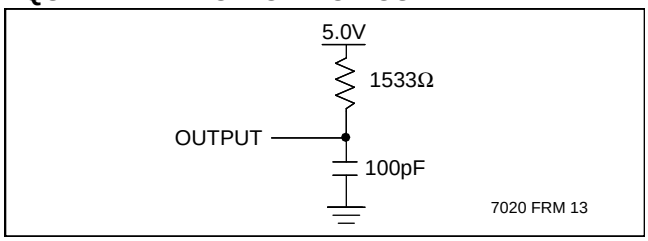
Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} x 0.5

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EQUIVALENT A.C. LOAD CIRCUIT



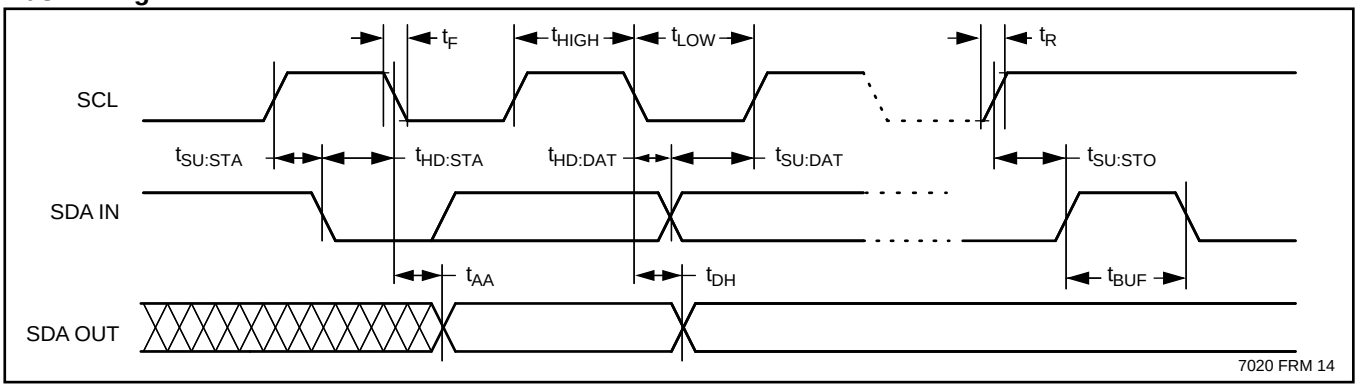
A.C. CHARACTERISTICS (Over recommended operating conditions)

DATA INPUT TIMING

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

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Bus Timing



POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-up to Read Operation	1	ms
t_{PUW}(4)	Power-up to Write Operation	5	ms

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Notes: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

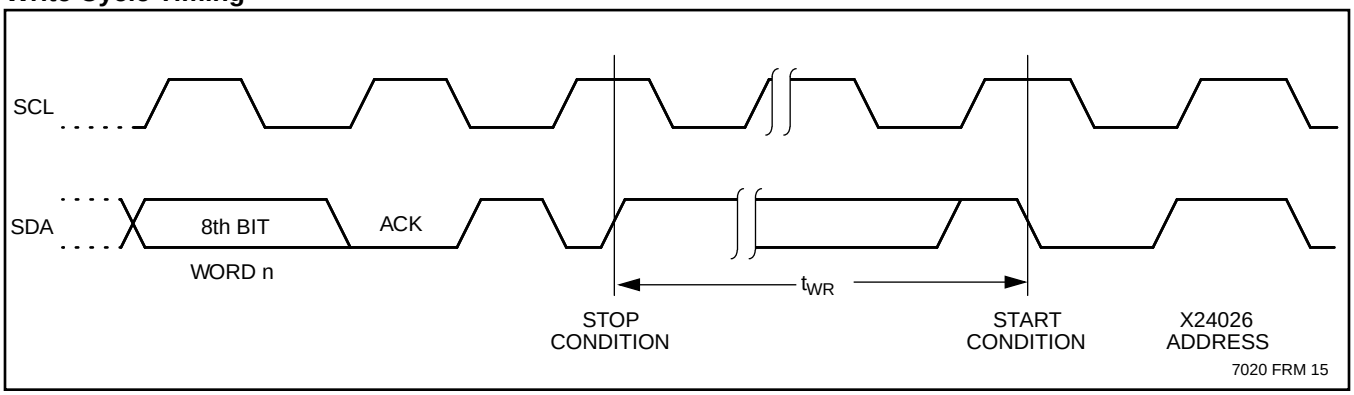
WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}(6)	Write Cycle Time		5	10	ms

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The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24026 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

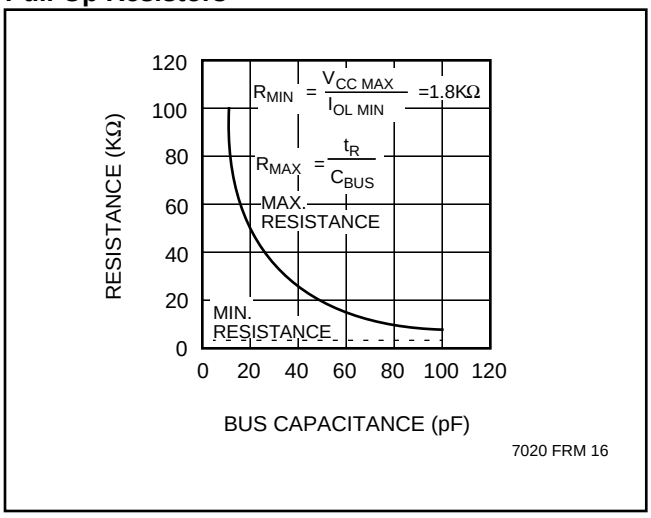
Write Cycle Timing



Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V)

(6) t_{WR} is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

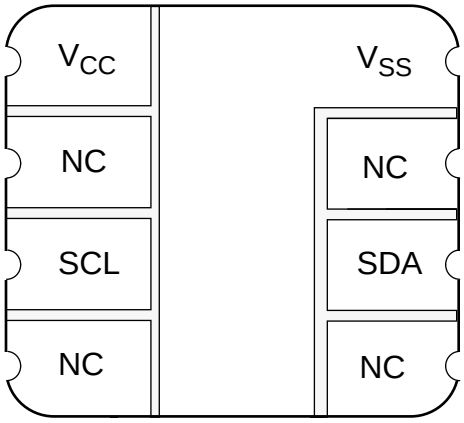
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



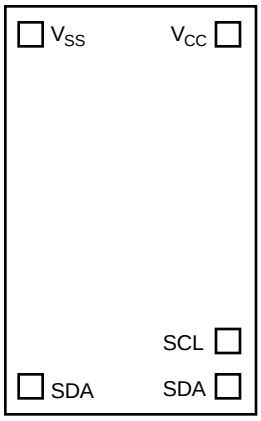
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

8 PAD CHIP ON BOARD SMART CARD MODULE TYPE X



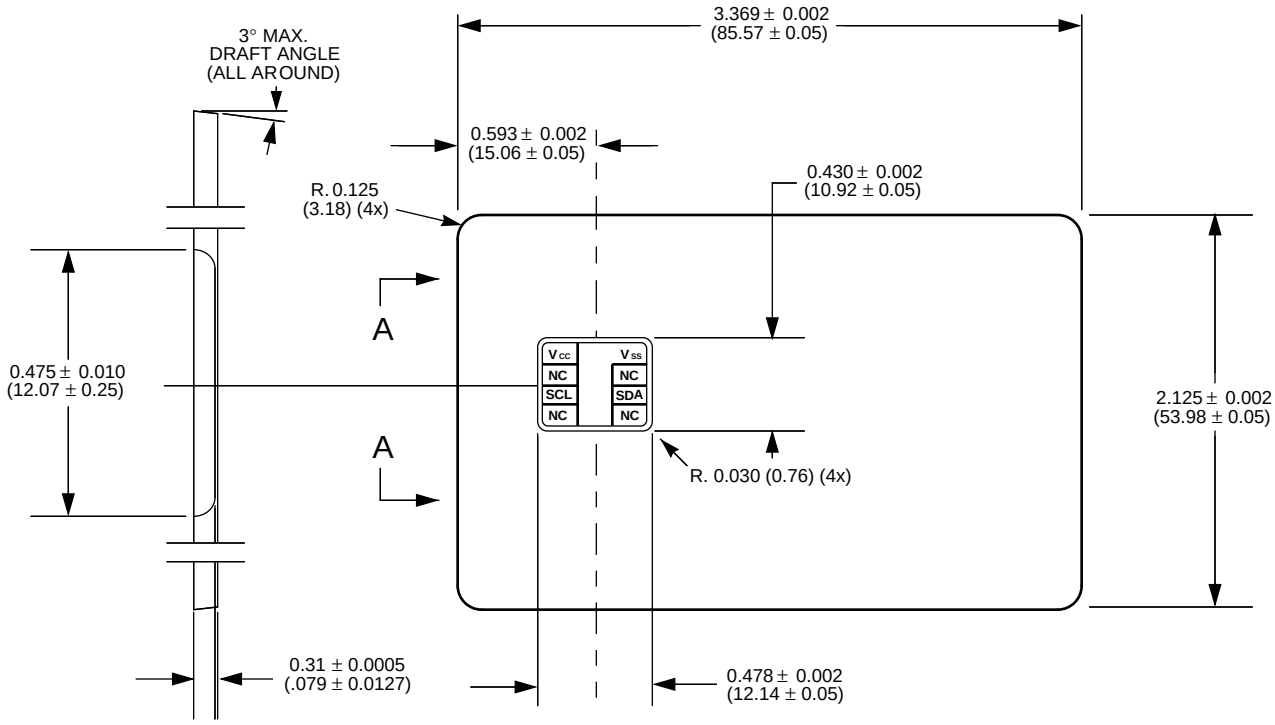
SmartCard Module generic



X24026

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X24026 SMART CARD TYPE Y



MOLD GATE DETAIL
SECTION A-A

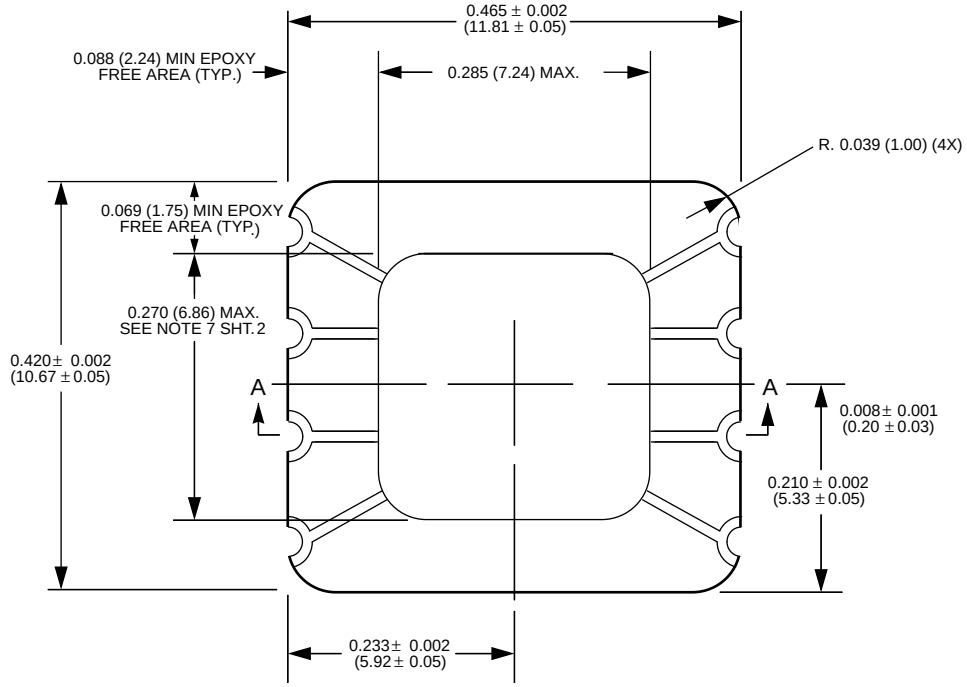
SCALE: 5x

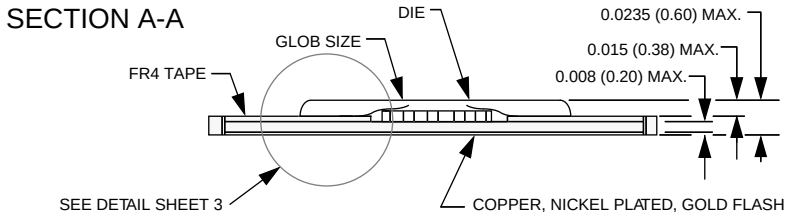
NOTES:

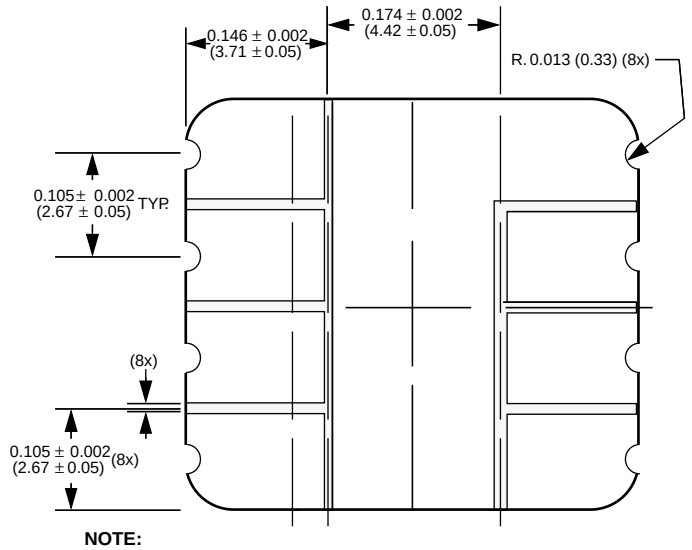
1. ALL DIMENSIONS ARE IN INCHES AND (MILLIMETERS).
2. SPECIFIED DIMS ARE MEASURED AT BOTTOM OF CAVITY.
3. MATERIAL: WHITE PVC MOLDED PLASTIC WITH ANTI-STATIC ADDITIVE.
4. SURFACE FINISH SUITABLE FOR OFFSET PRINTING.

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8 PAD CHIP ON BOARD SMART CARD MODULE TYPE X





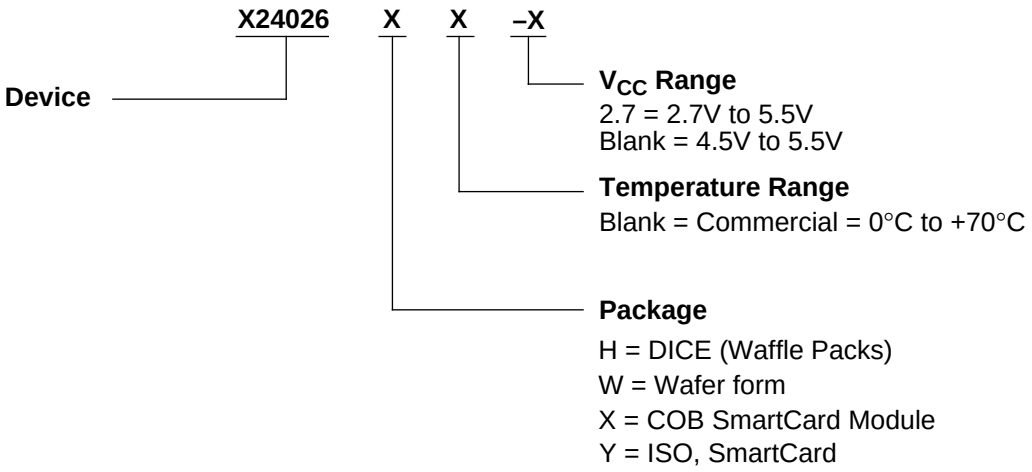


NOTE:
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

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ORDERING INFORMATION

X24026: 256 x 8 CMOS Serial E^2PROM



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LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.