2273 Current Mode PWM Controller

Features

- Burst Mode Control
- 5uA ultra-low startup current
- 1.8mA Low operating current
- Built-in Leading-edge blanking
- Built-in synchronous slope compensation circuit
- Built-in Soft-Start
- 65kHz fixed swith frequency
- Cycle by cycle over current protection (OCP)
- VCC over voltage clamp & under voltage lockout(UVLO)
- Over load protection (OLP)
- OTP and OVP shut down latch
- Maximum Gate output voltage clamped at 12V
- Frequency jittering
- Adjustable OVP through external Zener

Applications

Universal switch power supply equipment and offline AC/DC flyback power converter

- Power Adapter
- Set-Top Box Power Supplies
- Open-frame SMPS
- Battery Charger

General Description

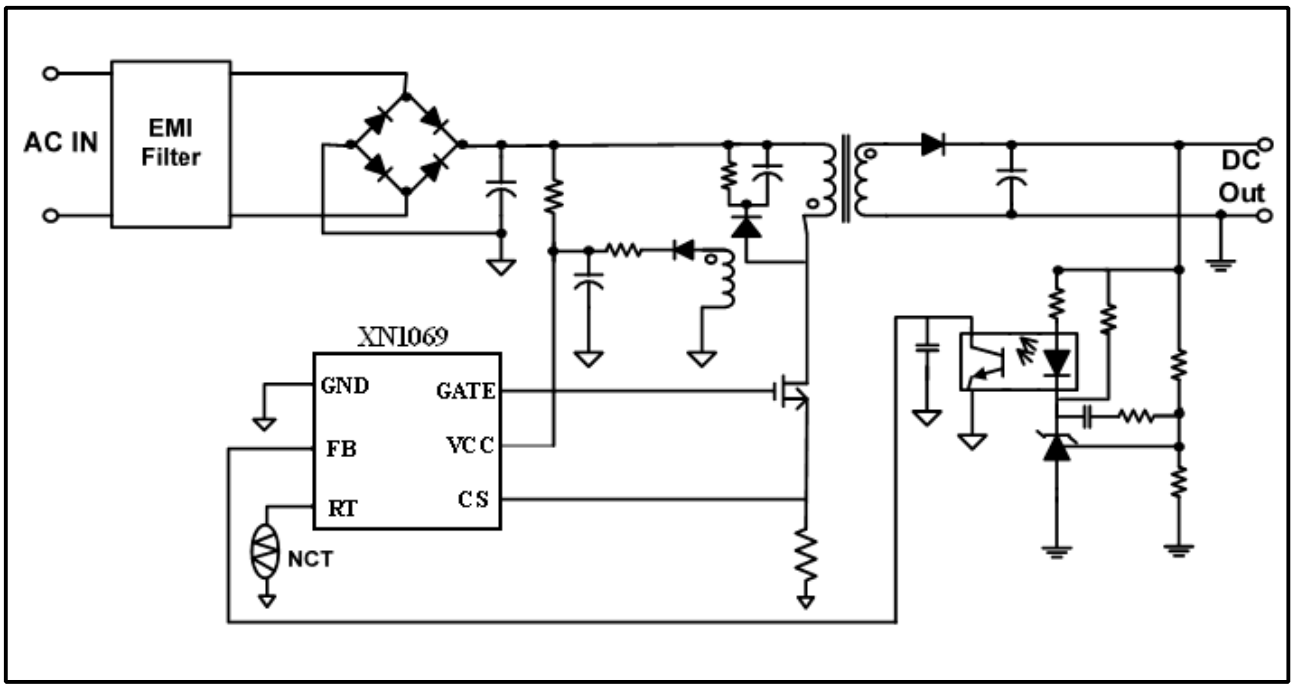
2273 is a high performance current mode PWM controller, optimized for low power power switch equipment.

For lower the standby power and higher RoHS compliant, the IC offers a Burst Mode control feature and ultra-low start-up current and operating current, that is, at the condition of no load or light load, 2273 can reduce the switch frequency linearly which minimize the switching power loss; the ultra-low startup current and operating current make a reliable power for startup design, and also large resistor can be used in the startup circuit to improve switching efficiency. The internal synchronous slope compensation circuit reduces the possible subharmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense(CS) input removes the signal glitch due to snubber diode circuit reverse recovery and thus greatly reduces the external component count and system cost in the design. 2273 offers comprehensive protection coverage with automatic self-recovery feature, including cycle by cycle over current protection (OCP), over load protection (OLP),VCC Clamp, under voltage lockout (UVLO), OTP and OVP shut down latch. The gate-driven output is clamped to maximum 12V to protect the internal MOSFET.

Excellent EMI performance is achieved by using the soft-switching and frequency jittering at the totem-pole-gate-drive output. The tone energy at below 20KHZ is minimized in the design and audio noise is eliminat- ed during operation. The 2273 is the ideal substitute of the linear power supply or the RCC-mod e power, for a better performance of the whole switch power system and a lower cost.

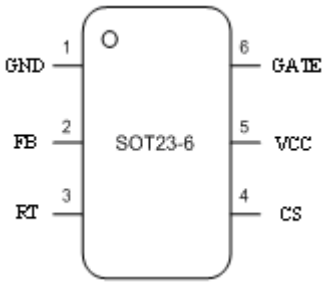
2273 is available in SOT23-6 package.

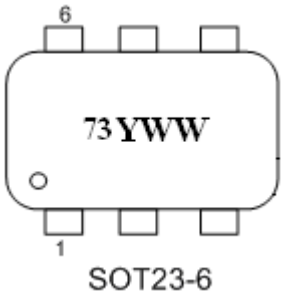
Typical Application Circuit



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Pin Definition and Device Marking



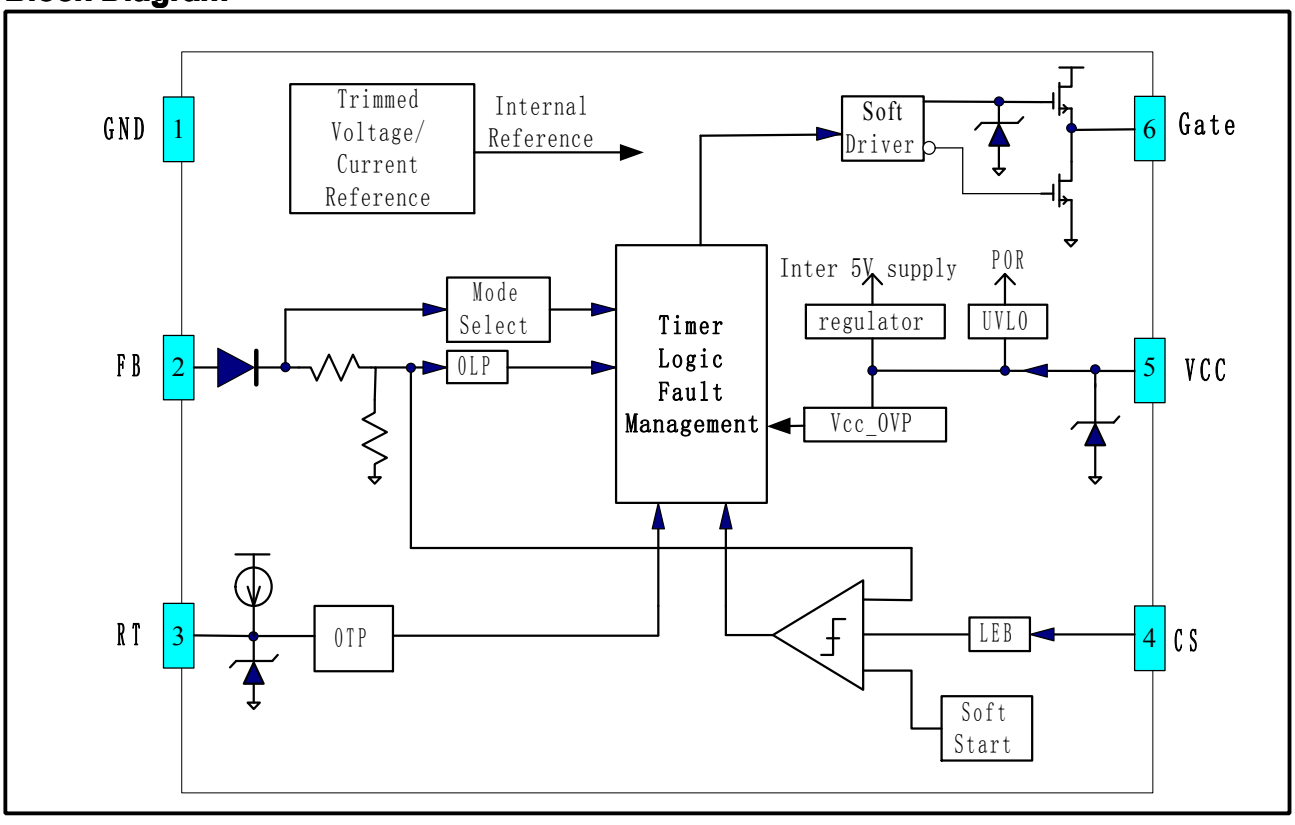


73: WS2273
Y: Year Code (0-9)
WW: Week Code (1-52)

Pin Function Description

Pin Name	Pin Number	Pin Type	Function Description
GND	1	GND	Ground.
FB	2	Feedback Input	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4. The internal protection circuit will automatically shutdown when the FB voltage level exceeds a preset threshold voltage.
RT	3	OTP Setting	Dual function pin. Either connected through a NTC resistor to ground for over temperature shut down/latch control or connected through Zener to VCC for adjustable over voltage protection.
CS	4	Current Monitoring	Current sense input.
VCC	5	Power	Power supply
GATE	6	Gate-driven output	Totem-pole gate driver output for power MOSFET.

Block Diagram



Ordering Information

Package	IC Marking Information	Purchasing Device Name
6-Pin SOT23-6, Pb-free	73XX	2273TP（SOT23-6）

Recommended Operating Condition

Symbol	Parameter	Value	Unit
VCC	VCC supply voltage	10~30	V
RT	RT resistor value	100	Kohm
TA	Operating temperature	-20~85	℃

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VCC	DC supply voltage	30	V
VFB	FB input voltage	-0.3~7	V
VCS	CS input voltage	-0.3~7	V
VRT	RT input voltage	-0.3~7	V
TJ	Operating junction temperature	-20~150	℃
TSTG	Storage temperature	-40~150	℃
VCV	VCC clamp voltage	26	V
ICC	VCC DC clamp current	10	mA

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section are not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

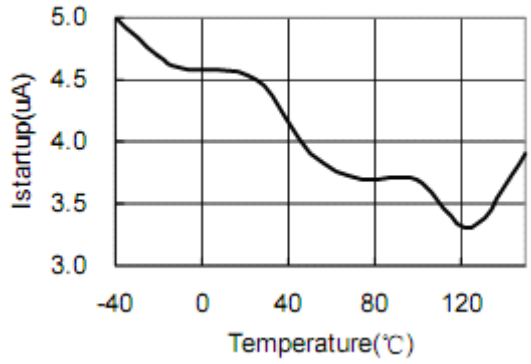
Electrical Characteristics (TA=25℃，VCC=16V, if not otherwise noted)

Supply Voltage (VCC)						
symbol	**parameter**	**Test condition**	**Min**	**Typ**	**Max**	**Unit**
VCC_OP	Operation voltage				30	V
UVLO_ON	Turn on threshold Voltage		6	7	8	V
UVLO_OFF	Turn-off threshold Voltage		12.5	13.5	14.5	V
I_VCC_ST	Start up current	VCC=13V		5	20	uA
I_VCC_OP	Operation Current	VFB=3V		1.8	2.5	mA
Vpull_up	Pull-up PMOS active			13		
VCC_Clamp	VCC Zener Clamp Voltage	IVCC=10mA	30	32	34	V
OVP(ON)	Over voltage protection voltage	CS=0.3V,FB=3V, Ramp up VCC until gate clock is off	26	28	30	
Vlatch_release	Latch release voltage			5		
Feedback Input Section						
VFB_Open	VFB Open Loop Voltage		3.9	4.2		V
Avcs	PWM input gain ΔVfb/ΔVcs			2		V/V
Vref_green	The threshold enter green mode			2.1		V
Vref_burst_H	The threshold exit burst mode			1.3		V
Vref_burst_L	The threshold enter burst mode			1.2		V
IFB_Short	FB Pin Short Current	FB Shorted to GND		0.4		mA
VTH_PL	Power limiting FB Threshold			3.7		V
TD_PL	Power limiting Debounce		80	88	96	ms
ZFB_IN	Input Impedance			16		kΩ
Max_Duty	Maximum duty cycle		75	80	85	%
Current CS Section						
SST	Soft Start time			4		ms
TLEB	Leading edge Blanking Time			220		ns
ZCS	Input impedance			40		kΩ
TD_OC	OCP control delay	GATE with 1nF to GND		120		ns
VTH_OC	OCP threshold	FB＝3V		0.75		V
Vocp_clamping				0.9		V
Oscillator Section						
Fosc	Normal Oscillation Frequency	VCC=14V,FB=3V,CS=0.3V	60	65	70	khz
Fosc_BM	Burst mode frequency			22		khz
Δf_temp	Frequency variation versus temp. Deviation	TEMP = -20 to 85℃		1		%
Δf_VCC	Frequency variation versus VCC	VCC = 12 to 25V		1		%
F_shuffling	Shuffling Frequency			32		Hz
Δf_OSC	Frequency Jittering			±4		%

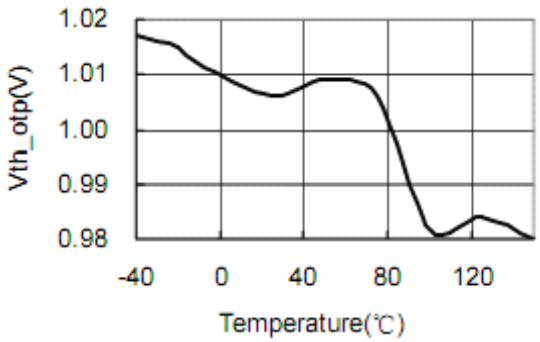
GATE Output Section						
VOL	Output voltage Low	VCC = 14V, Io = -5mA			1	V
VOH	Output voltage high	VCC = 14V, Io = 20mA	6			V
VClamp	Output clamp voltage			12		V
Tr	Rising time	GATE with 1nF to GND， Gate 从 1~12V		175		ns
Tf	Falling time	GATE with 1nF to GND， Gate 从 12~1V		85		ns
Over temperature protection						
IRT	Output current of RT pin		95	100	105	uA
Votp	Threshold voltage for OTP		0.95	1	1.05	V
Td_OTP	OTP debounce time			16		Cycle
VRT_FL	Float voltage at RT pin			2.3		V
Vth_OVP	External OVP threshold voltage			4		V

Typical Operating Characteristics

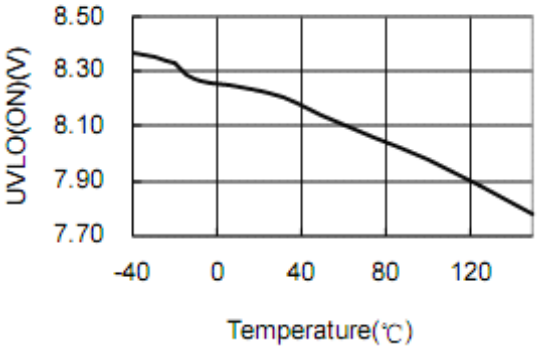
Istartup(uA) vs Temperature(℃)



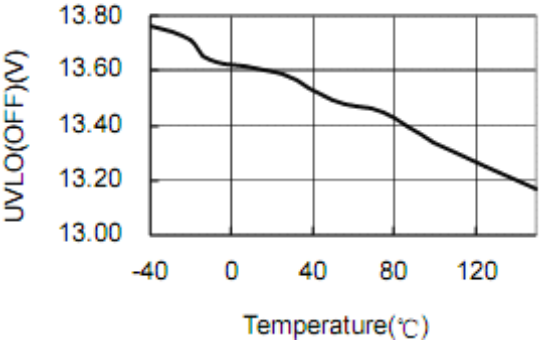
Vth_otp(V) vs Temperature(℃)



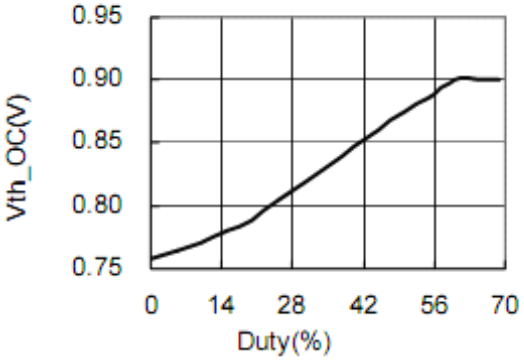
UVLO(ON)(V) vs Temperature(℃)



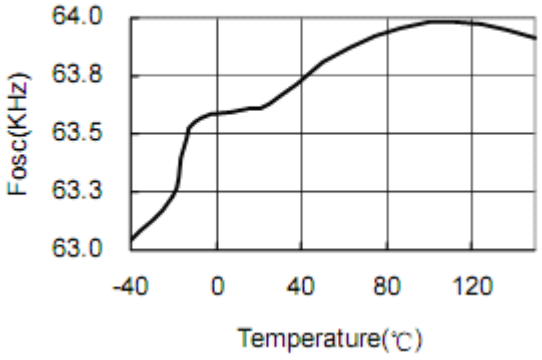
UVLO(OFF)(V) vs Temperature(℃)



Vth_OC(V)vs duty(%)



Fosc(KHz) vs Temperature(℃)



Function Description

2273 is a high performance current mode PWM controller, optimized for low power AC/DC application. Ultra low startup current and operating current together with burst mode feature minimize the standby power consumption and improve the switching efficiency. In addition to reduce the external component count, the internal synchronous slope compensation combines with the leading-edge blanking improves system large stability and reduces the possible subharmonic oscillation. 2273 also have multiform general recovery protection mode. The main function is described as below .

Startup Current and Startup Control

Startup current of 2273 is designed to be extremely low at 5uA, so that VCC could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss, predigest the design of startup circuit and provides reliable startup in application. For the design of AC/DC adaptor with universal input range, a startup resistor of 2 MΩ, 1/8 W could be used together with a VCC capacitor to provide a fast startup and low power dissipation solution.

Operating Current

The operating current of 2273 is low at 1.8mA. Excellent efficiency is achieved with low operating current together and extended burst mode control circuit.

Soft Start

2273 features an internal 4ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VCC reaches UVLO（OFF）, the CS peak voltage is gradually increaced from 0.15V to the maximum level. Every restart up is followed by a soft start.

Extended Burst Mode Operation

At zero load or light load, most of the power dissipation of the switching power supply comes from the MOSFET switching loss, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a period of time. Therefore reducing the switch event leads to reduction on the power loss and thus saving the energy.

For the burst mode control circuit, 2273 self adjusts the switching mode according to the loading condition. At the condition of no load or light/medium load, the FB input voltage drops below burst mode threshold level. Device enters Burst Mode control on the basis of the judgment. The gate drive output switches only when VCC voltage drops below a preset level and FB input is active. Otherwise the gate drive remains at off to minimize the switching loss and power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

The switching frequency is internally fixed at 65kHz. No external frequency setting components are required for PCB design simplification.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in 2273. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the internal MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds slope voltage onto the current sense input voltage for PWM generation. This greatly enhances the close loop stability at CCM and prevents possible subharmonic oscillation and thus reduces the output ripple voltage.

Gate Drive

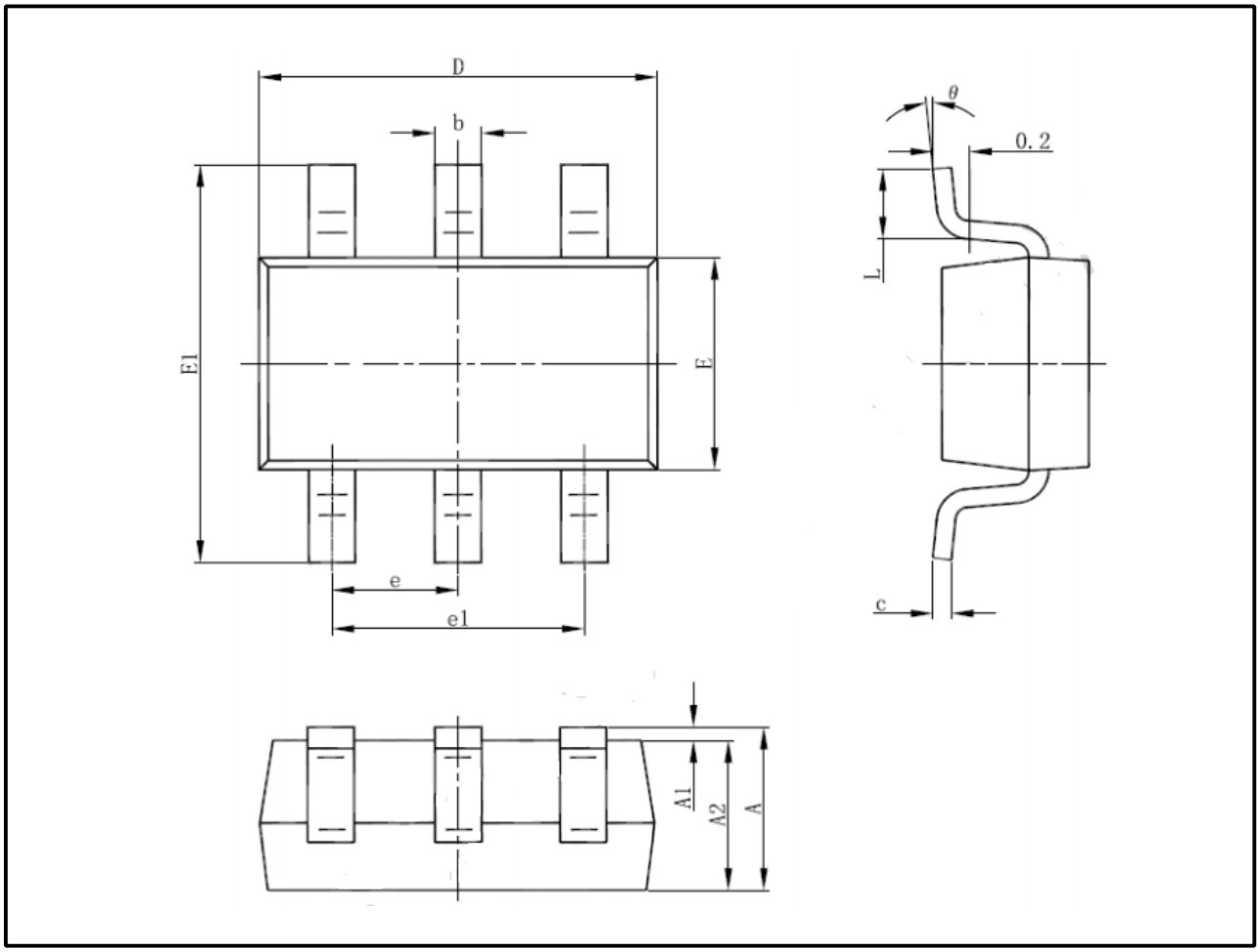
The gate drive strength which is too weak leads to over switch loss of MOSFET while too strong gate drive output compromises in the over EMI. A good tradeoff between output strength and dead time control is achieved through the design of the built-in totem pole gate. The low standby dissipation and good EMI system

design is easier to achieve through this dedicated devise. For MOSFET gate protection, an internal 12V clamp is added at higher than expected VCC input.

Protection Controls

Excellent system stability is achieved by the comprehensive protection of 2273. Including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, VCC Clamp, Under Voltage Lockout on VCC (UVLO), OTP and OVP shut down latch. At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the output power MOSFET. Device restarts when VCC voltage drops below UVLO limit. It is clamped when VCC is higher than threshold value. The power MOSFET is shut down when VCC drops below UVLO limit and device enters power on start-up sequence thereafter.

SOT23-6 Package Outline Dimensions



Symbol	Dimensions In Milimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.300	0.039	0.051
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°