



128Kx32 3.3V SRAM MULTICHIP PACKAGE PRELIMINARY*

FEATURES

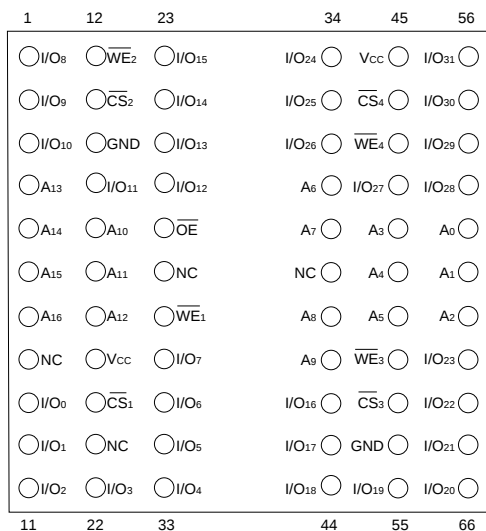
- Access Times of 15 **, 17, 20, 25, 35ns
- Low Voltage Operation
- Packaging
 - 66-pin, PGA Type, 1.075 inch square Hermetic Ceramic HIP (Package 400)
 - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880 inch) square (Package 509), 4.57mm (0.180 inch) high. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 2)
 - 68 lead, Hermetic CQFP (G1U), 23.8mm (0.940 inch) square (Package 509), 3.56mm (0.140 inch) high.
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS128K32V-XG2TX - 8 grams typical
 - WS128K32V-XG1UX - 5 grams typical
 - WS128K32V-XH1X - 13 grams typical

* This data sheet describes a product that is not fully qualified or characterized and is subject to change without notice.

** Commercial and Industrial temperature ranges only.

FIG. 1 PIN CONFIGURATION FOR WS128K32NV-XH1X

TOP VIEW



PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₆	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

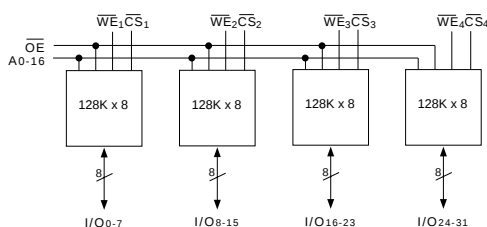
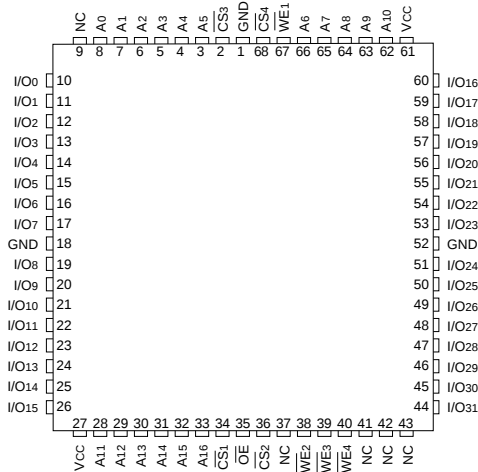




FIG. 2 PIN CONFIGURATION FOR WS128K32V-XG2TX AND WS128K32V-XG1UX

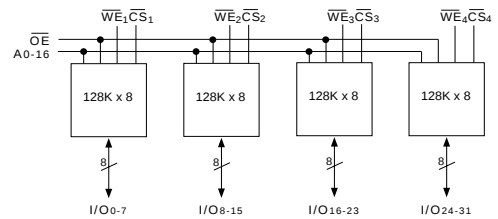
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	5.5	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

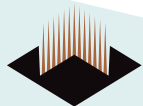
Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ 1-4 capacitance HIP (PGA)	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G2T/G1U			20	
$\overline{CS}$ 1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current (x 32 Mode)	I _{CC} x 32	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5MHz		500	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , f = 5MHz		32	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V



AC CHARACTERISTICS

($V_{CC} = 3.3V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter Read Cycle	Symbol	-15*		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		35		ns
Address Access Time	t_{AA}		15		17		20		25		35	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25		35	ns
Output Enable to Output Valid	t_{OE}		10		11		12		15		20	ns
Chip Select to Output in Low Z	t_{CLZ}^1	5		5		5		5		5		ns
Output Enable to Output in Low Z	t_{OLZ}^1	5		5		5		5		5		ns
Chip Disable to Output in High Z	t_{CHZ}^1		8		9		10		12		15	ns
Output Disable to Output in High Z	t_{OHZ}^1		8		9		10		12		15	ns

1. This parameter is guaranteed by design but not tested.

* Commercial and Industrial only.

AC CHARACTERISTICS

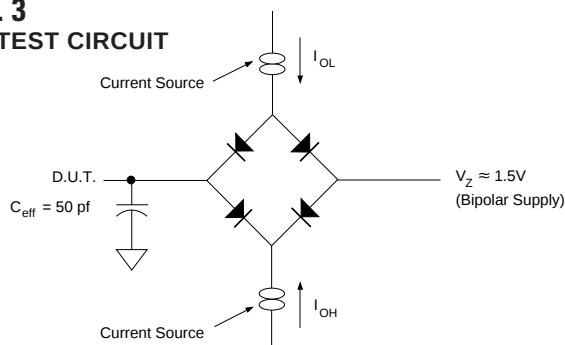
($V_{CC} = 3.3V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter Write Cycle	Symbol	-15*		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		35		ns
Chip Select to End of Write	t_{CW}	13		14		15		20		30		ns
Address Valid to End of Write	t_{AW}	13		14		15		20		30		ns
Data Valid to End of Write	t_{DW}	10		11		12		15		18		ns
Write Pulse Width	t_{WP}	13		14		15		20		30		ns
Address Setup Time	t_{AS}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		0		ns
Output Active from End of Write	t_{OW}^1	5		5		5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}^1		8		9		10		10		15	ns
Data Hold Time	t_{DH}	0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

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FIG. 3
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0$, $V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



FIG. 4
TIMING WAVEFORM - READ CYCLE

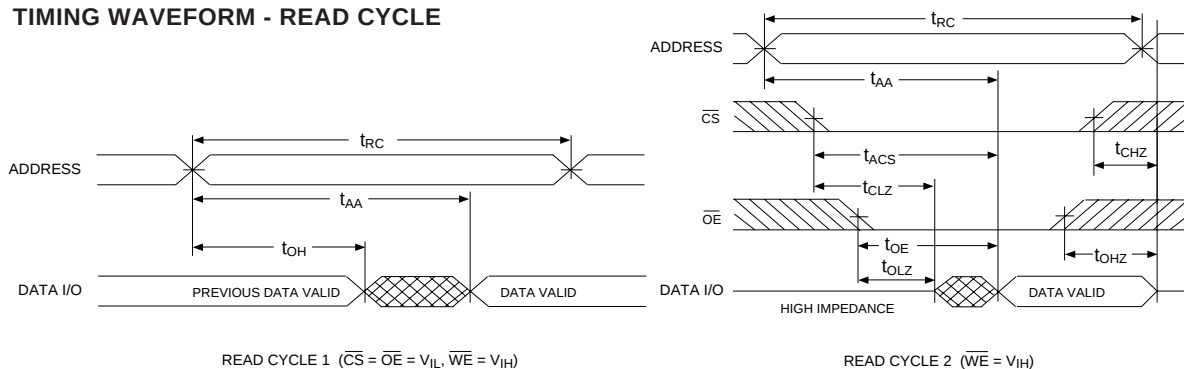


FIG. 5
WRITE CYCLE - $\overline{WE}$ CONTROLLED

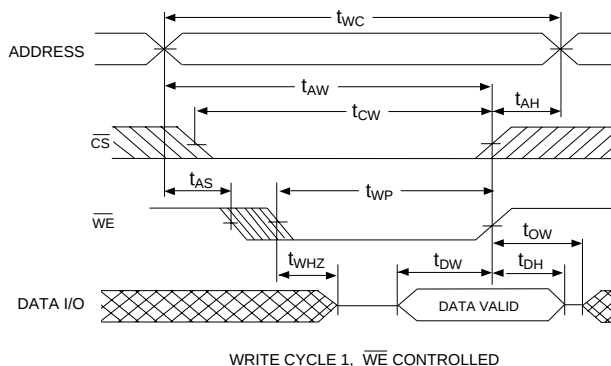
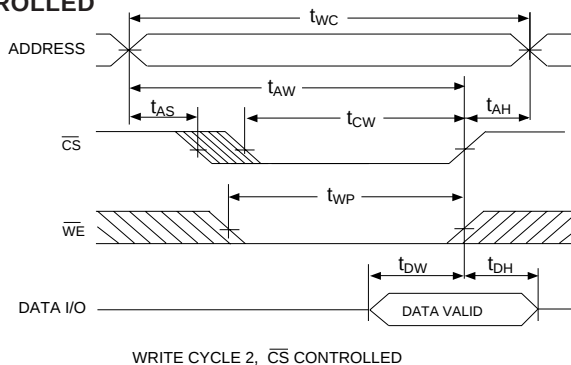


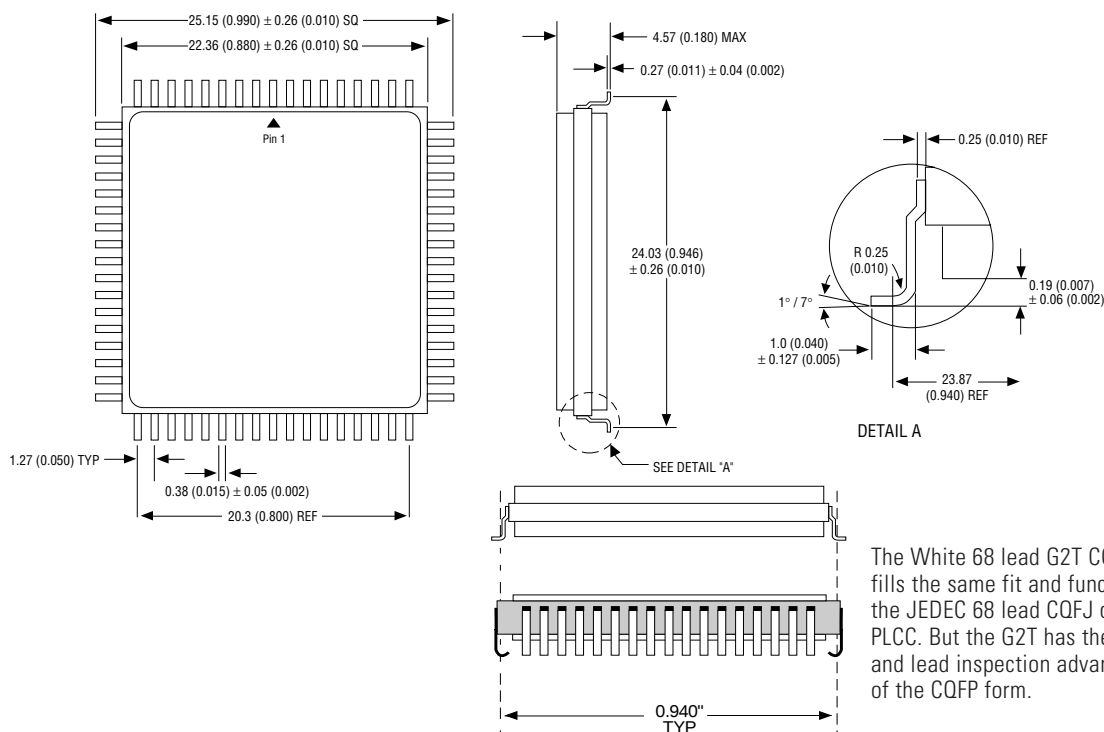
FIG. 6
WRITE CYCLE - $\overline{CS}$ CONTROLLED



**PACKAGE 400:** 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)

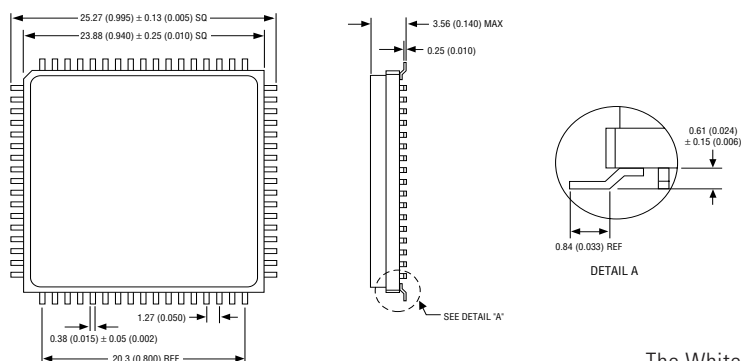


PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W S 128K 32 X V - XXX X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

H1 = Ceramic Hex-In-line Package, HIP (Package 400)

G2T = 22.4mm CQFP (Package 509)

G1U = 23.8mm Low Profile CQFP (Package 519)

ACCESS TIME (ns)

Low Voltage Supply 3.3V $\pm$ 10%

IMPROVEMENT MARK:

N = No Connect at pins 8, 21, 28, 39 in HIP for upgrade.

ORGANIZATION, 128Kx32

User configurable as 256Kx16 or 512Kx8

SRAM

WHITE ELECTRONIC DESIGNS CORP.