



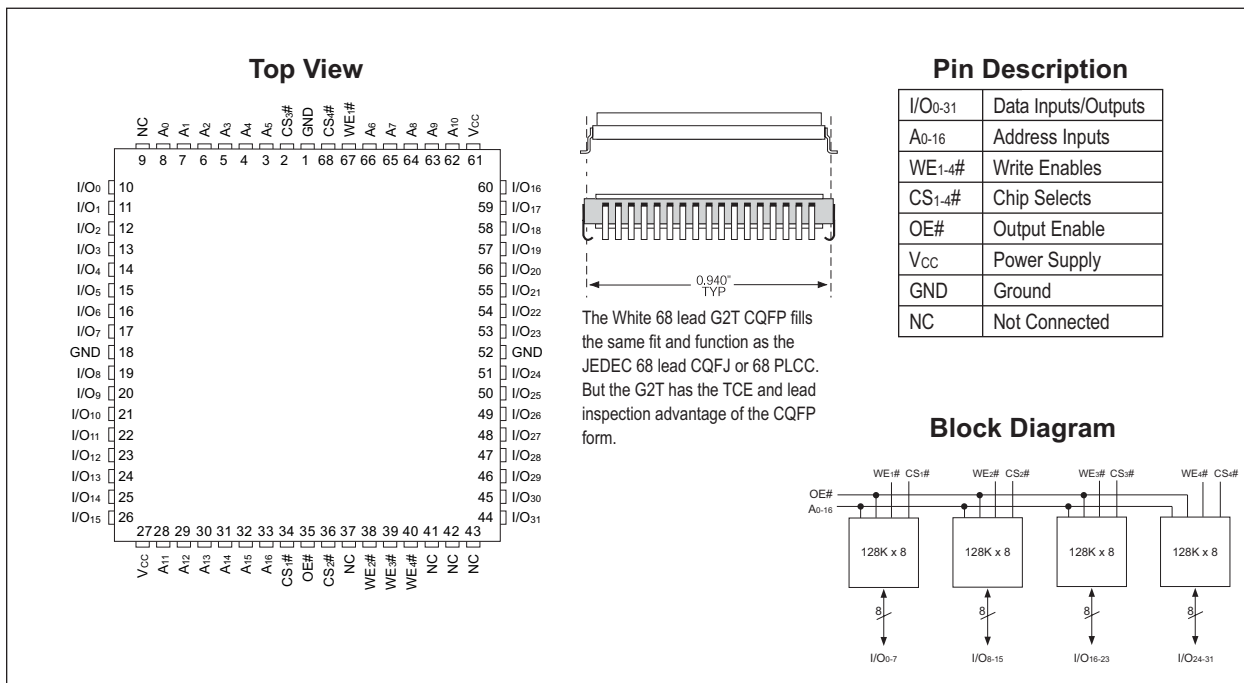
128Kx32 SRAM MULTICHIP PACKAGE, RADIATION TOLLERANT

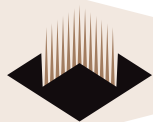
FEATURES

- Access Times of 35, 45, 55ns
- Packaging
 - 68 lead, 22.4mm CQFP (G2T), 4.57mm (0.180"), (Package 509)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Low Power Data Retention
- Commercial, Industrial and Military Temperature Ranges
- 5V Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS128K32-XG2TXE – 8 grams typical
- Radiation tolerant with epitaxial layer on die.
- 6T memory cells provide excellent protection against soft errors

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

FIGURE 1 – PIN CONFIGURATION FOR WS128K32N-XG2TXE





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (MIL)	T _A	-55	+125	°C

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C _{OE}	V _{IN} = 0V, f = 1.0 MHz	50	pF
WE1-4# capacitance	C _{WE}	V _{IN} = 0V, f = 1.0 MHz	20	pF
CS1-4# capacitance	C _{CS}	V _{IN} = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	C _{I/O}	V _{I/O} = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

RADIATION CHARACTERISTICS

Total Dose (TM1019.5)			Latch-up 25°C V _{CC} Max (MeV/mg/cm ²)	SEU LET Threshold (V _{CC} MIN) (MeV/mg/cm ²)	Cross Section /BIT (E-6 cm ²)
Functional (Krad)	Parametric (Krad)	Typical Iocsb (mA)			
30	30	1.2	>100	2	0.2

DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC}	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5		520	mA
Standby Current	I _{SB}	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5		8	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -40mA, V _{CC} = 4.5	2.4		V

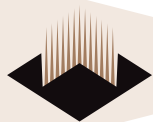
NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

-55°C ≤ T_A ≤ +125°C

Characteristic	Sym	Conditions	Min	Max	Units
Data Retention Voltage	V _{CC}	V _{CC} = 2.0V	2	—	V
Data Retention Quiescent Current	I _{CCDR}	CS ≥ V _{CC} - 0.2V	—	1	mA
Chip Disable to Data Retention Time (1)	T _{CDR}	V _{IN} ≥ V _{CC} - 0.2V	0	—	ns
Operation Recovery Time (1)	T _R	or V _{IN} ≤ 0.2V	T _{RC}	—	ns

NOTE: Parameter guaranteed, but not tested.



AC CHARACTERISTICS

$V_{CC} = 5.0V$, $GND = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		55		ns
Address Access Time	t_{AA}		35		45		55	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Select Access Time	t_{ACS}		35		45		55	ns
Output Enable to Output Valid	t_{OE}		15		20		30	ns
Chip Select to Output in Low Z	t_{CLZ}^1	3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}^1	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}^1		20		20		20	ns
Output Disable to Output in High Z	t_{OHZ}^1		12		15		20	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

$V_{CC} = 5.0V$, $GND = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	35		45		55		ns
Chip Select to End of Write	t_{CW}	25		35		45		ns
Address Valid to End of Write	t_{AW}	25		35		45		ns
Data Valid to End of Write	t_{DW}	20		25		25		ns
Write Pulse Width	t_{WP}	25		35		45		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}^1	0		0		0		ns
Write Enable to Output in High Z	t_{WHZ}^1		10		15		20	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIGURE 2 – AC TEST CIRCUIT

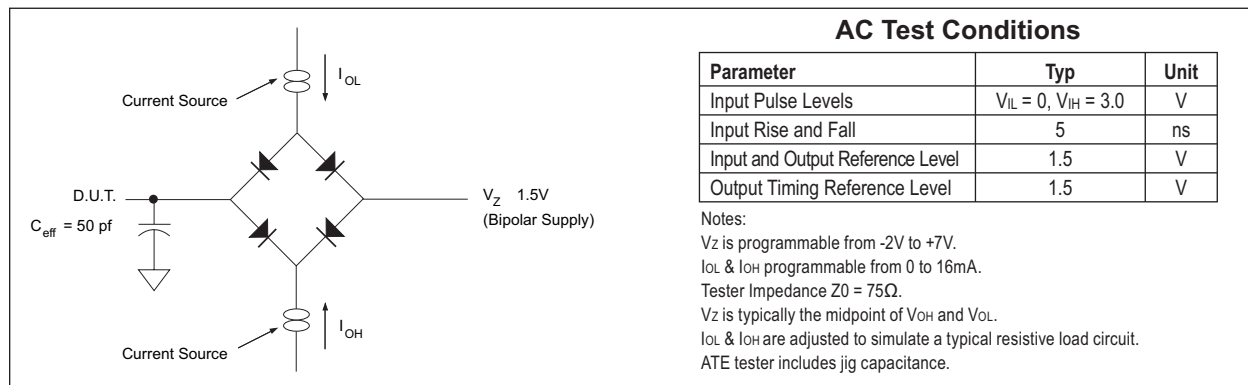




FIGURE 3 – TIMING WAVEFORM - READ CYCLE

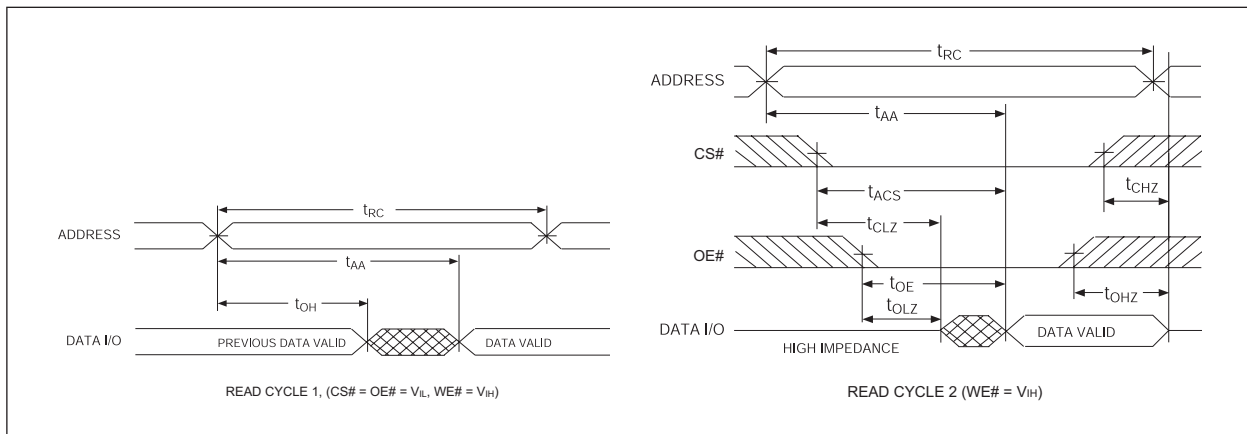


FIGURE 4 – WRITE CYCLE - WE# CONTROLLED

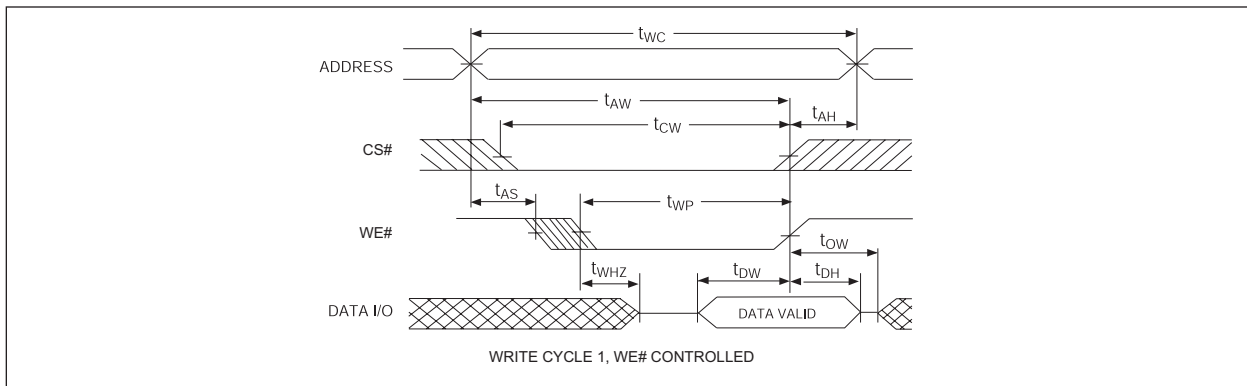
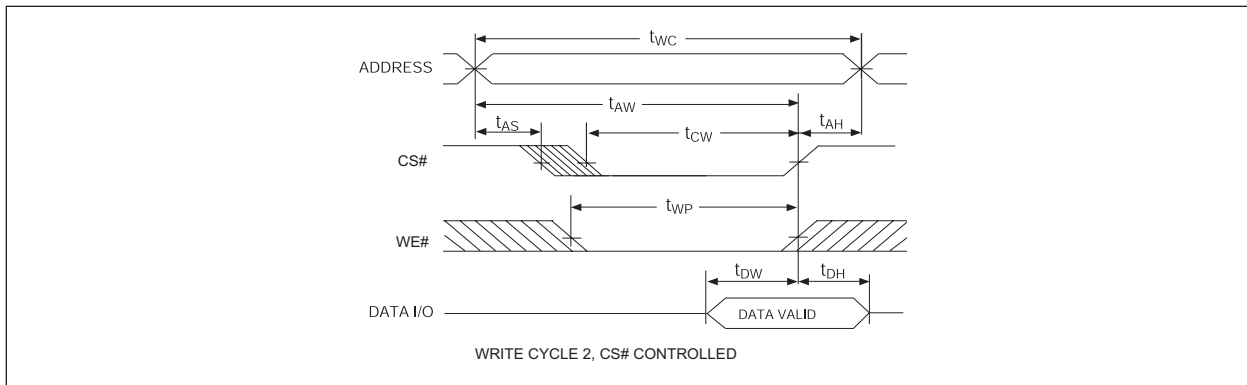
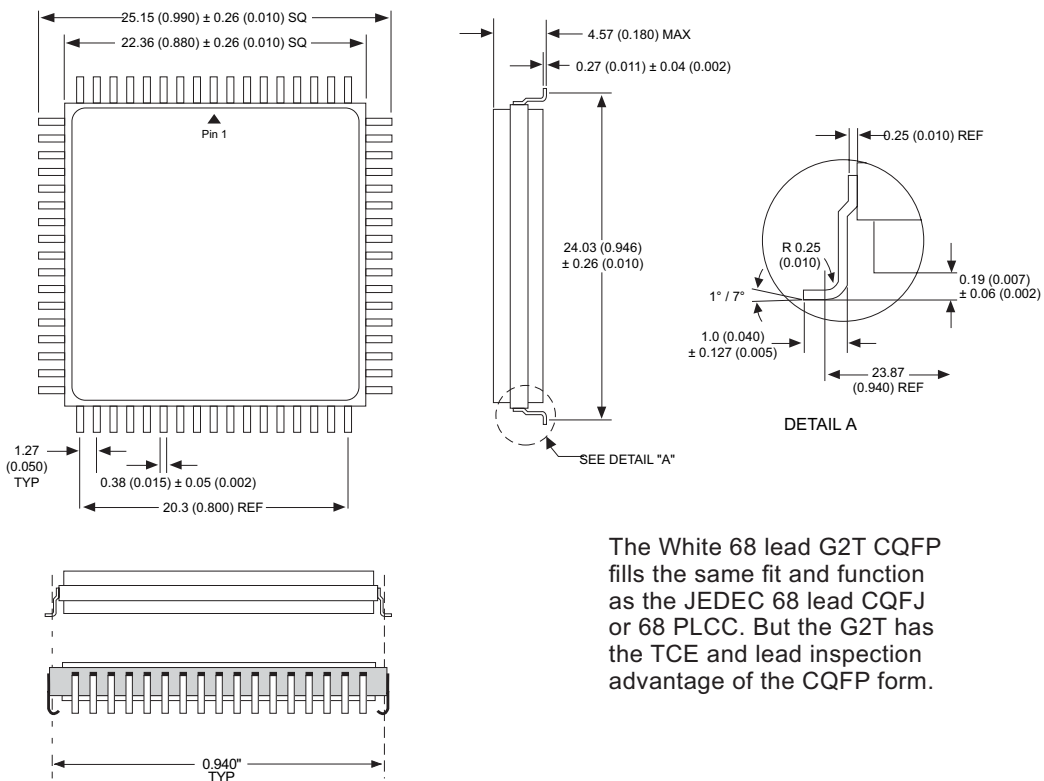


FIGURE 5 – WRITE CYCLE - CS# CONTROLLED





PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W S 128K 32 X - XXX X X E X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

E = Epitaxial Layer on die

DEVICE GRADE:

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

G2T = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 510)

ACCESS TIME (ns)

IMPROVEMENT MARK:

N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades

ORGANIZATION, 128Kx32

User configurable as 256Kx16 or 512Kx8

SRAM

WHITE ELECTRONIC DESIGNS CORPORATION

* Low Power Data Retention only available in G2T Package Type