



512Kx8 MONOLITHIC SRAM

FEATURES

- Access Times 15, 17, 20ns
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
 - 36 lead Ceramic SOJ (Package 100)
 - 36 lead Ceramic Flat Pack (Package 226)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
 - 32 pin Ceramic DIP (Package 300)
 - 32 lead Ceramic SOJ (Package 101)
 - 32 lead Ceramic Thinpack™ Flat Pack (Package 321)
- 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
- Low Power CMOS
- Low Voltage Operation
 - 3.3V ± 10% Power Supply
- Commercial, Industrial and Military Temperature Range
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
 - No clock or refresh required
- Three State Output

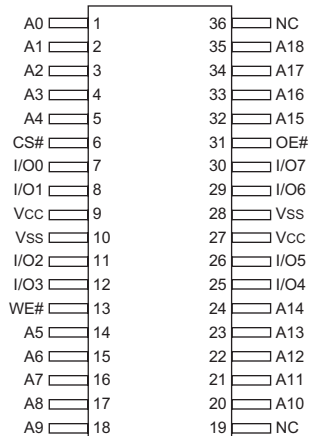
* This product is subject to change without notice.

REVOLUTIONARY PINOUT

EVOLUTIONARY PINOUT

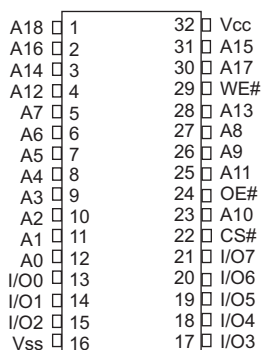
36 FLAT PACK
36 CSOJ

TOP VIEW



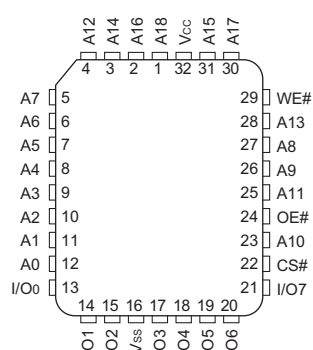
32 DIP
32 CSOJ (DE)
32 FLAT PACK (FF)

TOP VIEW



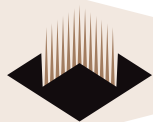
32 CLCC

TOP VIEW



PIN DESCRIPTION

A0-18	Address Inputs
I/O 0-7	Data Input/Output
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
Vcc	Power Supply
Vss	Ground



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Range to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	4.6	V

TRUTH TABLE

CS#	OE#	WE#	MODE	DATA I/O	POWER
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil)	T _A	-55	+125	°C

CAPACITANCE

T_A = +25°C

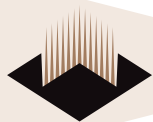
Parameter	Symbol	Conditions	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0 V, f = 1.0 MHz	12	pF
Output capacitance	C _{OUT}	V _{OUT} = 0 V, f = 1.0 MHz	12	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 3.6, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC}	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6		100	mA
Standby Current	I _{SS}	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6		50	mA
Output Low Voltage	V _{OL}	I _{OL} = 4.0mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V



AC CHARACTERISTICS

 $V_{CC} = 5.0V$, $GND = 0V$, $-55^{\circ}C \leq T_A \leq 125^{\circ}C$

Parameter Read Cycle	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20	ns
Output Enable to Output Valid	t_{OE}		8		8		10	ns
Chip Select to Output in Low Z	t_{CLZ1}	1		1		1		ns
Output Enable to Output in Low Z	t_{OLZ1}	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ1}		8		8		10	ns
Output Disable to Output in High Z	t_{OHZ1}		8		8		10	ns

1. This parameter is guaranteed by design but not tested.

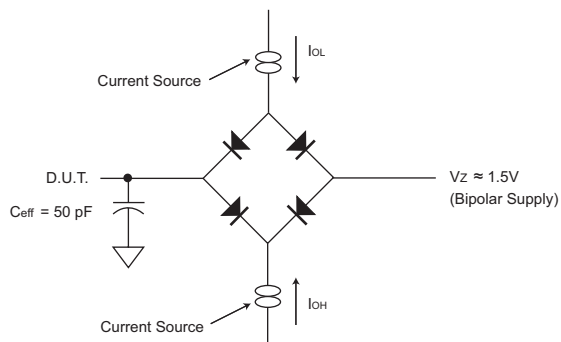
AC CHARACTERISTICS

 $V_{CC} = 5.0V$, $GND = 0V$, $-55^{\circ}C \leq T_A \leq 125^{\circ}C$

Parameter Write Cycle	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	12		12		14		ns
Address Valid to End of Write	t_{AW}	12		12		14		ns
Data Valid to End of Write	t_{DW}	9		9		10		ns
Write Pulse Width	t_{WP}	12		14		14		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW1}	2		3		3		ns
Write Enable to Output in High Z	t_{WHZ1}		8		8		9	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0$, $V_{IH} = 2.5$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

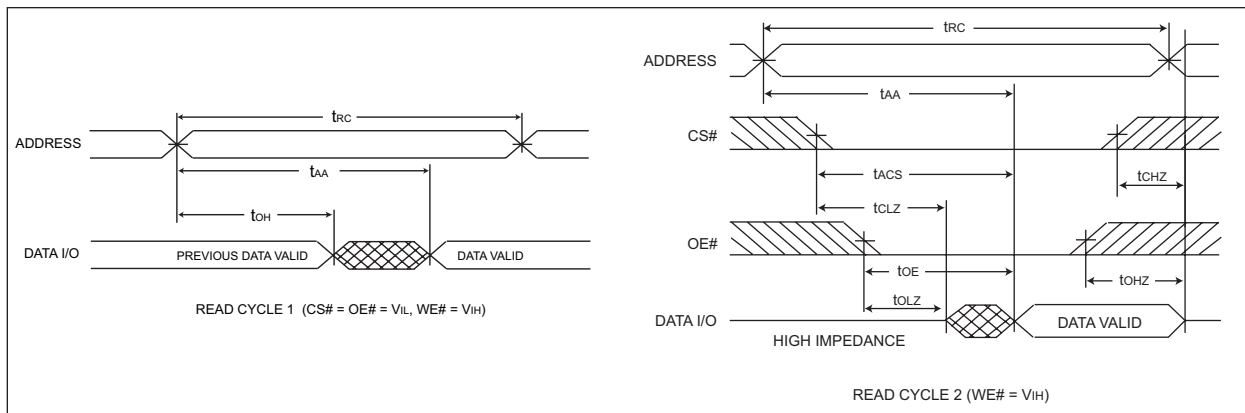
Notes:

 V_Z is programmable from -2V to +7V. I_{OL} & I_{OH} programmable from 0 to 16mA.Tester Impedance $Z_0 = 75\Omega$. V_Z is typically the midpoint of V_{OH} and V_{OL} . I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

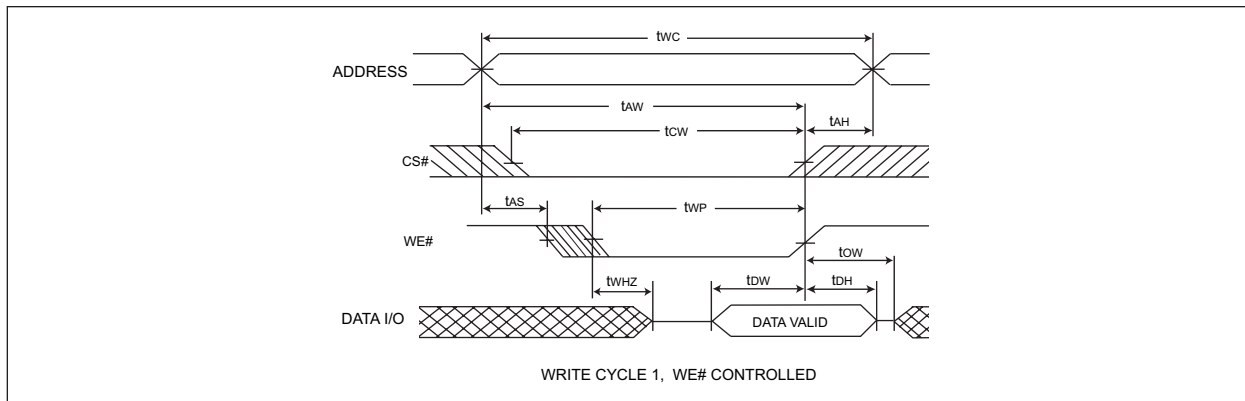
ATE tester includes jig capacitance.



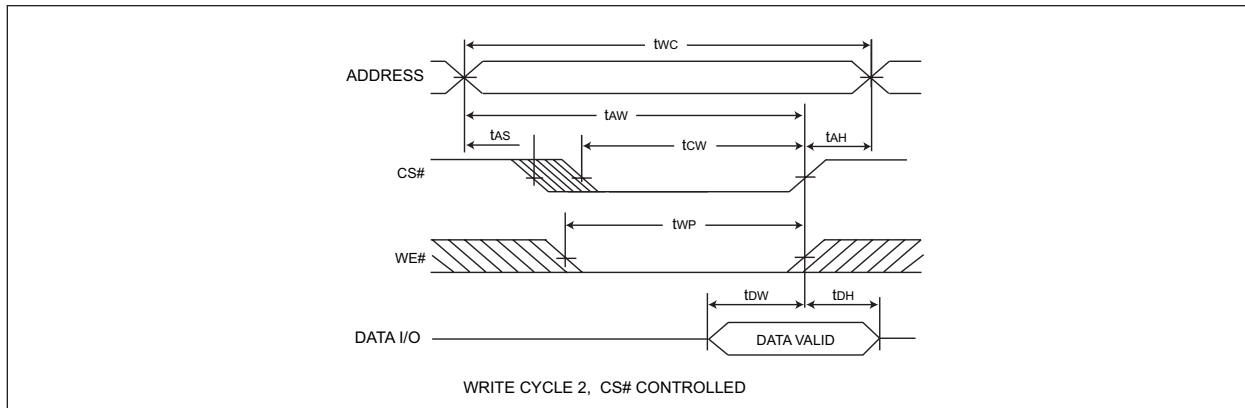
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - WE# CONTROLLED

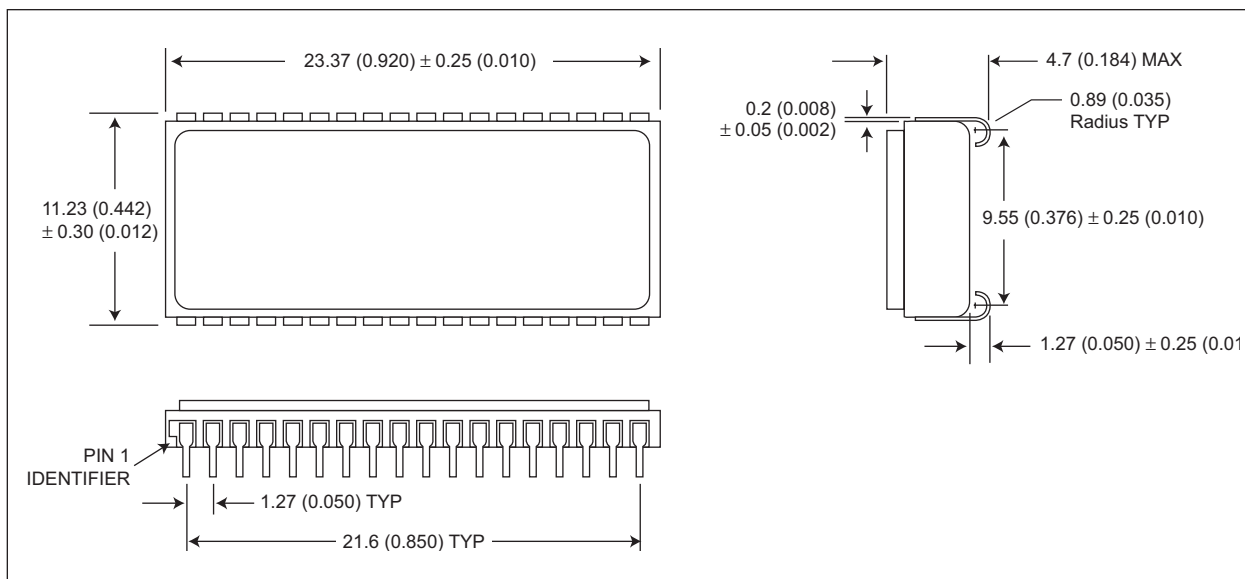


WRITE CYCLE - CS# CONTROLLED



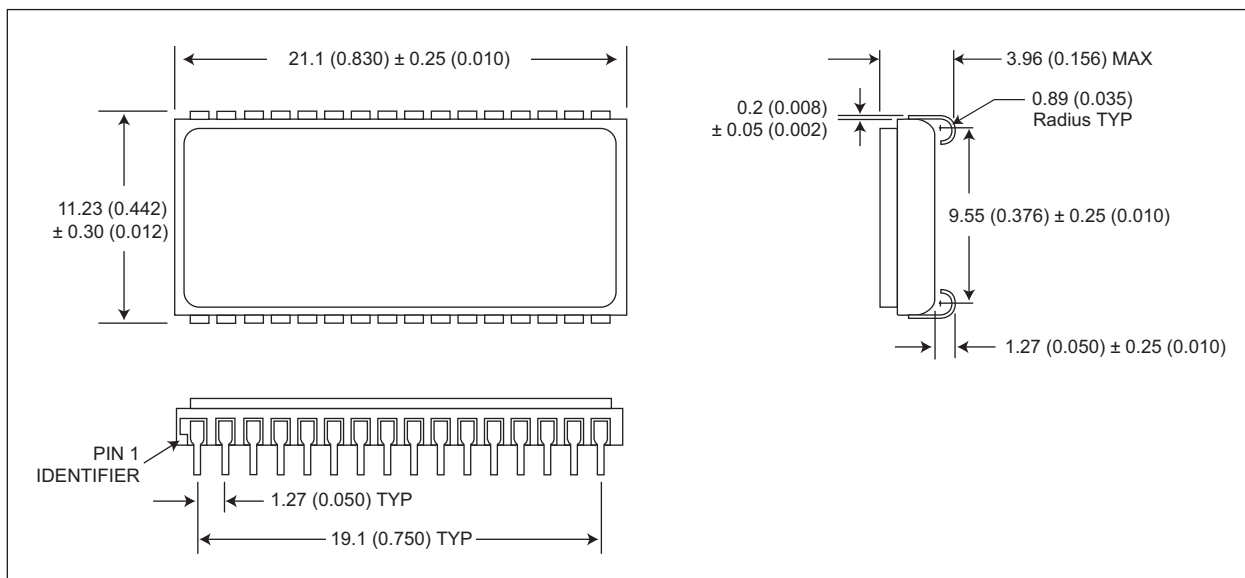


PACKAGE 100: 36 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

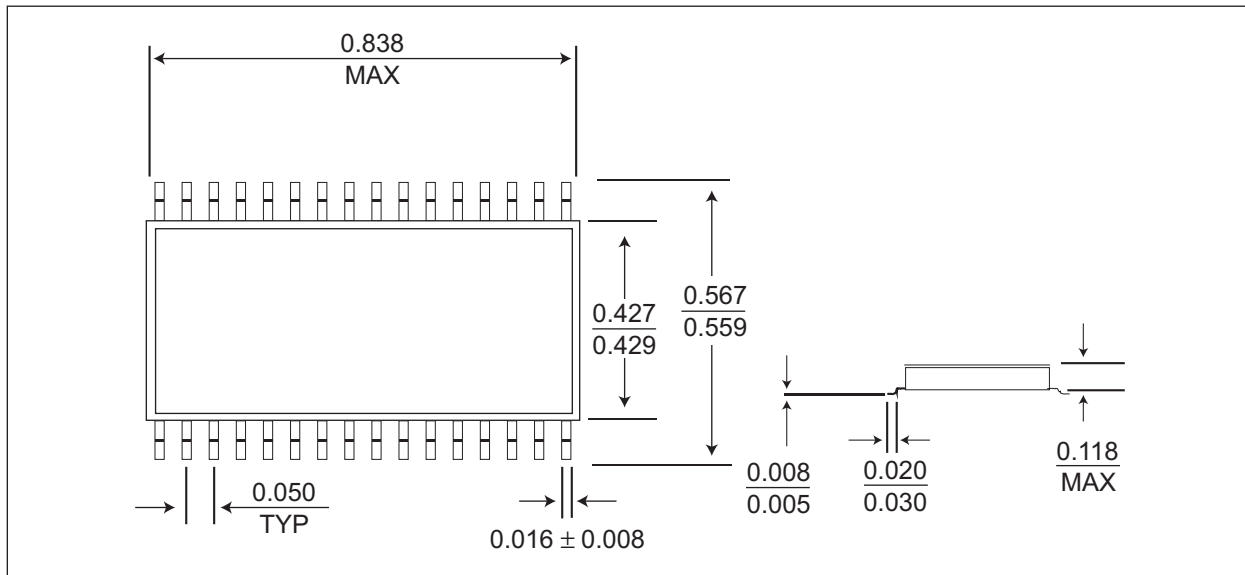
PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

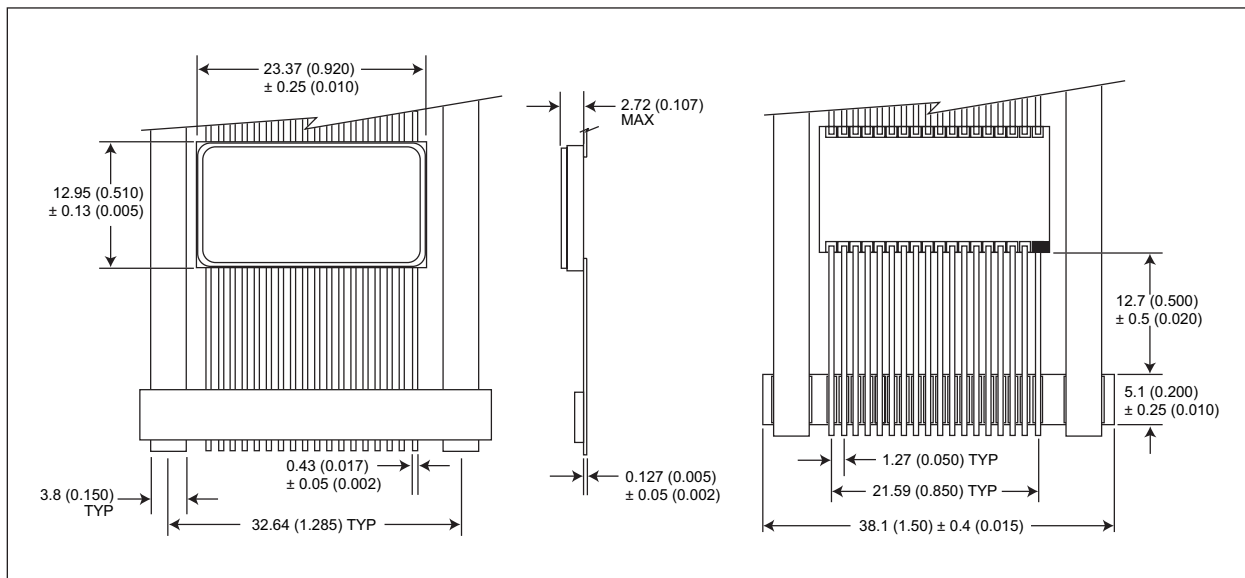


PACKAGE 321: 32 PIN CERAMIC THINPACK™ FLATPACK



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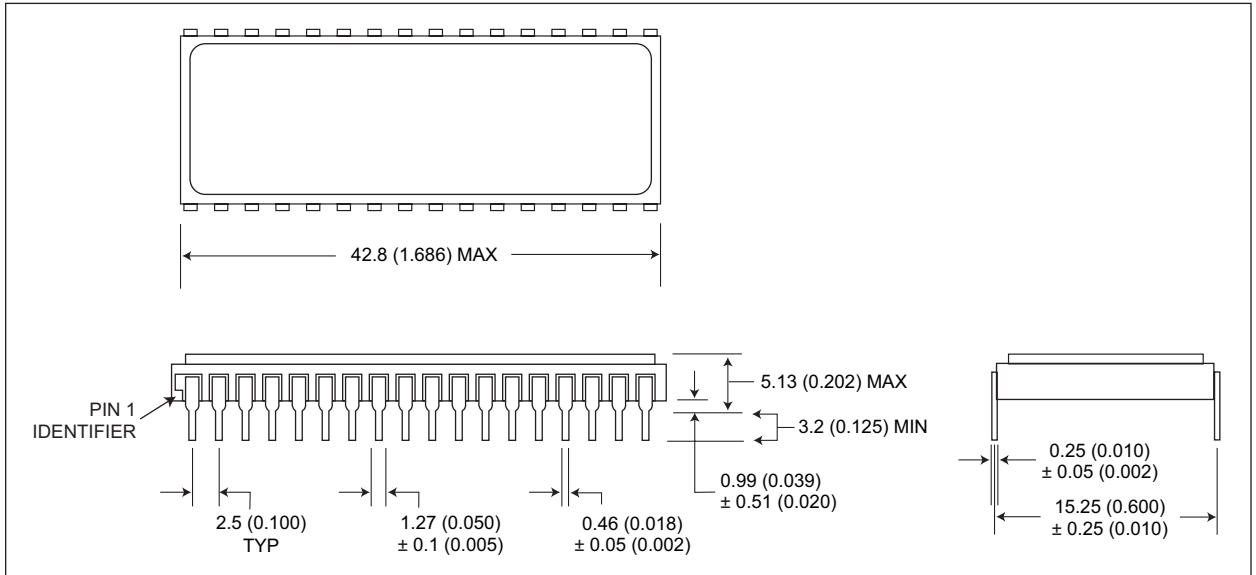
PACKAGE 226: 36 LEAD, CERAMIC FLAT PACK



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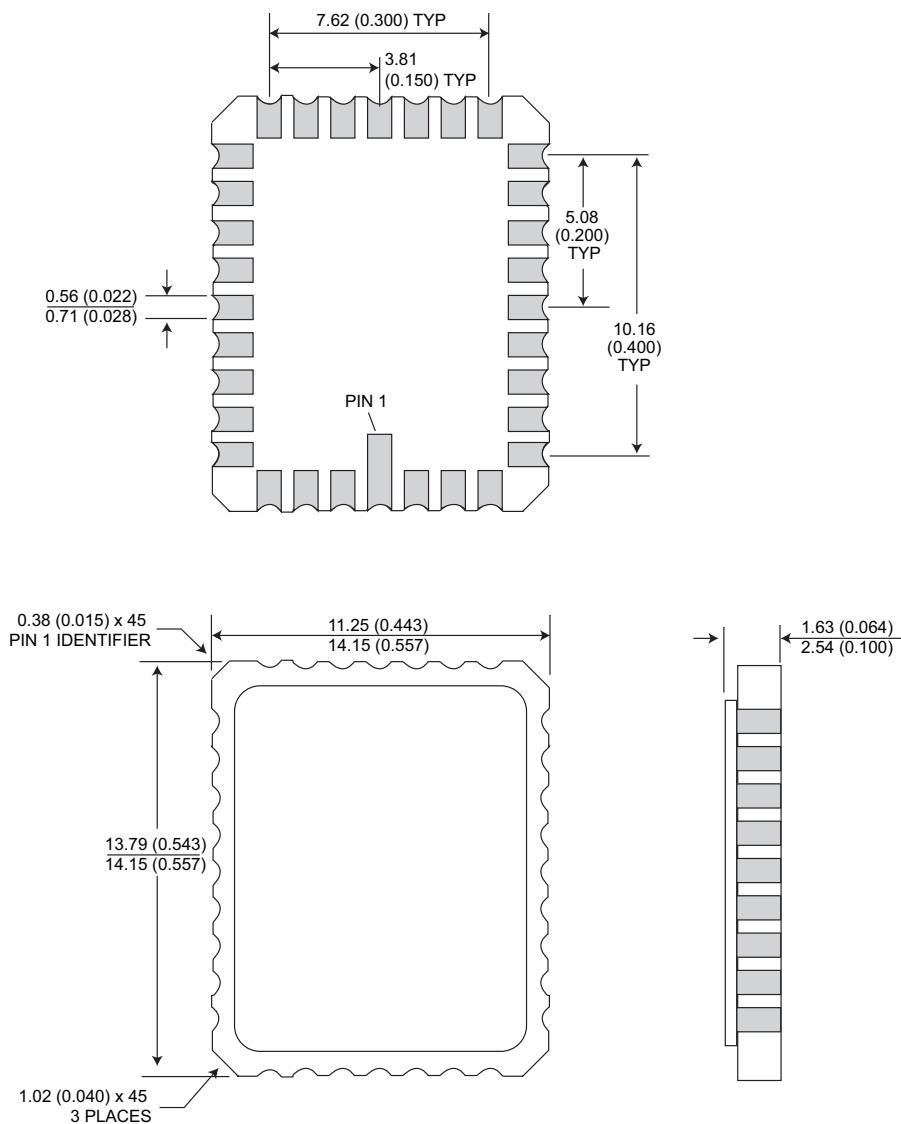
PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

	W	M	S	512K 8	V	-	XXX	X	X	X
WHITE ELECTRONIC DESIGNS CORP.	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
MONOLITHIC	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
SRAM	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
ORGANIZATION, 512K x 8	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
LOW VOLTAGE SUPPLY 3.3V ± 10%	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
ACCESS TIME (ns)	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
PACKAGE:	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
C = 32 pin Ceramic 0.600" DIP (Package 300)										
CL = 32 pin Rectangular Ceramic Leadless Chip Carrier (Package 601)										
DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary										
DJ = 36 Lead Ceramic SOJ (Package 100)										
F = 36 Lead Ceramic Flat Pack (Package 226)										
FF = 32 Lead Ceramic Thinpack™ Flat Pack (Package 321)										
DEVICE GRADE:	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
M = Military Screened	-55°C ≤ T _A ≤ 125°C									
I = Industrial	-40°C ≤ T _A ≤ 85°C									
C = Commercial	0°C ≤ T _A ≤ 70°C									
LEAD FINISH:	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Blank = Gold plated leads										
A = Solder dip leads										