WM8805

8:1 Digital Interface Transceiver with PLL

DESCRIPTION

The WM8805 is a high performance consumer mode S/PDIF transceiver with support for 8 received Channels and 1 transmitted Channel.

A crystal derived, or externally provided high quality master clock is used to allow low jitter recovery of S/PDIF supplied master clocks.

Generation of all typically used audio clocks is possible using the high performance internal PLL. A dedicated CLKOUT pin provides a high drive clock output.

A pass through option is provided which allows the device simply to be used to clean up (de-jitter) the received digital audio signals.

The device may be used under software control or stand alone hardware control modes. In software control mode, both 2-wire with read back and 3-wire interface modes are supported.

Status and error monitoring is built-in and results can be read back over the control interface, on the GPO pins or streamed over the audio data interface in 'With Flags' mode (audio data with status flags appended).

The audio data interface supports I^2S, left justified, right justified and DSP audio formats of 16-24 bit word length, with sample rates from 32 to 192ks/s.

The device is supplied in a 28-lead Pb-free SSOP package.

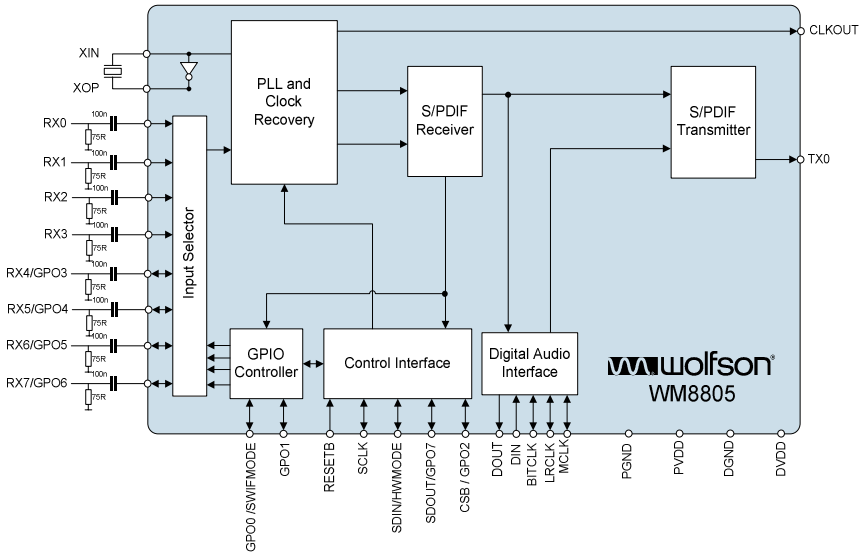
FEATURES

- S/PDIF (IEC60958-3) compliant.
- Advanced jitter attenuating PLL with low intrinsic period jitter of 50 ps RMS.
- S/PDIF recovered clock using PLL, or stand alone crystal derived clock generation.
- Supports 10 – 27MHz crystal clock frequencies.
- 2-wire / 3-Wire serial or hardware control interface.
- Programmable Audio data interface modes:
  - I^2S, Left, Right Justified or DSP
  - 16/20/24 bit word lengths
- 8 channel receiver input and 1 channel transmit output.
- Auto frequency detection / synchronisation.
- Selectable output status data bits.
- Up to 8 configurable GPO pins.
- De-emphasis flag output.
- Non-audio detection including DOLBY™ and DTS™.
- Channel status changed flag.
- Configurable clock distribution with selectable output MCLK rate of 512fs, 256fs, 128fs and 64fs.
- 2.7 to 3.6V digital and PLL supply voltages.
- 28-lead SSOP package.

APPLICATIONS

- Surround Sound AV processors and Hi-Fi systems
- Music industry applications
- DVD-P/DVD-RW
- Digital TV

BLOCK DIAGRAM



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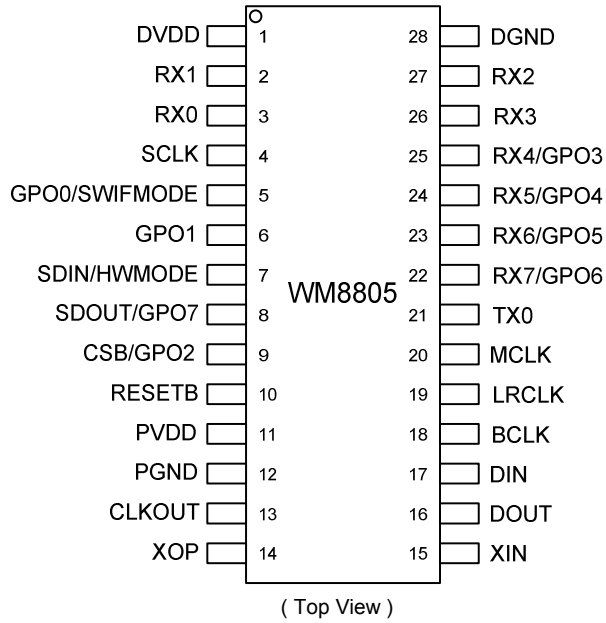
PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8805GEDS	-25 to +85°C	28-lead SSOP (Pb-free)	MSL1	260°C
WM8805GEDS/R	-25 to +85°C	28-lead SSOP (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	Type	DESCRIPTION
1	DVDD	Supply	Digital core supply
2	RX1	Digital In	S/PDIF receive channel 1
3	RX0	Digital In	S/PDIF receive channel 0
4	SCLK	Digital In/Out	Control interface clock / TRANS_ERR flag in hardware control mode. See note 2.
5	GPO0 / SWIFMODE	Digital In/Out	General purpose digital output or selected functionality at hardware reset. See note 2.
6	GPO1	Digital Out	General purpose digital output
7	SDIN / HWMODE	Digital Input	Control interface data input and hardware/software mode select at hardware reset. See note 2.
8	SDOUT / GPO7	Digital In/Out	Control interface data output / NON_AUDIO flag in hardware control mode / GPO in 2-wire software control mode. See note 2.
9	CSB / GPO2	Digital In/Out	Chip select / UNLOCK flag in hardware control mode / GPO in 2-wire software control mode. See note 2.
10	RESETB	Digital Input	System reset (active low)
11	PVDD	Supply	PLL core supply
12	PGND	Supply	PLL ground
13	CLKOUT	Digital Out	High drive clock output at 64fs, 128fs, 256fs and 512fs
14	XOP	Digital Output	Crystal output
15	XIN	Digital Input	Crystal input
16	DOUT	Digital Out	Audio interface data output
17	DIN	Digital In	Audio interface data input
18	BCLK	Digital In/Out	Audio interface bit clock
19	LRCLK	Digital In/Out	Audio interface left/right word clock
20	MCLK	Digital In/Out	Master clock input or output
21	TX0	Digital Out	S/PDIF transmit
22	RX7 / GPO6	Digital In/Out	S/PDIF receive channel 7 or general purpose digital output
23	RX6 / GPO5	Digital In/Out	S/PDIF receive channel 6 or general purpose digital output
24	RX5 / GPO4	Digital In/Out	S/PDIF receive channel 5 or general purpose digital output
25	RX4 / GPO3	Digital In/Out	S/PDIF receive channel 4 or general purpose digital output
26	RX3	Digital In	S/PDIF receive channel 3
27	RX2	Digital In	S/PDIF receive channel 2
28	DGND	Supply	Digital ground

Notes:

1. Digital input pins have Schmitt trigger input buffers.
2. Refer to Table 6 Device Configuration at Power up or Hardware Reset

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital core and I/O buffer supply voltage	-0.3V	+5V
PLL supply voltage	-0.3V	+5V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature	-65°C	+150°C

Note:

1. PLL and digital supplies must always be within 0.3V of each other.
2. PLL and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Ground	DGND			0		V
PLL supply range	PVDD		2.7		3.6	V
Ground	PGND			0		V

Note:

1. PLL and digital supplies must always be within 0.3V of each other.
2. PLL and digital grounds must always be within 0.3V of each other.

SUPPLY CURRENT

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply current	I_{DVDD}	DVDD = 3.3V		14.9		mA
PLL supply current	I_{PVDD}	PVDD = 3.3V		1.7		mA
Power consumption		DVDD/PVDD = 3.3V		54.8		mW
Standby Power consumption		DVDD/PVDD = 3.3V Device powered down		0.11		mW

ELECTRICAL CHARACTERISTICS

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Jitter Characteristics						
Intrinsic Period Jitter	J_i			50		ps
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DVDD	V
Input HIGH level	V_{IH}		0.7 x DVDD			V
Output LOW	V_{OL}				0.1 x DVDD	V
Output HIGH	V_{OH}		0.9 x DVDD			V
CLOCKOUT buffer drive capability	I_{source}	CMOS 20pF load	25			mA
	I_{sink}		25			mA
S/PDIF Receiver Characteristics						
Input Resistance				23		kΩ

MASTER CLOCK TIMING

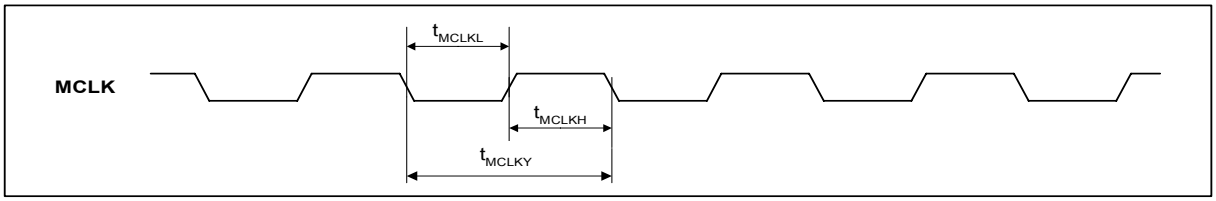


Figure 1 Master Clock Timing Requirements

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information – Slave Mode						
MCLK System clock cycle time	t_{MCLKY}		27			ns
MCLK System clock pulse width high	t_{MCLKH}		11			ns
MCLK System clock pulse width low	t_{MLCKL}		11			ns
MCLK Duty cycle			40:60		60:40	%

Table 1 Slave Mode MCLK Timing Requirements

DIGITAL AUDIO INTERFACE – MASTER MODE

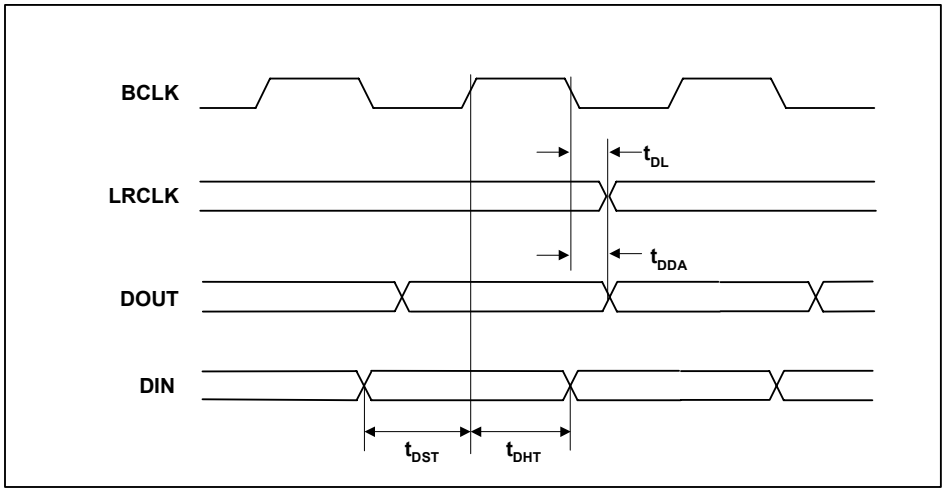


Figure 2 Digital Audio Data Timing – Master Mode

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
LRCLK propagation delay from BCLK falling edge	t_{DL}		0		10	ns
DOUT propagation delay from BCLK falling edge	t_{DDA}		0		10	ns
DIN setup time to BCLK rising edge	t_{DST}		10			ns
DIN hold time from BCLK rising edge	t_{DHT}		10			ns

Table 2 Digital Audio Data Timing – Master Mode

DIGITAL AUDIO INTERFACE – SLAVE MODE

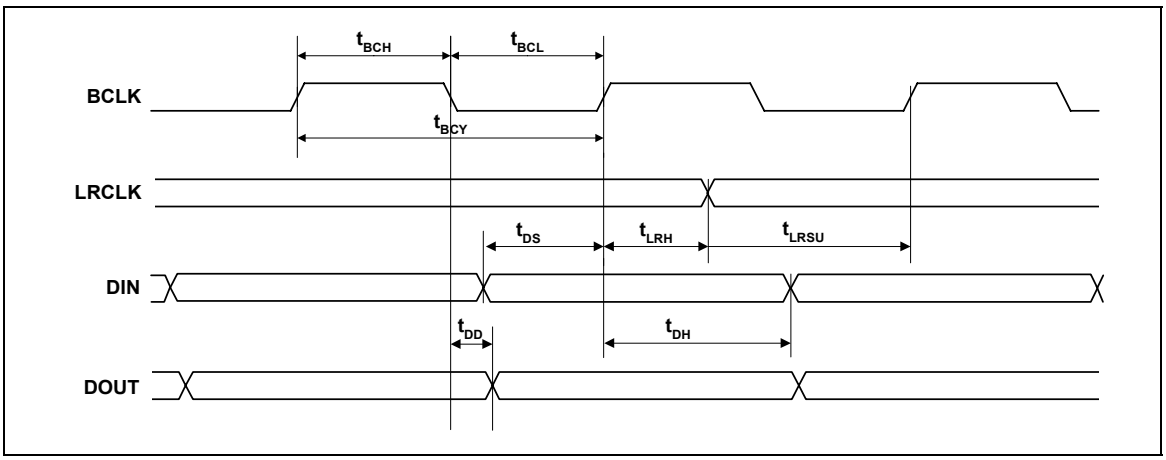


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}		10			ns
LRCLK hold time from BCLK rising edge	t_{LRH}		10			ns
DIN set-up time to BCLK rising edge	t_{DS}		10			ns
DIN hold time from BCLK rising edge	t_{DH}		10			ns
DOUT propagation delay from BCLK falling edge	t_{DD}		0		10	ns

Table 3 Digital Audio Data Timing – Slave Mode

CONTROL INTERFACE – 3-WIRE MODE

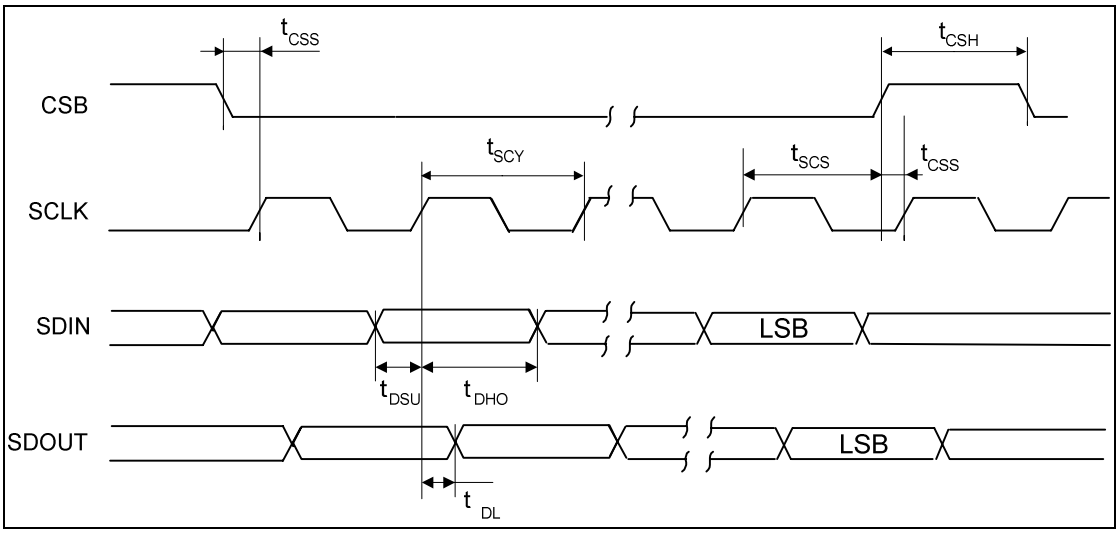


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	60			ns
SCLK cycle time	t_{SCY}	80			ns
SCLK duty cycle		40/60		60/40	%
SDIN to SCLK set-up time	t_{DSU}	20			ns
SDIN hold time from SCLK rising edge	t_{DHO}	20			ns
SDOUT propagation delay from SCLK rising edge	t_{DL}			5	ns
CSB pulse width high	t_{CSH}	20			ns
CSB rising/falling to SCLK rising	t_{CSS}	20			ns
SCLK glitch suppression	t_{ps}	2		8	ns

Table 4 Control Interface Timing – 3-Wire Serial Control Mode

CONTROL INTERFACE – 2-WIRE MODE

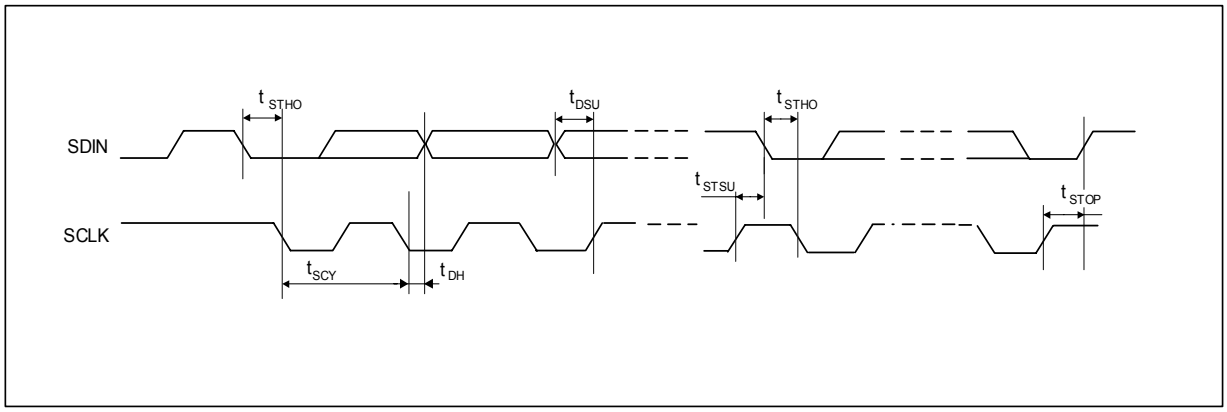


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK cycle time	t_{SCY}	2500			ns
SCLK duty cycle		40/60		60/40	%
SCLK frequency				400	kHz
Hold Time (Start Condition)	t_{STHO}	600			ns
Setup Time (Start Condition)	t_{STSU}	600			ns
Data Setup Time	t_{DSU}	100			ns
SDIN, SCLK Rise Time				300	ns
SDIN, SCLK Fall Time				300	ns
Setup Time (Stop Condition)	t_{STOP}	600			ns
Data Hold Time	t_{DHO}			900	ns
SCLK glitch suppression	t_{ps}	2		8	ns

Table 5 Control Interface Timing – 2-Wire Serial Control Mode

DEVICE DESCRIPTION

INTRODUCTION

FEATURES

- IEC-60958-3 compatible with 32 to 192k frames/s support.
- Supports AES-3 data frames.
- Support for reception and transmission of S/PDIF data.
- Clock synthesis PLL with reference clock input and low jitter output.
- Supports input reference clock frequencies from 10MHz to 27MHz.
- Dedicated high drive clock output pin.
- Register controlled channel status bit configuration.
- Register read-back of recovered channel status bits and error flags.
- Detection of non-audio data, sample rate and de-emphasis.
- Programmable GPOs for error flags and frame status flags.

The WM8805 is an IEC-60958 compatible S/PDIF transceiver with support for up to eight received S/PDIF data streams and one transmitted S/PDIF data stream.

The receiver performs data and clock recovery, and transmits recovered data from the chip either through the digital audio interface or, alternatively, the device can loop the received S/PDIF data back out through the S/PDIF transmitter producing a de-jittered S/PDIF transmit data stream. The recovered clock may be routed to a high drive output pin for external use. If there is no S/PDIF input data stream the PLL can be configured to output all standard MCLK frequencies or it can be configured to maintain the frequency of the last received S/PDIF data stream.

The transmitter generates S/PDIF frames where audio data may be sourced from the S/PDIF receiver or the digital audio interface. Timing for the S/PDIF transmitter interface can be sourced from the internally derived MCLK in loop through mode or it can be taken from an external source.

S/PDIF FORMAT

S/PDIF is a serial, bi-phase-mark encoded data stream. An S/PDIF frame consists of two sub-frames. Each sub-frame is made up of:

- Preamble – a synchronization pattern used to identify the start of a 192-frame block or sub-frame
- 4-bit Auxiliary Data (AUX) – ordered LSB to MSB
- 20-bit Audio Data (24-bit when combined with AUX) – ordered LSB to MSB
- Validity Bit – a 1 indicates invalid data in the associated sub-frame
- User Bit – over 192-frames, this forms a User Data Block
- Channel Bit – over 192-frames, this forms a Channel Status Block
- Parity Bit – used to maintain even parity over the sub-frame (not including the preamble)

An S/PDIF Block consists of 192 frames. Channel and user blocks are incorporated within the 192-frame S/PDIF Block. For Consumer mode only the first 40-frames are used to make up the Channel and User blocks. Figure 6 illustrates the S/PDIF format. The WM8805 does not support transmission of user channel data. Received user channel data may be accessed via GPO pins.

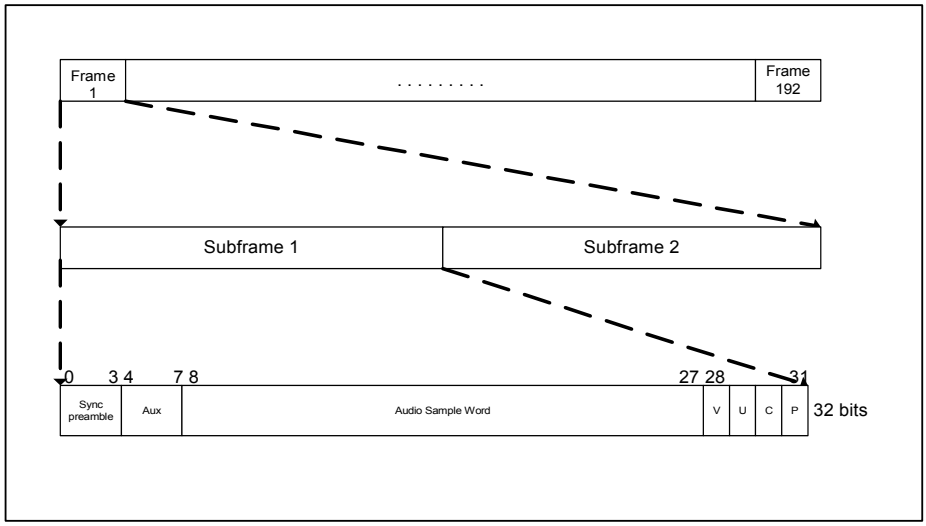


Figure 6 S/PDIF Format

POWER UP CONFIGURATION

The operating mode of the WM8805 is dependent upon the state of SDIN, SCLK, SDOUT, CSB and GPO0 when the device is powered up or a hardware reset occurs. Table 6 summarises the configuration options.

		HW RESET = 0			HW RESET = 1		
		SWMODE		HWMODE	SWMODE		HWMODE
PIN	SDIN	HWMODE / SWMODE Select			SDIN		N/A
	SCLK	N/A		AIF_MS	SCLK		GPO (TRANS_ERR)
	SDOUT	N/A		AIF_CONF[0]	2-wire	3-wire	GPO (NON_AUDIO)
					GPO	SDOUT	
	CSB	2-wire	3-wire	TXSRC	2-wire	3-wire	GPO
		Device Address	N/A		GPO	CSB	(UNLOCK)
	GPO0	2-wire/3-wire Mode Select		AIF_CONF[1]	GPO		GPO (GEN_FLAG)

Note: AIF_CONF[1:0] configures the audio interface when the device operates in hardware mode. Refer to Table 16 for description of modes.

Table 6 Device Configuration at Power up or Hardware Reset

When the device powers up, all power up configuration pins are configured as inputs for a minimum of 9.4us and a maximum of 25.6us following the release of the external reset. The times are based on 27MHz and 10MHz crystal clock frequencies respectively. This enables the pins to be sampled and the device to be configured before the pins are released to their selected operating conditions. Figure 7 illustrates how SDIN is sampled.

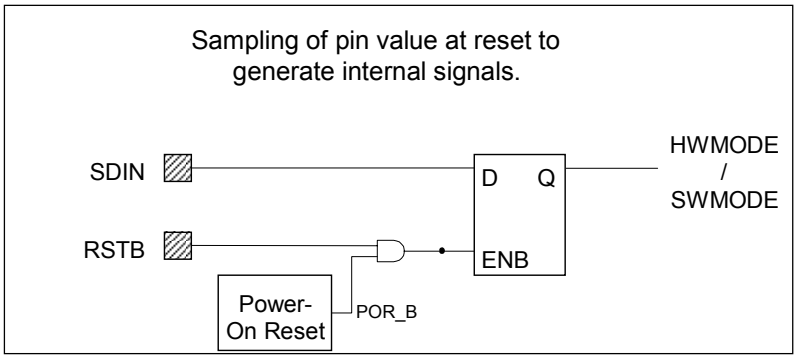


Figure 7 Pin Sampling On Power Up or Hardware Reset

If the device is powered up in Software control mode, all functions of the device are powered down by default and must be powered up individually by writing to the relevant bits of the PWRDN register (Table 7). In Hardware Control Mode, all functions of the device are powered up by default.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 PWRDN 1Eh	0	PLLPD	1	**PLL Powerdown** 0 = PLL enabled 1 = PLL disabled
	1	SPDIFRXPD	1	**S/PDIF Receiver Powerdown** 0 = S/PDIF receiver enabled 1 = S/PDIF receiver disabled
	2	SPDIFTXPD	1	**S/PDIF Transmitter Powerdown** 0 = S/PDIF transmitter enabled 1 = S/PDIF transmitter disabled
	3	OSCPD	0	**Oscillator Power Down** 0 = Power Up 1 = Power Down
	4	AIFPD	0	**Digital Audio Interface Power Down** 0 = Power Up 1= Power Down
	5	TRIOP	0	**Tri-state all Outputs** 0 = Outputs not tri-stated 1 = Outputs tri-stated

Table 7 Power Down Register

CONTROL INTERFACE OPERATION

Control of the WM8805 is implemented in either hardware control mode or software control mode. The method of control is determined by sampling the state of the SDIN/HWMODE pin at power up or at a hardware reset. If SDIN/HWMODE is low during power up the device is configured in hardware control mode, otherwise the device is configured in software control mode.

SDIN/HWMODE	
0	Hardware mode
1	Software mode

Table 8 Hardware or Software Mode Select

Software control is achieved using a 3-wire (3-wire write, 4-wire read) or a 2-wire serial interface.

The serial interface format is configured by sampling the state of the GPO0/SWIFMODE pin on power up or at a hardware reset. If the GPO0/SWIFMODE pin is low the interface is configured in 2-wire mode, otherwise the interface is configured in 3-wire SPI compatible mode.

GPO0/SWIFMODE	
0	2-wire interface
1	3-wire interface

Table 9 Software Mode Control Interface Select

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE – REGISTER WRITE

SDIN is used for the program data, SCLK is used to clock in the program data and CSB is used to latch in the program data. SDIN is sampled on the rising edge of SCLK. The 3-wire interface write protocol is shown in Figure 8.

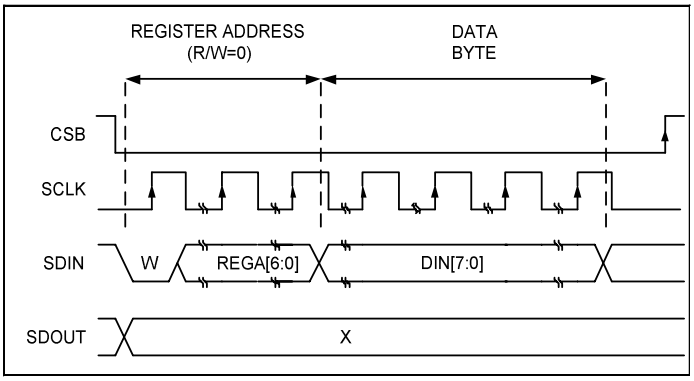


Figure 8 3-Wire Serial Interface Register Write Protocol

- W is a control bit indicating a read or write operation. 0 =write operation, 1 = read operation
- REGA[6:0] is the register Address.
- DIN[7:0] is the data to be written to the register being addressed.
- CSB is edge sensitive – the data is latched on the rising edge of CSB.

3-WIRE SERIAL CONTROL MODE REGISTER READ-BACK

Not all registers can be read. Only the device ID (registers R0, R1 and R2) and the status registers can be read. These status registers are labelled as “read only” in the Register Map section.

The read-only status registers can be read back via the SDOUT pin. The registers can be read by one of two methods, selected by the CONT register bit and the ‘W’ control bit. The oscillator must be powered up before 3-wire control interface read-back is possible.

When CONT =1 and ‘W’=0, a single read-only register can be read back by writing to any other register or to a dummy register. The register to be read is determined by the READMUX[2:0] bits. When a write to the device is performed, the device will respond by returning the status byte of the register selected by the READMUX register bits. The data is returned on the SDOUT pin. This 3-wire interface read-back method using a write access is shown in Figure 9.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 SPDRX1 1Dh	2:0	READMUX [2:0]	000	**Status Register Select** Determines which status register is to be read back: 000 = Interrupt Status Register 001 = Channel Status Register 1 010 = Channel Status Register 2 011 = Channel Status Register 3 100 = Channel Status Register 4 101 = Channel Status Register 5 110 = S/PDIF Status Register
	3	CONT	0	**Continuous Read Enable** 0 = Continuous read-back mode disabled 1 = Continuous read-back mode enabled

Table 10 Read-back Control Register

The SDOUT pin is tri-state unless CSB is held low; therefore CSB must be held low for the duration of the read.

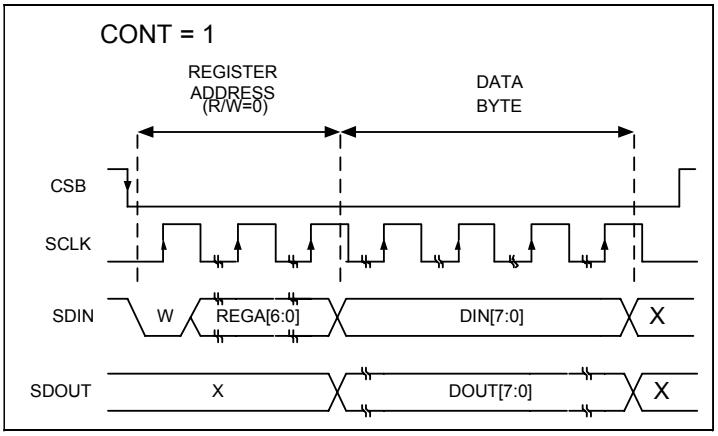


Figure 9 3-Wire Control Interface Read-Back Method 1

The second method of reading the read only status registers is If CONT=0 and ‘W’=1. Using this method the user can read back directly from a register by reading the register address. The device will respond with the contents of the register. The protocol for this read-back method is shown in Figure 10.

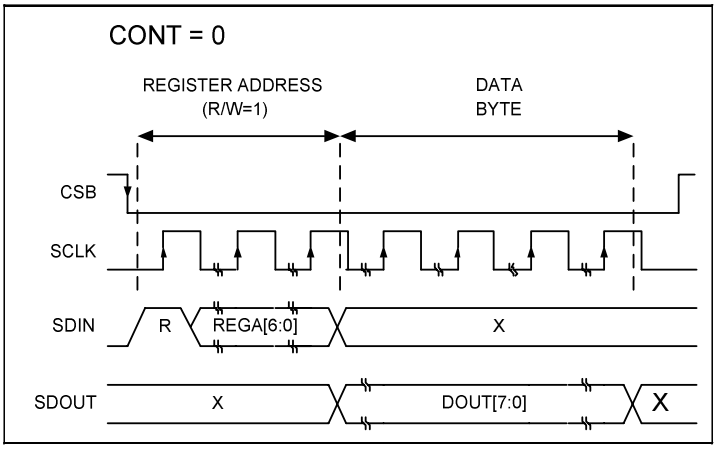


Figure 10 3-Wire Control Interface Read-Back Method 2

2-WIRE SERIAL CONTROL WITH READ-BACK MODE

The WM8805 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus and each device has a unique 7-bit address (see Table 11).

The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address, DEVA(7:1), and data, REG(6:0), will follow. All devices on the 2-wire bus will shift in the next eight bits on SDIN (7-bit address DEVA(7:1), + read/write 'W' bit, MSB first). If the device address received matches the address of the WM8805, the WM8805 responds by driving SDIN low on the next clock pulse (ACK). This is a device acknowledgement of an address match. If the address does not match that of the WM8805, the device returns to the idle condition and waits for a new start condition and valid address.

Once the WM8805 has acknowledged a matching address, the controller sends the first byte of control data, which is the WM8805 register address (REGA[6:0]). The WM8805 then acknowledges reception of the control data byte by pulling SDIN low for one clock pulse (another ACK). The controller then sends the second byte of control data (DIN[7:0], i.e. the eight bits of register data to be written), and the WM8805 acknowledges again by pulling SDIN low (another ACK).

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8805 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device returns to the idle condition.

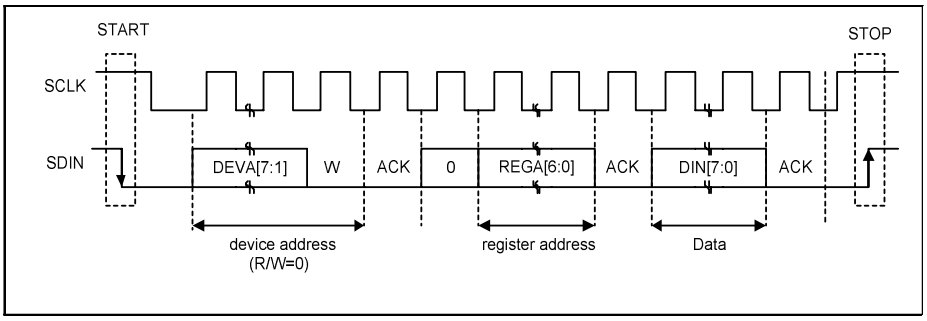


Figure 11 2-Wire Serial Control Interface Write

Multiple consecutive register writes can be performed in 2-wire control mode by setting the CONT bit high. This method allows the entire register map to be defined in a one continuous write operation.

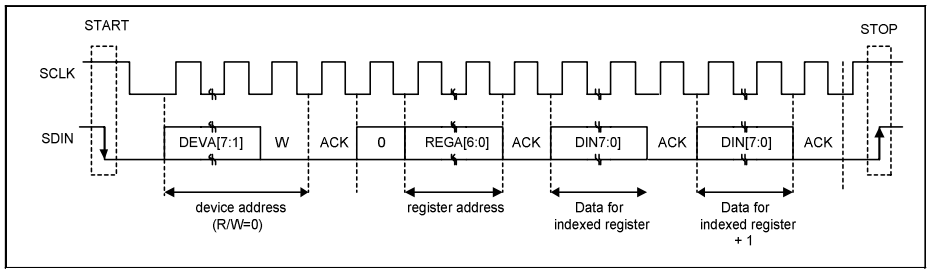


Figure 12 2-Wire Serial Control Interface Multi-Write

The WM8805 has two possible device addresses, which can be selected using the CSB pin during hardware reset.

CSB STATE	DEVICE ADDRESS IN 2-WIRE MODE	ADDRESS (X=R/W BIT)	
		X=0	X= 1
Low	0111010x	0x7A	0x75
High	0111011x	0x76	0x77

Table 11 2-Wire Interface Address Selection

2-WIRE SERIAL CONTROL MODE -REGISTER READ-BACK

The WM8805 allows read-back of certain registers in 2-wire mode. The protocol is similar to that used to write to the device. The controller will issue the device address followed by a write bit, the register index will then be passed to the WM8805. At this point the controller will issue a repeated start condition and resend the device address along with a read bit. The WM8805 will acknowledge this and the WM8805 will become a slave transmitter. The WM8805 will transmit the data from the indexed register on SDIN MSB first. When the controller receives the data it will not acknowledge receipt of the data indicating that it will resume master transmitter control of SDIN. The controller will then issue a stop command completing the read cycle. Figure 13 illustrates the read protocol.

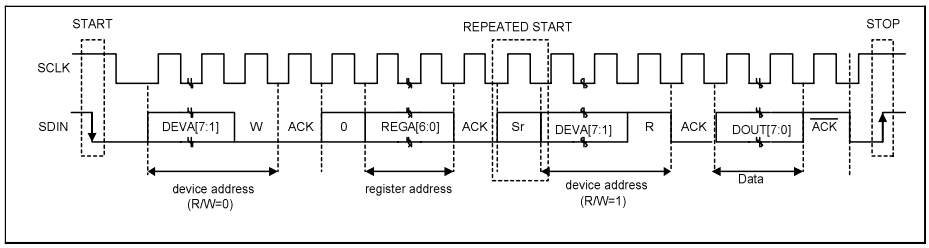


Figure 13 2-Wire Serial Control Interface Read (CONT=0)

2-WIRE SERIAL CONTROL MODE – CONTINUOUS READ-BACK

As in 3-wire mode, there are two methods of reading back data: continuous and non-continuous read-back. Continuous read-back is selected by setting CONT to 1. In continuous read-back mode, the device will return the indexed register first followed by consecutive registers in increasing index order until the controller does not acknowledge the data then issues a stop sequence. This is shown in Figure 14

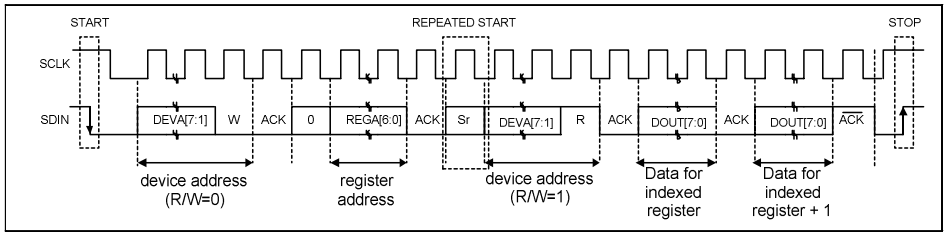


Figure 14 2-Wire Serial Interface Continuous Read-Back (CONT=1)

SOFTWARE REGISTER RESET

Writing to register 0000000 will reset the WM8805. This will reset all register bits to their default values. Note that the WM8805 is powered down by default so writing to this register will power down the device.

DEVICE ID AND REVISION IDENTIFICATION

Registers 0,1 and 2 can be read to identify the device ID and IC revision number. Refer to Table 12 for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R00 RST/DEVID1 00h	7:0	RESET	N/A	Writing to this register will apply a reset to the device.
		DEVID1[7:0]	00000101	Reading from this register will return the second part of the device ID 00000101 = 0x05
R01 DEVID2 01h (read only)	7:0	DEVID2[7:0]	10001000	Reading from this register will return the first part of the device ID 10001000 = 0x88
R02 DEVREV 02h	3:0	DEVREV [3:0]	N/A	Reading from this register will return the device revision. 0x1 = revision 1

Table 12 Software Reset Register and Device ID

HARDWARE CONTROL MODE

The WM8805 can be operated in either software or hardware control modes. The method of control is determined by sampling the state of the SDIN pin during power up or hard reset. If SDIN is LOW during power up or hardware reset, the WM8805 will be switched into hardware control mode.

PIN	0	1
SDIN	Hardware Control Mode	Software Control Mode

Table 13 Hardware / Software Mode Configuration

In hardware control mode the user has limited control over the configuration of the device. Most of the features will assume default values but some can be configured using external pins. When the device is configured in hardware control mode, all functions of the device are powered up.

The clock and data recovery module with the WM8805 will require a 12 MHz crystal derived master clock as the default values for this module cannot be altered in Hardware Control mode.

MASTER / SLAVE MODE SELECTION

The WM8805 can be configured in either master or slave mode In software control mode this is set by writing to AIF_MS in the AIFRX register. In hardware control mode this is controlled by sampling the SCLK pin on power up or hardware reset.

PIN (HARDWARE MODE)	REGISTER (SOFTWARE MODE)	0	1
SCLK	AIF_MS	Slave Mode	Master Mode

Table 14 Master / Slave Mode Configuration in Hardware Mode

DIGITAL ROUTING CONTROL

See page 20 for a full description of the signal routing options available in the WM8805. In Software control mode the values set in registers TXSRC and RXINSEL determine the S/PDIF Rx data source and destination. In hardware control mode the device can receive data only from RX0 but can set the value of TXSRC directly using the CSB pin. This determines the S/PDIF transmitter data source

PIN (HARDWARE MODE)	REGISTER (SOFTWARE MODE)	0	1
CSB	TXSRC	S/PDIF Rx	AIF Rx

Table 15 S/PDIF Transmitter Digital Routing Control Configuration

AUDIO INTERFACE CONTROL

In software control mode the audio data word length and audio data format can be set independently for the receiver and transmitter sides of the interface. However, in hardware control mode both sides of the interface are combined and the configuration is set using SDOUT and GPO0 pins as described in Table 6 and Table 16. Note that AIF_CONF[1:0] configures the audio interface when the device operates in hardware mode.

GPO0 / AIFCONF[1]	SDOUT / AIFCONF[0]	DESCRIPTION
0	0	16-bit I^2S
0	1	24-bit I^2S
1	0	24-bit Left Justified With Flags
1	1	16-bit Right Justified

Table 16 Digital Audio Interface Control in Hardware Control Mode

STATUS INFORMATION

In hardware control mode the WM8805 outputs a selection of status flags for the user. Table 17 describes the flags which are available and the output pins on which they are available.

PIN	STATUS FLAG
SCLK	TRANS_ERR
SDOUT	NON_AUDIO
CSB	UNLOCK
GPO0	GEN_FLAG

Table 17 Hardware Control Mode Status Flag Configuration

A full description of the status flags is given in Table 45.

DIGITAL ROUTING CONTROL

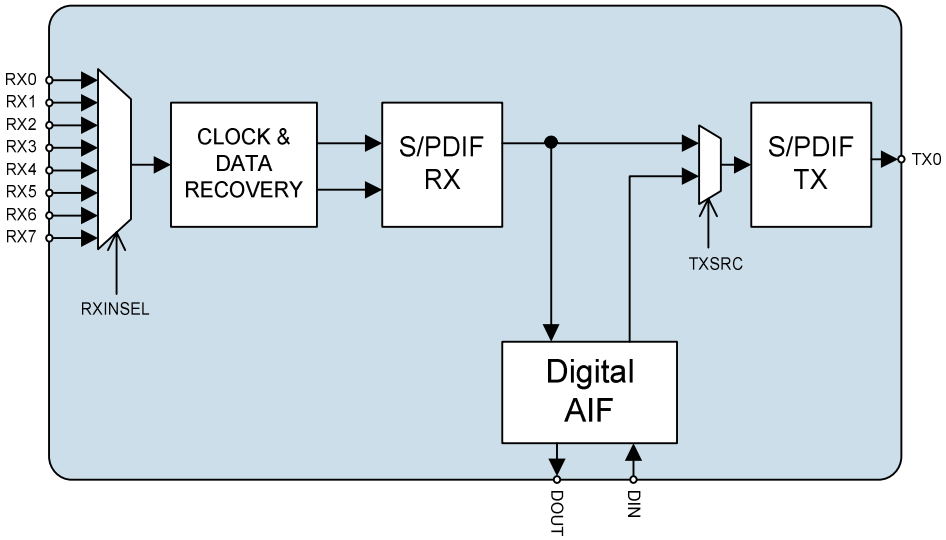


Figure 15 Digital Routing Paths within the WM8805

Digital signal routing within the WM8805 is controlled by two registers, RXINSEL and TXSRC. RXINSEL selects the S/PDIF input which is passed through the clock and data recovery circuit to the S/PDIF receiver and TXSRC selects the data source that is passed to the S/PDIF transmitter.

In order to ensure proper operation when changing TXSRC, the S/PDIF transmitter module should be powered down prior to changing the TXSRC control register and powered up again once the routing path has been changed.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 PLL6 08h	2:0	RXINSEL[2:0]	000	**S/PDIF Rx Input Select** Select the S/PDIF input to pass to the receiver circuit. 000 – RX0 001 – RX1 010 – RX2 011 – RX3 100 – RX4 101 – RX5 110 – RX6 111 – RX7
R30 PWRDN 1Eh	2	SPDIFTXPD	1	**S/PDIF Transmitter Powerdown** 0 = S/PDIF transmitter enabled 1 = S/PDIF transmitter disabled
R21 SPDTX4 15h	6	TXSRC	1	**S/PDIF Transmitter Data Source** 0 = S/PDIF Received Data – SPDIFTXCLK Source = CLK2 1 = Digital Audio Interface Received Data – SPDIFTXCLK Source = MCLK Input/Output Signal at MCLK Pin

Table 18 Digital Signal Routing Control Registers

MASTER CLOCK AND PHASE LOCKED LOOP

SOFTWARE MODE INTERNAL CLOCKING

The WM8805 is equipped with a comprehensive clocking scheme that provides maximum flexibility and function and many configurable routing possibilities for the user in software mode. An overview of the software mode clocking scheme is shown in Figure 16.

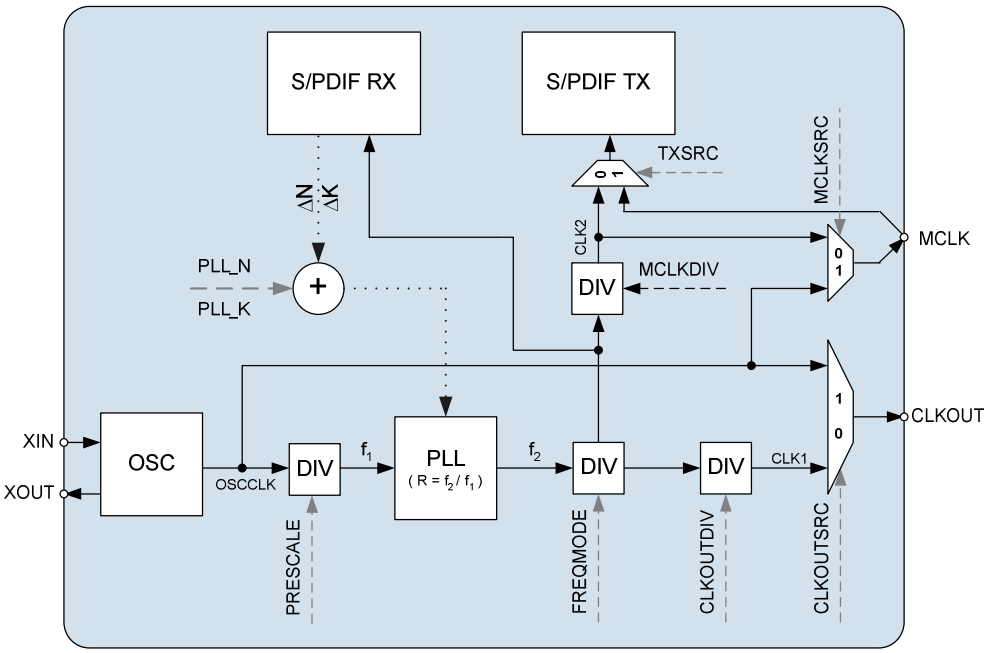


Figure 16 Software Mode Clocking Scheme Overview

The clocking scheme can be divided into four sections. These are detailed as follows:

OSCILLATOR

The primary function of the oscillator is to generate the oscillator clock (OSCCLK) for the PLL input. Whenever the PLL or the S/PDIF receiver is enabled, the oscillator must be used to generate the OSCCLK signal for the PLL.

The secondary function of the oscillator is to generate the OSCCLK so that it can be selected internally as the clock source for:

- The MCLK output pin, when the pin is configured as an output.
- The CLKOUT output pin, when enabled.

The oscillator has one control bit as shown in Table 19. The oscillator must be powered up to generate the OSCCLK signal.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 PWRDN 1Eh	3	OSCPD	1	**Oscillator Power Down Control** 0 = Power up 1 = Power down

Table 19 Oscillator Control

The oscillator uses a Pierce type oscillator drive circuit. This circuit requires an external crystal and appropriate external loading capacitors. The oscillator circuit contains a bias generator within the WM8805 and hence an external bias resistor is not required. Crystal frequencies between 10 and 14.4MHz or 16.28 and 27MHz can be used in software mode. The recommended circuit is shown in the recommended components diagram, please refer to Figure 29.

Alternatively, an external CMOS compatible clock signal can be applied to the XIN pin in the absence of a crystal, although this is not recommended when using the PLL as the PLL requires a jitter-free OSCCLK signal for optimum performance.

PHASE-LOCKED LOOP (PLL)

The WM8805 has an on-chip phase-locked loop (PLL) circuit that can be used to synthesise clock signals from the external oscillator clock. The PLL can be used to:

- Generate clocks necessary for the S/PDIF receiver to lock on to and recover S/PDIF data from an incoming S/PDIF data stream.
- Generate clocks which may be used to drive the MCLK and/or CLKOUT pins.
- Generate clocks which may be used by the S/PDIF transmitter to encode and transmit a S/PDIF data stream.

The PLL can be enabled or disabled using the PLLPD register bit as shown in Table 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 PWRDN 1Eh	0	PLLPD	1	**PLL Power Down Control** 0 = Power up PLL 1 = Power down PLL

Table 20 PLL Power Down Control

The PLL has two modes of operation:

- **S/PDIF Receive Mode (Automatic PLL Mode – Selected if S/PDIF Receiver Enabled)**

In S/PDIF receive mode, the PLL is automatically controlled by the S/PDIF receiver to allow the receiver to use the PLL to lock on to and track the incoming S/PDIF data stream.

Please refer to the S/PDIF Receiver section within the Internal Clocking description for full details.

If the CLKOUT or MCLK clocks are sourced from either CLK1 or CLK2 in this mode, the frequency of these signals will be modified based on the clock rate of the incoming S/PDIF data stream. If the sample rate of the incoming stream is changed, the MCLK and CLKOUT signals will continue to be output, but will not be valid until the S/PDIF receiver has locked to the incoming stream at the new sample rate. If the incoming S/PDIF stream stops, the PLL N and K values will be frozen and the output clocks will continue at the frequency set by the last recovered S/PDIF stream. If the S/PDIF input stream is removed then it is possible for the PLL to detect small pulse as the data is being removed. This may result in the output clocks changing to an invalid frequency. Note also that if the device is power-on and configured with no S/PDIF input data stream, then the PLL will default to approximately 24MHz.

- **User Mode (Manual PLL Mode – Selected if S/PDIF Receiver Disabled)**

In user mode, the user has full control over the PLL function and operation. In this mode, the user can accurately specify the PLL N and K multiplier values (using the PLL_N and PLL_K registers), divider values (PRESCALE and FREQMODE) and can hence control the generated CLK1 and CLK2 frequencies. Refer to Table 21 for details of the registers available for configuration in this mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 PLL1 03h	7:0	PLL_K[7:0]	00100001	Fractional (K) part of PLL frequency ratio (R). Value K is one 22-digit binary number spread over registers R3, R4 and R5 as shown. **Note: PLL_K must be set to specific values when the S/PDIF receiver is used. Refer to S/PDIF Receiver clocking section for details.**
R4 PLL2 04h	7:0	PLL_K[15:8]	11111101	
R5 PLL3 05h	5:0	PLL_K[21:16]	00110110	
R6 PLL4 06h	3:0	PLL_N[3:0]	0111	Integer (N) part of PLL frequency ratio (R). Use values in the range 5 ≤ PLL_N ≤ 13 as close as possible to 8 **Note: PLL_N must be set to specific values when the S/PDIF receiver is used. Refer to S/PDIF Receiver clocking section for details.**

Table 21 User Mode PLL_K and PLL_N Multiplier Control

PLL CONFIGURATION

The PLL performs a configurable frequency multiplication of the input clock signal (f_1). The multiplication factor of the PLL (denoted by 'R') is variable and is defined by the relationship: $R = (f_2 \div f_1)$.

The multiplication factor is set using register bits PLL_N and PLL_K (refer to Table 21). The multiplication effect of both the N and K multipliers are additive (i.e. if N is configured to provide a multiplication factor of 8 and K is configured to provide a multiplication factor of 0.192, the overall multiplication factor is 8 + 0.192 = 8.192).

In order to choose and configure the correct values for PLL_N and PLL_K, multiplication factor R must first be calculated. Once value R is calculated, the value of PLL_N is the integer (whole number) value of R, ignoring all digits to the right of the decimal point. For example, if R is calculated to be 8.196523, PLL_N is simply 8.

Once PLL_N is calculated, the PLL_K value is simply the integer value of (2^{22} (R-PLL_N)). For example, if R is 8.196523 and PLL_N is 8, PLL_K is therefore (2^{22} (8.196523-8)), which is 824277 (ignoring all digits to the right of the decimal point).

Note: the PLL is designed to operate with best performance (shortest lock time and optimum stability) when f_2 is between 90 and 100MHz and PLL_N is 8. However, acceptable PLL_N values lie in the range 5 ≤ PLL_N ≤ 13. Do not use values outwith this range and it is recommended that the chosen value of PLL_N is as close to 8 as possible for optimum performance.

An output divider is provided to allow the f_2 clock signal to be divided to a frequency suitable for use as the source for the MCLK, CLKOUT or S/PDIF transmitter. The divider output is configurable and is set by the FREQMODE bits. The PLL is also equipped with a pre-scale divider which offers frequency divide by one or two before the OSCCLK signal is fed to the PLL. Please refer to Table 22 for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 PLL4 06h	4	PRESCALE	0	**PLL Pre-scale Divider Select** 0 = Divide by 1 (PLL input clock = oscillator clock) 1 = Divide by 2 (PLL input clock = oscillator clock ÷ 2)
R7 PLL5 07h	1:0	FREQMODE[1:0]	10	**PLL Post-scale Divider Select** Selects the PLL output divider value in conjunction with MCLKDIV and CLKOUTDIV. Refer to Table 23 for details of FREQMODE operation. **Note: FREQMODE[1:0] bits are automatically set in S/PDIF Receive Mode.**

Table 22 Pre and Post PLL Clock Divider Control

PLL CONFIGURATION EXAMPLE

Consider the situation where the oscillator clock (OSCCLK) input frequency is fixed at 12MHz and the required MCLK frequency is 12.288MHz.

1. Calculate the f_2, FREQMODE and MCLKDIV Values

The PLL is designed to operate with best performance when the f_2 clock is between 90 and 100MHz. The necessary MCLK frequency is 12.288MHz. Choose MCLKDIV and FREQMODE values to set the f_2 frequency in the range of 90 to 100MHz. In this case, the default values (MCLKDIV = 0 and FREQMODE[1:0] = 10) will set the f_2 frequency at 98.304MHz; this value is within the 90 to 100MHz range and is hence acceptable.

- MCLKDIV = 0
- FREQMODE[1:0] = 10
- f_2 = 98.304MHz

2. Calculate R Value

Using the relationship: R = ($f_2 \div f_1$), the value of R can be calculated.

- R = ($f_2 \div f_1$)
- R = (98.304 ÷ 12)
- R = 8.192

3. Calculate PLL_N Value

The value of PLL_N is the integer (whole number) value of R, ignoring all digits to the right of the decimal point. In this case, R is 8.192, hence PLL_N is 8.

4. Calculate PLL_K Value

The PLL_K value is simply the integer value of (2^{22} (R-PLL_N)).

- PLL_K = integer part of (2^{22} x (8.192 – 8))
- PLL_K = integer part of 805306.368
- PLL_K = 805306 (decimal) / C49BA (hex)

A number of example configurations are shown in Table 23. Many other configurations are possible; Table 23 shows only a small number of valid possibilities.

OSC CLK (MHz)	PRE-SCALE	F_1 (MHz)	F_2 (MHz)	R	PLL_N (Hex)	PLL_K (Hex)	FREQ MODE [1:0]	MCLK DIV	MCLK (MHz)	CLKOUT DIV [1:0]	CLK OUT (MHz)
12	0	12	98.304	8.192	8	C49BA	00	1	24.576	01	49.152
12	0	12	98.304	8.192	8	C49BA	10	0	12.288	00	24.576
12	0	12	98.304	8.192	8	C49BA	10	1	6.144	01	12.288
12	0	12	98.304	8.192	8	C49BA	10	0	12.288	10	6.144
12	0	12	98.304	8.192	8	C49BA	10	1	6.144	11	3.072
24	1	12	90.3168	7.5264	7	21B089	01	0	22.5792	00	45.1584
24	1	12	90.3168	7.5264	7	21B089	10	0	11.2896	00	22.5792
24	1	12	90.3168	7.5264	7	21B089	10	1	5.6448	01	11.2896
24	1	12	90.3168	7.5264	7	21B089	10	0	11.2896	10	5.6448
24	1	12	90.3168	7.5264	7	21B089	10	1	5.6448	11	2.8224
27	1	13.5	98.304	7.2818	7	1208A5	10	0	12.288	01	12.288
27	1	13.5	98.304	7.2818	7	1208A5	10	1	6.144	10	6.144
27	1	13.5	90.3168	6.6901	6	2C2B24	10	0	11.2896	01	11.2896
27	1	13.5	90.3168	6.6901	6	2C2B24	10	1	5.6448	10	5.6448

Table 23 User Mode PLL Configuration Examples

When considering settings not shown in this table, the key configuration parameters which must be selected for optimum operation are:

- $90MHz \leq f_2 \leq 100MHz$
- $5 \leq PLL_N \leq 13$
- OSCCLOCK = 10 to 14.4MHz or 16.28 to 27MHz

PLL INTEGER AND FRACTIONAL CONTROL MODES

The PLL can be operated in either fractional or integer control modes. In PLL User Mode, it is recommended that the PLL should be operated in fractional control mode at all times. When the S/PDIF receiver is enabled, the PLL **must** be operated in fractional control mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 PLL5 07h	2	FRACEN	1	**Integer/Fractional PLL Mode Select** 0 = Integer PLL (PLL_N value used, PLL_K value ignored) 1 = Fractional PLL (both PLL_N and PLL_K values used) **Note: FRACEN must be set to enable the fractional PLL when using S/PDIF Receive Mode.**

Table 24 PLL Fractional/Integer Mode Select

MASTER CLOCK (MCLK)

The master clock (MCLK) signal is used to supply reference clock signals to the following circuit blocks:

- The Digital Audio Interface
- The S/PDIF Transmitter

The master clock (MCLK) pin can be configured as either a clock input or output depending on the digital audio interface mode as shown in Table 25.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 AIFRX 1Ch	6	AIF_MS	0	**Audio Interface Mode Select** 0 = Slave Mode – MCLK Input 1 = Master Mode – MCLK Output

Table 25 Audio Interface Mode Select

When MCLK is configured as an output, the MCLK source and rate can be selected using the control bits shown in Table 26. The MCLK rate select can only be used when the MCLK output source is selected as the PLL clock. If the oscillator clock is selected as the PLL source, the MCLK frequency is equal to the oscillator clock frequency.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 PLL5 07h	3	MCLKDIV	0	**MCLK Divider Select** (Only valid when CLK2 is selected as MCLK output source) See Table 27 for MCLKDIV configuration in PLL user mode. See Table 28 for MCLKDIV configuration in PLL S/PDIF receive mode.
R8 PLL6 08h	7	MCLKSRC	0	**MCLK Output Source Select** 0 = Select CLK2 1 = Select OSCCLK

Table 26 Master Clock Output Control

FREQMODE[1:0]	F_2 TO CLK1 DIVISION FACTOR				F_2 TO CLK2 DIVISION FACTOR	
	CLKOUTDIV[1:0]				MCLKDIV	
	00	**01**	**10**	**11**	**0**	**1**
00	÷2	÷2	÷4	÷8	÷2	÷4
01	÷2	÷4	÷8	÷16	÷4	÷8
10	÷4	÷8	÷16	÷32	÷8	÷16
11	÷6	÷12	÷24	÷48	÷12	÷24

Table 27 PLL User Mode Clock Divider Configuration

CLKOUTDIV[1:0]	CLK1 FREQUENCY	MCLKDIV	CLK2 FREQUENCY
00	512fs	**0**	256fs
01	256fs	**1**	128fs
10	128fs		
11	64fs		

Table 28 PLL S/PDIF Receive Mode Clock Divider Configuration

Note: The fs values shown above are relative to the S/PDIF recovered sample rate.

When MCLK is configured as an input, the reference clock rate for the S/PDIF transmitter (when the digital audio interface received data is configured as the S/PDIF transmitter data source) is controlled by the frequency of the MCLK signal at the MCLK pin.

Refer to the “Digital Audio Interface” datasheet section for details of configuring MCLK for appropriate digital audio interface operation.

CLOCK OUTPUT (CLKOUT)

The high-drive clock output (CLKOUT) pin can be used as a clock output. This pin is intended to be used as a clock source pin for providing the central clock reference for an audio system.

The CLKOUT clock source can be selected from either the OSCCLK or CLK1 signals. The control bits for the CLKOUT signal are shown in Table 29.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 PLL5 07h	5:4	CLKOUTDIV[1:0]	01	**CLKOUT Divider Select** (Only valid when CLK1 is selected as CLKOUT output source) See Table 27 for CLKOUTDIV[1:0] configuration in PLL user mode. See Table 28 for CLKOUTDIV[1:0] configuration in PLL S/PDIF receive mode.
R8 PLL6 08h	3	CLKOUTSRC	1	**CLKOUT Pin Source Select** 0 = Select CLK1 1 = Select OSCCLK
	4	CLKOUTDIS	1	**CLKOUT Pin Disable** 0 = Pin Disabled (Pin tri-stated) 1 = Pin Enabled

Table 29 Clock Output (CLKOUT) Control

S/PDIF TRANSMITTER

When the S/PDIF transmitter is enabled and configured (using TXSRC) to use the S/PDIF received data, the S/PDIF transmitter is clocked from the CLK2 signal. When the transmitter's data source is the digital audio interface, the transmitter reference clock source is the MCLK signal at the MCLK input/output pin. Refer to Table 30 for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 SPDTX4 15h	6	TXSRC	1	**S/PDIF Transmitter Data Source** 0 = S/PDIF Received Data – SPDIFTXCLK Source = CLK2 1 = Digital Audio Interface Received Data – SPDIFTXCLK Source = MCLK Input/Output Signal at MCLK Pin

Table 30 S/PDIF Transmitter Data/MCLK Source Control

The S/PDIF transmitter requires a clock reference signal (either CLK2 or MCLK) when enabled. The applied MCLK signal can be either128fs, 256fs, 384fs, 512fs, 768fs or 1152fs relative to the sample rate of the transmitted data.

S/PDIF RECEIVER

In S/PDIF receive mode, the PLL_N and PLL_K values are automatically modified by the S/PDIF receiver to allow the receiver to use the PLL to lock on to and track the incoming S/PDIF data stream.

The S/PDIF receiver has four clocking modes based on the incoming S/PDIF stream sample rate. The modes are:

- Mode 1: Incoming S/PDIF sample rate = 176.4kHz – 1% to 192kHz +1%
- Mode 2: Incoming S/PDIF sample rate = 88.2kHz -1% to 96kHz +1%
- Mode 3: Incoming S/PDIF sample rate = 44.1kHz -1% to 48kHz +1%
- Mode 4: Incoming S/PDIF sample rate = 32kHz +/- 1%

Before the S/PDIF receiver is enabled, it is important that the PLL_N and PLL_K register values are manually configured in a specific default state so that the S/PDIF receiver can correctly modify the PLL_N and PLL_K values and hence establish correct PLL control.

The PLL_N and PLL_K register values must also be manually re-configured when a change of the clocking mode is detected and the change is to mode 1 or from mode 1.

The specified f_2 frequencies that must be configured using the PLL_N and PLL_K register values for reception of specific S/PDIF sample rates are as follows:

- Mode 1 (176.4/192kHz sample rate): f_2 = **98.304MHz**
- Modes 2/3/4 (32/44.1/48/88.2/96kHz Sample Rates): f_2 = **94.3104MHz**

The FREQMODE[1:0] bits are automatically controlled by the S/PDIF receiver when the receiver is enabled and do not need to be configured in any particular initial state by the user before the S/PDIF receiver is enabled.

Refer to Table 23 and Table 28 for details of MCLKDIV and CLKOUTDIV configuration when the S/PDIF receiver is enabled.

The PLL register settings are configured by default to allow 32/44.1/48/88.2/96kHz (modes 2/3/4) sample rate S/PDIF receiver operation using a 12MHz crystal clock. The PLL register settings must be updated if:

- Any crystal clock frequency other than 12MHz is used.

  OR

- A S/PDIF stream with 192kHz sample rate (mode 1) is detected.

In either case, reprogramming of the PLL_N and PLL_K values (and the PRESCALE value, depending on the crystal frequency) is necessary.

Refer to Table 31 for details of a number of recommended PLL configurations. Many other configurations are possible; please refer to PLL Configuration section for details regarding how to calculate alternative settings.

OSC CLK (MHz)	PRE-SCALE	S/PDIF RECEIVER SAMPLE RATE(S) (kHz)	F1 (MHz)	F2 (MHz)	R	PLL_N (Hex)	PLL_K (Hex)	COMMENT
11.2896	0	32 / 44.1 / 48 / 88.2 / 96	11.2896	94.3104	8.3537	8	16A3B3	Set N, K
11.2896	0	192	11.2896	98.304	8.7075	8	2D4766	Set N, K
12	0	32 / 44.1 / 48 / 88.2 / 96	12	94.3104	7.8592	7	36FD21	Default Setting
12	0	192	12	98.304	8.192	8	C49BA	Set N, K
12.288	0	32 / 44.1 / 48 / 88.2 / 96	12.288	94.3104	7.675	7	2B3333	Set K
12.288	0	192	12.288	98.304	8	8	0	Set N, K
19.2	1	32 / 44.1 / 48 / 88.2 / 96	9.6	94.3104	9.824	9	346C6A	Set Prescale, N, K
19.2	1	192	9.6	98.304	10.24	A	F5C28	Set Prescale, N, K
24	1	32 / 44.1 / 48 / 88.2 / 96	12	94.3104	7.8592	7	36FD21	Set Prescale
24	1	192	12	98.304	8.192	8	C49BA	Set Prescale, N, K
27	1	32 / 44.1 / 48 / 88.2 / 96	13.5	94.3104	6.986	6	3F19E5	Set Prescale, N, K
27	1	192	13.5	98.304	7.2818	7	1208A5	Set Prescale, K

Table 31 S/PDIF Receive Mode PLL Initial Configuration Examples

The recommended configuration sequences are as follows:

TO INITIALLY CONFIGURE THE SYSTEM FOR S/PDIF RECEIVER STARTUP:

1. Write appropriate calculated values (relative to oscillator frequency) to PRESCALE, PLL_N and PLL_K registers for 32/44.1/48/88.2/96kHz (modes 2/3/4) S/PDIF receiver sample rate operation.
2. Enable PLL by clearing PLLPD bit.
3. Enable S/PDIF receiver by clearing SPDIFRXPD bit.
4. Read S/PDIF Status Register REC_FREQ[1:0] bits to identify recovered S/PDIF sample frequency and clocking mode.

5. If indicated sample rate is 192kHz, then the user must know what the sampling frequency is (176.4kHz or 192kHz) since these cannot be distinguished. The user should then write appropriate calculated values (relative to oscillator frequency) to PRESCALE, PLL_N and PLL_K for 176.4/192kHz (mode 1) S/PDIF receiver sample rate operation.

TO CONFIGURE THE SYSTEM WHEN CLOCKING MODE (SAMPLE RATE) CHANGES TO OR FROM MODE 1 (176.4/192KHZ):

Any sample rate change between clocking modes (for example, from 44.1kHz (mode 3) to 192kHz (mode 1)) will be flagged to the application processor via the INT_N interrupt flag. The application processor must then read the Interrupt Status Register. If the UPD_REC_FREQ flag is set, indicating that the clocking mode has changed, proceed as follows:

1. Read S/PDIF Status Register REC_FREQ[1:0] bits to identify recovered S/PDIF sample rate frequency and clocking mode. If "192kHz" is indicated then since this is indistinguishable from 176.4kHz, the user must be aware of what the sampling frequency is.

2. Write appropriate calculated values (relative to oscillator frequency) to PLL_N and PLL_K based on indicated recovered S/PDIF sample frequency and clocking mode.

This procedure is only strictly necessary when switching to or from 192kHz (mode 1) because the PLL_N and PLL_K values are the same for 32/44.1/48/88.2/96kHz (modes 2/3/4) sample rate operation. It is, however, good interrupt service routine practice to write the appropriate PLL_N and PLL_K values when every clocking mode change is detected. The setup for 176.4 kHz and 192kHz are however slightly different. The setting up of these different configurations are described in the following paragraphs.

176.4KHZ OR 192K MODE ENABLE

The difference between a sample rate of 176.4kHz and 192kHz requires the system to be configured slightly differently. This requires that the S/PDIF Rx sample rates are known (176.4kHz or 192kHz). Both sampling frequencies also require that the register bit SPD_192K_EN is set to a 1. If the SPD_192K_EN register bit is not set to a 1, then TRANS_ERR errors will be generated and this will result in the UNLOCK status being continually set (indicating an UNLOCK status).

176.4KHZ OPERATION

To operate at fs=176.4 kHz, then the PLL_K and PLL_N settings should be set up as in mode 2/3/4. In this case the the PLL will lock onto the S/PDIF Rx data stream correctly if fs=176.4kHz. If however the sample rate is changed to fs=192kHz (and the PLL is not reconfigured) then the S/PDIF Rx interface will indicate UNLOCK and TRANS_ERR. The UNLOCK signal will continually toggle between a locked and unlocked state.

192KHZ OPERATION

To operate at fs=192kHz, then the PLL_K and PLL_N settings should be set up as in mode 1. In this case the the PLL will lock onto the S/PDIF Rx data stream correctly if fs=192kHz. If however the sample rate is changed to fs=176.4kHz (and the PLL is not reconfigured) then the S/PDIF Rx interface will indicate UNLOCK and TRANS_ERR. The UNLOCK signal will continually toggle between a locked and unlocked state. Note that this is the default setting for hardware mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 SPDRX1 1Dh	7	SPD_192K_EN	1	**S/PDIF Receiver 192kHz Support Enable** 0 = disabled, S/PDIF receiver maximum supported sampling frequency is 96kHz 1 = enabled, S/PDIF receiver maximum supported sampling frequency is 192kHz

Table 32 176.4/192 kHz Sample Rate Enable

HARDWARE MODE INTERNAL CLOCKING

In hardware mode, the user has no access to the internal clocking control registers and hence a default configuration is loaded at reset to provide maximum functionality.

An overview of the hardware mode clocking scheme is shown in Figure 17.

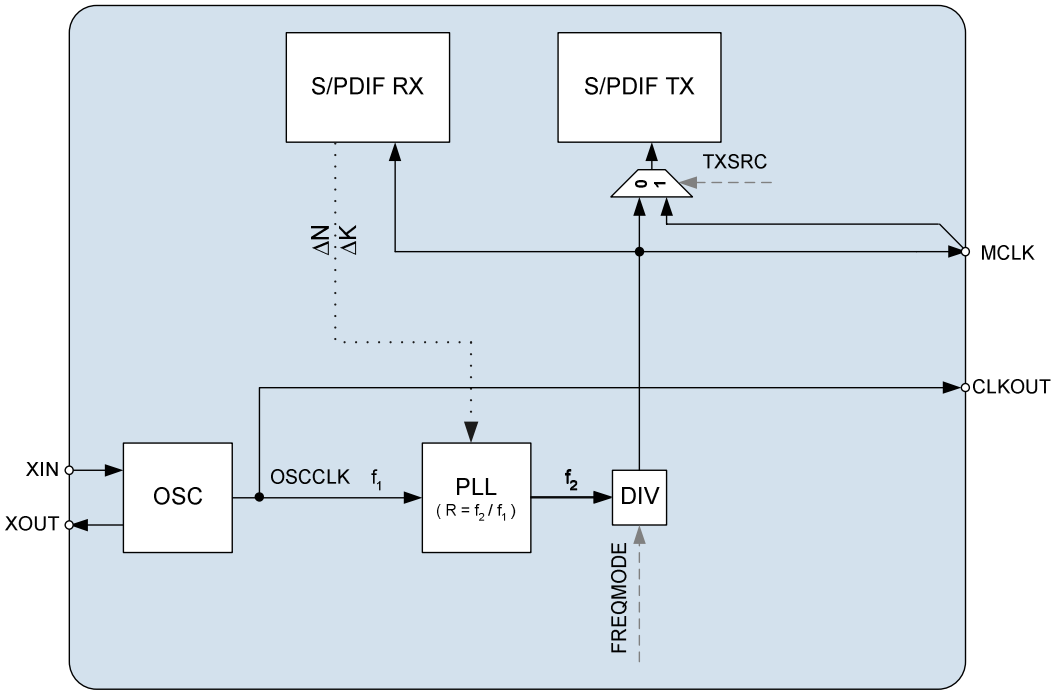


Figure 17 Hardware Mode Clocking Scheme Overview

The S/PDIF receiver is enabled and hence the PLL operates in S/PDIF receiver mode and all PLL and S/PDIF receiver control is fully automatic. All supported S/PDIF receiver sample rates can be used.

The clock source for the S/PDIF transmitter is selected by TXSRC, which is latched from the CSB/GPO2 pin at reset. The clock source for the MCLK pin is selected by the AIF_MS bit which is latched from the SCLK pin at reset.

FREQMODE control is fully automatic to ensure that the MCLK output is maintained at 256fs relative to the S/PDIF received sample rate.

In hardware mode, the OSCCLK **must** be 12MHz and hence the external crystal (or applied XIN clock) must be 12MHz. No other OSCCLK frequencies are supported in hardware mode.

Please refer to the Software Mode Internal Clocking section for detailed descriptions of the component blocks used in hardware mode.

S/PDIF TRANSMITTER

The S/PDIF transmitter generates the S/PDIF frames, and outputs on the TX0 pin. The audio data for the frame can be taken from one of two sources, selectable using the TXSRC register. The transmitter can be powered down using the SPDIFTXD register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 PLL4 06h	5	TXVAL_SF0	0	**Overwrite Mode S/PDIF Transmitter Validity Sub-Frame 0** 0 = transmit validity = 0 1 = transmit validity = 1
	6	TXVAL_SF1	0	**Overwrite Mode S/PDIF Transmitter Validity Sub-Frame 1** 0 = transmit validity = 0 1 = transmit validity = 1
	7	TXVAL_ OVWR	0	**S/PDIF Transmitter Validity Overwrite Mode Enable** 0 = disabled, validity bit is 0 when the S/PDIF transmitter sources PCM audio interface, or it matches the S/PDIF input validity when the S/PDIF transmitter sources the S/PDIF receiver. 1 = enabled, validity bit transmitted for subframe 0 is defined by TXVAL_SF0, validity bit transmitted for subframe 1 is defined by TXVAL_SF1.
R21 SPDTX4 15h	6	TXSRC	1	**S/PDIF Transmitter Data Source** 0 = S/PDIF received data. 1 = Audio Interface received data
	7	TXSTATSRC	0	**S/PDIF Transmitter Channel Status Data Source** 0 = Received channel status data 1 = Transmit channel status registers Note 1: Only used if TXSRC=0 Note 2: See section User Data below
R30 PWRDN 1Eh	2	SPDIFTXPD	1	**S/PDIF Transmitter Powerdown Enable** 0 = S/PDIF transmitter enabled 1 = S/PDIF transmitter disabled

Table 33 S/PDIF Transmitter Control

The WM8805 also transmits the preamble and VUCP bits (Validity, User Data, Channel Status and Parity bits).

VALIDITY BIT

By default, set to 0 (to indicate valid data) with the following exceptions:

1. TXSRC=0 (S/PDIF receiver), where Validity is the value recovered from the S/PDIF input stream by the S/PDIF receiver.
2. TXVAL_OVWR=1, where Validity is the value set in registers TXVAL_SF0 and TXVAL_SF1.

USER DATA

Set to 0 as User Data configuration is not supported in the WM8805 – if TXSRC=0 and TXSTATSRC=0 (S/PDIF receiver) User Data is set by the receiver.

CHANNEL STATUS DATA

The Channel Status bits form a 192-frame block - transmitted at 1 bit per sub-frame. Each sub-frame forms its own 192-frame block. The WM8805 is a consumer mode device and only the first 40 bits of the block are used. All data transmitted from the WM8805 is stereo, so the channel status data is the same for both channels. The only exception to this is the channel number bits (23:20) which can be changed to indicate if the channel is left or right in the stereo image. Bits within this block can be configured by setting the Channel Bit Control registers (see Table 34 - Table 38). If TXSRC is the S/PDIF receiver, the Channel bits are transmitted with the same values recovered by the receiver – unless TXSTATSRC is set, in which case they are set by the Channel Bit Control registers.

PARITY BIT

This bit maintains even parity for data as a means of basic error detection. It is generated by the transmitter.

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R18 SPDTX1 12h	0	CON/PRO	0	0	**Use Of Channel Status Block** 0 = Consumer Mode 1 = Professional Mode (not supported by WM8805).
	1	AUDIO_N	1	0	**Linear PCM Identification**. 0 = S/PDIF transmitted data is audio PCM. 1 = S/PDIF transmitted data is not audio PCM.
	2	CPY_N	2	0	**Copyright Information** 0 = Transmitted data has copyright asserted. 1 = Transmitted data has no copyright assertion.
	5:3	DEEMPH[2:0]	5:3	000	**Additional Format Information** 000 = Data from Audio interface has no pre-emphasis. 001 = Data from Audio interface has pre-emphasis. All other modes are reserved and should not be used.
	7:6	CHSTMODE [1:0]	7:6	00	**Channel Status Mode** 00 = Only valid mode for consumer applications.

Table 34 S/PDIF Transmitter Channel Status Bit Control Register 1

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R19 SPDTX2 13h	7:0	CATCODE [7:0]	15:8	00000000	**Category Code** Refer to S/PDIF specification (IEC 60958-3) for full details. 0x00h indicates “general” mode.

Table 35 S/PDIF Transmitter Channel Status Bit Control Register 2

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION	
R20 SPDTX3 14h	3:0	SRCNUM [3:0]	19:16	0000	**Source Number** Refer to S/PDIF specification (IEC 60958-3) for full details.	
	5:4	CHNUM1[1:0]	21:20	00	**Channel Number for Subframe 1**	
					CHNUM1	**Channel Status Bits[21:20]**
					00	Do not use channel number
					01	Send to Left Channel
					10	Send to Right Channel
					11	Do not use channel number
	7:6	CHNUM2[1:0]	23:22	00	**Channel Number for Subframe 2**	
					CHNUM2	**Channel Status Bits[23:22]**
					00	Do not use channel number
					01	Send to Left Channel
					10	Send to Right Channel
					11	Do not use channel number

Table 36 S/PDIF Transmitter Channel Bit Control Register 3

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R21 SPDTX4 15h	3:0	FREQ[3:0]	27:24	0001	**Indicated Sampling Frequency** Refer to S/PDIF specification (IEC 60958-3) for full details. 0001 = Sampling Frequency not indicated.
	5:4	CLKACU[1:0]	29:28	11	**Clock Accuracy of Transmitted Clock** 00 = Level II 01 = Level I 10 = Level III 11 = Interface frame rate not matched to sampling frequency.

Table 37 S/PDIF Transmitter Channel Status Bit Control Register 4

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R22 SPDTX5 16h	0	MAXWL	32	1	**Maximum Audio Sample Word Length** 0 = 20 bits 1 = 24 bits
	3:1	TXWL[2:0]	35:33	101	**Audio Sample Word Length** Used with MAXWL to indicate Tx word length 000 = Word Length Not Indicated
					TXWL[2:0] / **MAXWL==1** / **MAXWL==0** 001 / 20 bits / 16 bits 010 / 22 bits / 18 bits 100 / 23 bits / 19 bits 101 / 24 bits / 20 bits 110 / 21 bits / 17 bits All other combinations reserved
	7:4	ORGSAMP [3:0]	39:36	0000	**Original Sampling Frequency** Refer to S/PDIF specification (IEC 60958-3) for full details.

Table 38 S/PDIF Transmitter Channel Status Bit Control Register 5

S/PDIF RECEIVER

INPUT SELECTION

The S/PDIF receiver has up to 8 dedicated inputs. These inputs can be configured as either single ended CMOS or as a 500mVp-p comparator input, depending upon the state of the SPDIFINMODE register. Inputs RX4 – RX7 can be configured as CMOS GPO pins by setting SPDGPO = 1. The GPO pins are configured according to Table 52. All inputs go to a selection mux which passes a single input into the S/PDIF receiver for decoding. The S/PDIF receiver can be powered down if not in use by setting the SPDIFRXPD register bit. If the S/PDIF receiver is powered down the system will wait until then end of the current S/PDIF frame before powering down.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 SPDRX1 1Ch	5	SPDGPO	0	**RX4-7 Configuration Select** When set high the pin is a GPO pin. 0 – S/PDIF inputs 1 – GPO outputs
	6	WL_MASK	0	**S/PDIF Receiver Word Length Truncation Mask** 0 = disabled, data word is truncated as described in Table 44. 1 = enabled, data word is not truncated.
	7	SPD_192K_EN	1	**S/PDIF Receiver 192kHz Support Enable** 0 = disabled, S/PDIF receiver maximum supported sampling frequency is 96kHz 1 = enabled, S/PDIF receiver maximum supported sampling frequency is 192kHz
R30 PWRDN 1Eh	1	SPDIFRXPD	1	**S/PDIF Receiver Powerdown** 0 = S/PDIF receiver enabled 1 = S/PDIF receiver disabled
R8 PLL6 08h	2:0	RXINSEL[2:0]	000	**S/PDIF Rx Input Select** Select the S/PDIF input to pass to the receiver circuit. 000 – RX0 001 – RX1 010 – RX2 011 – RX3 100 – RX4 101 – RX5 110 – RX6 111 – RX7
R9 SPDMODE 09h	7:0	SPDIFINMODE	11111111	**S/PDIF Input Mode Select** Selects the input circuit type for the receiver input. The LSB represents RX0 and the MSB represents RX7 0 = CMOS input 1 = Comparator input. Compatible with 500mVppAC coupled consumer S/PDIF input signals. Refer to S/PDIF specification (IEC 60958-3) for full details.

Table 39 S/PDIF Receiver Input Selection Registers

AUDIO DATA HANDLING

The S/PDIF receiver recovers the data and VUCP bits from each sub-frame. The WM8805 can detect when the data is not in PCM format. See Non-Audio Detection section for more detail.

The received data can also be output over the audio interfaces in any of the data formats supported, or data may also be re-transmitted on TX0, de-jittering the data stream.

USER DATA

The WM8805 can output recovered user data via the GPO pins. See Table 52 for General Purpose Pin control.

CHANNEL STATUS DATA

The channel status bits are recovered from the incoming data stream and are used to control various functions of the device.

The S/PDIFRx interface always receives 24 bits of data in bits 4 to 27 of the SPDIF payload. The audio sample can be either 20 bits if AUX bits not used or up to 24bits if AUX bits used. So the audio sample can be 20,21,22,23 or 24 bit. The source (wherever the S/PDIF data is coming from) of the S/PDIF data stream must set the MAXWL and RXWL within the status bits to indicate the size of the audio sample. This is then recovered by the S/PDIF Rx interface. The S/PDIF Rx interface ALWAYS receives 24 bits, but if the actual length of the audio data sample (indicated by MAXWL and RXWL) is less than 24 bits, then the user has the option to truncate these 24 bits to the actual size. These truncated bits are then sent to either the SPDIF Tx or the AIF. Truncation may allow users to process data faster. If the user does not want this truncation to happen then they must mask the truncation using the WL_MASK. In this case all 24 bits of data received are transferred.

The audio data sample can be transferred to either the AIF or the SPDIF Tx.

When the audio data sample is transferred to the AIF, and if the AIF is operating in a mode which has less data bits, then the WM8805 will reduce the audio data sample to the length of the AIF. For example, if the AIF is operating in 16 bit mode, but the SPDIF Rx receives an audio data sample length of 21 bits, then the WM8805 will reduce the 21 bits to 16 bits by removing the LSBs. This cannot be masked. If the AIF is operating in 24 bit mode, then the full 21 bits are transferred on the AIF, with the LSBs set to 000.

When the audio data sample is transferred to the SPDIF TX, then the full audio data sample (24 bits) is written to the SPDIF Tx. Unless it has been truncated using the WL-MASK bits.

It is assumed that the channel status is stereo and hence only channel one data is read. The channel status data is stored in five read-only registers which can be read back over the serial interface (see Serial Interface Read-back). The CSUD interrupt is asserted when the recovered channel status data is different to that currently stored in the read only registers. The registers are updated and the interrupt is asserted when the last bit of channels status data is recovered. The interrupt will remain asserted until one of the channel status registers is read. If another change to channel status data occurs before the last block has been read, the interrupt will de-assert when the first bit of differing channel status is received and will be asserted again when the last bit of the current channel status block is received.

The register descriptions for the channel status bits are given in Table 40 to Table 44.

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R13 RXCHAN1 0Dh (read-only)	0	CON/PRO	0	0	**Use Of Channel Status Block** 0 = Consumer Mode 1 = Professional Mode The WM8805 is a consumer mode device. Detection of professional mode may give erroneous behaviour.
	1	AUDIO_N	1	0	**Linear PCM Identification** 0 = Data word represents audio PCM samples. 1 = Data word does not represent audio PCM samples.
	2	CPY_N	2	0	**Copyright Information** 0 = Copyright is asserted for Rx data. 1 = Copyright is not asserted for Rx data.
	3	DEEMPH	3	0	**Additional Format Information** 0 = Recovered S/PDIF data has no pre-emphasis. 1 = Recovered S/PDIF data has pre-emphasis.
	5:4	Reserved	5:4	00	Reserved for additional de-emphasis modes.
	7:6	CHSTMODE [1:0]	7:6	00	**Channel Status Mode** 00 = Only valid mode for consumer applications.

Table 40 S/PDIF Receiver Channel Status Register 1

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R14 RXCHAN2 0Eh (read-only)	7:0	CATCODE [7:0]	15:8	00000000	**Category Code** Refer to S/PDIF specification (IEC 60958-3) for full details. 0x00h indicates “general” mode.

Table 41 S/PDIF Receiver Channel Status Register 2

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R15 RXCHAN3 0Fh (read-only)	3:0	SRCNUM [3:0]	19:16	0000	**S/PDIF Source Number** Refer to S/PDIF specification (IEC 60958-3) for full details.
	5:4	CHNUM1[1:0]	21:20	00	**Channel Number For Sub-frame 1** 00 = do not use channel number 01 = channel 1 to left channel 10 = channel 1 to right channel
	7:6	CHNUM2[1:0]	23:22	00	**Channel Number For Sub-frame 2** 00 = do not use channel number 01 = channel 2 to left channel 10 = channel 2 to right channel

Table 42 S/PDIF Receiver Channel Status Register 3

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R16 RXCHAN4 10h (read-only)	3:0	FREQ[3:0]	27:24	0001	**Indicated Sampling Frequency** Refer to S/PDIF specification (IEC 60958-3) for full details.
	5:4	CLKACU[1:0]	29:28	11	**Clock Accuracy of Received Clock** 00 = Level II 01 = Level I 10 = Level III 11 = Interface frame rate not matched to sampling frequency.

Table 43 S/PDIF Receiver Channel Status Register 4

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION		
R17 RXCHAN5 11h (read-only)	0	MAXWL	32	1	**Maximum Audio Sample Word Length** 0 = 20 bits 1 = 24 bits Note: see table in description of bits 3:1 of this register,		
	3:1	RXWL[2:0]	35:33	000	**Audio Sample Word Length** 000: Word Length Not Indicated		
					RXWL[2:0]	**MAXWL==1**	**MAXWL==0**
					001	20 bits	16 bits
					010	22 bits	18 bits
					100	23 bits	19 bits
					101	24 bits	20 bits
					110	21 bits	17 bits
					All other combinations are reserved and may give erroneous operation. Data will be truncated internally when these bits are set unless WL_MASK is set. See note 1.		
	7:4	ORGSAMP [3:0]	39:36	0000	**Original Sampling Frequency** Refer to S/PDIF specification (IEC 60958-3) for full details.		

Table 44 S/PDIF Receiver Channel Status Register 5

Note 1: MAXWL and RXWL[2:0] bits in recovered channel status data are used to truncate digital audio interface transmitted data. **Truncation replaces the lower data bits with 0. Truncation can be masked using the WL_MASK control bit. Truncation can be masked by the WL_MASK.** Refer to received channel status bit description

S/PDIF RECEIVER STATUS FLAGS

There are several S/PDIF receiver status flags which are recorded by the WM8805. The flags are described in Table 45. These flags are available via GPIO pins or status registers.

FLAG	DESCRIPTION	VISIBILITY
UNLOCK	Unlock Flag Indicates that the S/PDIF Rx clock recovery circuit is unlocked. 0 = Locked onto incoming S/PDIF stream. 1 = Not locked onto the incoming S/PDIF stream.	S/PDIF Status Register, GPO, CSB –hardware mode
INVALID	Invalid Flag Indicates that recovered S/PDIF data is marked as invalid. 0 = Data marked as valid 1 = Data marked as invalid	Interrupt Status Reg
TRANS_ERR	Transmission Error Flag Indicates that a transmission error has occurred. This signal is asserted when the preamble sequence is incorrectly received or there is a parity error or a bi-phase mark encoding error. 0 = No error detected in transmission 1 = Error in transmission	Interrupt Status Reg, GPO, SCLK –hardware mode
AUDIO_N	Audio Status Flag Recovered Channel Status bit 1. 0 = Data word represents audio PCM samples. 1 = Data word does not represent audio PCM samples.	Channel Status Register, S/PDIF Status Register
PCM_N	Non-PCM Flag Indicates that non-audio code (defined in IEC-61937) has been detected. 0 = Sync code not detected. 1 = Sync code detected – received data is not audio PCM.	S/PDIF Status Register
ZEROFLAG	Zero Flag Indicates detection of 1024 consecutive all zero frames 0 = 1024 consecutive all zero frames not detected 1 = 1024 consecutive all zero frames detected	GPO
CPY_N	Non-Copyright Flag Recovered Channel Status bit 2. 0 = Copyright is asserted for this data. 1 = Copyright is not asserted for this data. Note this signal is inverted and will cause an interrupt on logic 0.	Channel Status Register, S/PDIF Status Register, GPO
REC_FREQ[1:0]	Recovered Frequency Flag Indicates recovered S/PDIF clock frequency: 00 = 192kHz 01 = 96kHz or 88.2kHz 10 = 48kHz or 44.1kHz 11 = 32kHz	S/PDIF Status Register
INT_N	Interrupt Signal 0 = Interrupt has occurred 1 = No interrupt has occurred	GPO
V	Recovered validity bit for current sub-frame	GPO
U	Recovered user bit for current sub-frame	GPO
C	Recovered channel status bit for current sub-frame	GPO
SFRM_CLK	Sub-frame clock. 1 = Current sub-frame is sub-frame A 0 = Current sub-frame is sub -frame B	GPO
192BLK	Start OF 192 Frame Sequence Flag Indicates start of 192 frame block. Asserted duration of frame 0.	GPO
GEN_FLAG	General Error Flag Logical OR of TRANS_ERR, NON_AUDIO and UNLOCK. Used only in Hardware Control Mode	GPO0 - hardware Mode

NON_AUDIO	Non-Audio Flag Logical OR of PCM_N and AUDIO_N	Interrupt status register, GPO, SDOUT - hardware mode
CSUD	Channel Status Update Indicates that channel status registers have updated and may be read back over the serial interface.	Interrupt status register, GPO
DEEMPH	De-emphasis Flag 0 = Recovered data has no pre-emphasis 1 = Recovered data has pre-emphasis	S/PDIF Status Register, GPO

Table 45 S/PDIF Receiver Status Flags Description

As the Table 45 shows, these flags can be reported via GPO pins (see Table 52) or via Read-back registers.

'WITH FLAGS' MODE

The WM8805 features a 'With Flags' mode to enable the user to append status flags to the audio sample streamed transmitted from the digital audio interface. When WITHFLAG is set to 1 'With Flags' mode is enabled and the flags in Table 47 are appended to the LSB of the audio sample. If WITHFLAG is set to 0 'With Flags' mode is disabled and only the audio sample is transmitted from the digital audio interface.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 SPDRX1 1Dh	4	WITHFLAG	0	**Enable With Flags Mode** 0 = Disabled 1 = Enabled

Table 46 With Flags Mode Control Register

WITH FLAGS BIT ORDER	FLAG
0	V
1	U
2	C
3	192BLK
4	CSUD
5	TRANS_ERR
6	UNLOCK
7	NON_AUDIO

Table 47 Flags Appended to Audio Sample in 'With Flags' Mode

Diagrams illustrating 'With Flags' mode for each audio data format can be found on page 49 of the data sheet (Figure 23 to Figure 27).

Note: 24-bit RJ mode does not support 'With Flags' mode.

INTERRUPT GENERATION

The INT_N flag indicates that a change of status has occurred on one or more of the UNLOCK, INVALID, TRANS_ERR, CSUD, NON_AUDIO, CPY_N, REC_FREQ or DEEMPH status flags. To identify which flag caused the interrupt, the Interrupt Status Register (INTSTAT) must be read. INVALID and TRANS_ERR are level sensitive interrupts. When these signals are high an interrupt will be generated. The interrupt can be cleared by reading the interrupt status register, however, the interrupt will re-assert if the signal is still high. CSUD and REC_FREQ will generate an interrupt on a low to high transition and can be cleared by reading the interrupt status register. Once clear the interrupt will not re-assert until another low to high transition occurs. NON_AUDIO, CPY_N, UNLOCK and DEEMPH will generate an update signal on any change in flag status. The interrupt and update signals are latched and will remain asserted until they are cleared by reading the Interrupt Status Register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 INTSTAT 0Bh (read-only)	0	UPD_UNLOCK	-	**UNLOCK update signal** 0 = INT_N not caused by a toggle of UNLOCK flag 1 = INT_N caused by a toggle of UNLOCK flag
	1	INT_INVALID	-	**INVALID flag interrupt signal** 0 = INT_N not caused by INVALID flag 1 = INT_N caused by INVALID flag
	2	INT_CSUD	-	**INT_CSUD interrupt signal** 0 = INT_N not caused by CSUD flag 1 = INT_N caused by CSUD flag
	3	INT_TRANS_ERR	-	**TRANS_ERR flag interrupt signal** 0 = INT_N not caused by TRANS_ERR flag 1 = INT_N caused by TRANS_ERR flag
	4	UPD_NON_AUDIO	-	**NON_AUDIO update signal** 0 = INT_N not caused by a toggle of AUDIO_N or PCM_N flags 1 = INT_N caused by a toggle of AUDIO_N or PCM_N flags
	5	UPD_CPY_N	-	**CPY_N update signal** 0 = INT_N not caused by assertion of CPY_N flag 1 = INT_N caused assertion of CPY_N flag
	6	UPD_DEEMPH	-	**DEEMPH update signal** 0 = INT_N not caused by a toggle of DEEMPH flag 1 = INT_N caused by a toggle of DEEMPH flag
	7	UPD_REC_FREQ	-	**REC_FREQ update signal** 0 = INT_N not caused by assertion of REC_FREQ flag 1 = INT_N caused by assertion of REC_FREQ flag

Table 48 Interrupt Status Register

Where the INT_N has been asserted by an update signal (UPD_NON_AUDIO, UPD_CPY_N, UPD_REC_FREQ, UPD_UNLOCK or UPD_DEEMPH) the S/PDIF Status Register (SPDSTAT) can be interrogated to establish the updated value of the flag.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 SPDSTAT 0Ch (read-only)	0	AUDIO_N	-	**Audio Status Flag** Recovered channel status bit-1. 0 = Data word represents audio PCM samples. 1 = Data word does not represent audio PCM samples.
	1	PCM_N	-	**Non-PCM Flag** Indicates that non-audio code (defined in IEC-61937) has been detected. 0 = Sync code not detected. 1 = Sync code detected – received data is not audio PCM.
	2	CPY_N	-	**Non-Copyright Flag** Recovered Channel Status bit-2. 0 = Copyright is asserted for this data. 1 = Copyright is not asserted for this data.
	3	DEEMPH	-	**De-emphasis Flag** Recovered Channel Status bit-3. 0 = Copyright is asserted for this data. 1 = Copyright is not asserted for this data.
	5:4	REC_FREQ [1:0]	--	**Recovered Frequency Flag** Indicates recovered S/PDIF clock frequency: 00 = 192kHz 01 = 96kHz or 88.2kHz 10 = 48kHz or 44.1kHz 11 = 32kHz
	6	UNLOCK	-	**Unlock Flag** Indicates that the S/PDIF Rx clock recovery circuit is unlocked. 0 = Locked onto incoming S/PDIF stream. 1 = Not locked onto the incoming S/PDIF stream.

Table 49 S/PDIF Status Register

The interrupt and update signals used to generate INT_N can be masked at the users discretion. The MASK register bit (Table 50) prevents flags from asserting INT_N and from updating the Interrupt Status Register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 INTMASK 0Ah	7:0	MASK[7:0]	00000000	**Interrupt Mask Enable** When a flag is masked, it does not update the Error Register or cause an INT_N interrupt to be asserted. 0 = unmask, 1 = mask. MASK[0] = mask control for UPD_UNLOCK MASK[1] = mask control for INT_INVALID MASK[2] = mask control for INT_CSUD MASK[3] = mask control for INT_TRANS_ERR MASK[4] = mask control for UPD_NON_AUDIO MASK[5] = mask control for UPD_CPY_N MASK[6] = mask control for UPD_DEEMPH MASK[7] = mask control for UPD_REC_FREQ

Table 50 Interrupt Mask Control Register

ERROR HANDLING IN SOFTWARE MODE

When the TRANS_ERR flag is asserted, it indicates that the recovered Rx S/PDIF sub-frame is corrupted. This corruption can due to a BI-Phase error, a parity error or a pre-amble error. When the INVALID flag is asserted, it indicates that the recovered Rx S/PDIF sub-frame has been marked as being invalid by the source of the S/PDIF data. Both TRANS_ERR and INVALID indicate an error.

The S/PDIF receiver has two modes of handling for these errors, manual and automatic. The mechanism for each flag is similar. The mechanisms are described below.

MANUAL ERROR HANDLING

This manual handling of errored Rx S/PDIF data can be used when an application processor is being interrupted via the INT_N signal. Appropriate action should be taken by the application processor to handle the error condition

If the TRANS_ERR and INVALID error flags are not masked using the MASK register, the recovered S/PDIF Rx data is passed to the digital audio interface or to the S/PDIF transmitter irrespective of the state of the flag and the data content of the recovered stream.(Also refer to note below). In this case, the application processor will be interrupted via the INT_N signal.

AUTOMATIC ERROR HANDLING

This automatic handling of errored Rx S/PDIF data can be used when an application processor is not being interrupted via the INT_N signal leaving the WM8805 to handle the error condition.

If the TRANS_ERR and INVALID error flags are masked using the MASK register, the WM8805 output data from the S/PDIF Rx interface depends on the setting of FILLMODE. If FILLMODE=1, then the incoming data (which is errored) is overwritten with 0's. If FILLMODE=0, then the last valid data sample is repeatedly output.

For the INVALID flag, the automatic error handling can be disabled if ALWAYSVALID =1. If ALWAYSVALID is set, then the recovered Rx S/PDIF data, which is marked as invalid, will be allowed to pass to the digital audio interface or to the S/PDIF transmitter. The data will not be modified in any way.

Note:

For the S/PDIF receiver to S/PDIF transmitter data path, only the INVALID flag will cause data to be overwritten, the TRANS_ERR flag is not used to overwrite data which is passed to the S/PDIF transmitter.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 PLL6 08h	5	FILLMODE	0	**Fill Mode Overwrite Configuration** Determines S/PDIF receiver action when TRANS_ERR or INVALID flag is masked and error condition sets the flag: 0 = Data from S/PDIF receiver is overwritten with last valid data sample when flag is set. 1 = Data from S/PDIF receiver is overwritten as all zeros when flag is set.
	6	ALWAYSVALID	0	**Automatic Error Handling Configuration for INVALID Flag** 0 = INVALID flag automatic error handling enabled. 1 = INVALID flag automatic error handling disabled.

Table 51 S/PDIF Receiver Automatic Error Handling Configuration Registers

NON-AUDIO DETECTION

The SPDIF payload can contain PCM data for audio or non-audio applications. In the case where the payload contains the 96 bit synchronization code defined in IEC61937 then this indicates that the payload contains data which is not suitable for direct playback through an audio codec. This 96 bit code is defined as 4*16bits of '0'+Pa (16bits)+Pb (16bits)..

If the S/PDIFRx interface decodes this sync code then it sets the PCM_N bit.

When the PCM_N =1, then it indicates non-audio data. When the PCM_N =0, then it indicates that the SPDIF payload does not contain the synch code..

Another status bit, AUDIO_N status is recovered from the Channel Status block. It is bit 1 of the channel status. When AUDIO_N =0, then it indicates that the SPDIF payload contains audio PCM encoded data. This is also referred to as linear PCM data. When the AUDIO_N= 1, then it indicates that the SPDIF payload does not contain audio PCM data.

NON_AUDIO data is indicated by a logical OR of the AUDIO_N and PCM_N flags.

Any change of AUDIO_N or PCM_N status will cause an INT_N interrupt (UPD_NON_AUDIO) to be generated. If the MASK register bit for AUDIO_N or PCM_N is set, then the associated signal will not generate an interrupt (UPD_NON_AUDIO).

GENERAL PURPOSE OUTPUT (GPO) CONFIGURATION

The WM8805 has a maximum of eight configurable GPO pins depending upon the mode of operation of the device. By default GPO0 and GPO1 are available, however if 2-wire Software Control Mode is selected the CSB pin becomes GPO2 and the SDOUT pin becomes GPO7. Finally, if SPDGPO is set high, pins RX4-RX7 become GPO3-GPO6 respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 GPO01 17h	3:0	GPO0[3:0]	0000 (INT_N)	Flags and Status bits available on GPO pins 0000 = INT_N 0001 = V 0010 = U 0011 = C 0100 = TRANS_ERR 0101 = SFRM_CLK 0110 = 192BLK 0111 = UNLOCK 1000 = NON_AUDIO 1001 = CSUD 1010 = DEEMPH 1011 = CPY_N 1100 = ZEROFLAG 1101 = 0 ↓ 1111 = 0 **Note 1:** GPO2 and GPO7 are only available in 2-wire software control mode. **Note 2:** Refer to Table 45 for signal descriptions
	7:4	GPO1[3:0]	0111 (UNLOCK)	
R24 GPO23 18h	3:0	GPO2[3:0]	0111 (UNLOCK)	
	7:4	GPO3[3:0]	0101 (SFRM_ CLK)	
R25 GPO45 19h	3:0	GPO4[3:0]	0110 (192BCLK)	
	7:4	GPO5[3:0]	0011 (C)	
R26 GPO67 1Ah	3:0	GPO6[3:0]	0010 (U)	
	7:4	GPO7[3:0]	0100 (TRANS_ERR)	

Table 52 GPO Control Registers

DIGITAL AUDIO INTERFACE

Audio data is transferred to and from the WM8805 via the digital audio interface. Data from the digital audio interface transmitter may be passed to the S/PDIF transmitter or data from the S/PDIF receiver may be output on the digital audio interface receiver. The digital audio interface can be powered down using the AIFPD register bit described in Table 53.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 PWRDN 1Eh	5	AIFPD	1	**Digital Audio Interface Power Down.** 1= Power Down 0 = Power Up

Table 53 Digital Audio Interface Power Down Control

MASTER AND SLAVE MODES

The audio interface operates in either slave or master mode, selectable using the AIF_MS bit (see Table 55). In both master and slave modes DIN is always an input and DOUT is always an output. The default is slave mode.

In slave mode (AIF_MS=0), LRCLK and BCLK are inputs. DIN and LRCLK are sampled on the rising edge of BCLK. Data output, DOUT, changes on the falling edge of BCLK and the polarity of BCLK may be reversed independently on the transmit and receive sides of the interface using the AIFRX_BCP and AIFTX_BCP control bits, see Table 56.

In master mode (AIF_MS=1), LRCLK and BCLK are generated by the WM8805. As in slave mode, DIN is sampled on the rising edge of BCLK, and DOUT changes on the falling edge of BCLK and the polarity of BCLK may be reversed the transmit and receive sides of the interface with the AIFRX_BCP and AIFTX_BCP control bits.

The frequencies of LRCLK are derived from MCLK and are dependant on the MCLKDIV control bit. Table 54 shows the settings for MCLKDIV for common sample rates and MCLK frequencies.

SAMPLING RATE (LRCLK)	MASTER CLOCK (MCLK) FREQUENCY (MHZ)	
	128fs	256fs
	MCLKDIV = 1	MCLKDIV = 0
32kHz	4.096	8.192
44.1kHz	5.6448	11.2896
48kHz	6.144	12.288
96kHz	12.288	24.576
192kHz	24.576	Unavailable

Table 54 Master Mode LRCLK Frequency Selection

BCLK is also generated by the WM8805. The frequency of BCLK depends on the mode of operation. In 128fs mode (MCLKDIV = 1) BCLK = MCLK/2. In 256fs mode (MCLKDIV = 0) BCLK = MCLK/4. However if DSP mode is selected as the audio interface mode then BCLK=MCLK. Note that DSP mode cannot be used in 128fs mode for word lengths greater than 16-bits.

Master/Slave mode is selected with the following register:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 AIFRX 1Ch	6	AIF_MS	0	**Audio Interface Master/Slave Mode Select** 0 = Slave mode – MCLK, LRCLK and BCLK are inputs 1 = Master mode – MCLK, LRCLK and BCLK are outputs

Table 55 Master/Slave Mode Select Register

AUDIO DATA FORMATS

Five interface formats are supported:

- Left Justified Mode
- Right Justified Mode
- I^2S Mode
- DSP Mode A
- DSP Mode B

The MSB is sent first in all formats. Word lengths of 16, 20 and 24 bits are supported.

Audio data for each stereo channel is clocked with the BCLK signal. Data is time multiplexed with the LRCLK, indicating whether the left or right channel data is present. The LRCLK is also used as a timing reference to indicate the beginning or end of the data words.

In Left Justified, Right Justified and I^2S modes the minimum number of BCLKs per LRCLK period is two times the number of bits in the selected word length. LRCLK must be high for a minimum of *n* BCLKs and low for a minimum of *n* BCLKs, where *n* is the number of bits in an audio word. Any mark to space ratio on LRCLK is acceptable provided the above requirements are met.

The data may also be output in DSP Mode A or Mode B, with LRCLK used as a frame sync to identify the MSB of the first word. The minimum number of BCLKs per LRCLK period is two times the number of bits in the word length.

LEFT JUSTIFIED MODE

In Left Justified mode, the MSB of DIN is sampled by the WM8805 on the first rising edge of BCLK following an LRCLK transition. The MSB of the output data (DOUT) changes on the same falling edge of BCLK as LRCLK and may be sampled on the next rising edge of BCLK. LRCLK is high during the left samples and low during the right samples (Figure 18).

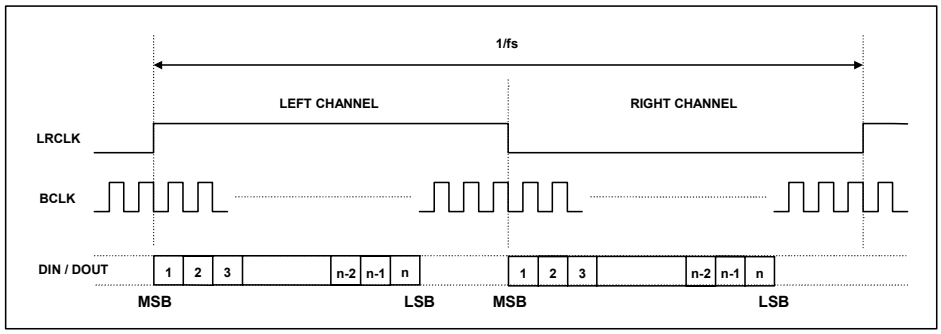


Figure 18 Left Justified Mode

RIGHT JUSTIFIED MODE

In Right Justified Mode, the LSB of DIN is sampled by the WM8805 on the rising edge of BCLK preceding an LRCLK transition. The LSB of the output data (DOUT) changes on the falling edge of BCLK preceding an LRCLK transition, and may be sampled on the next rising edge of BCLK. LRCLK is high during the left samples and low during the right samples (Figure 19).

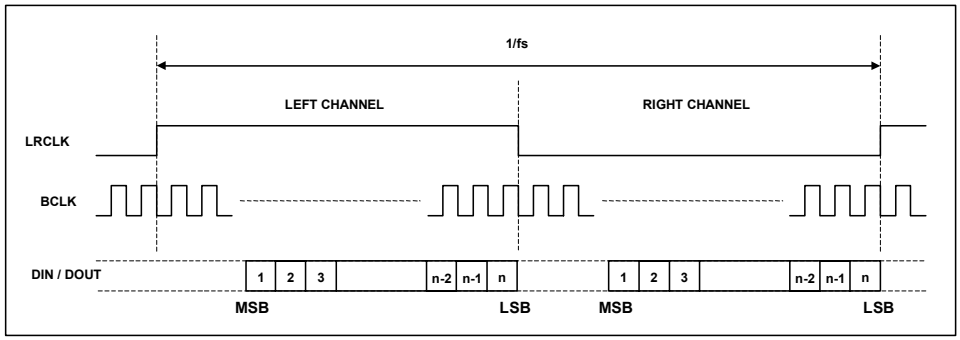


Figure 19 Right Justified Mode

I²S MODE

In I²S Mode, the MSB of DIN is sampled by the WM8805 on the second rising edge of BCLK following an LRCLK transition. The MSB of the output data changes on the first falling edge of BCLK following an LRCLK transition, and may be sampled on the next rising edge of BCLK. LRCLK is low during the left samples and high during the right samples (Figure 20).

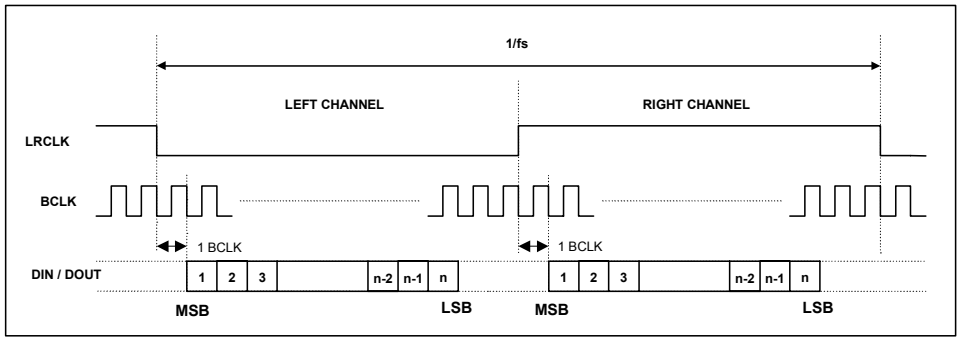


Figure 20 I²S Mode

DSP MODE A

In DSP Mode A, the MSB of the left channel data is sampled by the WM8805 on the second rising edge of BCLK following an LRCLK rising edge. The right channel data follows the left channel data (Figure 21).

The MSB of the left channel of the output data changes on the first falling edge of BCLK following a low to high LRCLK transition and may be sampled on the rising edge of BCLK. The right channel data is contiguous with the left channel data (Figure 21).

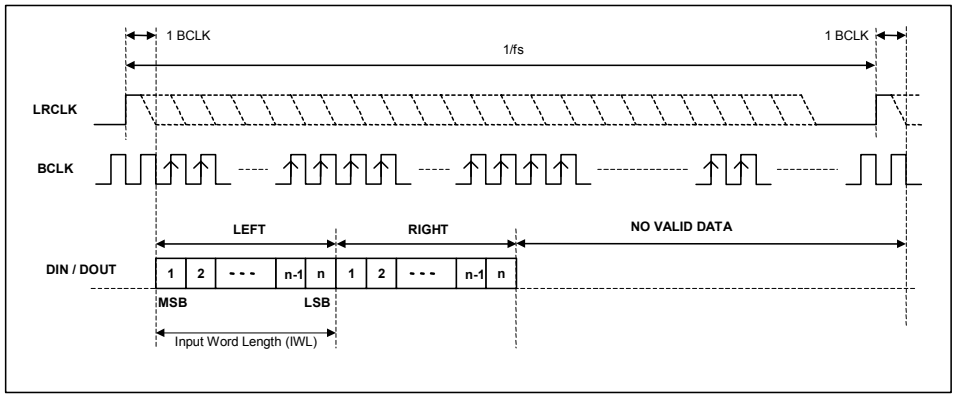


Figure 21 DSP Mode A

DSP MODE B

In DSP Mode B, the MSB of the left channel data is sampled by the WM8805 on the first BCLK rising edge following a LRCLK rising edge. The right channel data follows the left channel data (Figure 22).

The MSB of the output data changes on the same falling edge of BCLK as the low to high LRCLK transition and may be sampled on the rising edge of BCLK. The right channel data is contiguous with the left channel data (Figure 22).

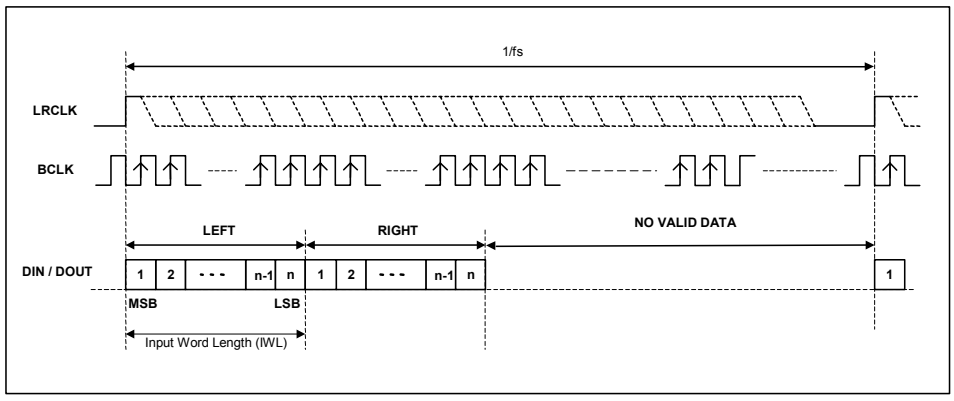


Figure 22 DSP Mode B

'WITH FLAGS' MODE

The following diagrams illustrate the position of the status flags within the audio sample for each audio data format when 'With Flags' mode is enabled. With flags mode is only available on pin DOUT. The WM8805 does not support Right Justified 24-Bit 'With Flags' mode.

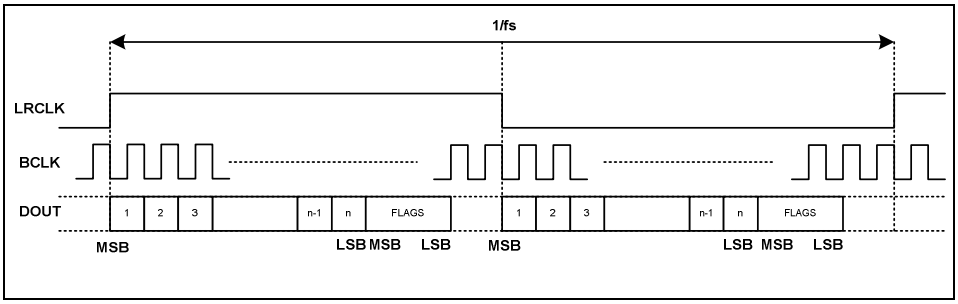


Figure 23 Left Justified 'With Flags' Mode

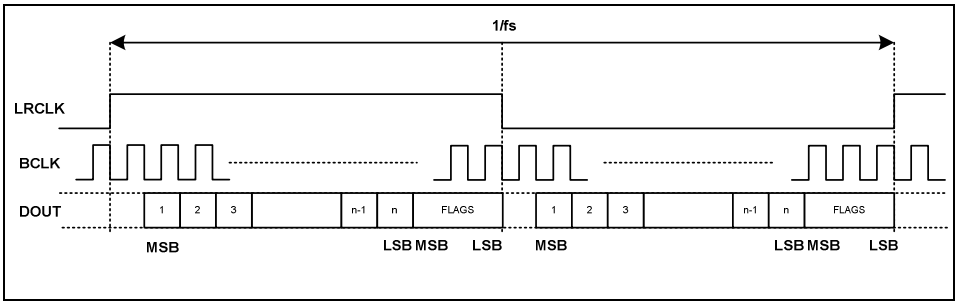


Figure 24 Right Justified 'With Flags' Mode

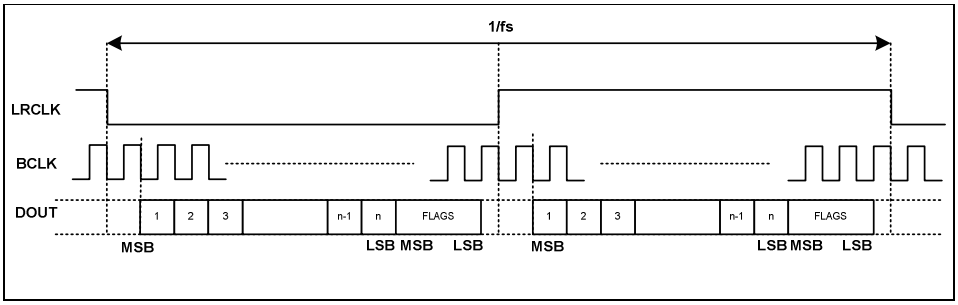


Figure 25 I^2S 'With Flags' Mode

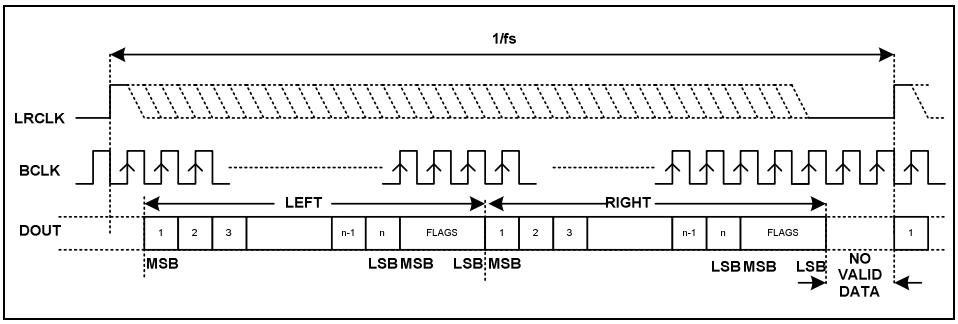


Figure 26 DSP Mode A 'With Flags'

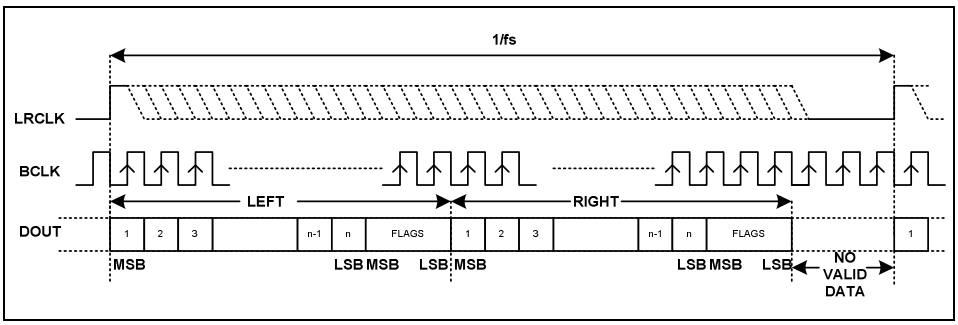


Figure 27 DSP Mode B 'With Flags'

AUDIO INTERFACE CONTROL

The register bits controlling the audio interface are summarised below. Note that dynamically changing the audio data format may cause erroneous operation, and hence is not recommended.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 SPDIFRX1 1Dh	4	WITHFLAG	0	'With Flags' Mode Select 0: 'With Flags' Mode disabled (see Note 3) 1: 'With Flags' Mode enabled
R27 AIFTX 1Bh	1:0	AIFTX_FMT[1:0]	10	Audio Data Format Select 11: DSP mode 10: I^2S mode 01: Left justified mode 00: Right justified mode
	3:2	AIFTX_WL[1:0]	01	Audio Data Word Length 11: 24 bits (see notes 1/2/3/6) 10: 24 bits (see notes 1/2/3/6) 01: 20 bits 00: 16 bits
	4	AIFTX_BCP	0	BCLK invert (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	5	AIFTX_LRP	0	Right, left and I^2S modes – LRCLK polarity and DSP mode select 1 = invert LRCLK polarity / DSP Mode B 0 = normal LRCLK polarity / DSP Mode A
R28 AIFRX 1Ch	1:0	AIFRX_FMT[1:0]	10	Audio Data Format Select 11: DSP mode 10: I^2S mode 01: Left justified mode 00: Right justified mode
	3:2	AIFRX_WL[1:0]	01	Audio Data Word Length 11: 24 bits (see note 1/2/3/6) 10: 24 bits 01: 20 bits 00: 16 bits
	4	AIFRX_BCP	0	BCLK Invert (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted See Note 4
	5	AIFRX_LRP	0	Right, left and I^2S modes – LRCLK polarity and DSP mode select 1 = invert LRCLK polarity / DSP Mode B 0 = normal LRCLK polarity / DSP Mode A See Note 5

Table 56 Audio Interface Control

Note 1: S/PDIF data frames contain a maximum of 24-bits of audio data

Note 2: In 24 bit I^2S mode, any data width of 24 bits or less is supported provided that LRCLK is high for a minimum of 24 BCLK cycles and low for a minimum of 24 BCLK cycles (48 BCLK cycles). If exactly 32 BCLK cycles occur in one LRCLK (16 high, 16 low) the chip will auto detect and operate in 16 bit data word length mode.

Note 3: 24 bit Right Justified 'With Flags' Mode is not supported.

Note 4: Must be set to the same value as AIFTX_BCP.

Note 5: Must be set to the same value as AIFTX_LRP.

Note 6: MAXWL and RXWL[2:0] bits in recovered channel status data are used to truncate digital audio interface transmitted data. The truncation replaces the lower data bits with 0. Refer to received channel status bit description.

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8805 can be configured using the Control Interface. Any unused bits which are not specified should be set to '0'. Not all registers can be read. Only the device ID (registers R0, R1 and R2) and the status registers can be read. These status registers are labelled as "read only".

REGISTER	NAME	ADDRESS [0:7]	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
R0	RST/DEVID 1	00	write: RESET read: DEVICEID[7:0]								-
R1	DEVID2	01	DEVICEID[15:8]								read only
R2	DEVREV	02	0	0	0	0	DEVREV[3:0]				read only
R3	PLL1	03	PLL_K[7:0]								00100001
R4	PLL2	04	PLL_K[15:8]								11111101
R5	PLL3	05	0	0	PLL_K[21:16]						00110110
R6	PLL4	06	TXVAL_ OVWR	TXVAL_SF1	TXVAL_SF0	PRESCALE	PLL_N[3:0]				00000111
R7	PLL5	07	0	0	CLKOUTDIV[1:0]		MCLKDIV	FRACEN	FREQMODE[1:0]		00010110
R8	PLL6	08	MCLKSRC	ALWAYSVALID	FILLMODE	CLKOUTDIS	CLKOUTSRC	RXINSEL[2:0]			00011000
R9	SPDMODE	09	SPDIFINMODE[7:0]								11111111
R10	INTMASK	0A	MASK[7:0]								00000000
R11	INTSTAT	0B	Interrupt Status								read only
R12	SPDSTAT	0C	S/PDIF Status								read only
R13	RXCHAN1	0D	RX Channel Info 1								read only
R14	RXCHAN2	0E	RX Channel Info 2								read only
R15	RXCHAN3	0F	RX Channel Info 3								read only
R16	RXCHAN4	10	RX Channel Info 4								read only
R17	RXCHAN5	11	RX Channel Info 5								read only
R18	SPDTX1	12	CHSTMODE[1:0]		DEEMPH[2:0]			CPY_N	AUDIO_N	CON/PRO	00000000
R19	SPDTX2	13	CATCODE[7:0]								00000000
R20	SPDTX3	14	CHNUM2[1:0]		CHNUM1[1:0]		SRCNUM[3:0]				00000000
R21	SPDTX4	15	TXSTATSRC	TXSRC	CLKACU[1:0]		FREQ[3:0]				01110001
R22	SPDTX5	16	ORGSAMP[3:0]				TXWL[2:0]			MAXWL	00001011
R23	GPO01	17	GPO1[3:0]				GPO0[3:0]				01110000
R24	GPO23	18	GPO3[3:0]				GPO2[3:0]				01010111
R25	GPO45	19	GPO5[3:0]				GPO4[3:0]				00110110
R26	GPO67	1A	GPO7[3:0]				GPO6[3:0]				01000010
R27	AIFTX	1B	0	0	AIFTX_LRP	AIFTX_BCP	AIFTX_WL[1:0]		AIFTX_FMT[1:0]		00000110
R28	AIFRX	1C	0	AIF_MS	AIFRX_LRP	AIFRX_BCP	AIFRX_WL[1:0]		AIFRX_FMT[1:0]		00000110
R29	SPDRX1	1D	SPD_192K_EN	WL_MASK	SPDGPO	WITHFLAG	CONT	READMUX[2:0]			10000000
R30	PWRDN	1E	0	0	TRIOP	AIFPD	OSCPD	SPDIFTXPD	SPDIFRXPD	PLLPD	00000111

Table 57 WM8805 Register Map

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R00 RST/DEVID1 00h	7:0	RESET	-	Writing to this register will apply a reset to the device. Reading from this register will return the second part of the device ID 00000101 = 05h
R01 DEVID2 01h (read only)	7:0	DEVID2	10001000	Reading from this register will return the first part of the device ID 10001000 = 88h
R02 DEVREV 02h	3:0	DEVREV[3:0]	-	
R3 PLL1 03h	7:0	PLL_K[7:0]	00100001	Fractional (K) part of PLL frequency ratio (R). Value K is one 22-digit binary number spread over registers R3, R4 and R5 as shown. **Note: PLL_K must be set to specific values when the S/PDIF receiver is used. Refer to S/PDIF Receiver clocking section for details.**
R4 PLL2 04h	7:0	PLL_K[15:8]	11111101	
R5 PLL3 05h	5:0	PLL_K[21:16]	00110110	
R6 PLL4 06h	3:0	PLL_N[3:0]	0111	Integer (N) part of PLL frequency ratio (R). Use values in the range 5 ≤ PLL_N ≤ 13 as close as possible to 8 **Note: PLL_N must be set to specific values when the S/PDIF receiver is used. Refer to S/PDIF Receiver clocking section for details.**
	4	PRESCALE	0	**PLL Pre-scale Divider Select** 0 = Divide by 1 (PLL input clock = oscillator clock) 1 = Divide by 2 (PLL input clock = oscillator clock ÷ 2)
	5	TXVAL_SF0	0	**Overwrite Mode S/PDIF Transmitter Validity Sub-Frame 0** 0 = transmit validity = 0 1 = transmit validity = 1
	6	TXVAL_SF1	0	**Overwrite Mode S/PDIF Transmitter Validity Sub-Frame 1** 0 = transmit validity = 0 1 = transmit validity = 1
	7	TXVAL_ OVWR	0	**S/PDIF Transmitter Validity Overwrite Mode Enable** 0 = disabled, validity bit is 0 when the S/PDIF transmitter sources PCM audio interface, or it matches the S/PDIF input validity when the S/PDIF transmitter sources the S/PDIF receiver. 1 = enabled, validity bit transmitted for subframe 0 is defined by TXVAL_SF0, validity bit transmitted for subframe 1 is defined by TXVAL_SF1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 PLL5 07h	1:0	MODE[1:0]	10	**PLL Post-scale Divider Select** Selects the PLL output divider value in conjunction with MCLKDIV and CLKOUTDIV. Refer to Table 23 for details of FREQMODE operation. **Note: FREQMODE[1:0] bits are automatically set in S/PDIF Receive Mode.**
	2	FRACEN	1	**Integer/Fractional PLL Mode Select** 0 = Integer PLL (PLL_N value used, PLL_K value ignored) 1 = Fractional PLL (both PLL_N and PLL_K values used) **Note: FRACEN must be set to enable the fractional PLL when using S/PDIF Receive Mode.**
	3	MCLKDIV	0	**MCLK Divider Select** (Only valid when CLK2 is selected as MCLK output source) See Table 23 for MCLKDIV configuration in PLL user mode. See Table 28 for MCLKDIV configuration in PLL S/PDIF receive mode.
	5:4	CLKOUTDIV[1:0]	01	**CLKOUT Divider Select** (Only valid when CLK1 is selected as CLKOUT output source) See Table 27 for CLKOUTDIV[1:0] configuration in PLL user mode. See Table 28 for CLKOUTDIV[1:0] configuration in PLL S/PDIF receive mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 PLL6 08h	2:0	RXINSEL[2:0]	000	**S/PDIF Rx Input Select** Select the S/PDIF input to pass to the receiver circuit. 000 – RX0 001 – RX1 010 – RX2 011 – RX3 100 – RX4 101 – RX5 110 – RX6 111 – RX7
	3	CLKOUTSRC	1	**CLKOUT Pin Source Select** 0 = Select CLK1 1 = Select OSCCLK
	4	CLKOUTDIS	1	**CLKOUT Pin Disable** 0 = Pin Disabled (Pin tri-stated) 1 = Pin Enabled
	5	FILLMODE	0	**Fill Mode Select** Determines S/PDIF receiver action when corrupt or invalid data is detected: 0 = Data from S/PDIF receiver remains static at last valid sample. 1 = Data from S/PDIF receiver is output as all zeros.
	6	ALWAYSVALID	0	**Always Valid Select** Used to ignore the INVALID flag. 0 = Use INVALID flag. 1 = Ignore INVALID flag.
	7	MCLKSRC	0	**MCLK Output Source Select** 0 = Select CLK2 1 = Select OSCCLK
R9 SPDMODE 09h	7:0	SPDIFINMODE	11111111	**S/PDIF Input Mode Select** Selects the input circuit type for the receiver input. The LSB represents RX0 and the MSB represents RX7 0 = CMOS input 1 = Comparator input. Compatible with 500mVppAC coupled consumer S/PDIF input signals. Refer to S/PDIF specification (IEC 60958-3) for full details.
R10 INTMASK 0Ah	7:0	MASK[7:0]	00000000	**Interrupt Mask Enable** When a flag is masked, it does not update the Error Register or cause an interrupt to be asserted. 0 = unmask, 1 = mask. MASK[0] = mask control for UPD_UNLOCK MASK[1] = mask control for INT_INVALID MASK[2] = mask control for INT_CSUD MASK[3] = mask control for INT_TRANS_ERR MASK[4] = mask control for UPD_NON_AUDIO MASK[5] = mask control for UPD_CPY_N MASK[6] = mask control for UPD_DEEMPH MASK[7] = mask control for UPD_REC_FREQ

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 INTSTAT 0Bh (read-only)	0	UPD_UNLOCK	-	**UNLOCK Update Signal** 0 = INT_N not caused by a toggle of UNLOCK flag 1 = INT_N caused by a toggle of UNLOCK flag
	1	INT_INVALID	-	**INVALID Flag Interrupt Signal** 0 = INT_N not caused by INVALID flag 1 = INT_N caused by INVALID flag
	2	INT_CSUD	-	**INT_CSUD Interrupt Signal** 0 = INT_N not caused by CSUD flag 1 = INT_N caused by CSUD flag
	3	INT_TRANS_ERR	-	**TRANS_ERR Flag Interrupt Signal** 0 = INT_N not caused by TRANS_ERR flag 1 = INT_N caused by TRANS_ERR flag
	4	UPD_NON_AUDIO	-	**NON_AUDIO Update Signal** 0 = INT_N not caused by a toggle of AUDIO_N or PCM_N flags 1 = INT_N caused by a toggle of AUDIO_N or PCM_N flags
	5	UPD_CPY_N	-	**CPY_N Update Signal** 0 = INT_N not caused by a toggle of CPY_N flag 1 = INT_N caused a toggle of CPY_N flag
	6	UPD_DEEMPH	-	**DEEMPH Update Signal** 0 = INT_N not caused by a toggle of DEEMPH flag 1 = INT_N caused by a toggle of DEEMPH flag
	7	UPD_REC_FREQ	-	**REC_FREQ Update Signal** 0 = INT_N not caused by a toggle of REC_FREQ flag 1 = INT_N caused by a toggle of REC_FREQ flag
R12 SPDSTAT 0Ch (read-only)	0	AUDIO_N	-	**Audio Status Flag** Recovered channel status bit-1. 0 = Data word represents audio PCM samples. 1 = Data word does not represent audio PCM samples.
	1	PCM_N	-	**Non-PCM Flag** Indicates that non-audio code (defined in IEC-61937) has been detected. 0 = Sync code not detected. 1 = Sync code detected – received data is not audio PCM.
	2	CPY_N	-	**Non-Copyright Flag** Recovered Channel Status bit-2. 0 = Copyright is asserted for this data. 1 = Copyright is not asserted for this data.
	3	DEEMPH	-	De-emphasis Flag Recovered Channel Status bit-3. 0 = Copyright is asserted for this data. 1 = Copyright is not asserted for this data.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5:4	REC_FREQ [1:0]	--	**Recovered Frequency Flag** Indicates recovered S/PDIF clock frequency: 00 = 192kHz 01 = 96kHz or 88.2kHz 10 = 48kHz or 44.1kHz 11 = 32kHz
	6	UNLOCK	-	**Unlock Flag** Indicates that the S/PDIF Rx clock recovery circuit is unlocked. 0 = Locked onto incoming S/PDIF stream. 1 = Not locked onto the incoming S/PDIF stream.
R13 RXCHAN1 0Dh (read-only)	0	CON/PRO	0	**Use Of Channel Status Block** 0 = Consumer Mode 1 = Professional Mode The WM8805 is a consumer mode device. Detection of professional mode may give erroneous behaviour.
	1	AUDIO_N	0	**Linear PCM Identification** 0 = Data word represents audio PCM samples. 1 = Data word does not represent audio PCM samples.
	2	CPY_N	0	**Copyright Information** 0 = Copyright is asserted for Rx data. 1 = Copyright is not asserted for Rx data.
	3	DEEMPH	0	**Additional Format information** 0 = Recovered S/PDIF data has no pre-emphasis. 1 = Recovered S/PDIF data has pre-emphasis.
	5:4	Reserved	00	Reserved for additional de-emphasis modes.
	7:6	CHSTMODE [1:0]	00	**Channel Status Mode** 00 = Only valid mode for consumer applications.
R14 RXCHAN2 0Eh (read-only)	7:0	CATCODE [7:0]	00000000	**Category Code** Category Code. Refer to S/PDIF specification (IEC 60958-3) for full details. 00h indicates “general” mode.
R15 RXCHAN3 0Fh (read-only)	3:0	SRCNUM [3:0]	0000	**S/PDIF Source Number** Indicates number of S/PDIF source. Refer to S/PDIF specification (IEC 60958-3) for full details.
	5:4	CHNUM1[1:0]	00	**Channel Number For Sub-frame 1** 00 = do not use channel number 01 = channel 1 to left channel 10 = channel 1 to right channel
	7:6	CHNUM2[1:0]	00	**Channel Number For Sub-frame 2** 00 = do not use channel number 01 = channel 2 to left channel 10 = channel 2 to right channel
R16 RXCHAN4	3:0	FREQ[3:0]	0001	**Indicated Sampling Frequency** Refer to S/PDIF specification (IEC 60958-3) for full details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10h (read-only)	5:4	CLKACU[1:0]	11	**Clock Accuracy of Received Clock** 00 = Level II 01 = Level I 10 = Level III 11 = Interface frame rate not matched to sampling frequency.
R17 RXCHAN5 11h (read-only)	0	MAXWL	1	**Maximum Audio Sample Word Length** 0 = 20 bits 1 = 24 bits
	3:1	RXWL[2:0]	000	**Audio Sample Word Length** 000: Word Length Not Indicated RXWL[2:0] / MAXWL==1 / MAXWL==0 001 / 20 bits / 16 bits 010 / 22 bits / 18 bits 100 / 23 bits / 19 bits 101 / 24 bits / 20 bits 110 / 21 bits / 17 bits All other combinations are reserved and should not be used.
	7:4	ORGSAMP [3:0]	0000	**Original Sampling Frequency** Refer to S/PDIF specification (IEC 60958-3) for full details
R18 SPDTX1 12h	0	CON/PRO	0	**Use Of Channel Status Block** 0 = Consumer Mode 1 = Professional Mode (not supported by WM8805)
	1	AUDIO_N	0	**Linear PCM Identification** 0 = S/PDIF transmitted data is audio PCM. 1 = S/PDIF transmitted data is not audio PCM.
	2	CPY_N	0	**Copyright Information** 0 = Transmitted data has copyright asserted. 1 = Transmitted data has no copyright assertion.
	5:3	DEEMPH[2:0]	000	**Additional Format Information** 000 = Data from Audio interface has no pre-emphasis. 001 = Data from Audio interface has pre-emphasis. All other modes are reserved and should not be used.
	7:6	CHSTMODE [1:0]	00	**Channel Status Mode** 00 = Only valid mode for consumer applications.
R19 SPDTX2 13h	7:0	CATCODE [7:0]	00000000	**Category Code** Refer to S/PDIF specification (IEC 60958-3) for full details. 00h indicates “general” mode.
R20 SPDTX3 14h	3:0	SRCNUM [3:0]	0000	**Source Number** No definitions are attached to data.
	5:4	CHNUM1[1:0]	00	**Channel Number for Subframe 1** CHNUM1 / Channel Status Bits[21:20] 00 / Do not use channel number 01 / Send to Left Channel 10 / Send to Right Channel

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				11 Do not use channel number
	7:6	CHNUM2[1:0]	00	**Channel Number for Subframe 2** **CHNUM2** / **Channel Status Bits[23:22]** 00 Do not use channel number 01 Send to Left Channel 10 Send to Right Channel 11 Do not use channel number
R21 SPDTX4 15h	3:0	FREQ[3:0]	0001	**Indicated Sampling Frequency** Refer to S/PDIF specification (IEC 60958-3) for full details. 0001 = Sampling Frequency not indicated.
	5:4	CLKACU[1:0]	11	**Clock Accuracy of Transmitted Clock** 00 = Level II 01 = Level I 10 = Level III 11 = Interface frame rate not matched to sampling frequency.
	6	TXSRC	1	**S/PDIF Transmitter Data Source** 0 = S/PDIF received data. 1 = Audio Interface received data
	7	TXSTATSRC	0	**S/PDIF Transmitter Channel Status Data Source** 0 = Received channel status data 1 = Transmit channel status registers Note : Only used if TXSRC=0
R22 SPDTX5 16h	0	MAXWL	1	**Maximum Audio Sample Word Length** 0 = 20 bits 1 = 24 bits
	3:1	TXWL[2:0]	101	**Audio Sample Word Length** Used with MAXWL to indicate Tx word length 000 = Word Length Not Indicated **TXWL[2:0]** / **MAXWL==1** / **MAXWL==0** 001 / 20 bits / 16 bits 010 / 22 bits / 18 bits 100 / 23 bits / 19 bits 101 / 24 bits / 20 bits 110 / 21 bits / 17 bits All other combinations reserved
	7:4	ORGSAMP [3:0]	0000	**Original Sampling Frequency** Refer to S/PDIF specification (IEC 60958-3) for full details.
R23 GPO01 17h	3:0	GPO0[3:0]	0000	Flags and Status bits available on GPO pins 0000 = INT_N 0001 = V 0010 = U 0011 = C 0100 = TRANS_ERR 0101 = SFRM_CLK 0110 = 192BLK 0111 = UNLOCK 1000 = NON_AUDIO
	7:4	GPO1[3:0]	0111	
R24 GPO23 18h	3:0	GPO2[3:0]	0111	
	7:4	GPO3[3:0]	0101	
R25 GPO45 19h	3:0	GPO4[3:0]	0110	
	7:4	GPO5[3:0]	0011	
R26	3:0	GPO6[3:0]	0010	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
GPO67 1Ah	7:4	GPO7[3:0]	0100	1001 = CSUD 1010 = DEEMPH 1011 = CPY_N 1100 = ZEROFLAG 1101 = 0 ↓ 1111 = 0 **Note:** GPO2 and GPO7 are only available in 2-wire software control mode.
R27 AIFTX 1Bh	1:0	AIFTX_FMT[1:0]	10	**Audio Data Format Select** 11: DSP mode 10: I^2S mode 01: Left justified mode 00: Right justified mode
	3:2	AIFTX_WL[1:0]	01	**Audio Data Word Length Select** 11: 24 bits 10: 24 bits 01: 20 bits 00: 16 bits
	4	AIFTX_BCP	0	**BCLK Invert** (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	5	AIFTX_LRP	0	Right, left and I^2S modes – LRCLK polarity and DSP mode select 1 = invert LRCLK polarity / DSP Mode B 0 = normal LRCLK polarity / DSP Mode A
R28 AIFRX 1Ch	1:0	AIFRX_FMT[1:0]	10	**Audio Data Format Select** 11: DSP mode 10: I^2S mode 01: Left justified mode 00: Right justified mode
	3:2	AIFRX_WL[1:0]	01	**Audio Data Word Length Select** 11: 24 bits 10: 24 bits 01: 20 bits 00: 16 bits
	4	AIFRX_BCP	0	**BCLK Invert** (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	5	AIFRX_LRP	0	Right, left and I^2S modes – LRCLK polarity and DSP mode select 1 = invert LRCLK polarity / DSP Mode B 0 = normal LRCLK polarity / DSP Mode A
	6	AIF_MS	0	**Audio Interface Master/Slave Interface Select** 0 = Slave Mode – LRCLK, BCLK are inputs 1= Master Mode – LRCLK and BCLK are outputs

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 SPDRX1 1Dh	2:0	READMUX [2:0]	000	**Interrupt Status Register Select** Determines which status register is to be read back: 000 = Interrupt Status Register 001 = Channel Status Register 1 010 = Channel Status Register 2 011 = Channel Status Register 3 100 = Channel Status Register 4 101 = Channel Status Register 5 110 = S/PDIF Status Register
	3	CONT	0	**Continuous Read Enable** 0 = Continuous read-back mode disabled 1 = Continuous read-back mode enabled
	4	WITHFLAG	0	**'With Flags' Mode Select** 0: 'With Flags' Mode disabled 1: 'With Flags' Mode enabled
	5	SPDGPO	0	**RX4-7 Configuration Select** When set high the pin is a GPO pin. 0 – S/PDIF inputs 1 – GPO outputs
	6	WL_MASK	0	**S/PDIF Receiver Word Length Truncation Mask** 0 = disabled, data word is truncated as described in Table 44. 1 = enabled, data word is not truncated.
	7	SPD_192K_EN	1	**S/PDIF Receiver 192kHz Support Enable** 0 = disabled, S/PDIF receiver maximum supported sampling frequency is 96kHz 1 = enabled, S/PDIF receiver maximum supported sampling frequency is 192kHz
R30 PWRDN 1Eh	0	PLLPD	1	**PLL Powerdown** 0 = Enable PLL 1 = Disable PLL
	1	SPDIFRXPD	1	**S/PDIF Receiver Powerdown** 0 = S/PDIF receiver enabled 1 = S/PDIF receiver disabled
	2	SPDIFTXPD	1	**S/PDIF Transmitter Powerdown** 0 = S/PDIF transmitter enabled 1 = S/PDIF transmitter disabled
	3	OSCPD	0	**Oscillator Power Down** 0 = Power Up 1 = Power Down
	4	AIFPD	0	**Digital Audio Interface Power Down** 1= Power Down 0 = Power Up
	5	TRIOP	0	**Tri-state all Outputs** 0 = Outputs not tri-stated 1 = Outputs tri-stated

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

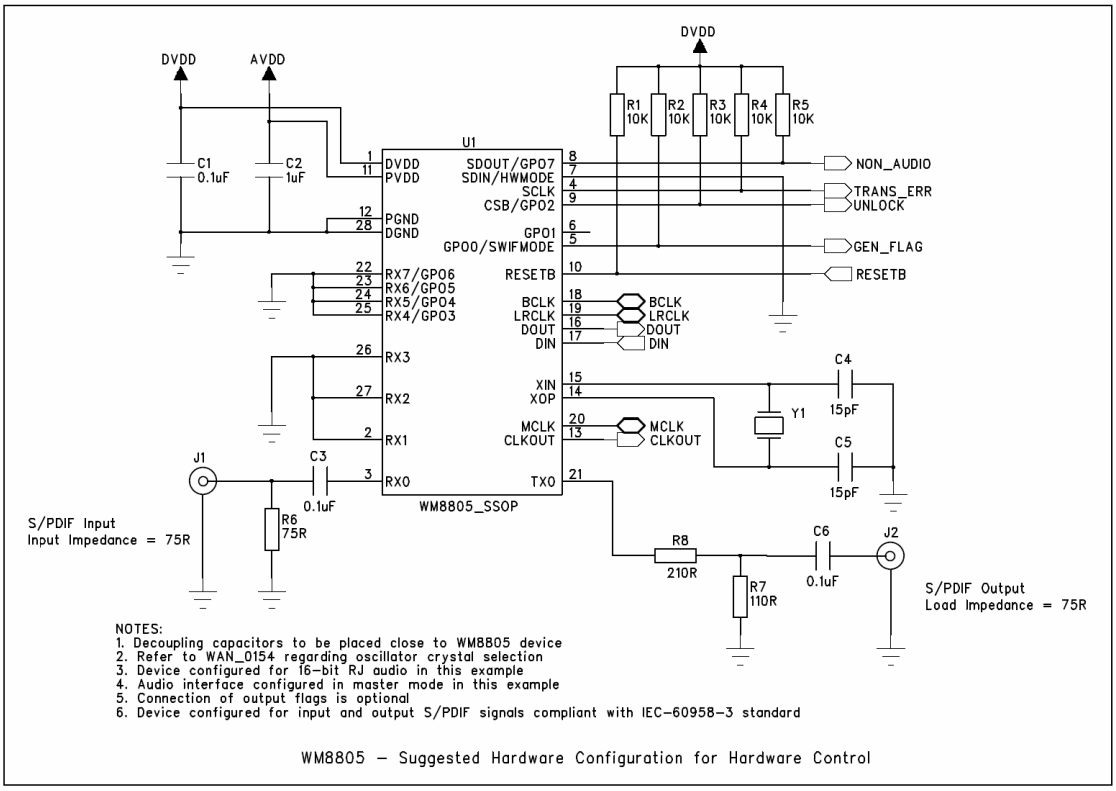


Figure 28 Recommended External Components for Hardware Control Mode

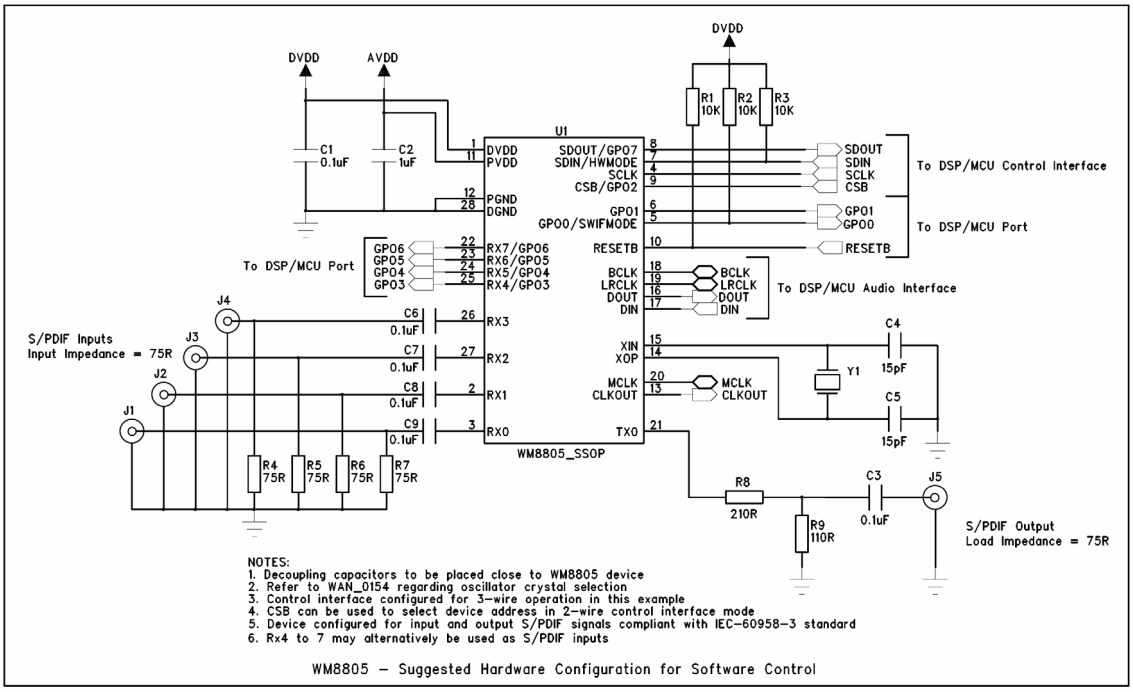
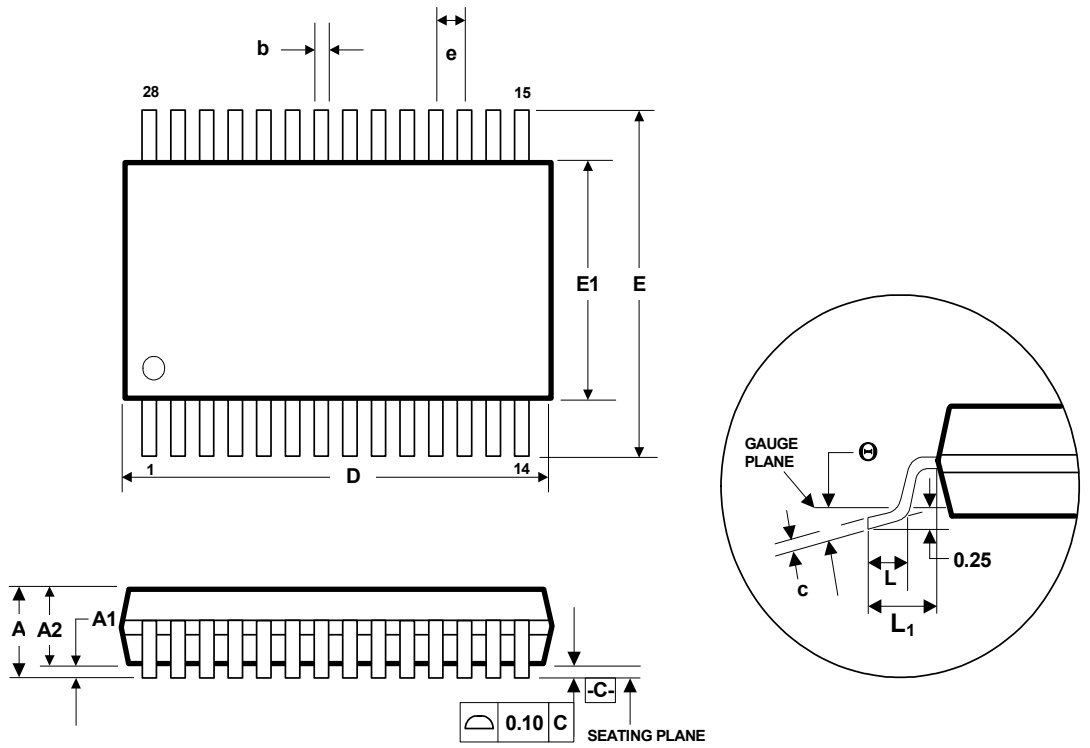


Figure 29 Recommended External Components for Software Control Mode

PACKAGE DIMENSIONS

DS: 28 PIN SSOP (10.2 x 5.3 x 1.75 mm) **DM007.E**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	0.25
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	9.90	10.20	10.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1		1.25 REF	
θ	0°	4°	8°
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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