WM7230, WM7230E

Bottom Port Digital Silicon Microphone

DESCRIPTION

The WM7230 is a low-profile silicon digital microphone. It offers high Signal to Noise Ratio (SNR) and low power consumption and is suited to a wide variety of consumer applications.

The WM7230 incorporates Wolfson's proprietary CMOS/MEMS membrane technology, offering high reliability and high performance in a miniature, low-profile package. The WM7230 is designed to withstand the high temperatures associated with automated flow solder assembly processes. (Note that conventional microphones can be damaged by this process.)

The WM7230 incorporates a high performance ADC, which outputs a single-bit Pulse Density Modulated (PDM) audio data stream. The WM7230 supports selectable left/right channel assignment for a two-channel digital microphone interface, enabling efficient connection of multiple microphones in stereo/array configurations.

The WM7230E variant offers a tighter tolerance on the microphone sensitivity, giving reduced variation between parts. This removes the need for in-line production calibration of part-to-part microphone variations.

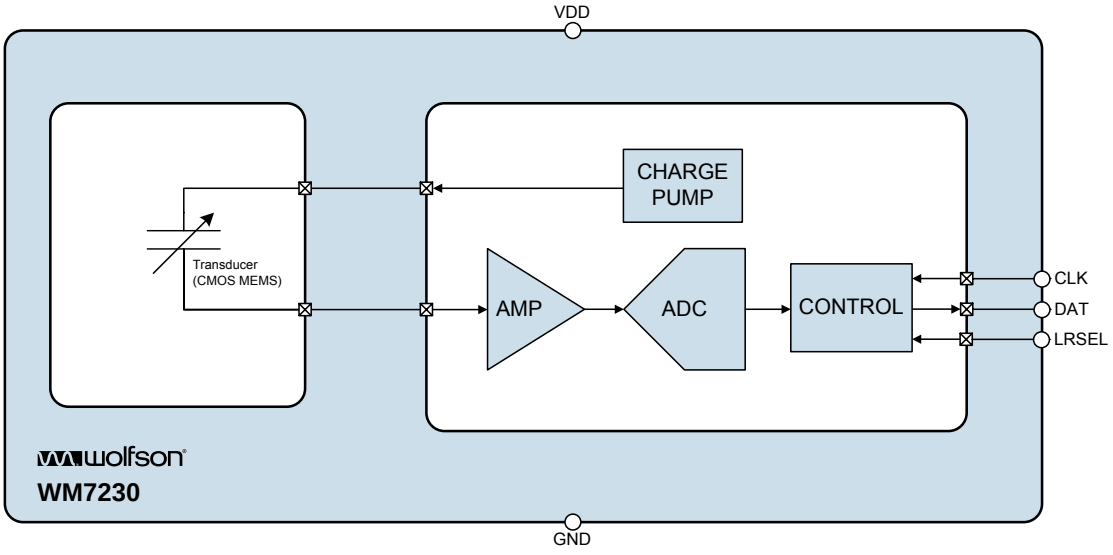
FEATURES

- High SNR; selectable sensitivity tolerance options
  - WM7230 – SNR 61dB, Sensitivity +/-3dB
  - WM7230E – SNR 61dB, Sensitivity +/-1dB
- Low power
  - Sleep Mode - 2µA
  - Normal Operation - 700µA
- Low profile packaging
- Support for automated flow solder assembly
- PDM Digital audio output
- Stereo/array operation
- Proprietary ADC technology
  - Reduced clock jitter sensitivity
  - Low noise floor modulation
  - Stable in overload condition
- Bottom Port Package
- 1.64V to 3.7V supply
- 4.00 mm x 3.00 mm x 1.00mm Thin Package Design

APPLICATIONS

- Mobile telephone handsets
- Portable computers
- Portable media players
- Digital still cameras
- Digital video cameras
- Bluetooth headsets
- Portable navigation devices

BLOCK DIAGRAM

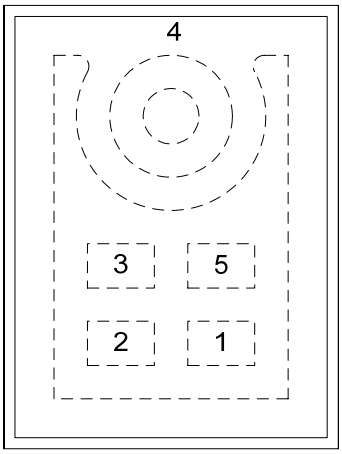


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PIN CONFIGURATION



TOP VIEW

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	CLK	Digital Input	Clock input
2	DAT	Digital Output	PDM Data Output
3	VDD	Supply	Power Supply
4	GND	Supply	Ground
5	LRSEL	Digital Input	Channel Select 0 = Data output following falling CLK edge 1 = Data output following rising CLK edge

ORDERING INFORMATION

DEVICE	DESCRIPTION	TEMPERATURE RANGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM7230IMS/V	Standard	-40 to +100°C	MSL2A	+260°C
WM7230IMS/RV	Standard (tape and reel)	-40 to +100°C	MSL2A	+260°C
WM7230IMSE/V	Standard Enhanced	-40 to +100°C	MSL2A	+260°C
WM7230IMSE/RV	Standard Enhanced (tape and reel)	-40 to +100°C	MSL2A	+260°C

Note:

Reel quantity = 4800

All devices are Pb-free and Halogen free.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL2A = out of bag storage for 4 weeks at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply Voltage (VDD)	-0.3V	+4.2V
Voltage range digital inputs (LRSEL and CLK)	GND-0.3V	VDD+0.3V
Operating temperature range, T_A	-40ºC	+100ºC
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-40ºC	+100ºC

IMPORTANT ASSEMBLY GUIDELINES

Do not put a vacuum over the port hole of the microphone. Placing a vacuum over the port hole can damage the device.

Do not board wash the microphone after a re-flow process. Board washing and the associated cleaning agents can damage the device. Do not expose to ultrasonic cleaning methods.

Do not use vapour phase re-flow process. The vapour can damage the device.

Please refer to application note WAN0273 (MEMS MIC Assembly and Handling Guidelines) for further assembly and handling guidelines.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Supply Range	VDD	1.64		3.7	V
Ground	GND		0		V
Clock Frequency	F_{CLK}	1		3.25	MHz

ACOUSTIC AND ELECTRICAL CHARACTERISTICS

Test Conditions: VDD=1.8V, 1kHz test signal, CLK=2.4MHz, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Directivity				Omni-directional		
Sensitivity (WM7230)	S	94 dB SPL	-29	-26	-23	dBFS
Sensitivity (WM7230E)	S	94 dB SPL	-27	-26	-25	dBFS
Acoustic Overload		THD < 10%		120		dB SPL
Signal to Noise Ratio	SNR	A-Weighted		61		dB
Total Harmonic Distortion	THD	100dB SPL		0.1	1	%
Dynamic Range	DR	A-weighted noise floor to 1% THD		85		dB
Frequency Response		+3dB High frequency		17000		Hz
Acoustic Noise Floor		A-weighted		33		dB SPL
Electrical Noise Floor		A-weighted		-87		dBFS
Power Supply Rejection	PSR	217Hz Square Wave 100mV pk-pk		-70		dBFS
Digital Input / Output						
CLK Input HIGH Level	V_{IH}		0.65 x VDD			V
CLK Input LOW Level	V_{IL}				0.35 x VDD	V
DAT Output HIGH Level	V_{OH}	I_{OH} = +1mA	0.9 x VDD			V
DAT Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1 x VDD	V
Input capacitance (CLK)	C_{IN}			0.5		pF
Maximum load capacitance (DAT)	C_{LOAD}				100	pF
Input Leakage					1	µA
Short Circuit Output Current	I_{SC}	DAT connected to GND			10	mA
Miscellaneous						
Current Consumption	I_{VDD}	Active Mode		700		µA
		SLEEP Mode		2	10	
Start-up Time		From OFF		10		ms
		From SLEEP		10		
CLK Sleep Frequency					1.0	kHz

TERMINOLOGY

1. Sensitivity (dBFS) – Sensitivity is a measure of the microphone output response to the acoustic pressure of a 1kHz 94dB SPL (1Pa RMS) sine wave. This is referenced to the output Full Scale Range (FSR) of the microphone.
2. Full Scale Range (FSR) - Sensitivity, Electrical Noise Floor and Power Supply Rejection are measured with reference to the output Full Scale Range (FSR) of the microphone. FSR is defined as the amplitude of a 1kHz sine wave output whose positive peak value reaches 100% density of logic 1s and whose negative peak value reaches 0% density of logic 1s. This is the largest undistorted 1kHz sine wave that will fit in the digital output numerical range. Note that, because the definition of FSR is based on a sine wave, it is possible to support a square wave test signal output whose level is +3dBFS.
3. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the output response of a 1kHz 94dB SPL sine wave and the idle noise output.
4. Total Harmonic Distortion (%) – THD is the ratio of the RMS sum of the harmonic distortion products in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (ie. test frequency) output.
5. All performance measurements are carried out with 20kHz low pass 'brick-wall' filter and, where noted, an A-weighted filter. Failure to use these filters will result in higher THD and lower SNR values than are found in the Acoustic and Electrical Characteristics. The brick wall filter removes out of band noise.

6. SLEEP Mode is enabled when the CLK input is below the CLK Sleep Frequency noted above. This is a power-saving mode. Normal operation resumes automatically when the CLK input is above the CLK Sleep Frequency. Note that the VDD supply is still required in SLEEP mode.

AUDIO INTERFACE TIMING

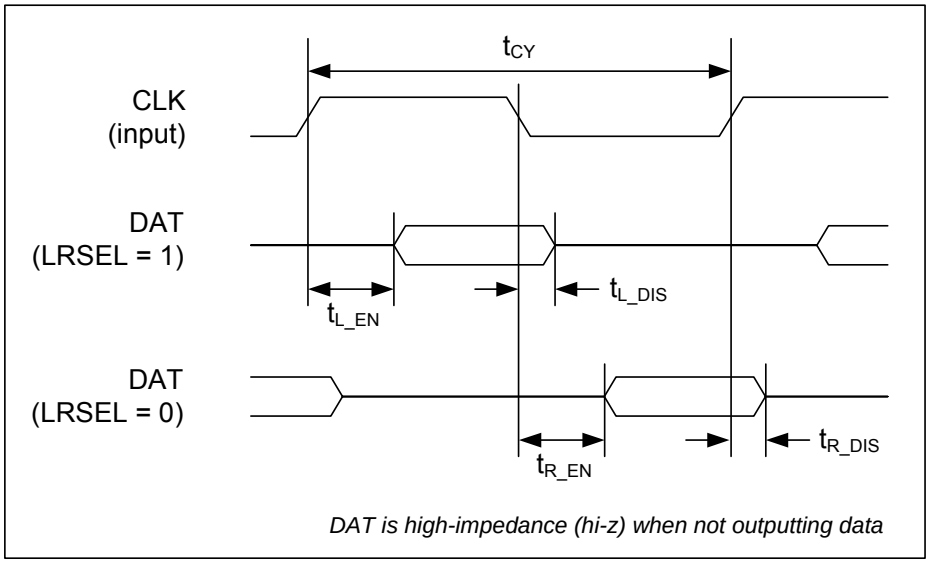


Figure 1 Digital Microphone Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Microphone Interface Timing					
CLK cycle time	t_{CY}	308		1000	ns
CLK duty cycle		60:40		40:60	
DAT enable from rising CLK edge (LRSEL = 1)	t_{L_EN}		18		ns
DAT disable from falling CLK edge (LRSEL = 1)	t_{L_DIS}			16	ns
DAT enable from falling CLK edge (LRSEL = 0)	t_{R_EN}		18		ns
DAT disable from rising CLK edge (LRSEL = 0)	t_{R_DIS}			16	ns

Notes:

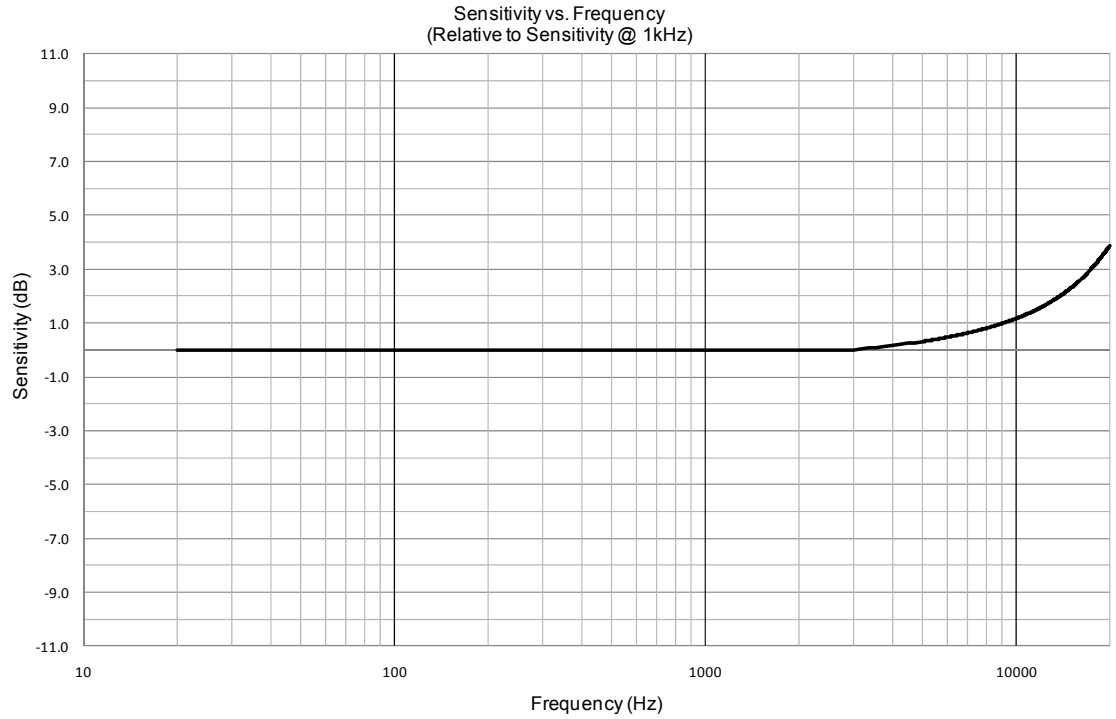
1. The DAT output is high-impedance when not outputting data; this enables the outputs of two microphones to be connected together with the data from one microphone interleaved with the data from the other. (The microphones must be configured to transmit on opposite channels in this case.)

2. In a typical configuration, the Left channel is transmitted following the rising CLK edge (LRSEL = 1). In this case, the Left channel should be sampled by the receiving device on the falling CLK edge,

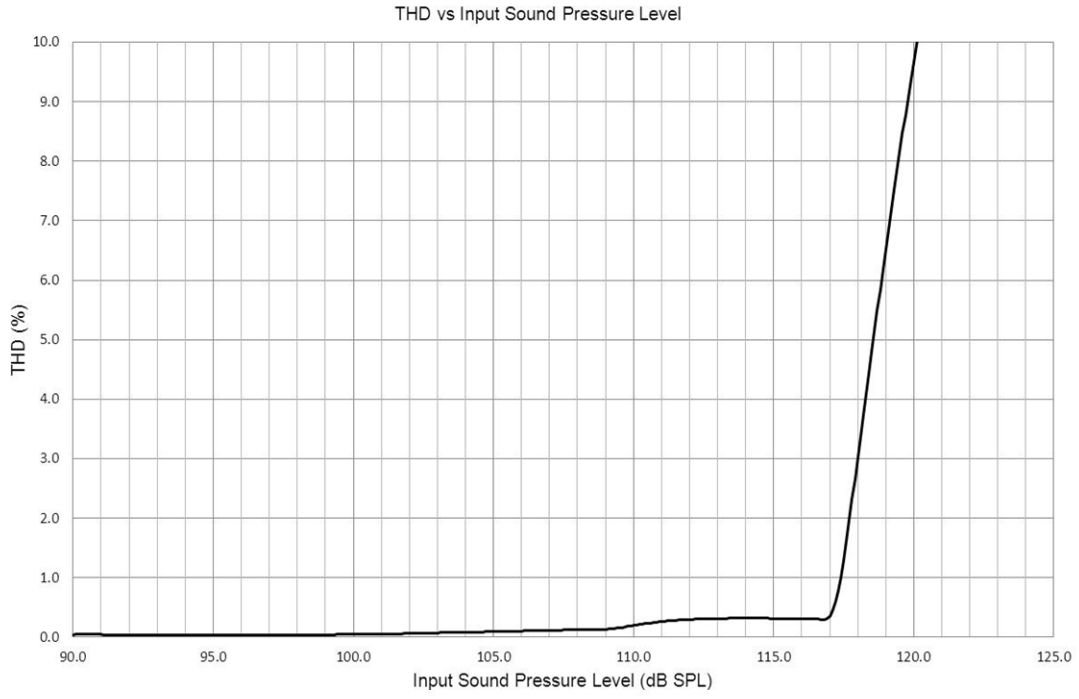
3. Similarly, the Right channel is typically transmitted following the falling CLK edge (LRSEL = 0). In this case, the Right channel should be sampled by the receiving device on the rising CLK edge.

TYPICAL PERFORMANCE

FREQUENCY RESPONSE



THD RATIO



APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

It is recommended to connect a 0.1µF decoupling capacitor between the VDD and GND pins of the WM7230. A ceramic 0.1µF capacitor with X7R dielectric or better is suitable. The capacitor should be placed as close to the WM7230 as possible.

OPTIMISED SYSTEM RF DESIGN

For optimised RF design please refer to document WAN0278 (Recommended PCB Layout for Microphone RF Immunity in Mobile Cell Phone Applications) for further information.

CONNECTION TO A WOLFSON AUDIO CODEC

Wolfson provides a range of audio CODECs incorporating a digital microphone input interface; these support direction connection to digital microphones such as the WM7230.

Stereo connection of two WM7230 digital microphones to the WM8994 CODEC is illustrated in Figure 2.

A 0.1µF decoupling capacitor is recommended; this should be positioned close to the VDD pin of the WM7230. A ceramic 0.1µF capacitor with X7R dielectric or better is suitable.

Further information on the WM8994 is provided in the product datasheet, which is available from the Wolfson website. The equivalent connections can be made to other Wolfson devices supporting a digital microphone interface.

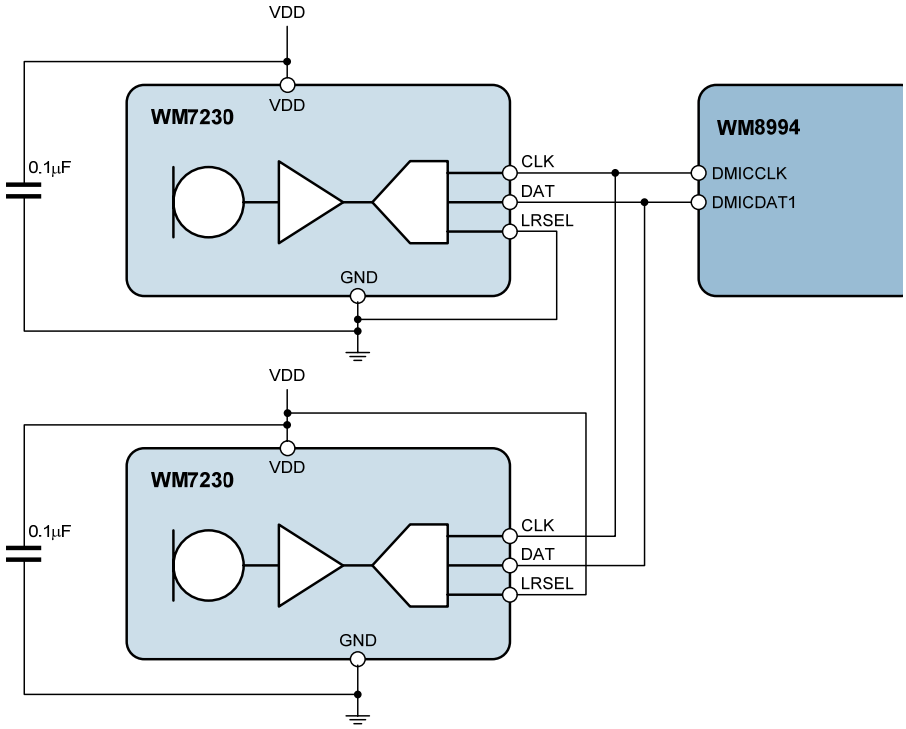


Figure 2 Stereo WM7230 Digital Microphone Connection to WM8994

RECOMMENDED PCB LAND PATTERNS

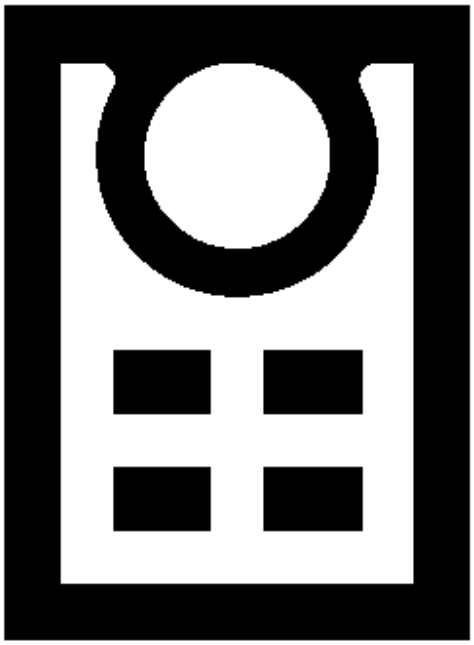
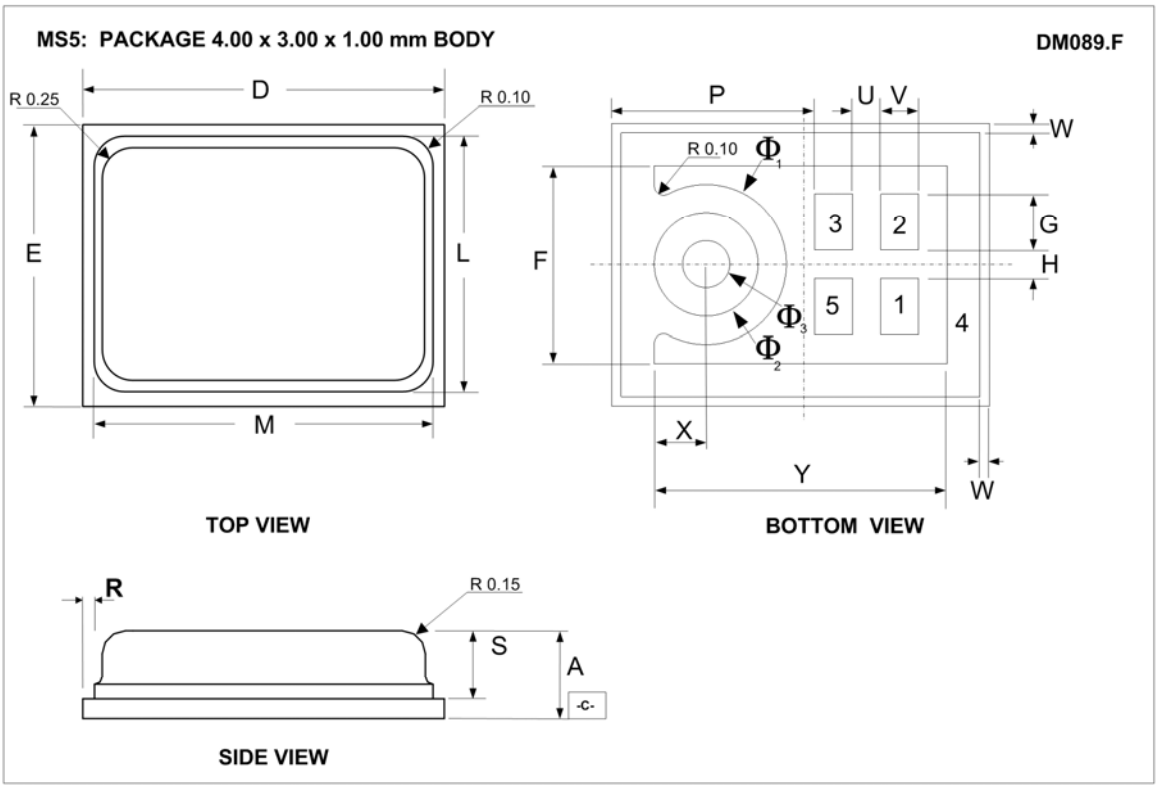


Figure 3 Recommended Customer PCB Land Pattern

(Note that all dimensions can be obtained from the package dimensions)

PACKAGE DIMENSIONS (LGA)



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.90	1.00	1.10	
D	3.90	4.00	4.10	
E	2.90	3.00	3.10	
F		2.10		
G		0.60		
H		0.30		
L	2.75	2.80	2.85	
M	3.75	3.80	3.85	
P		2.15		
R		0.10		
S		0.79		
U		0.30		
V		0.40		
W		0.10		
X		0.55		
Y		3.10		
Φ_1		1.70		
Φ_2		1.10		
Φ_3		0.50		Port Hole

NOTES:
1. THE SEATING PLANE IS REPRESENTED BY PRIMARY DATUM -C-
2. THE DEVIATION FROM THE SEATING PLANE DUE TO WARPAGE OR TWIST IS SPECIFIED AS MAX 50μm (FLATNESS).
3. LID SHOULD BE PARALLEL TO THE SEATING PLANE ±50μm.

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
20/10/10	1.0/2.0	PH	Front page description and features re-worded. Description of LRSEL pin updated. Electrical Characteristics re-ordered, and terminology updated. Microphone interface timing drawing and descriptions updated. Frequency response graph added. Illustration of recommended external components replaced with text. Connection to Wolfson CODEC text and illustration updated. Recommended PCB land patterns moved to Applications Information.
26/10/10	1.0/2.0	JMacD	Package Diagram DM089.D added
23/11/10		CST	Specification of FSR corrected. Specification for THD corrected Time to data valid changed to minimum Grammatical errors
28/01/11	2.0	JMacD	Reel quantity added to order information
01/05/11	2.1	JMacD	Updated the LRSEL pin description , Timing diagram and notes for the rising and falling clock edges. Sleep mode current updated to 2uA Updated the reel quantity Updated the start up time Updated the new freq response and THD curves Updated +3dB frequency cut off Updated VDD to 1.64V
06/09/11	2.1	JMacD	Package Diagram updated to DM089.E. References and dimension letters changed to be consistent with all mems package diagrams. Lid dimensions updated. Swapped dimensions L and E. Added marking area boundary
16/12/11	2.2	KC	Introduced E variant with sensitivity +/-1dB Added E variant ordering info Added voltage range digital input Updated the CODEC to WM8994 Added Reference to WAN_0273
22/06/12	2.3	MR/JMacD	Dynamic Range added, p5 Active mode current changed to 700uA, p1 and p5 CLK cycle time min and max updated, p6 Package Diagram updated to DM089F
08/10/12	2.4	JMacD	Optimised System RF Design added.