WAS7222Q

USB High speed (480Mbps), DPDT Analog Switch **Http//:www.willsemi.com**

Descriptions

The WAS7222Q is a high performance, double pole double throw (DPDT) CMOS analog switch that operates from a single +2.3V to +5.5V power supply.

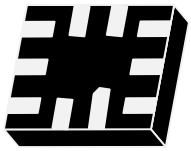
The WAS7222Q is designed for switching of high-speed USB2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os.

The WAS7222Q has low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480Mbps). Each switch is bi-directional and offers little attenuation of the high-speed signals at the outputs. Its bandwidth is quite marginal to pass high-speed USB 2.0 differential signals (480Mbps) with good signal integrity.

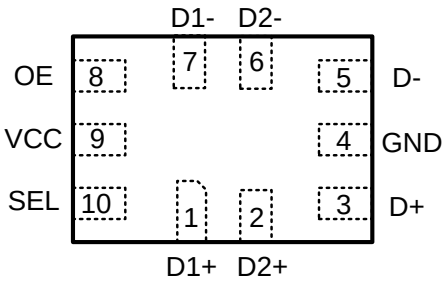
The WAS7222Q is featured with special circuitry on the D+/D-, which allows the device to withstand a VBUS short to D+ or D- when the USB devices are either powered off or on.

The SEL/OE pin has overvoltage protection that allows voltages above VCC, up to 7.0V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage. The WAS7222Q is also featured with smart circuitry to minimize VCC leakage current even when SEL/OE control voltage is lower than VCC supply voltage. In other word, there is no need of additional device to shift SEL/OE level to be the same as that of VCC in real application.

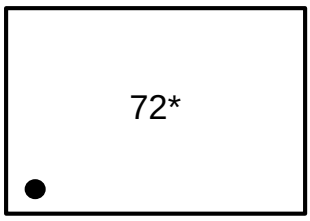
The WAS7222Q is available in QFN1418-10L package. Standard products are Pb-Free and halogen-Free.



QFN1418-10L



Pin configuration (Top view)



Marking

72 = Device code

*** = Month (A~Z)**

Order information

Device	Package	Shipping
WAS7222Q-10/TR	QFN1418-10L	3000/Reel&Tape

Applications

- Cell phones
- MID
- Router
- Other electronics equipments

Features

- Supply voltage : 2.3 ~ 5.5V
- -3dB Bandwidth : 550MHz @ C_L=5pF
- Off isolation : -36dB @ 250MHz
- Crosstalk : -47dB @ 250MHz
- Low quiescent current : <1uA

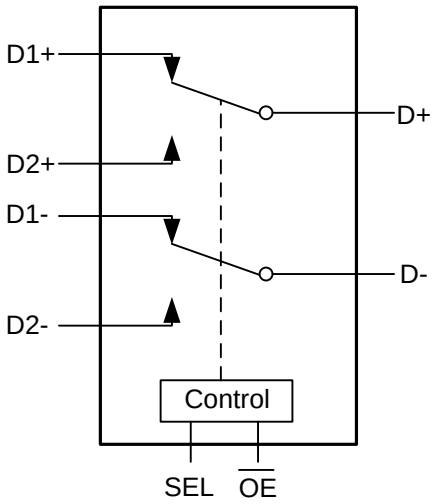
Pin descriptions

Pin Number	Symbol	Descriptions
1	D1+	Port A data 1 terminal, normally closed
2	D2+	Port A data 2 terminal, normally open
3	D+	Port A common data terminal, Connect to D1+ or D2+ according to SEL logic
4	GND	Ground
5	D-	Port B common data terminal, Connect to D1- or D2- according to SEL logic
6	D2-	Port B data 2 terminal, normally open
7	D1-	Port B data 1 terminal, normally closed
8	$\overline{OE}$	Enable control, Active low
9	VCC	Power supply
10	SEL	Switch select pin, digital logic low or high.

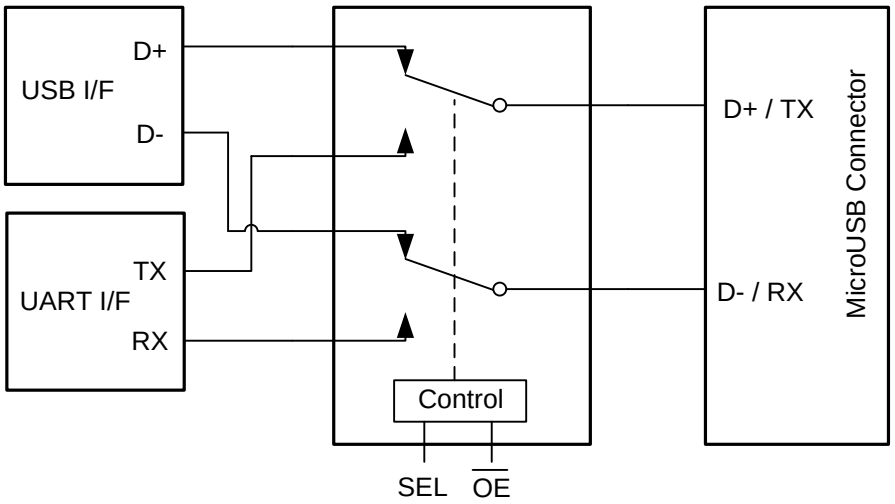
Function descriptions

SEL	$\overline{OE}$	Function
X	H	Bus switch disconnected
L	L	D+ connect to D1+ and D- connect to D1-
H	L	D+ connect to D2+ and D- connect to D2-

Logic symbol and typical applications



Logic Symbol



Typical Applications

Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage range	VCC	-0.5 ~ 6.5	V
Data input/output voltage range	V_{DATA}	-0.5 ~ 6.5	V
Select input voltage range	V_{SEL}	-0.5 ~ 6.5	V
Continues output current	I_{OUT}	±50	mA
Junction temperature range	T_J	150	^oC
Lead temperature range	T_L	260	^oC
Storage temperature range	T_{STG}	-65 ~ 150	^oC
Thermal resistance	$R_{\theta JA}$	250	$^oC/W$
ESD protection (HBM)	I/O to VCC, I/O to GND	±7000	V
	I/O to I/O	±5000	V

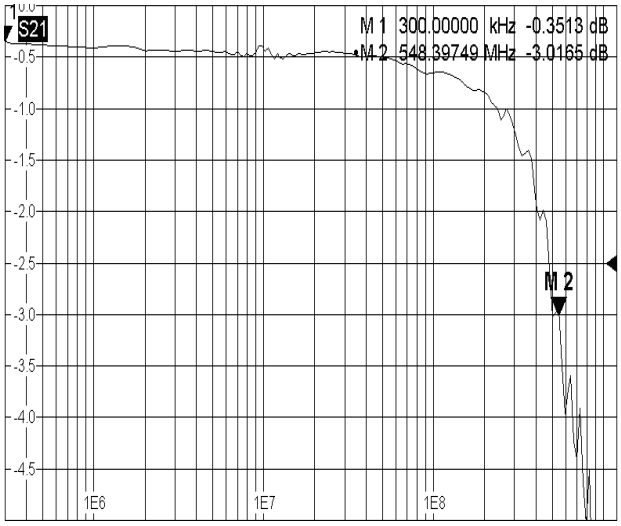
Recommend operating ratings

Parameter	Symbol	Value	Unit
Supply voltage range	VCC	2.3 ~ 5.5	V
Data input/output voltage range	V_{DATA}	0.0 ~ VCC	V
Select input voltage range	V_{SEL}	0.0 ~ VCC	V
Enable control input voltage range	V_{OE}	0.0 ~ VCC	V
Operating temperature range	T_A	-40 ~ 85	^oC

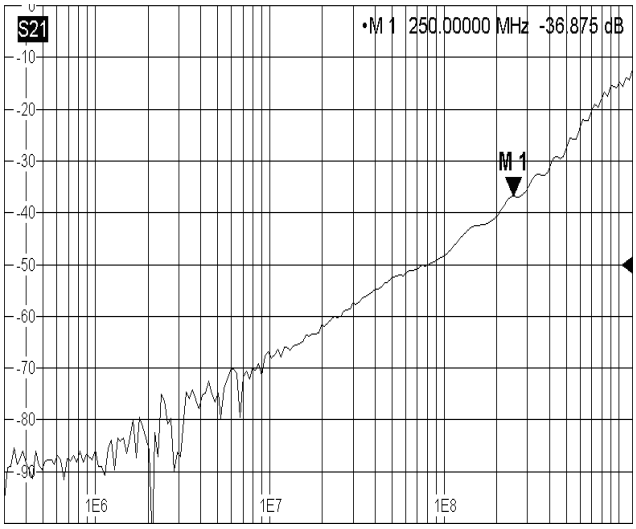
Electronics Characteristics (Ta=25°C, VCC=4.5V, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Select and OE logic high level	V_{IH}	VCC=3.0～4.5	1.7			V
		VCC=2.3～3.0	1.4			V
Select and OE logic low level	V_{IL}	VCC=3.0～4.5			0.6	V
		VCC=2.3～3.0			0.4	V
Supply quiescent current	I_{CC}	I_{OUT}=0, V_{SEL} >1.5V or V_{SEL}<0.7V Refer to figure1			1.0	uA
Select input leakage current	I_{SEL}	V_{SEL}=VCC			±1.0	uA
Off state switch leakage current	I_{OFF}	See figure 2			±1.0	uA
On state switch leakage current	I_{ON}	See figure 3			±1.0	uA
On-Resistance	R_{ON}	VCC=3.0V, V_{DATA}=0~0.4V, I_{OUT}=8mA, See figure 4		5.0	7.5	Ω
On-Resistance match	ΔR_{ON}	VCC=3.0V, V_{DATA}=0~0.4V, I_{OUT}=8mA, See figure 4		0.15	0.20	Ω
On-Resistance flatness	$R_{FLAT(ON)}$	VCC=3.0V, V_{DATA}=0~1.0V, I_{OUT}=8mA, See figure 4		1.8	2.2	Ω
Propagation delay time	T_{PLH} / T_{PHL}	C_L=10pF, R_L=50Ω See figure 5		0.3	1.2	ns
Select input to switch on time	T_{ON}	C_L=10pF, R_L=50Ω See figure 6		75	120	ns
Select input to switch off time	T_{OFF}	C_L=10pF, R_L=50Ω See figure 6		40	80	ns
Break-Before-Make time	T_{BBM}	Generated by design	0.5			ns
-3dB Bandwidth	BW	R_L=50Ω, C_L=5pF		550		MHz
		R_L=50Ω, C_L=0pF		800		
Off isolation	OIRR	R_L=50Ω, F=250MHz		-36		dB
Crosstalk	Xtalk	R_L=50Ω, F=250MHz		-47		dB
Charge injection (Select input to common I/O)	Qg	C_L=0.1nF, VCC=3.3V R_G=0Ω, V_G=GND		5		pC
Select pin input capacitance	C_{IN}	VCC=0V		5		pF
D1n, D2n,Dn Off capacitance	C_{OFF}	VCC=3.3V, $\overline{OE}$=3.3V		5		pF
D1n, D2n,Dn On capacitance	C_{ON}	VCC=3.3V, $\overline{OE}$=0V		6.5		pF

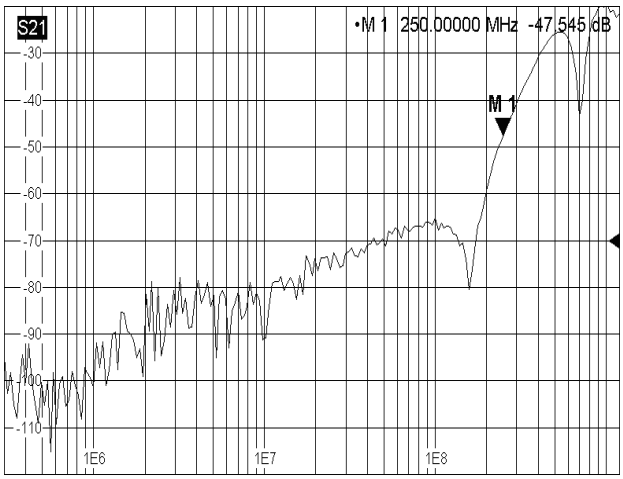
Typical Characteristics (Ta=25°C, VCC=4.5V, unless otherwise noted)



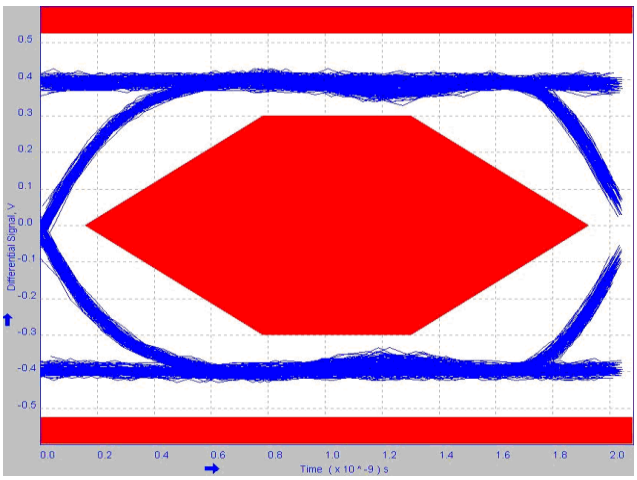
Bandwidth



Off isolation



Crosstalk



Eye Diagram (480Mbps)

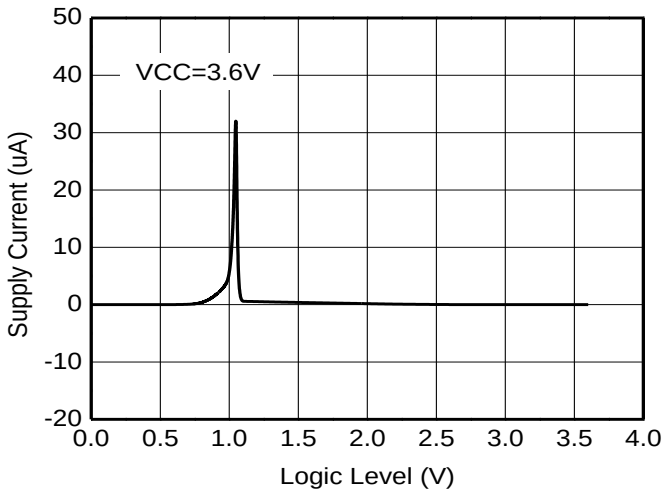
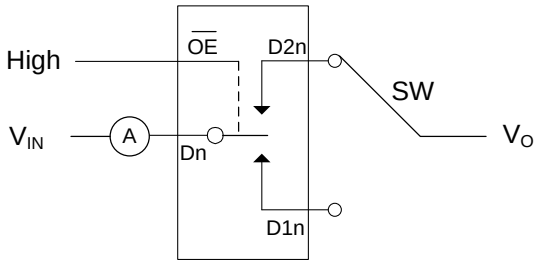


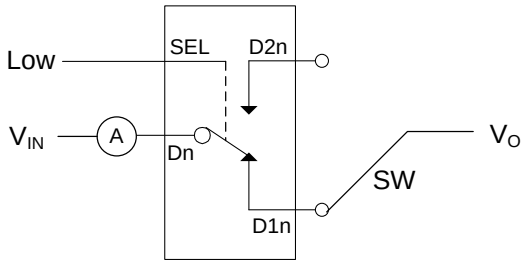
Figure 1: Supply current vs. Logic level

Test Circuit



Conditions：V_{IN}=4.5V, VO=GND

Figure 2: Off state switch leakage current



Conditions：V_{IN}=4.5V，V_O=Open

Figure 3: On state switch leakage current

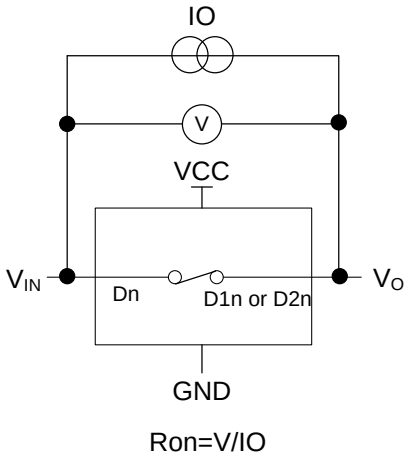


Figure 4: On-Resistance

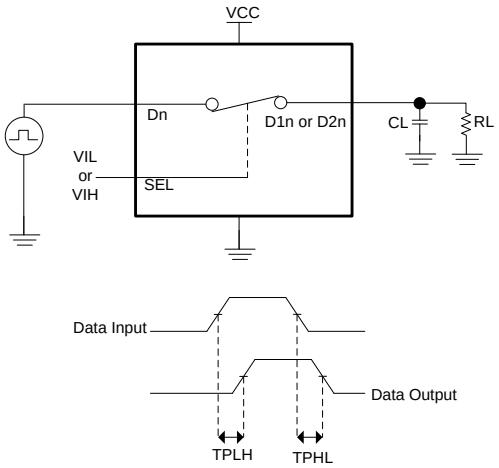
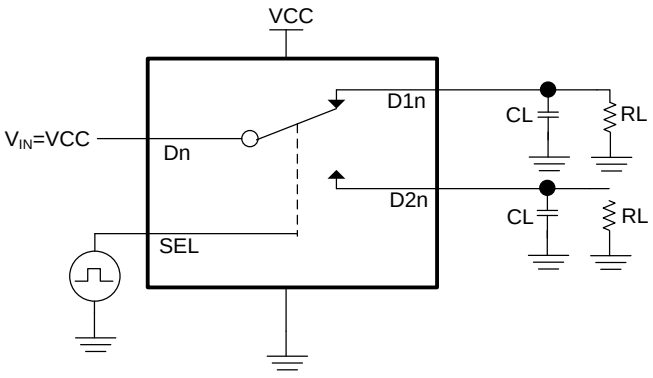


Figure 5: Propagation delay time



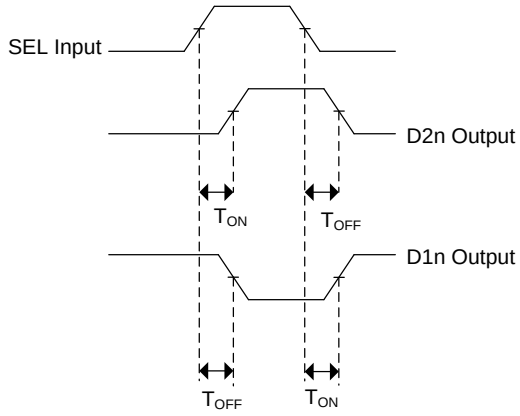
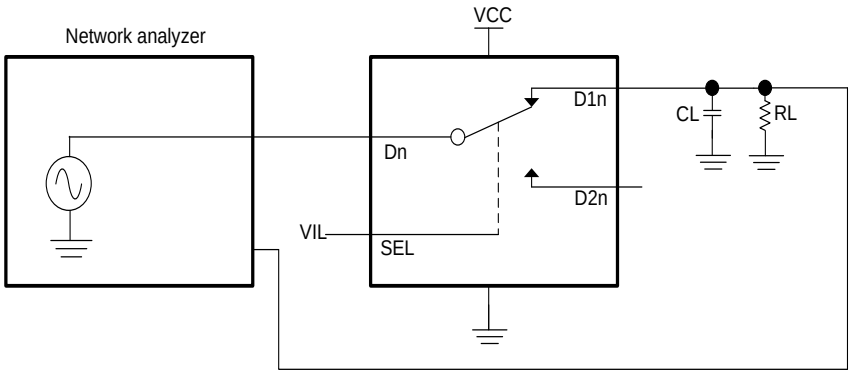
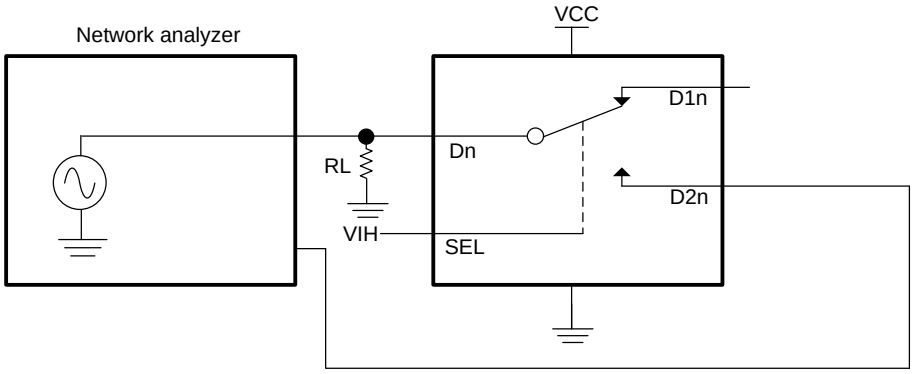


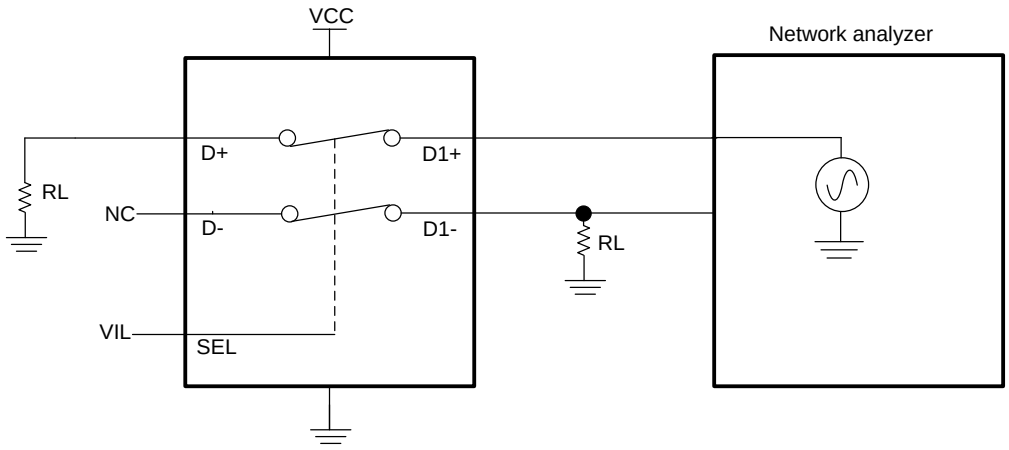
Figure 6: Select input to switch on/off time



Bandwidth (BW)



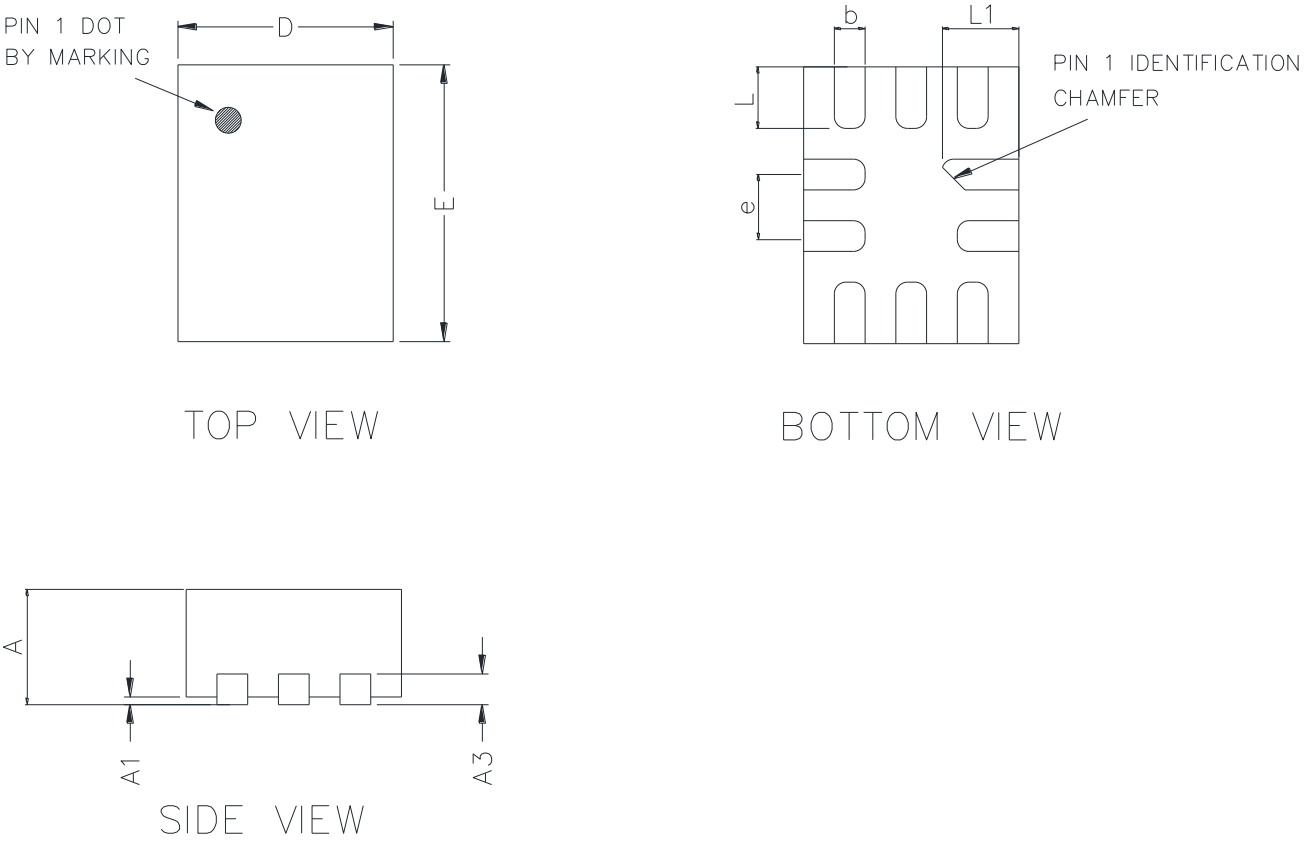
Off isolation (OIRR)



Crosstalk (Xtalk)

PACKAGE OUTLINE DIMENSIONS

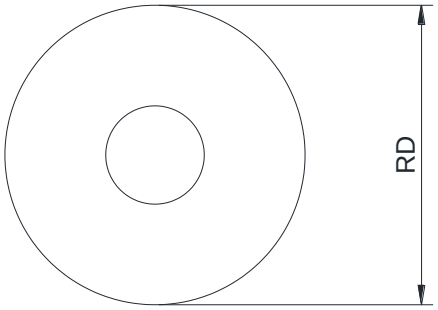
QFN1418-10L



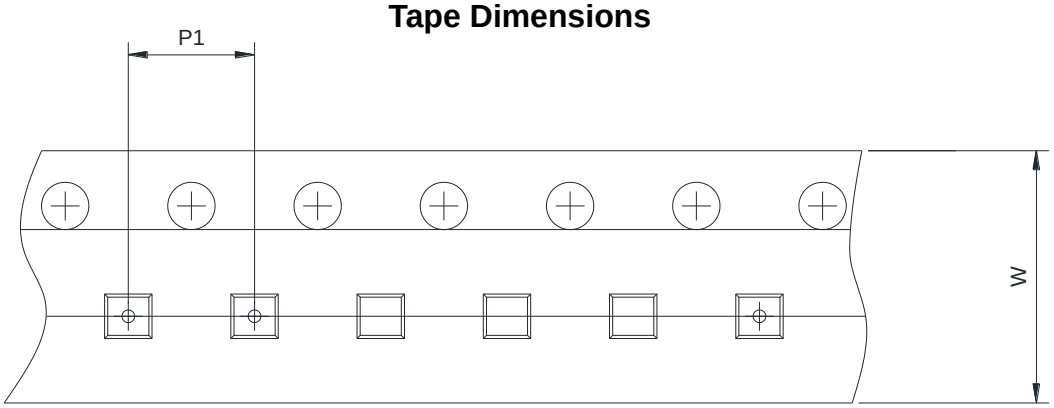
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.00	-	0.05
A3	0.15 Ref.		
D	1.35	1.40	1.45
E	1.75	1.80	1.85
b	0.15	0.20	0.25
L	0.30	0.40	0.50
L1	0.40	0.50	0.60
e	0.40 BSC		

TAPE AND REEL INFORMATION

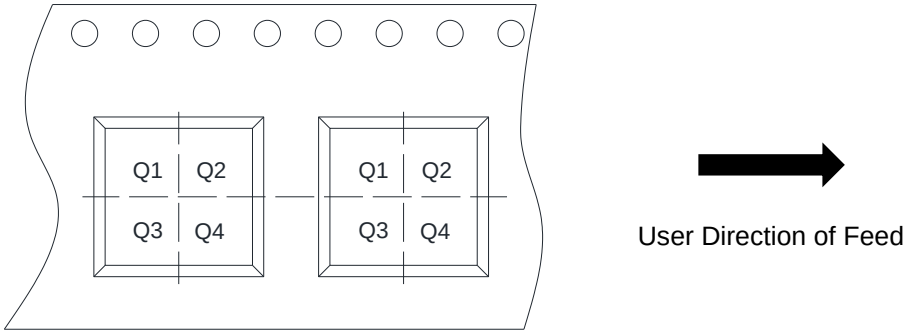
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch ☐ 13inch
W	Overall width of the carrier tape	☑ 8mm ☐ 12mm
P1	Pitch between successive cavity centers	☐ 2mm ☑ 4mm ☐ 8mm
Pin1	Pin1 Quadrant	☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4