



**W83194BR-SD**  
**W83194BG-SD**

**Winbond Clock Generator For  
INTEL P4 Springdale Series Chipset**

Date: Mar./22/2006    Revision: 1.2

# W83194BR-SD/W83194BG-SD



## W83194BR-SD/W83194BG-SD Revision history

| VERSION | DATE       | PAGE     | DESCRIPTION                                                                                         |
|---------|------------|----------|-----------------------------------------------------------------------------------------------------|
|         |            | n.a.     | All of the versions before 0.50 are for internal use.                                               |
| 0.5     | 07/07/03   | n.a.     | First published preliminary version.                                                                |
| 0.6     | 12/18/03   | 7~15, 20 | Correction IC version, add register default value and correction some description and default value |
| 1.0     | 05/05/04   |          | Update on web                                                                                       |
| 1.1     | 4/13/2005  | 23       | Add disclaimer                                                                                      |
| 1.2     | 12/20/2005 |          | Add Lead-free part number                                                                           |
|         |            |          |                                                                                                     |

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## 1. GENERAL DESCRIPTION

The W83194BR-SD is a Clock Synthesizer for Intel P4 Springdale series chipset. W83194BR-SD provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, SRC, PCI, and 3V66 clocks setting. All clocks are externally selectable with smooth transitions.

The W83194BR-SD provides I<sup>2</sup>C serial bus interface to program the registers to enable or disable each clock outputs and provides +/-0.25%, +/-0.5% center type and -0.5%, -1.0% down type spread spectrum or programmable S.S.T. scale to reduce EMI.

The W83194BR-SD also has watchdog timer and reset output pin to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-SD accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

## 2. FEATURES

- 2 pairs current mode differential clock for CPU and Chipset
- 1 pairs current mode differential clock for SRC
- 3 3V66 clock outputs
- 1 3V66/VCH clock output default 66MHz
- 9 PCI synchronous clocks, 3 free running
- 2 48MHz clock outputs for USB and DOT
- 1 24\_48MHz for I/O chip, default 48MHz
- 3 REF 14.318MHz clock outputs
- SRC/AGP/PCI clock out supports synchronous and asynchronous mode
- 3V66 leads PCICLK from 1.5ns to 3.5ns
- I<sup>2</sup>C 2-Wire serial interface supports block and byte mode read/write
- Step-less frequency programming
- Smooth frequency switch with selections from 100 to 400MHz
- Programmable clock outputs Slew rate control and Skew control
- +/- 0.25% center type spread spectrum in table mode
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Watch Dog Timer and RESET# output pins
- 48-pin SSOP package

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## 3. PIN CONFIGURATION

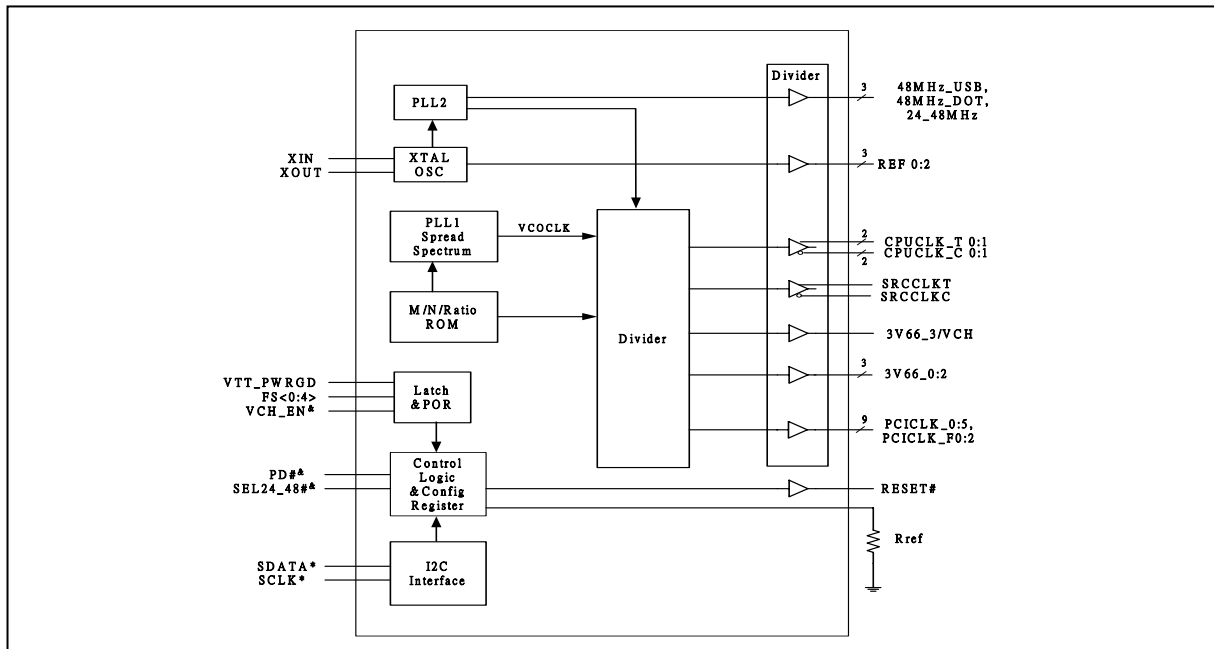
|                     |    |    |                    |
|---------------------|----|----|--------------------|
| FS1*/REF0           | 1  | 48 | VDDA               |
| FS0*/REF1           | 2  | 47 | GND                |
| REF2                | 3  | 46 | IREF               |
| VDDREF              | 4  | 45 | RESET#             |
| XIN                 | 5  | 44 | GND                |
| XOUT                | 6  | 43 | CPUCLKT1           |
| GND                 | 7  | 42 | CPUCLKC1           |
| FS2*/PCICLK_F0      | 8  | 41 | VDDCPU             |
| FS4*/PCICLK_F1      | 9  | 40 | CPUCLKT0           |
| PCICLK_F2           | 10 | 39 | CPUCLKC0           |
| VDDPCI              | 11 | 38 | GND                |
| GND                 | 12 | 37 | SRCCCLKT           |
| PCICLK0             | 13 | 36 | SRCCCLKC           |
| PCICLK1             | 14 | 35 | VDD                |
| PCICLK2             | 15 | 34 | VTT_PWRGD/PD#*     |
| PCICLK3             | 16 | 33 | SDATA*             |
| VDDPCI              | 17 | 32 | SCLK*              |
| GND                 | 18 | 31 | 3V66_0             |
| PCICLK4             | 19 | 30 | 3V66_1             |
| PCICLK5             | 20 | 29 | GND                |
| SEL24_48#*/24_48MHz | 21 | 28 | VDD3V66            |
| FS3*/48MHz_USB      | 22 | 27 | 3V66_2             |
| 48MHz_DOT           | 23 | 26 | 3V66_3/VCH/VCH_EN* |
| GND                 | 24 | 25 | VDD48              |

#: Active low

\*: Internal pull up resistor 120KΩ to VDD

&: Internal Pull-down resistor 120KΩ to GND

## 4. BLOCK DIAGRAM



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## 5. PIN DESCRIPTION

| BUFFER TYPE SYMBOL   | DESCRIPTION                                          |
|----------------------|------------------------------------------------------|
| IN                   | Input                                                |
| IN <sub>td120k</sub> | Latch input pin and internal 120K $\Omega$ pull down |
| IN <sub>tp120k</sub> | Latch input pin and internal 120K $\Omega$ pull up   |
| OUT                  | Output                                               |
| OD                   | Open Drain                                           |
| I/O                  | Bi-directional Pin                                   |
| I/OD                 | Bi-directional Pin, Open Drain                       |
| #                    | Active Low                                           |
| *                    | Internal 120k $\Omega$ pull-up                       |
| &                    | Internal 120k $\Omega$ pull-down                     |

### 5.1 Crystal I/O

| PIN | PIN NAME | TYPE | DESCRIPTION                                                                     |
|-----|----------|------|---------------------------------------------------------------------------------|
| 5   | XIN      | IN   | Crystal input with internal loading capacitors (18pF) and feedback resistors.   |
| 6   | XOUT     | OUT  | Crystal output at 14.318 MHz nominally with internal loading capacitors (18pF). |

### 5.2 CPU, SRC, 3V66, PCI Clock Outputs

| PIN            | PIN NAME                              | TYPE                        | DESCRIPTION                                                                                                                        |
|----------------|---------------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------|
| 40, 43, 39, 42 | CPUCLKT [0:1]<br>CPUCLKC [0:1]        | OUT                         | 0.7V Current mode differential clock outputs for CPU and Chipset.                                                                  |
| 37, 36         | SRCCLKT,<br>SRCCLKC                   | OUT                         | 0.7V Current mode differential clock outputs for Chipset, 100 MHz(default) or 200 MHz outputs selected by I2C register.            |
| 26             | 3V66_3/VCH<br>VCH_EN <sup>&amp;</sup> | OUT<br>IN <sub>td120k</sub> | 66 MHz(default) or 48 MHz outputs selected by hardware trapping data on 26 pin VCH_EN <sup>&amp;</sup> selecting.                  |
| 31, 30, 27     | 3V66_0,<br>3V66_1, 3V66_2             | OUT                         | 3.3V output clocks for the chipset and AGP slot.                                                                                   |
| 8              | PCICLK_F0                             | OUT                         | PCI clock output.                                                                                                                  |
|                | FS2 <sup>&amp;</sup>                  | IN <sub>td120k</sub>        | Latched input for FS2 at initial power up for H/W selecting the output frequency clocks. This is internal 120K $\Omega$ pull down. |

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## CLOCK GEN. FOR INTEL P4 SPRINGDALE/PRESCOTT SERIES CHIPSET

CPU, SRC, 3V66, PCI Clock Outputs continued

| PIN                       | PIN NAME             | TYPE                 | DESCRIPTION                                                                                                                |
|---------------------------|----------------------|----------------------|----------------------------------------------------------------------------------------------------------------------------|
| 9                         | PCICLK7_F1           | OUT                  | PCI clock output.                                                                                                          |
|                           | FS4 <sup>&amp;</sup> | IN <sub>td120k</sub> | Latched input for FS4 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull down. |
| 10                        | PCICLK_F2            | OUT                  | PCI clock outputs.                                                                                                         |
| 13, 14, 15,<br>16, 19, 20 | PCICLK [0:5]         | OUT                  | PCI clock outputs.                                                                                                         |

### 5.3 Fixed Frequency Outputs

| PIN | PIN NAME                   | TYPE                 | DESCRIPTION                                                                                                                                                |
|-----|----------------------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | REF0                       | OUT                  | 14.318 MHz output.                                                                                                                                         |
|     | FS1*                       | IN <sub>tp120k</sub> | Latched input for FS1 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull up.                                   |
| 2   | REF1                       | OUT                  | 14.318 MHz output.                                                                                                                                         |
|     | FS0*                       | IN <sub>tp120k</sub> | Latched input for FS0 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull up.                                   |
| 3   | REF2                       | OUT                  | 14.318 MHz output.                                                                                                                                         |
| 21  | 24_48 MHz                  | OUT                  | 48 MHz clock output.                                                                                                                                       |
|     | SEL24_48# <sup>&amp;</sup> | IN <sub>td120k</sub> | Latched input at initial power up for 24_48 MHz selecting the output frequency clocks. This is internal 120KΩ pull down, 1 = 24 MHz, 0 = 48 MHz (default). |
| 22  | 48 MHz_USB                 | OUT                  | 48 MHz clock output.                                                                                                                                       |
|     | FS3 <sup>&amp;</sup>       | IN <sub>td120k</sub> | Latched input for FS3 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull down.                                 |
| 23  | 48 MHz_DOT                 | OUT                  | 48 MHz clock output.                                                                                                                                       |

### 5.4 I2C Control Interface

| PIN | PIN NAME | TYPE | DESCRIPTION                                                                               |
|-----|----------|------|-------------------------------------------------------------------------------------------|
| 33  | SDATA*   | I/OD | Serial data of I <sup>2</sup> C 2-wire control interface with internal pull-up resistor.  |
| 32  | SCLK*    | IN   | Serial clock of I <sup>2</sup> C 2-wire control interface with internal pull-up resistor. |

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## 5.5 Output Control Pins

| PIN                | PIN NAME              | TYPE           | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                             |                    |                   |                |         |         |                       |              |           |
|--------------------|-----------------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-------------------|----------------|---------|---------|-----------------------|--------------|-----------|
| 46                 | IREF                  | IN             | Deciding the reference current for the CPUCLK pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current. The table is show as follows. <table border="1"> <tr> <th>Board Target Trace</th><th>Reference R, Iref</th><th>Output Current</th><th>Ioh @ Z</th></tr> <tr> <td>50 Ohms</td><td>R = 475 Iref = 2.32mA</td><td>Ioh = 6*Iref</td><td>0.7V @ 50</td></tr> </table> | Board Target Trace | Reference R, Iref | Output Current | Ioh @ Z | 50 Ohms | R = 475 Iref = 2.32mA | Ioh = 6*Iref | 0.7V @ 50 |
| Board Target Trace | Reference R, Iref     | Output Current | Ioh @ Z                                                                                                                                                                                                                                                                                                                                                                                                                 |                    |                   |                |         |         |                       |              |           |
| 50 Ohms            | R = 475 Iref = 2.32mA | Ioh = 6*Iref   | 0.7V @ 50                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                   |                |         |         |                       |              |           |
| 45                 | RESET#                | OD             | System reset signal when the watchdog is time out. This pin will generate 250 mS when the watchdog timer is timeout.                                                                                                                                                                                                                                                                                                    |                    |                   |                |         |         |                       |              |           |
| 34                 | VTT_PWRGD             | IN             | Power good input signal comes from ACPI with high active. This 3.3V input is level sensitive strobe used to determine FS [4:0] input are valid and is ready to sample. This pin is high active.                                                                                                                                                                                                                         |                    |                   |                |         |         |                       |              |           |
|                    | PD#*                  | IN             | Power Down Function. This is internal 120KΩ pull up. This is multi-function pin. When the VTT_PWRGD signal is asserted (this is, turns from a logical Low to high), the pin will be switched into the function of power down (PD#).                                                                                                                                                                                     |                    |                   |                |         |         |                       |              |           |

## 5.6 Power an GND Pins

| PIN                           | PIN NAME | TYPE | DESCRIPTION                    |
|-------------------------------|----------|------|--------------------------------|
| 4                             | VDDREF   | PWR  | 3.3V power supply for REF.     |
| 11, 17                        | VDDPCI   | PWR  | 3.3V power supply for PCI.     |
| 25                            | VDD48    | PWR  | 3.3V power supply for 48 MHz.  |
| 28                            | VDD3V66  | PWR  | 3.3V power supply for 3V66.    |
| 35                            | VDD      | PWR  | 3.3V power supply.             |
| 41                            | VDDCPU   | PWR  | 3.3V power supply for CPU.     |
| 48                            | VDDA     | PWR  | 3.3V power supply analog core. |
| 7, 12, 18, 24, 29, 38, 44, 47 | GND      | PWR  | Ground pin for 3.3 V           |

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## 6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3).

| FS4 | FS3 | FS2 | FS1 | FS0 | CPU (MHZ) | SRC (MHZ) | 3V66(MHZ) | PCI (MHZ) |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|
| 0   | 0   | 0   | 0   | 0   | 100.0     | 100/200   | 66.6      | 33.3      |
| 0   | 0   | 0   | 0   | 1   | 200.0     | 100/200   | 66.6      | 33.3      |
| 0   | 0   | 0   | 1   | 0   | 133.3     | 100/200   | 66.6      | 33.3      |
| 0   | 0   | 0   | 1   | 1   | 166.6     | 100/200   | 66.6      | 33.3      |
| 0   | 0   | 1   | 0   | 0   | 200.0     | 100/200   | 66.6      | 33.3      |
| 0   | 0   | 1   | 0   | 1   | 400.0     | 100/200   | 66.6      | 33.3      |
| 0   | 0   | 1   | 1   | 0   | 266.6     | 100/200   | 66.6      | 33.3      |
| 0   | 0   | 1   | 1   | 1   | 333.3     | 100/200   | 66.6      | 33.3      |
| 0   | 1   | 0   | 0   | 0   | 100.9     | 100/200   | 66.6      | 33.3      |
| 0   | 1   | 0   | 0   | 1   | 202       | 100/200   | 66.6      | 33.3      |
| 0   | 1   | 0   | 1   | 0   | 134.6     | 100/200   | 66.6      | 33.3      |
| 0   | 1   | 0   | 1   | 1   | 168.3     | 100/200   | 66.6      | 33.3      |
| 0   | 1   | 1   | 0   | 0   | 115       | 100/200   | 66.6      | 33.3      |
| 0   | 1   | 1   | 0   | 1   | 230       | 100/200   | 66.6      | 33.3      |
| 0   | 1   | 1   | 1   | 0   | 153.3     | 100/200   | 66.6      | 33.3      |
| 0   | 1   | 1   | 1   | 1   | 191.6     | 100/200   | 66.6      | 33.3      |
| 1   | 0   | 0   | 0   | 0   | 100       | 100/200   | 66.6      | 33.3      |
| 1   | 0   | 0   | 0   | 1   | 200       | 100/200   | 66.6      | 33.3      |
| 1   | 0   | 0   | 1   | 0   | 133.3     | 100/200   | 66.6      | 33.3      |
| 1   | 0   | 0   | 1   | 1   | 166.6     | 100/200   | 66.6      | 33.3      |
| 1   | 0   | 1   | 0   | 0   | 200       | 100/200   | 66.6      | 33.3      |
| 1   | 0   | 1   | 0   | 1   | 400       | 100/200   | 66.6      | 33.3      |
| 1   | 0   | 1   | 1   | 0   | 266.6     | 100/200   | 66.6      | 33.3      |
| 1   | 0   | 1   | 1   | 1   | 333.3     | 100/200   | 66.6      | 33.3      |
| 1   | 1   | 0   | 0   | 0   | 105       | 100/200   | 66.6      | 33.3      |
| 1   | 1   | 0   | 0   | 1   | 210       | 100/200   | 66.6      | 33.3      |
| 1   | 1   | 0   | 1   | 0   | 140       | 100/200   | 66.6      | 33.3      |
| 1   | 1   | 0   | 1   | 1   | 175       | 100/200   | 66.6      | 33.3      |
| 1   | 1   | 1   | 0   | 0   | 110       | 100/200   | 66.6      | 33.3      |
| 1   | 1   | 1   | 0   | 1   | 220       | 100/200   | 66.6      | 33.3      |
| 1   | 1   | 1   | 1   | 0   | 146.6     | 100/200   | 66.6      | 33.3      |
| 1   | 1   | 1   | 1   | 1   | 183.3     | 100/200   | 66.6      | 33.3      |

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## 7. I<sup>2</sup>C CONTROL AND STATUS REGISTERS

(The register No. Is increased by 1 if use byte data read/write protocol)

### 7.1 Register 0: Frequency Select (Default =10H)

| BIT | NAME         | PWD | DESCRIPTION                                                                                                                                                      |
|-----|--------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SSEL [4]     | 0   | Software frequency table selection through I <sup>2</sup> C                                                                                                      |
| 6   | SSEL [3]     | 0   |                                                                                                                                                                  |
| 5   | SSEL [2]     | 0   |                                                                                                                                                                  |
| 4   | SSEL [1]     | 1   |                                                                                                                                                                  |
| 3   | SSEL [0]     | 0   |                                                                                                                                                                  |
| 2   | EN_SSEL      | 0   | Enable software table selection FS [4:0].<br>0 = Hardware table setting (Jump mode).<br>1 = Software table setting through Bit7~3. (Jump less mode)              |
| 1   | SPSPEN       | 0   | Enable spread spectrum mode under clock output.<br>0 = Spread Spectrum mode disable<br>1 = Spread Spectrum mode enable                                           |
| 0   | EN_SAFE_FREQ | 0   | After watchdog timeout<br>0 = Reload the hardware FS [4:0] latched pins setting.<br>1 = Reload the desirable frequency table selection defined at Reg-5 Bit 4~0. |

### 7.2 Register 1: SRC/CPU Clock (1 = Enable, 0 = Disable) (Default = E3H)

| BIT | NAME                 | PWD | DESCRIPTION                                                   |
|-----|----------------------|-----|---------------------------------------------------------------|
| 7   | SRCCLKT<br>SRCCLKC   | 1   | Pin 37,36 SRCCLK T/C output control                           |
| 6   | CPUCLKT1<br>CPUCLKC1 | 1   | Pin 43,42 CPUCLKT1/C1 output control                          |
| 5   | CPUCLKT0<br>CPUCLKC0 | 1   | Pin 40,39 CPUCLKT0/C0 output control                          |
| 4   | FS4                  | X   | Power on latched value of FS4 (9) pin, Default 0 (Read only)  |
| 3   | FS3                  | X   | Power on latched value of FS3 (22) pin. Default 0 (Read only) |
| 2   | FS2                  | X   | Power on latched value of FS2 (8) pin. Default 0 (Read only)  |
| 1   | FS1                  | X   | Power on latched value of FS1 (1) pin. Default 1 (Read only)  |
| 0   | FS0                  | X   | Power on latched value of FS0 (2) pin. Default 1 (Read only)  |

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### 7.3 Register 2: PCI Clock (1 = Enable, 0 = Disable) (Default = FFH)

| BIT | NAME    | PWD | DESCRIPTION                  |
|-----|---------|-----|------------------------------|
| 7   | PCI_F2  | 1   | Pin 10 PCI_F2 output control |
| 6   | PCI_F1  | 1   | Pin 9 PCI_F1 output control  |
| 5   | PCI_F0  | 1   | Pin 8 PCI_F0 output control  |
| 4   | Reserve | 1   | Reserved                     |
| 3   | PCI_5   | 1   | Pin 20 PCI5 output control   |
| 2   | PCI_4   | 1   | Pin 19 PCI4 output control   |
| 1   | Reserve | 1   | Reserved                     |
| 0   | PCI3    | 1   | Pin 16 PCI3 output control   |

### 7.4 Register 3: PCI, 3V66 Clock (1 = Enable, 0 = Disable) (Default = EFH)

| BIT | NAME   | PWD | DESCRIPTION                                                                                                                                                    |
|-----|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | PCI2   | 1   | Pin 15 PCI2 output control                                                                                                                                     |
| 6   | PCI1   | 1   | Pin 14 PCI1 output control                                                                                                                                     |
| 5   | PCI0   | 1   | Pin 13 PCI0 output control                                                                                                                                     |
| 4   | VCH_EN | X   | Pin 26 3V66_3 / VCH output select<br>1: VCH output, 0: 3V66 output (Default)<br>Default value follow hardware trapping data on VCH_EN <sup>&amp;</sup> pin 26. |
| 3   | 3V66_3 | 1   | Pin 26 3V66_3 / VCH output control                                                                                                                             |
| 2   | 3V66_2 | 1   | Pin 27 3V66_2 output control                                                                                                                                   |
| 1   | 3V66_1 | 1   | Pin 30 3V66_1 output control                                                                                                                                   |
| 0   | 3V66_0 | 1   | Pin 31 3V66_0 output control                                                                                                                                   |

### 7.5 Register 4: 24\_48 MHz, REF Control (1 = Enable, 0 = Disable) (Default = FCH)

| BIT | NAME      | PWD | DESCRIPTION                     |
|-----|-----------|-----|---------------------------------|
| 7   | 24_48 MHz | 1   | Pin 21 24_48 MHz output control |
| 6   | DOT48     | 1   | Pin 23 DOT48 output control     |
| 5   | USB48     | 1   | Pin 22 USB48 output control     |
| 4   | REF2      | 1   | Pin 3 REF2 output control       |
| 3   | REF1      | 1   | Pin 2 REF1 output control       |
| 2   | REF0      | 1   | Pin 1 REF0 output control       |
| 1   | MODE1     | 0   | Clock output mode selection     |
| 0   | MODE0     | 0   | Refer to Table-1                |

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Table-1: Clock output mode selection

| MODE               | NORMAL MODE              | CPU OVER CLOCK MODE           | CPU/SRC OVER CLOCK MODE       |
|--------------------|--------------------------|-------------------------------|-------------------------------|
| MODE1/0            | 00                       | 01                            | 10                            |
| CPU over clock     | Byte 8 & 9               | Byte 8 & 9                    | Byte 8 & 9                    |
| SRC over clock     | Byte 8 & 9               | Byte 4 & 10<br>(asynchronous) | Byte 8 & 9                    |
| AGP/PCI over clock | Byte 8 & 9               | Byte 4 & 10<br>(asynchronous) | Byte 4 & 10<br>(asynchronous) |
| Spreading          | All clocks are Effective | CPU is effective Only.        | CPU and SRC are Effective.    |

## 7.6 Register 5: Watchdog Control (Default = 00H)

| BIT | NAME         | PWD | DESCRIPTION                                                                                                                                                                                                             |
|-----|--------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SEL24        | X   | Pin 21 24 / 48 MHz output selection<br>1: 24 MHz, 0: 48 MHz. (Default)<br>Default value follow hardware trapping data on SEL24_48# pin.                                                                                 |
| 6   | EN_WD        | 0   | Program this bit =><br>1: Enable Watchdog Timer feature.<br>0: Disable Watchdog Timer feature.<br>Read-back this bit =><br>During timer count down the bit read back to 1.<br>If count to zero, this bit read back to 0 |
| 5   | WD_TIMEOUT   | 0   | Read Back only. Timeout Flag.<br>1: Watchdog has ever started and counts to zero.<br>0: Watchdog is restarted and counting.                                                                                             |
| 4   | SAF_FREQ [4] | 0   | These bits will be reloaded in Reg-0 to select frequency table. As the watchdog is timeout and EN_SAFE_FREQ = 1.                                                                                                        |
| 3   | SAF_FREQ [3] | 0   |                                                                                                                                                                                                                         |
| 2   | SAF_FREQ [2] | 0   |                                                                                                                                                                                                                         |
| 1   | SAF_FREQ [1] | 0   |                                                                                                                                                                                                                         |
| 0   | SAF_FREQ [0] | 0   |                                                                                                                                                                                                                         |

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## 7.7 Register 6: Watchdog Timer (Default =08H)

| BIT | NAME        | PWD | DESCRIPTION                                                                                                                                                                                             |
|-----|-------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | WD_TIME [7] | 0   | Setting the down count depth. One bit resolution represents 250 mS. Default time depth is 8*250 mS = 2.0 second. If the watchdog timer is counting, this register will return present down count value. |
| 6   | WD_TIME [6] | 0   |                                                                                                                                                                                                         |
| 5   | WD_TIME [5] | 0   |                                                                                                                                                                                                         |
| 4   | WD_TIME [4] | 0   |                                                                                                                                                                                                         |
| 3   | WD_TIME [3] | 1   |                                                                                                                                                                                                         |
| 2   | WD_TIME [2] | 0   |                                                                                                                                                                                                         |
| 1   | WD_TIME [1] | 0   |                                                                                                                                                                                                         |
| 0   | WD_TIME [0] | 0   |                                                                                                                                                                                                         |

## 7.8 Register 7: Asynchronous Program (Default = 40H)

| BIT | NAME      | PWD | DESCRIPTION                                                                 |
|-----|-----------|-----|-----------------------------------------------------------------------------|
| 7   | Tri-state | 0   | Tri-state all output if set 1                                               |
| 6   | Reserve   | 1   | Reserved                                                                    |
| 5   | Reserve   | 0   | Reserved                                                                    |
| 4   | Reserve   | 0   | Reserved                                                                    |
| 3   | Reserve   | 0   | Reserved                                                                    |
| 2   | Reserve   | 0   | Reserved                                                                    |
| 1   | ASEL<1>   | 0   | Asynchronous AGP/PCI frequency table selection                              |
| 0   | ASEL<0>   | 0   | ASEL<1:0><br>00: 66.6 MHz      01:72.1 MHz<br>10: 79.9 MHz      11:68.7 MHz |

## 7.9 Register 8: M/N Program (Default = 8AH)

| BIT | NAME      | PWD | DESCRIPTION                                                           |
|-----|-----------|-----|-----------------------------------------------------------------------|
| 7   | N_DIV [8] | 1   | Programmable N divisor value. Bit 7 ~0 are defined in the Register 8. |
| 6   | M_DIV [6] | 0   | Programmable M divisor value.                                         |
| 5   | M_DIV [5] | 0   |                                                                       |
| 4   | M_DIV [4] | 0   |                                                                       |
| 3   | M_DIV [3] | 1   |                                                                       |
| 2   | M_DIV [2] | 0   |                                                                       |
| 1   | M_DIV [1] | 1   |                                                                       |
| 0   | M_DIV [0] | 0   |                                                                       |

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### 7.10 Register 9: M/N Program (Default = CEH)

| BIT | NAME      | PWD | DESCRIPTION                                                                 |
|-----|-----------|-----|-----------------------------------------------------------------------------|
| 7   | N_DIV [7] | 1   | Programmable N divisor value bit 7 ~ 0. The bit 8 is defined in Register 7. |
| 6   | N_DIV [6] | 1   |                                                                             |
| 5   | N_DIV [5] | 0   |                                                                             |
| 4   | N_DIV [4] | 0   |                                                                             |
| 3   | N_DIV [3] | 1   |                                                                             |
| 2   | N_DIV [2] | 1   |                                                                             |
| 1   | N_DIV [1] | 1   |                                                                             |
| 0   | N_DIV [0] | 0   |                                                                             |

### 7.11 Register 10: M/N Program (Default = 13H)

| BIT | NAME    | PWD | DESCRIPTION                                                          |
|-----|---------|-----|----------------------------------------------------------------------|
| 7   | Reserve | 0   | Reserved                                                             |
| 6   | N3<6>   | 0   | Programmable N3 divisor bit 6 ~ 0 for synchronism SRC/AGP/PCI clock. |
| 5   | N3<5>   | 0   |                                                                      |
| 4   | N3<4>   | 1   |                                                                      |
| 3   | N3<3>   | 0   |                                                                      |
| 2   | N3<2>   | 0   |                                                                      |
| 1   | N3<1>   | 1   |                                                                      |
| 0   | N3<0>   | 1   |                                                                      |

### 7.12 Register 11: Spread Spectrum Programming (Default = 2FH)

| BIT | NAME        | PWD | DESCRIPTION                                                                                                                    |
|-----|-------------|-----|--------------------------------------------------------------------------------------------------------------------------------|
| 7   | SP_UP [3]   | 0   | Spread Spectrum Up Counter bit 3 ~ bit 0.                                                                                      |
| 6   | SP_UP [2]   | 0   |                                                                                                                                |
| 5   | SP_UP [1]   | 1   |                                                                                                                                |
| 4   | SP_UP [0]   | 0   |                                                                                                                                |
| 3   | SP_DOWN [3] | 1   | Spread Spectrum Down Counter bit 3 ~ bit 0<br>2's complement representation.<br>Ex: 1 -> 1111; 2 -> 1110; 7 -> 1001; 8 -> 1000 |
| 2   | SP_DOWN [2] | 1   |                                                                                                                                |
| 1   | SP_DOWN [1] | 1   |                                                                                                                                |
| 0   | SP_DOWN [0] | 1   |                                                                                                                                |

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## 7.13 Register 12: Divider Ratio (Default = C6H)

| BIT | NAME  | PWD | DESCRIPTION                                                                      |
|-----|-------|-----|----------------------------------------------------------------------------------|
| 7   | SRC_H | 1   | SRC frequency select, 1: 100 MHz, 0: 200 MHz                                     |
| 6   | DS9   | 1   | Define the AGP divider ratio,<br>Table-2 integrate the all divider configuration |
| 5   | DS5   | 0   | Define the AGP divider ratio                                                     |
| 4   | DS4   | 0   | Table-2 integrate the all divider configuration                                  |
| 3   | DS3   | 0   | Define the SRC divider ratio                                                     |
| 2   | DS2   | 1   | Refer to Table-2                                                                 |
| 1   | DS1   | 1   | Define the SRC divider ratio                                                     |
| 0   | DS0   | 0   | Refer to Table-2                                                                 |

Table-2 CPU, SRC, AGP, PCI divider ratio selection Table

| <div> <div>MSB</div> <div>LSB</div> </div> |   | CPU  |      | SRC  |      | AGP     |       |       |       |
|--------------------------------------------|---|------|------|------|------|---------|-------|-------|-------|
|                                            |   | Bit0 |      | Bit2 |      | Bit5, 4 |       |       |       |
|                                            |   | 0    | 1    | 0    | 1    | 00      | 01    | 10    | 11    |
| Bit1/<br>Bit3/Bit6                         | 0 | Div2 | Div3 | Div2 | Div3 | Div5    | Div6  | Div7  | Div8  |
|                                            | 1 | Div4 | Div5 | Div4 | Div5 | Div10   | Div12 | Div12 | Div12 |

## 7.14 Register 13: Control (Default = 0FH)

| BIT | NAME       | PWD | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                          |
|-----|------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | EN_MN_PROG | 0   | 0: Output frequency depend on frequency table<br>1: Program all clock frequency by changing M/N value<br>The equation is $VCO = 14.318MHz * (N+4) / M$ .<br>Once the watchdog timer timeout, the bit will be clear. Then the frequency will be decided by hardware default FS<4:0> or desired frequency select SAF_FREQ [4:0] depend on EN_SAFE_FREQ (Reg9 - bit 7). |
| 6   | Reserve    | 0   | Reserved                                                                                                                                                                                                                                                                                                                                                             |
| 5   | Reserve    | 0   |                                                                                                                                                                                                                                                                                                                                                                      |
| 4   | Reserve    | 0   |                                                                                                                                                                                                                                                                                                                                                                      |
| 3   | IVAL<3>    | 1   | Charge pump current selection                                                                                                                                                                                                                                                                                                                                        |
| 2   | IVAL<2>    | 1   |                                                                                                                                                                                                                                                                                                                                                                      |
| 1   | IVAL<1>    | 1   |                                                                                                                                                                                                                                                                                                                                                                      |
| 0   | IVAL<0>    | 1   |                                                                                                                                                                                                                                                                                                                                                                      |

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### 7.15 Register 14: Control (Default = 27H)

| BIT | NAME      | PWD | DESCRIPTION                                                                                                                                                                 |
|-----|-----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | CPUT_DRI  | 0   | CPUT output state in during POWER DOWN or Stop mode assertion.<br>1: Driven (2*Iref), 0: Tristate (Floating)<br>CPUC always tri-state (floating) in power down Assertion.   |
| 6   | SRCT_DRI  | 0   | SRC_T output state in during POWER DOWN or Stop mode assertion.<br>1: Driven (6*Iref), 0: Tristate (Floating)<br>SRC_C always tri-state (floating) in power down Assertion. |
| 5   | SPCNT [5] | 1   | Spread Spectrum Programmable time, the resolution is 280ns.<br>Default period is 11.8us                                                                                     |
| 4   | SPCNT [4] | 0   |                                                                                                                                                                             |
| 3   | SPCNT [3] | 0   |                                                                                                                                                                             |
| 2   | SPCNT [2] | 1   |                                                                                                                                                                             |
| 1   | SPCNT [1] | 1   |                                                                                                                                                                             |
| 0   | SPCNT [0] | 1   |                                                                                                                                                                             |

### 7.16 Register 15: Control (Default =3CH)

| BIT | NAME      | PWD | DESCRIPTION                                                                                                       |
|-----|-----------|-----|-------------------------------------------------------------------------------------------------------------------|
| 7   | INV_CPU   | 0   | Invert the CPU phase 0: Default, 1: Inverse                                                                       |
| 6   | Reserve   | 0   | Reserved                                                                                                          |
| 5   | Reserve   | 1   | Reserved                                                                                                          |
| 4   | SPSP1     | 1   | Spread Spectrum type select.<br>00: Down 1%<br>01: Down 0.5%<br>10: Center $\pm 0.5\%$<br>11: Center $\pm 0.25\%$ |
| 3   | SPSP0     | 1   |                                                                                                                   |
| 2   | ASKEW [2] | 1   |                                                                                                                   |
| 1   | ASKEW [1] | 0   |                                                                                                                   |
| 0   | ASKEW [0] | 0   | CPU to AGP skew control.                                                                                          |

### 7.17 Register 16: Control (Default = 24H)

| BIT | NAME    | PWD | DESCRIPTION                                 |
|-----|---------|-----|---------------------------------------------|
| 7   | INV_AGP | 0   | Invert the AGP phase 0: Default, 1: Inverse |
| 6   | INV_PCI | 0   | Invert the PCI phase 0: Default, 1: Inverse |

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Register 16: Control (Default = 24H), continued

| BIT | NAME      | PWD | DESCRIPTION             |
|-----|-----------|-----|-------------------------|
| 5   | SSKEW [2] | 1   | CPU to SRC skew control |
| 4   | SSKEW [1] | 0   |                         |
| 3   | SSKEW [0] | 0   |                         |
| 2   | PSKEW [2] | 1   | CPU to PCI skew control |
| 1   | PSKEW [1] | 0   |                         |
| 0   | PSKEW [0] | 0   |                         |

### 7.18 Register 17: Slew Rate Control (Default = 00H)

| BIT | NAME      | PWD | DESCRIPTION                         |
|-----|-----------|-----|-------------------------------------|
| 7   | PCI_F2_S2 | 0   | PCI_F2 slew rate control            |
| 6   | PCI_F2_S1 | 0   | 11: Strong, 00: Weak, 10/01: Normal |
| 5   | PCI_F0_S2 | 0   | PCI_F1 / PCI_F0 slew rate control   |
| 4   | PCI_F0_S1 | 0   | 11: Strong, 00: Weak, 10/01: Normal |
| 3   | AGP_32_S2 | 0   | 3V66_3 / 3V66_2 slew rate control   |
| 2   | AGP_32_S1 | 0   | 11: Strong, 00: Weak, 10/01: Normal |
| 1   | AGP_10_S2 | 0   | 3V66_1 / 3V66_0 slew rate control   |
| 0   | AGP_10_S1 | 0   | 11: Strong, 00: Weak, 10/01: Normal |

### 7.19 Register 18: Slew Rate Control (Default = 00H)

| BIT | NAME      | PWD | DESCRIPTION                         |
|-----|-----------|-----|-------------------------------------|
| 7   | PCI_75_S2 | 0   | PCI7, 6, 5 slew rate control        |
| 6   | PCI_75_S1 | 0   | 11: Strong, 00: Weak, 10/01: Normal |
| 5   | PCI_42_S2 | 0   | PCI4, 3, 2 slew rate control        |
| 4   | PCI_42_S1 | 0   | 11: Strong, 00: Weak, 10/01: Normal |
| 3   | PCI_10_S2 | 0   | PCI1, 0 slew rate control           |
| 2   | PCI_10_S1 | 0   | 11: Strong, 00: Weak, 10/01: Normal |
| 1   | REF_S2    | 0   | REF slew rate control               |
| 0   | REF_S1    | 0   | 11: Strong, 00: Weak, 10/01: Normal |

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### 7.20 Register 19: Control (Default = 0AH)

| BIT | NAME       | PWD | DESCRIPTION                                                                                               |
|-----|------------|-----|-----------------------------------------------------------------------------------------------------------|
| 7   | CPUSTOP_EN | 0   | Stop all CPU clocks. 1: Enable stop feature, 0: Disable                                                   |
| 6   | PCISTOP_EN | 0   | Stop SRC clock and all PCI clocks except free running parts.<br>1: Enable stop feature, 0: Disable        |
| 5   | SRCS_EN    | 0   | Allow PCISTOP pin to affect SRC output state<br>1: Allow, 0: Ignore the PCISTOP pin effect (Free running) |
| 4   | INV_DOT48  | 0   | Invert the DOT48 phase<br>0: In phase with USB48, 1: 180 degrees out of phase                             |
| 3   | INV_USB48  | 1   | Invert the USB48 phase<br>0: In phase with DOT48, 1: 180 degrees out of phase                             |
| 2   | USB48_S2   | 0   | USB48/DOT48/USB24_48 slew rate control<br>11: Strong, 00: Weak, 10/01: Normal                             |
| 1   | USB48_S1   | 1   |                                                                                                           |
| 0   | INV_SRC    | 0   | Invert the SRC phase, 0: Default, 1: Inverse                                                              |

### 7.21 Register 20: Winbond Chip ID – Project Code (Ready Only) (Default = 47H)

| BIT | NAME        | PWD | DESCRIPTION                            |
|-----|-------------|-----|----------------------------------------|
| 7   | CHPI_ID [7] | 0   | Winbond Chip ID. W83194BR-SD (SA5847). |
| 6   | CHPI_ID [6] | 1   | Winbond Chip ID.                       |
| 5   | CHPI_ID [5] | 0   | Winbond Chip ID.                       |
| 4   | CHPI_ID [4] | 0   | Winbond Chip ID.                       |
| 3   | CHPI_ID [3] | 0   | Winbond Chip ID.                       |
| 2   | CHPI_ID [2] | 1   | Winbond Chip ID.                       |
| 1   | CHPI_ID [1] | 1   | Winbond Chip ID.                       |
| 0   | CHPI_ID [0] | 1   | Winbond Chip ID.                       |

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### 7.22 Register 21: Reserved (Ready Only) (Default = 50H)

| BIT | NAME     | PWD | DESCRIPTION |
|-----|----------|-----|-------------|
| 7   | Reserved | 0   | Reserved    |
| 6   | Reserved | 1   |             |
| 5   | Reserved | 0   | Reserved    |
| 4   | Reserved | 1   |             |
| 3   | Reserved | 0   | Reserved    |
| 2   | Reserved | 0   |             |
| 1   | Reserved | 0   | Reserved    |
| 0   | Reserved | 0   |             |

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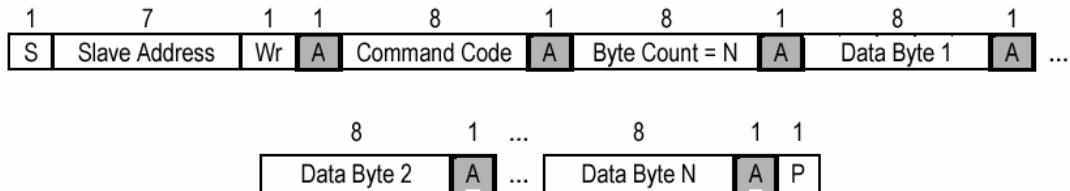


## 8. ACCESS INTERFACE

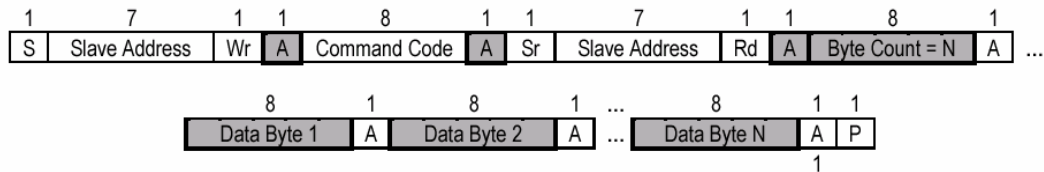
The W83194BR-SD provides I<sup>2</sup>C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-SD is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I<sup>2</sup>C address is defined at 0xD2.

### Block Read and Block Write Protocol

#### 8.1 Block Write Protocol

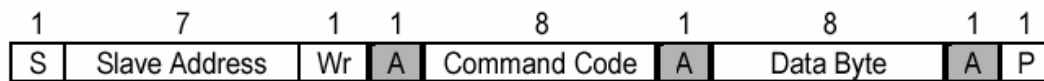


#### 8.2 Block Read Protocol

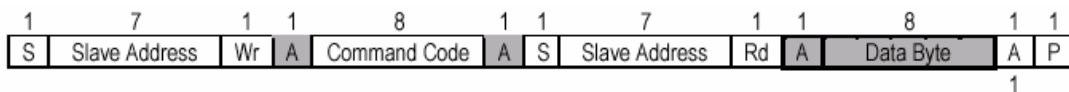


## In block mode, the command code must filled 00H

#### 8.3 Byte Write Protocol



#### 8.4 Byte Read Protocol



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## 9. SPECIFICATIONS

### 9.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

| PARAMETER                               | RATING           |
|-----------------------------------------|------------------|
| Absolute 3.3V Core Supply Voltage       | -0.5V to +4.6V   |
| Absolute 3.3V I/O Supply Voltage        | -0.5 V to +4.6 V |
| Operating 3.3V Core Supply Voltage      | 3.135V to 3.465V |
| Operating 3.3V I/O Supply Voltage       | 3.135V to 3.465V |
| Storage Temperature                     | -65°C to +150°C  |
| Ambient Temperature                     | -55°C to +125°C  |
| Operating Temperature                   | 0°C to +70°C     |
| Input ESD Protection (Human body model) | 2000V            |

### 9.2 General Operating Characteristics

VDDREF = VDDA = VDDCPU = VDD3V66 = VDDPCI = VDD48 = 3.3V  $\pm 5\%$ , TA = 0°C to +70°C, CI = 10pF

| PARAMETER                | SYM.             | MIN. | MAX. | UNITS           | TEST CONDITIONS                                  |
|--------------------------|------------------|------|------|-----------------|--------------------------------------------------|
| Input Low Voltage        | V <sub>IL</sub>  |      | 0.8  | V <sub>DC</sub> |                                                  |
| Input High Voltage       | V <sub>IH</sub>  | 2.0  |      | V <sub>DC</sub> |                                                  |
| Output Low Voltage       | V <sub>OL</sub>  |      | 0.4  | V <sub>DC</sub> | All outputs using 3.3V power                     |
| Output High Voltage      | V <sub>OH</sub>  | 2.4  |      | V <sub>DC</sub> | All outputs using 3.3V power                     |
| Operating Supply Current | I <sub>dd</sub>  |      | 350  | mA              | CPU = 100 to 400 MHz<br>PCI = 33.3 MHz with load |
| Input Pin Capacitance    | C <sub>in</sub>  |      | 5    | pF              |                                                  |
| Output Pin Capacitance   | C <sub>out</sub> |      | 6    | pF              |                                                  |
| Input Pin Inductance     | L <sub>in</sub>  |      | 7    | nH              |                                                  |

### 9.3 Skew Group Timing Clock

VDDREF = VDDA = VDDCPU = VDD3V66 = VDDPCI = VDD48 = 3.3V  $\pm 5\%$ , TA = 0°C to +70°C, CI = 10 pF

| PARAMETER             | MIN. | TYP. | MAX. | UNITS | TEST CONDITIONS  |
|-----------------------|------|------|------|-------|------------------|
| 3V66 to PCI Skew      | 1.5  | 2.6  | 3.5  | nS    | Measured at 1.5V |
| CPU to CPU Skew       |      |      | 100  | pS    | Crossing point   |
| 3V66 to 3V66 Skew     |      |      | 250  | pS    | Measured at 1.5V |
| PCI to PCI Skew       |      |      | 500  | pS    | Measured at 1.5V |
| 48 MHz to 48 MHz Skew |      |      | 1000 | pS    | Measured at 1.5V |
| REF to REF Skew       |      |      | 500  | pS    | Measured at 1.5V |

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### 9.4 CPU 0.7V Electrical Characteristics

VDDA = VDDCPU = 3.3V  $\pm$ 5 %, TA = 0°C to +70°C, Test load Rs = 33, Rp = 49.9  $\Omega$  CI = 10pF, Vol = 0.14V, Voh = 0.56V, Vr = 475, IREF = 2.32 mA, Ioh = 6\*IREF

| PARAMETER                        | MIN. | MAX. | UNITS | TEST CONDITIONS |
|----------------------------------|------|------|-------|-----------------|
| Rise Time                        | 175  | 700  | pS    | 100 to 200 MHz  |
| Fall Time                        | 175  | 700  | pS    | 100 to 200 MHz  |
| Absolute Crossing Point Voltages | 250  | 550  | mV    | 100 to 200 MHz  |
| Cycle to Cycle Jitter            |      | 125  | pS    | 100 to 200 MHz  |
| Duty Cycle                       | 45   | 55   | %     | 100 to 200 MHz  |

### 9.5 SRC 0.7V Electrical Characteristics

VDD = 3.3V  $\pm$ 5 %, TA = 0°C to +70°C, Test load Rs = 33, Rp = 49.9  $\Omega$  CI = 10pF, Vol = 0.14V, Voh = 0.56V, Vr = 475, IREF = 2.32 mA, Ioh = 6\*IREF

| PARAMETER                        | MIN. | MAX. | UNITS | TEST CONDITIONS |
|----------------------------------|------|------|-------|-----------------|
| Rise Time                        | 175  | 700  | pS    | 100 to 200 MHz  |
| Fall Time                        | 175  | 700  | pS    | 100 to 200 MHz  |
| Absolute crossing point Voltages | 250  | 550  | mV    | 100 to 200 MHz  |
| Cycle to Cycle jitter            |      | 125  | pS    | 100 to 200 MHz  |
| Duty Cycle                       | 45   | 55   | %     | 100 to 200 MHz  |

### 9.6 3V66 Electrical Characteristics

VDD3V66 = 3.3V  $\pm$ 5 %, TA = 0°C to +70°C, Test load, CI = 10pF

| PARAMETER              | MIN. | MAX. | UNITS | TEST CONDITIONS           |
|------------------------|------|------|-------|---------------------------|
| Rise Time              | 500  | 2000 | pS    | Measure from 0.4V to 2.4V |
| Fall Time              | 500  | 2000 | pS    | Measure from 2.4V to 0.4V |
| Cycle to Cycle Jitter  |      | 250  | pS    | Measure 1.5V point        |
| Duty Cycle             | 45   | 55   | %     |                           |
| Pull-Up Current Min.   | -33  |      | mA    | Vout = 1.0V               |
| Pull-Up Current Max.   |      | -33  | mA    | Vout = 3.135V             |
| Pull-Down Current Min. | 30   |      | mA    | Vout = 1.95V              |
| Pull-Down Current Max. |      | 38   | mA    | Vout = 0.4V               |

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### 9.7 PCI Electrical Characteristics

VDDPCI = 3.3V  $\pm$ 5 %, TA = 0°C to +70°C, Test load, CI = 10pF,

| PARAMETER              | MIN. | MAX. | UNITS | TEST CONDITIONS           |
|------------------------|------|------|-------|---------------------------|
| Rise Time              | 500  | 2000 | pS    | Measure from 0.4V to 2.4V |
| Fall Time              | 500  | 2000 | pS    | Measure from 2.4V to 0.4V |
| Cycle to Cycle Jitter  |      | 250  | pS    | Measure 1.5V point        |
| Duty Cycle             | 45   | 55   | %     |                           |
| Pull-Up Current Min.   | -33  |      | mA    | Vout = 1.0V               |
| Pull-Up Current Max.   |      | -33  | mA    | Vout = 3.135V             |
| Pull-Down Current Min. | 30   |      | mA    | Vout = 1.95V              |
| Pull-Down Current Max. |      | 38   | mA    | Vout = 0.4V               |

### 9.8 24M, 48M Electrical Characteristics

VDD48 = 3.3V  $\pm$ 5 %, TA = 0°C to +70°C, Test load, CI = 10pF,

| PARAMETER              | MIN. | MAX. | UNITS | TEST CONDITIONS           |
|------------------------|------|------|-------|---------------------------|
| Rise Time              | 500  | 2000 | pS    | Measure from 0.4V to 2.4V |
| Fall Time              | 500  | 2000 | pS    | Measure from 2.4V to 0.4V |
| Long Term Jitter       |      | 500  | pS    | Measure 1.5V point        |
| Duty Cycle             | 45   | 55   | %     |                           |
| Pull-Up Current Min.   | -33  |      | mA    | Vout = 1.0V               |
| Pull-Up Current Max.   |      | -33  | mA    | Vout = 3.135V             |
| Pull-Down Current Min. | 30   |      | mA    | Vout = 1.95V              |
| Pull-Down Current Max. |      | 38   | mA    | Vout = 0.4V               |

### 9.9 REF Electrical Characteristics

VDDREF = 3.3V  $\pm$ 5 %, TA = 0°C to +70°C, Test load, CI = 10 pF

| PARAMETER              | MIN. | MAX. | UNITS | TEST CONDITIONS           |
|------------------------|------|------|-------|---------------------------|
| Rise Time              | 1000 | 4000 | pS    | Measure from 0.4V to 2.4V |
| Fall Time              | 1000 | 4000 | pS    | Measure from 2.4V to 0.4V |
| Cycle to Cycle Jitter  |      | 1000 | pS    | Measure 1.5V point        |
| Duty Cycle             | 45   | 55   | %     |                           |
| Pull-Up Current Min.   | -33  |      | mA    | Vout = 1.0V               |
| Pull-Up Current Max.   |      | -33  | mA    | Vout = 3.135V             |
| Pull-Down Current Min. | 30   |      | mA    | Vout = 1.95V              |
| Pull-Down Current Max. |      | 38   | mA    | Vout = 0.4V               |

## W83194BR-SD/W83194BG-SD

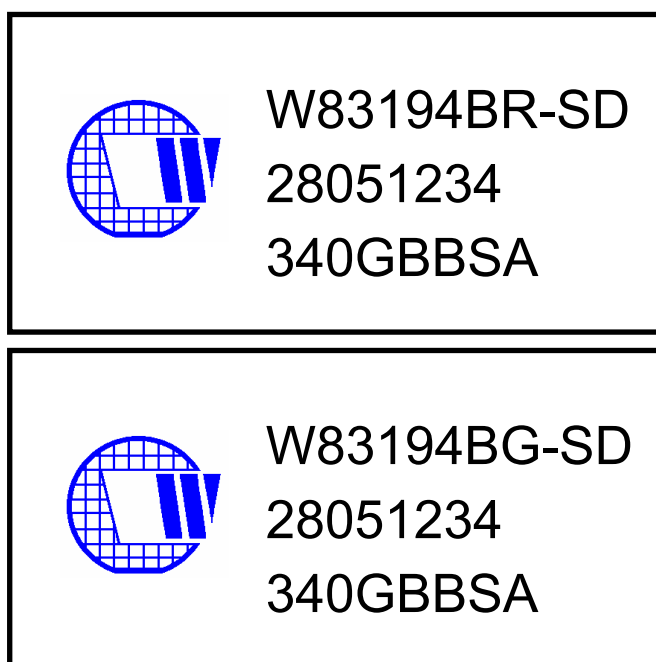


CLOCK GEN. FOR INTEL P4 SPRINGDALE/PRESCOTT SERIES CHIPSET

### 10. ORDERING INFORMATION

| PART NUMBER | PACKAGE TYPE                  | PRODUCTION FLOW          |
|-------------|-------------------------------|--------------------------|
| W83194BR-SD | 48 PIN SSOP                   | Commercial, 0°C to +70°C |
| W83194BG-SD | 48 PIN SSOP (Pb-free package) | Commercial, 0°C to +70°C |

### 11. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-SD, W83194BG-SD

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 340 G B B SA

340: packages made in '2003, week 40

G: assembly house ID; L means Lingsen, O means OSE, G means GR

B: Internal use code

B: IC revision

SA: mask version

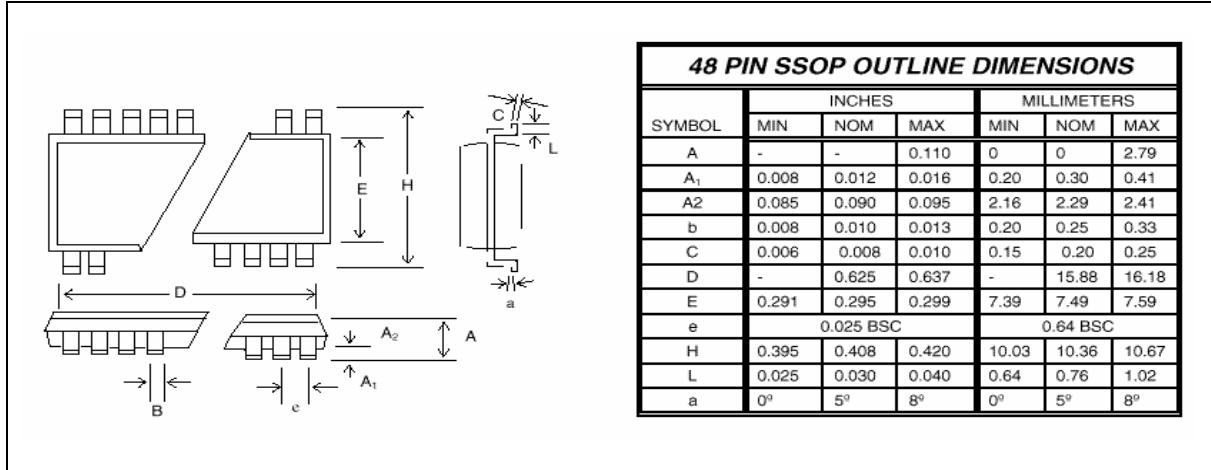
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Publication Release Date: March, 22, 2006

## W83194BR-SD/W83194BG-SD



### 12. PACKAGE DRAWING AND DIMENSIONS



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### Important Notice

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